55-kW Variable 3X DC-DC Converter for Plug-in Hybrid Electric Vehicles

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***Abstract*—This paper presents an alternative to the traditional dc-dc converter interfacing the battery with the inverter dc bus in plug-in hybrid electric vehicle (HEV) traction drives. The boost converter used in commercial HEVs meets with obstacles when it comes to upgrading the power rating and achieving high efficiency while downsizing the converter. A four-level flying-capacitor dc-dc converter is explored that can overcome these drawbacks by dramatically reducing the inductance requirement. A special case of the four-level converter, the 3X dc-dc converter, operates at three discrete output/input voltage ratios, thus further reducing the inductance requirement to a minimal value (almost zero). When further compared to its switched-capacitor dc-dc converter counterparts, the 3X dc-dc converter can be operated at variable output/input voltage ratios without sacrificing efficiency, and it lowers the capacitance requirement by utilizing the parasitic inductance. The operating principle, current ripple analysis, the transient control to limit the inrush current, and power loss analysis are introduced. Experimental results of a 55-kW prototype are provided to demonstrate the principle and analysis of this topology.**

***Index Terms*—DC-DC power conversion, multilevel converter, pulse width modulation, voltage dividers, voltage multipliers.**

I. Introduction

MANY commercial hybrid electric vehicle (HEV) systems, such as Prius, Camry, and Fusion, use a traditional bidirectional dc-dc converter to interface the battery and the inverter dc bus. For example, the powertrain configuration of the Camry hybrid is shown in Fig. 1. In this system, the dc-dc converter boosts the battery voltage from 244 V to three optimized discrete voltage levels up to 650 V according to the motor/generator speeds [1]. When combined with the continuous adjustment of modulation indices of the inverters, both the motor and generator and their individual inverters are able to operate in the most efficient region to accommodate the wide speed and power demand of the vehicle. In this traditional dc-dc boost converter, an inductor is employed. Besides its large size and heavy weight, the lossy inductor limits the operating temperature. Because of the inductor, the efficiency of the dc-dc converter is relatively low compared to the inverter.

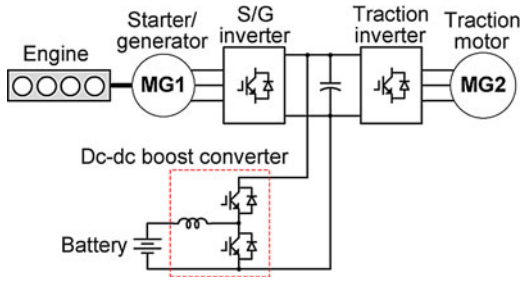

Fig. 1. Powertrain configuration of conventional series-parallel HEV.

Nowadays, the economical and environmental benefits from commercial HEVs have stimulated global interest in further developing plug-in hybrid electric vehicles (PHEVs). For the pure electric drive operation of PHEVs, the dc-dc boost converter has to deliver the full power needed by the traction drive, not just the difference between MG1 and MG2 as would be the case in blended operation mode with the engine running (Fig. 1). For example, the present dc-dc converter in the Prius is rated at 20-kW peak power (10-kW continuous power) [2], which is not enough for all-electric operation at higher speeds and has to be upgraded from 20-kW to 55-kW peak power (30-kW continuous) for PHEV's pure electric drive. It is not viable to simply resort to increasing the switching frequency to limit the size, weight, and cost of the converter since the core and copper loss of the inductor will go up as a result of the increased switching frequency and the power rating. In addition, the semiconductor heat dissipation in the converter limits the switching frequency. In response, multiphase dc-dc converters [3]–[5] were developed for high power HEVs and fuel cell vehicles (FCVs). The inductor design is still a challenging issue for increasing the converter efficiency and power density.

Multilevel dc-dc converter topologies [6]–[9] have been proposed for many applications. By contrast to the traditional dc-dc converter, a three-level flying-capacitor dc-dc converter greatly reduces the inductance requirement in addition to other benefits such as much lower device voltage rating and fast dynamic response [7], [8]. In this paper, further investigation and theoretical analysis are performed to utilize the multilevel structure to achieve high voltage boost and high power for PHEVs. A four-level flying-capacitor dc-dc converter is presented, as shown in

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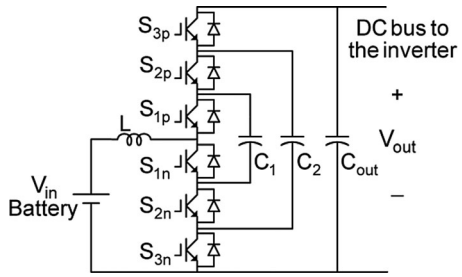

Fig. 2. Four-level flying-capacitor dc-dc converter.

Fig. 2, to replace the traditional dc-dc converter. This four-level structure can further reduce the input current ripple. More interestingly, a closer and further look into the input current ripple will reveal that the inductor can be eliminated or minimized when the converter operates at three discrete voltage ratios: 1X, 2X, and 3X. Power loss induced by the bulky inductor is diminished. Therefore, the operation of the four-level dc-dc converter at three discrete voltage ratios (thus named a variable 3X dc-dc converter) will be proposed later in this paper. The transition to achieve the three variable voltage ratios will be analyzed, followed by the experimental verification on a 55-kW 3X dc-dc converter prototype. It should be noted that a fixed 1:3 voltage ratio dc-dc converter has been introduced in [10], [11], however, they cannot be used for the aforementioned HEV and PHEV applications that require variable voltage levels. The primarily new contribution of this paper resides in the introduction of the variable 3X operation and smooth transition between voltage levels.

II. Four-Level Flying-Capacitor DC-DC Converter

In this section, the general operation and features of the four-level flying-capacitor dc-dc converter are explained and discussed first. The relationship between the input current ripple and voltage ratio is derived for the four-level converter and extended to the three- and two-level converters for comparison purposes. The current ripple comparison indicates a dramatic reduction of the inductance requirement. Analysis reveals three operation modes and the relationships between them. In addition, the analytical results will be further used in a later section for transitions from one voltage level to another of the variable 3X operation.

As shown in Fig. 2, each pair of switches S_{jp} and S_{jn} (j = 1, 2, 3) conduct complementarily and are clamped by capacitors C_1, C_2, and C_{out}. An input inductor (L) on the battery side plays the same role as in the traditional boost converter. It should be noted that this structure has the capability of bidirectional power flow. This paper focuses on the boost mode operation, that is, power flows from the battery (low voltage side, V_{in}) to the high voltage dc bus (V_{out}) to inverter(s). Under the boost mode, each lower-side switch S_{jn} is controlled as the active switch, and the antiparallel diode of the high-side switch S_{jp} conducts as the complementary switch. This four-level converter can be operated as a three-level converter as well, based on a switching pattern proposed in this paper.

First, the four-level operation can be divided into three operation ranges. The PWM signals and key waveforms in these three ranges are depicted in Fig. 3(a), (b), and (c). The PWM signals for both upper and lower switches, S_{jp} and S_{jn}, are shown in the figures, thus valid for both boost and buck operations. For example, the PWM signals for S_{jp}, represented by blue dash lines, indicate the conduction intervals of the anti-parallel diodes in the boost mode, whereas they represent PWM signals for the switches in the buck mode. The switching states are shown in Fig. 4. The voltages of capacitors C_1 and C_2 are controlled to be $V_{out}/3$ and $2V_{out}/3$, respectively. A duty cycle D is defined as the ratio of the duration that the switch S_{jn} conducts over one switching cycle, T. For $0 \le D \le 1/3$, as can be inferred from Fig. 3(a), the converter operates in a sequence of Fig. 4(a)-(d)-(b)-(d)-(c)-(d) over one switching cycle. The input voltage V_{in} equals the average value of the leg voltage v_m in steady state according to the voltage-second balance of the inductor. The leg voltage v_m is switched between two potentials, $2V_{out}/3$ and V_{out}, as shown in Fig. 3(a). For instance, when only S_{3n} is turned ON as shown in the switching state of Fig. 4 (a), C_2 gets charged, making $v_m = 2V_{out}/3$; when S_{3n} is OFF as shown in Fig. 4(d), the current freewheels through the anti-parallel diodes of S_{1p}, S_{2p} and S_{3p}, making $v_m = V_{out}$. Similarly for other switching states, when only one of the switches S_{jn} is ON as shown in Fig. 4(a), (b) and (c), $v_m = 2V_{out}/3$; otherwise $v_m = V_{out}$ in the freewheeling states in Fig. 4(d). Thus, one can get

$$V_{in} = \bar{V}_m = 3\left(\frac{1}{3} - D\right)V_{out} + 3D \cdot \frac{2V_{out}}{3} = (1-D)\,V_{out}. \tag{1}$$

During this operation range, each inner capacitor, C_1 and C_2, gets charged and discharged equally for a duration of DT over one switching cycle as shown in Fig. 3(a). However, due to gate delays and device tolerance, the voltage of each capacitor, C_1 and C_2, may settle down to a value slightly deviated from their theoretical values, $V_{out}/3$ and $2V_{out}/3$, respectively, as described in [12]. Therefore, in order to maintain their voltages as desired, an accurate duty cycle control is needed. This capacitor voltage balancing issue has been addressed and analyzed in the literature [8], [12]–[15].

When the duty cycle increases and enters the range of $1/3 \le D \le 2/3$, three new switching states as shown in Fig. 4 (e), (f), and (g) replace the previous freewheeling state. As a result, v_m is switched between two potentials: $V_{out}/3$ and $2V_{out}/3$, as shown in Fig. 3(b). The operating sequence follows Fig. 4(a)-(f)-(b)-(g)-(c)-(e) over one cycle. Likewise, when $2/3 \le D \le 1$, a new state comes into play. All the switches S_{1n}, S_{2n}, and S_{3n} conduct as shown in Fig. 4(h). Consequently, v_m presents two voltage levels: 0 and $V_{out}/3$, as shown in Fig. 3(c). The corresponding operating sequence is Fig. 4(e)-(h)-(f)-(h)-(g)-(h) repetitively. In spite of the above three variation ranges for D, it can be proven that the input and output voltage relationship expressed in (1) always holds true. Apparently, it is the same as the traditional boost converter. The buck mode can be analyzed similarly. It can be proven that the output/input voltage ratio for the buck mode is also the same as that for the buck converter. However, it can be seen from Fig. 3, that not only the effective

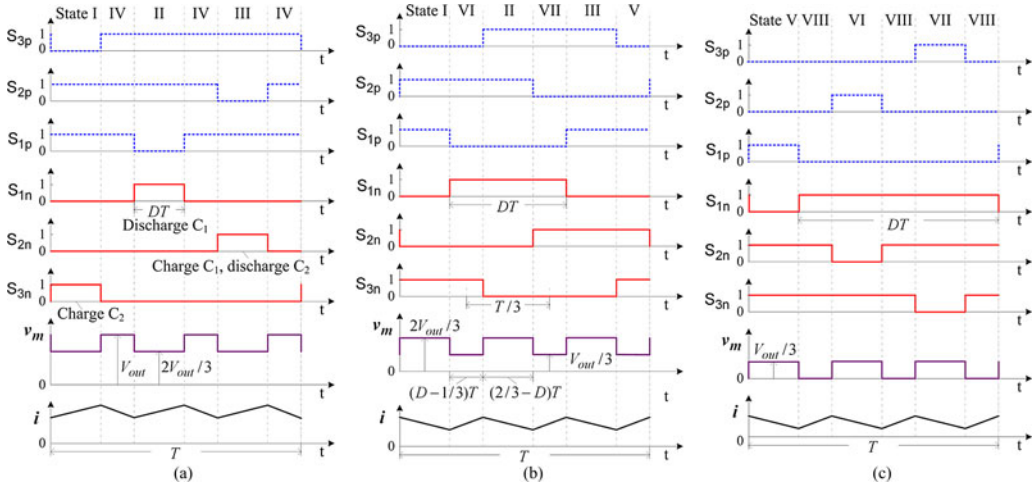

Fig. 3. PWM signals and key waveforms of the four-level operation. (a) $0 \le D \le 1/3$. (b) $1/3 \le D \le 2/3$. (c) $2/3 \le D \le 1$.

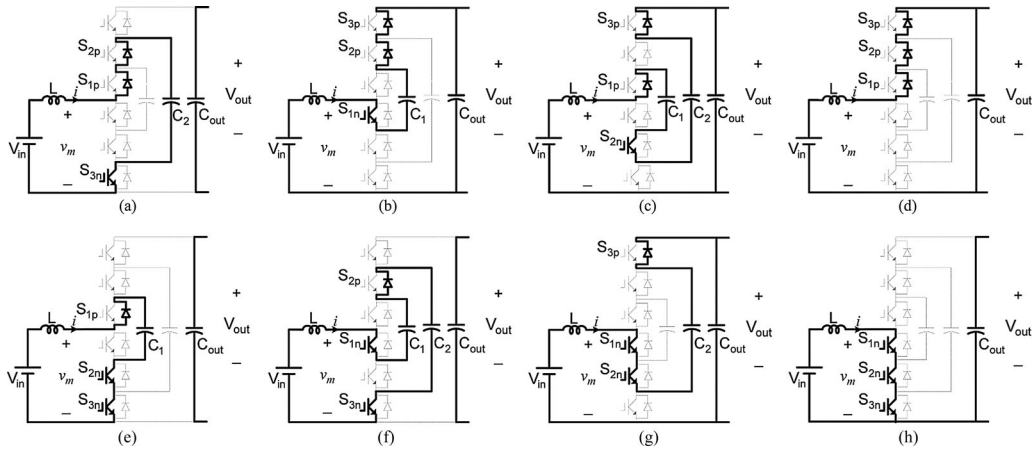

Fig. 4. Switching states of the four-level operation in boost mode. (a) State I. (b) State II. (c) State III. (d) State IV. (e) State V. (f) State VI. (g) State VII. (h) State VIII.

switching frequency is tripled but also the volt-second across the inductor is minimized when seen from the inductor in this four-level converter, thus having great potential to reduce inductor requirements.

Given an input voltage $V_{\rm in}$ in (1), the duty cycle, D, can be expressed as a function of $V_{\rm in}$ and $V_{\rm out}$. According to the inductor current change in each state, the input current ripple can be expressed as a function of $V_{\rm in}$ and $V_{\rm out}$

$$\Delta i = \begin{cases} \dfrac{V_{\rm in}T}{L}\left(1-\dfrac{2}{3}\dfrac{V_{\rm out}}{V_{\rm in}}\right)\left(1-\dfrac{V_{\rm in}}{V_{\rm out}}\right), & \text{for } 1 \le \dfrac{V_{\rm out}}{V_{\rm in}} \le \dfrac{3}{2}; \\ \dfrac{V_{\rm in}T}{L}\left(1-\dfrac{V_{\rm out}}{3V_{\rm in}}\right)\left(\dfrac{2}{3}-\dfrac{V_{\rm in}}{V_{\rm out}}\right), & \text{for } \dfrac{3}{2} \le \dfrac{V_{\rm out}}{V_{\rm in}} \le 3; \\ \dfrac{V_{\rm in}T}{L}\left(\dfrac{1}{3}-\dfrac{V_{\rm in}}{V_{\rm out}}\right), & \text{for } \dfrac{V_{\rm out}}{V_{\rm in}} \ge 3. \end{cases} \tag{2}$$

Second, the four-level converter can be operated as a three-level converter, when the capacitors, C_2 and $C_{\rm out}$, are connected in parallel by continuously turning ON switch S_{3n}. The PWM signals and key waveforms are shown in Fig. 5. Note that the duty cycle, D is only the duty cycle for S_{1n} and S_{2n} in this case. Fig. 6 shows the switching states for this three-level operation. The voltage of C_1 is controlled to equal $V_{\rm out}/2$. By applying the same analysis as before, the three-level operation can be divided into two operation ranges. When $0 \le D \le 1/2$, as shown in Fig. 5(a), the operation sequence is Fig. 6(a)-(c)-(b)-(c); otherwise when $1/2 \le D \le 1$, as shown in Fig. 5(b), the sequence is Fig. 6(a)-(d)-(b)-(d). It was derived in [8] that the voltage relationship can be also expressed by (1). The current ripple can be obtained as

$$\Delta i = \begin{cases} \dfrac{V_{\rm in}T}{L}\left(1-\dfrac{V_{\rm out}}{2V_{\rm in}}\right)\left(1-\dfrac{V_{\rm in}}{V_{\rm out}}\right), & \text{for } 1 \le \dfrac{V_{\rm out}}{V_{\rm in}} \le 2; \\ \dfrac{V_{\rm in}T}{L}\left(\dfrac{1}{2}-\dfrac{V_{\rm in}}{V_{\rm out}}\right), & \text{for } \dfrac{V_{\rm out}}{V_{\rm in}} \ge 2. \end{cases} \tag{3}$$

For comparison purposes, the current ripple of the traditional two-level (2 L) boost converter can be calculated as

$$\Delta i = \frac{V_{\rm in}T}{L}\left(1-\frac{V_{\rm in}}{V_{\rm out}}\right). \tag{4}$$

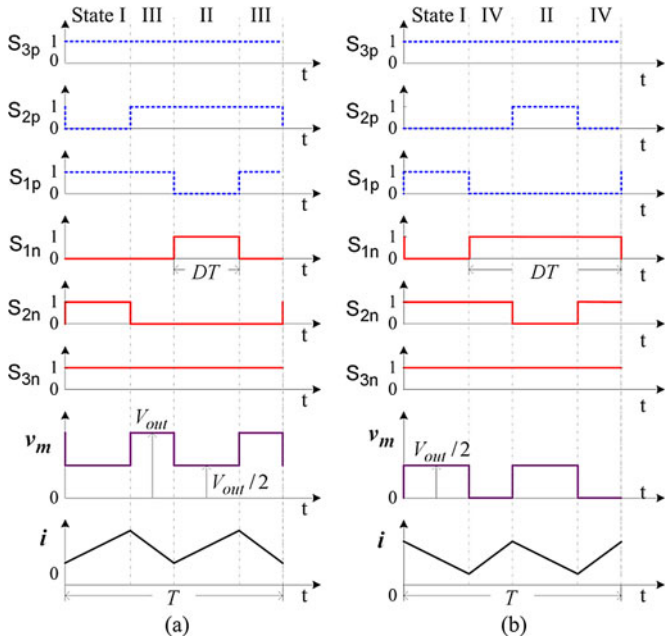

Fig. 5. PWM signals and key waveforms of the three-level operation. (a) $0 \leq D \leq 1/2$. (b) $1/2 \leq D \leq 1$.

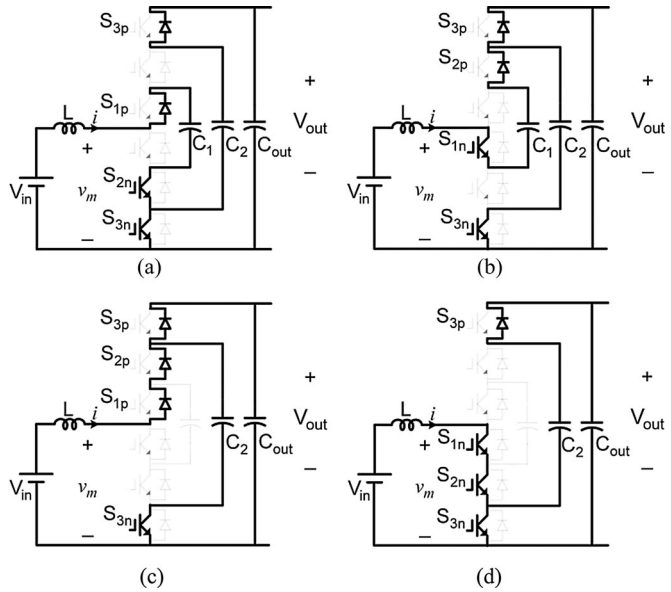

Fig. 6. Switching states of the three-level operation in boost mode. (a) State I. (b) State II. (c) State III. (d) State IV.

The normalized inductor current ripples of the four-level and three-level converters are compared with that of the traditional boost converter in Fig. 7. The base value is the current ripple of the traditional boost converter at a boost ratio of three. It is evident that the maximum current ripple of the four-level converter is almost 1/10 of the traditional dc-dc boost converter's over $1 \leq V_{\text{out}}/V_{\text{in}} \leq 4$. In other words, given the same current ripple specification, a much smaller inductor is sufficient for this four-level converter.

One concern about the four-level converter is that six semiconductor switching devices have to be used instead of two in

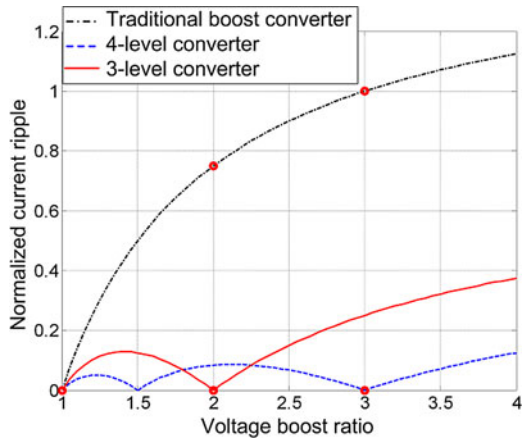

Fig. 7. Comparison of normalized current ripples.

the traditional two-level boost converter. The total switching device power rating (TDPR) or total device power stress (TDPS) of a converter circuit is an indication of how much total silicon area is needed for the semiconductor devices. The following analysis shows that both two- and four-level converters have the same TDPR, thus requiring similar or the same amount of silicon areas. For the six switches in the four-level converter operation, the TDPR is

$$\text{TDPR}_{\_4L} = 6 \cdot \left(\frac{V_{\text{out}}}{3}\right) \cdot I_{\text{in}} = 2 \cdot m \cdot P_o \tag{5}$$

where $m = V_{\text{out}}/V_{\text{in}}$ and output power, $P_o = V_{\text{in}}\, I_{\text{in}} = V_{\text{out}}\, I_{\text{out}}$. For the two switches in the traditional two level bidirectional boost converter, the TDPR is

$$\text{TDPR}_{\_2L} = 2 \cdot V_{\text{out}} \cdot I_{\text{in}} = 2 \cdot m \cdot P_o. \tag{6}$$

As can be seen from (5) and (6), they have the same total device power rating. For the traditional boost converter, each switch has to sustain the full dc voltage, whereas the switches in the four-level converter only sustain 1/3 of the dc voltage. For example, the Camry hybrid uses the traditional dc-dc boost converter, in which each switch employs four IGBTs and four diodes in parallel to reach the current (400 A) and voltage (650 V) ratings [16]. However, if the four-level converter is used, each switch needs to sustain only 1/3 of the output voltage, thus much lower voltage and higher current IGBT can be used without the need for paralleling. A different way to look at the four-level converter is that it uses three IGBTs in series to reach the required power rating, instead of parallel in the traditional boost converter. Therefore, the four-level converter is an attractive candidate to replace the traditional boost converter for PHEVs. More interestingly, when the converter operates at three discrete voltage ratios: one, two and three times the input voltage (3X), as marked with dots in Fig. 7, the inductor current in the four-level dc-dc converter becomes ripple free. This implies that the inductance requirement is zero. The question left-to-be-answered is how to produce three discrete voltage ratios with smooth transition from one level to another. As mentioned previously, three discrete voltage levels are enough and have been used in many HEVs such as Camry for optimum operation of the power train.

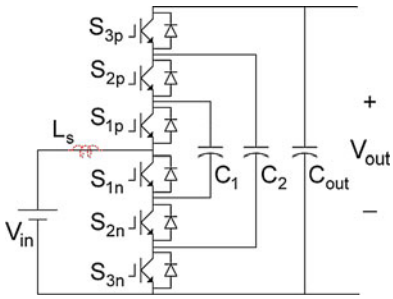

Fig. 8. 3X dc-dc converter.

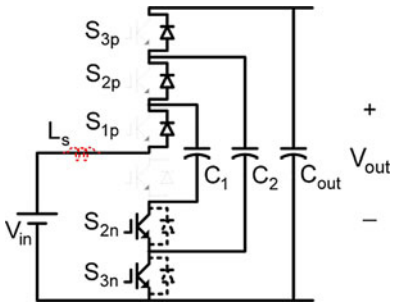

Fig. 9. Switching state for 1X mode.

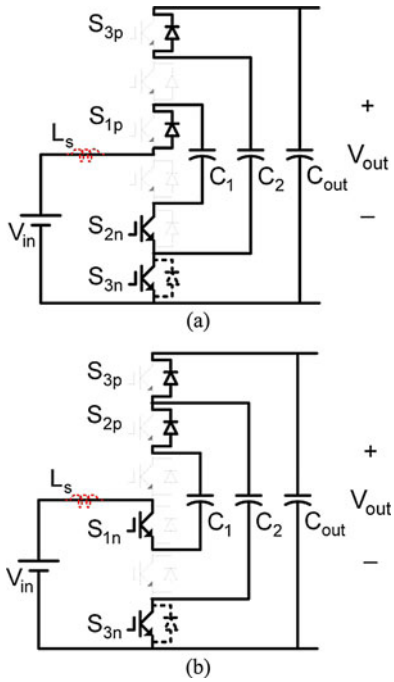

Fig. 10. Switching states for 2X mode. (a) Switching state I. (b) Switching state II.

III. Variable 3X DC-DC Converter and Its Operation Principle

Fig. 8 shows the proposed variable 3X dc-dc converter in which no magnetic inductor is needed on the input side for three discrete voltage output levels: 1X, 2X, and 3X the input voltage. In the figure, L_s represents stray inductance of the circuit, which can be the equivalent series inductance (ESL) within the battery pack and the parasitic inductance of the cable connecting the converter to the battery in the PHEV. A fixed ratio of 1:3 was presented in [10], [11] to interface the 14/42 V accessory power supplies in vehicles. However, this fixed voltage ratio is not suited for HEV and PHEV applications, in which a variable dc voltage is needed. In this paper, we further explore the possible operation of variable voltage ratios and their smooth transitions. Compared with other switched-capacitor dc-dc converters [17]–[28], the proposed variable 3X dc-dc converter has the simplest structure and finds its niche in the PHEV application where only discrete voltage ratios are desired from the battery to the traction drive dc bus voltage.

Because of its bidirectional nature, the 3X dc-dc converter can be viewed as a multiplier (step up) or a divider (step down) depending on power flow direction. The switching states, as shown in Figs. 9–11, represent the boost mode operation for the three voltage ratios: 1X, 2X, and 3X.

1X: To achieve the voltage ratio of 1, namely 1X, the converter operates in just one switching state as shown in Fig. 9, with switches S_{2n} and S_{3n} always ON. Thus, all the capacitors are connected in parallel with the input voltage, which ensures the voltage ratio of 1X. Under this 1X operation, it is apparent that there is no voltage balancing problem.

2X: While C_2 and $C_{\rm out}$ are always paralleled by having S_{3n} continuously ON, the converter alternates with 50%:50% duty cycle between two switching states, I and II, as illustrated in Fig. 10 (a) and (b). In switching state I with S_{2n} ON, the capacitor C_1 is paralleled with the input battery and charged to the battery voltage, and in switching state II with S_{1n} ON, C_1 is connected in series with the battery and discharged to the parallel of C_2 and $C_{\rm out}$. As a result, the voltage of the capacitor C_1 is maintained close to the battery voltage and the output voltage becomes 2X input battery voltage. The capacitor voltages should be well clamped and balanced. Note that the antiparallel diode (in the bold dashed line) of S_{3n} may conduct when the discharge current of C_2 is greater than the input current charging C_1.

3X: When the desired ratio is 3X, the converter circulates among switching states I, II, and III as shown in Fig. 11(a), (b) and (c), with 1/3 duty cycle each state. In state I, $V_{C1} = V_{\rm in}$; in state II, $V_{C2} = V_{C1} + V_{\rm in}$; in state III, $V_{\rm out} = V_{C2} + V_{\rm in}$. After these three states, the capacitor voltages will all be balanced automatically, as demonstrated in [10], [11]. The output voltage is three times (3X) the input voltage.

IV. Transient Current Control During Voltage Transitions

In steady state, the capacitor voltages are well balanced and the voltage differences are very small, so the current through the switches is well limited, as demonstrated in [10]. Theoretically, the 3X dc-dc converter does not need any input inductance in steady-state operation for any of the three output voltage levels. However, during a transition when the output voltage changes between $V_{\rm in}$ and $2V_{\rm in}$, or between $2V_{\rm in}$ and $3V_{\rm in}$, the voltage differences are very large, which can lead to high transient current through the devices and capacitors. In order to limit this transient

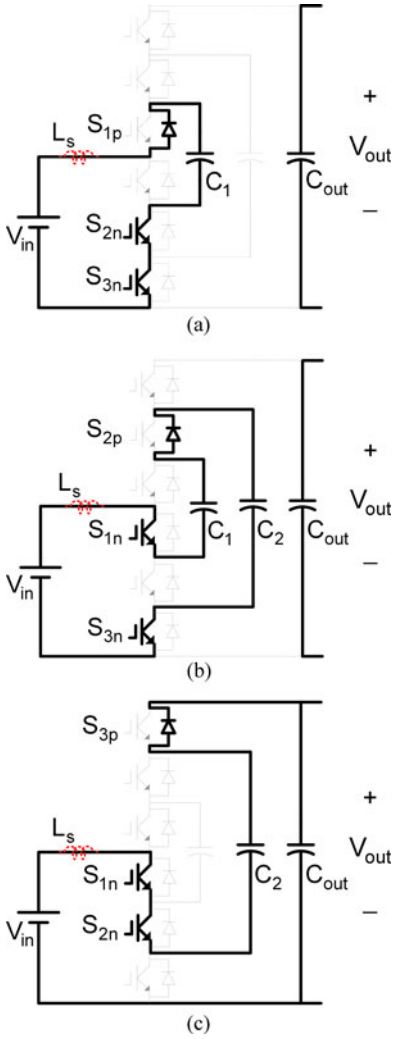

Fig. 11. Switching states for 3X mode. (a) Switching state I. (b) Switching state II. (c) Switching state III.

current, a variable duty-ratio PWM with a higher switching frequency is proposed for the transitions. In addition, a minimum inductance indicated as L_s in Fig. 8 is required for limiting the transient current, which will be discussed later.

A. Changing the Output Voltage From $1V_{\rm in}$ to $2V_{\rm in}$

Before changing the output voltage from $1V_{\rm in}$ to $2V_{\rm in}$, all three capacitors are initially charged to $1V_{\rm in}$ in 1X mode. In the transition, C_2 and $C_{\rm out}$ should be charged up to $2V_{\rm in}$ gradually. To simplify analysis, assume that the stray inductance is large enough for the inductor current to be continuous. (The transient input current does not have to be continuous, in principle). Therefore, the transient operation can be referred to the same sequence of Fig. 6(a)-(c)-(b)-(c) for the voltage ratio of $1 \leq V_{\rm out}/V_{\rm in} \leq 2$. The corresponding PWM signal in any switching cycle can be referred to Fig. 5(a), except that the duty cycle, D, has to be increased gradually over the transition to limit inrush current. The duty cycle is again defined in Fig. 5(a) for S_{1n} and S_{2n}. As a result, the transition is divided into two active switching states and one freewheeling state between them. In the two active switching states, the switching signals are given to the switches as shown in Fig. 6(a) and (b). The resultant leg voltage, v_m, equals V_{C1} in Fig. 6(a), and it equals $V_{\rm out} - V_{C1}$ in Fig. 6(b) for the duration of DT, respectively. After each active state, the switches S_{1n} and S_{2n} are turned OFF. Therefore, the input current flows through the antiparallel diodes S_{1p} and $S_{2p,}$ as shown in Fig. 6(c). The resultant leg voltage, v_m, equals $V_{\rm out}$ for the duration of $(1/2–D)T$. According to the inductor voltage-second balance in steady state, the relationship of the input voltage and output voltage still satisfies (1) as follows:

$$V_{\rm in} = DV_{c1} + D\left(V_{\rm out} - V_{c1}\right) + 2\left(\frac{1}{2} - D\right)V_{\rm out}$$
$$= (1-D)\,V_{\rm out}. \quad (7)$$

From the steady-state boundary condition of 1X and 2X modes, the duty cycle should vary from 0 to 1/2 to change the output smoothly to $2V_{\rm in}$. As illustrated in Fig. 12, the PWM duty cycle of the active switches S_{1n} and S_{2n} have to increase gradually from 0 to 1/2, with a higher transient switching frequency.

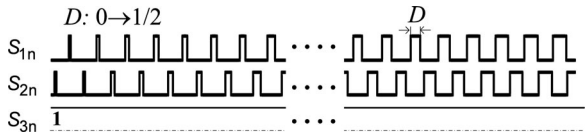

Fig. 12. PWM signals of the active switches during the 1X to 2X transition showing gradual duty cycle increase from 0 to 1/2.

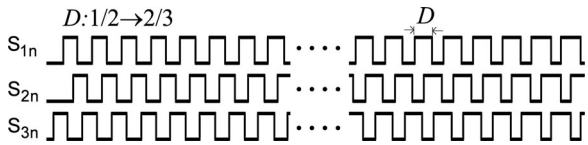

Fig. 13. PWM signals of the active switches during 2X to 3X transition showing gradual increase of duty cycle from 1/2 to 2/3.

B. Changing the Output Voltage From $2V_{\rm in}$ to $3V_{\rm in}$

Applying the same principle to the transition from $2V_{\rm in}$ to $3V_{\rm in}$, the switching states can be referred to the sequence of Fig. 4(e)-(a)-(f)-(b)-(g)-(c). The corresponding PWM signals and their time interval are marked in Fig. 3(b) over one switching cycle. Likewise, by averaging the leg voltage, v_m, the same voltage relation can be derived as (1). The ideal duty cycle for the active switches varies gradually from 1/2 to 2/3 during this transition, as illustrated in Fig. 13.

C. Changing the Output Voltage From $3V_{\rm in}$ to $2V_{\rm in}$

The control strategy for the transition from $3V_{\rm in}$ to $2V_{\rm in}$ is to reduce the initial three switching states, Fig. 11(a), (b), and (c), of the 3X operation to the first two switching states, Fig. 11(a) and (b), and to control the two switching states with 50%:50% duty cycle. The output capacitor $C_{\rm out}$ is disconnected from the source and will be gradually discharged by the load. When the output voltage decreases to the voltage of C_2, the antiparallel diode of S_{3p} conducts and clamps the output voltage to $2V_{\rm in}$. The PWM signals for this transition are shown in Fig. 14.

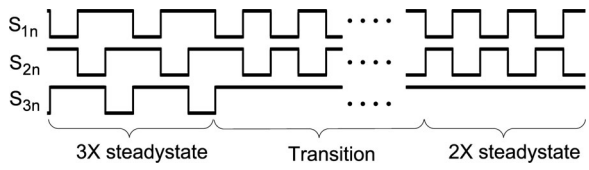

Fig. 14. PWM signals of the active switches in the 3X to 2X transition.

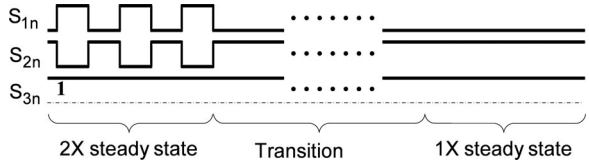

Fig. 15. PWM signals of the active switches in the 2X to 1X transition.

D. Changing the Output Voltage From $2V_{\rm in}$ to $1V_{\rm in}$

In a similar manner, a transition from 2X to 1X can be implemented by the gate signals illustrated in Fig. 15 to keep S_{2n} and S_{3n} ON. When the three capacitor voltages decrease and become equal, the converter settles down to the 1X mode steady-state operation, as shown in Fig. 9.

V. Minimum Requirement of Parasitic Inductance

In this section, an analysis is made to determine how much parasitic inductance is needed to limit the transition current within the rated input current. The voltages across C_1 and C_2 are assumed constant in each short switching period, $T_{\rm tr}$. Based on the above transient PWM control methods, the two worst cases for high transient currents are considered among all the transition modes.

A. $V_{\rm out}$: $1V_{\rm in}\rightarrow 2V_{\rm in}$

During this transition, the input current change (ripple) can be calculated according to the active switching state II, illustrated in Fig. 6(b)

$$\begin{aligned}\Delta i &= \frac{V_{Ls}\times DT_{\rm tr}}{L_s}\\ &= \frac{\left(V_{\rm in}+V_{c1}-V_{\rm out}\right)DT_{\rm tr}}{L_s}\\ &= \frac{V_{\rm in}\left(1-2D\right)DT_{\rm tr}}{L_s\left(1-D\right)}\\ &\le \Delta I_{\max}\end{aligned} \tag{8}$$

where $V_{c1}=V_{\rm in}, V_{\rm out}=V_{\rm in}/\left(1-D\right)$ for $0\le D\le 1/2$, and $\Delta I_{\max}$ is a given maximum current value allowed.

The maximum Δi occurs at $D=0.29$ in the above function, which should be limited to no larger than the specified maximum current allowed, $\Delta I_{\max}$.

B. $V_{\rm out}$: $2V_{\rm in}\rightarrow 3V_{\rm in}$

Similarly, the current change in the 2X to 3X transition is computed according to the active switching state III in Fig. 4(g)

$$\begin{aligned}\Delta i &= \frac{\left(V_{\rm in}+V_{c2}-V_{\rm out}\right)DT_{\rm tr}}{L_s}\\ &= \frac{V_{\rm in}\left(2-3D\right)\left(D-1/3\right)T_{\rm tr}}{L_s\left(1-D\right)}\\ &\le \Delta I_{\max}\end{aligned} \tag{9}$$

where $V_{c2}=2V_{\rm in}, V_{\rm out}=V_{\rm in}/\left(1-D\right)$ for $1/2\le D\le 2/3$.

The maximum Δi occurs at $D=0.53$ in the above function.

In comparison of the maximum current changes in both cases, the minimum inductance requirement can be calculated as 4.1 μH for a 480-A allowable current change, assuming that the 55-kW 3X dc-dc converter is switched at 20-kHz transient switching frequency and 230-V input voltage. The requirement of the parasitic inductance can be further reduced by increasing the switching frequency during transitions. In practice, a further lower parasitic inductance than the above conservative calculated value is tolerable, because the capacitance of C_1 and C_2 is finite and the voltages are not constant, which further reduces transient inrush current. In practice, the total ESL of a battery pack and connection cable should be sufficient, especially when the battery is placed in the trunk area far away from the converter which is under the hood in most HEVs and PHEVs. Otherwise, a small air-core inductor can be added when the parasitic inductance is not enough.

VI. Power Loss Analysis

Power loss analysis is usually estimated for assessing the converter parameters. It can be calculated numerically based on the current in the charge/discharge loop. Thus, the following analysis starts with modeling the input current. Each *n*X steady-state operation can be modeled with its equivalent circuit. Take the 3X mode for instance. The equivalent circuits are illustrated in Fig. 16. There is a lumped constant voltage drop $V_{\rm on}$ resulting from two IGBTs and one diode in the serial loop. The voltage drop of one IGBT is modeled as a constant voltage plus a current times its equivalent series resistance (ESR). In the first state of $t=0\sim(T_s/3)$, C_1 is charged by the battery, as modeled in Fig. 16(a). The input current can be solved as

$$\begin{aligned}i &= e^{-\alpha_1 t}\\ &\times\left[I(0)\cos\omega_1 t+\left(C_1\Delta V_1\frac{\alpha_1^2+\omega_1^2}{\omega_1}-\frac{\alpha_1 I(0)}{\omega_1}\right)\sin\omega_1 t\right]\end{aligned} \tag{10}$$

where $I(0)$ is the initial input current through the ESL in the charging loop, and $\Delta V_1=V_{\rm in}-V_{\rm on}-V_{C1}(0)$ is the initial voltage difference. $\alpha_i=R_{si}/(2L_s)$ in each state; $i=1,2,3$ implies three states; the resonance frequency in each switching state can be explicitly found by the equivalent loop capacitance and ESL: $\omega_i=\sqrt{1/(L_sC_{\rm loopi})-[R_{si}/(2L_s)]^2}$. In State I, $C_{\rm loop1}=C_1$.

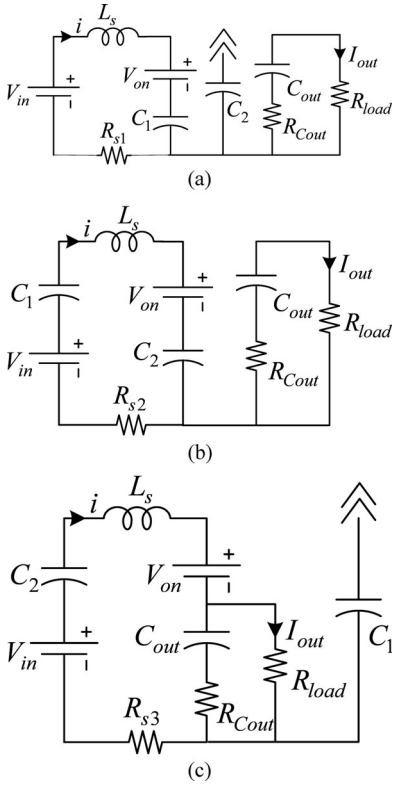

Fig. 16. Equivalent circuit for the 3X mode. (a) Switching state I. (b) Switching state II. (c) Switching state III.

In the same way, for the second state of $t = (T_s/3) \sim (2T_s/3)$ as modeled in Fig. 16 (b), the input current is expressed in (11).

$$i = e^{-\alpha_2 (t - T_s/3)} \left[I\left(\frac{T_s}{3}\right) \times \cos\omega_2 \left(t - \frac{T_s}{3}\right) + \left(C_{\text{loop2}} \Delta V_2 \frac{\alpha_2^2 + \omega_2^2}{\omega_2} - \frac{\alpha_2 \times I(T_s/3)}{\omega_2} \right) \sin\omega_2 \left(t - \frac{T_s}{3}\right) \right] \tag{11}$$

where $\Delta V_2 = (V_{\text{in}} - V_{\text{on}}) + V_{C1}(T_s/3) - V_{C2}(T_s/3)$, $C_{\text{loop2}} = C_1 \times C_2/(C_1 + C_2)$.

For $t = (2T_s/3) \sim T_s$, the output capacitor gets charged as modeled in Fig. 16(c). The load current, I_{out} can be approximated as a constant dc, considering the very small output voltage ripple. The input current can be expressed in (12) as a function of both initial input current and load current.

$$i = e^{-\alpha_3 (t - 2T_s/3)} \left\{ \left[I\left(\frac{2T_s}{3}\right) - \frac{C_2 I_{\text{out}}}{C_2 + C_{\text{out}}} \right] \times \cos\omega_3 \left(t - \frac{2T_s}{3}\right) + \left[C_{\text{loop3}} (\Delta V_3 - K)(\alpha_3^2 + \omega_3^2) - \alpha_3 \left(I\left(\frac{2T_s}{3}\right) - \frac{C_2 I_{\text{out}}}{C_2 + C_{\text{out}}} \right) \right] \cdot \frac{1}{\omega_3} \sin\omega_3 \left(t - \frac{2T_s}{3}\right) \right\} + \frac{C_2}{C_{\text{out}} + C_2} I_{\text{out}} \tag{12}$$

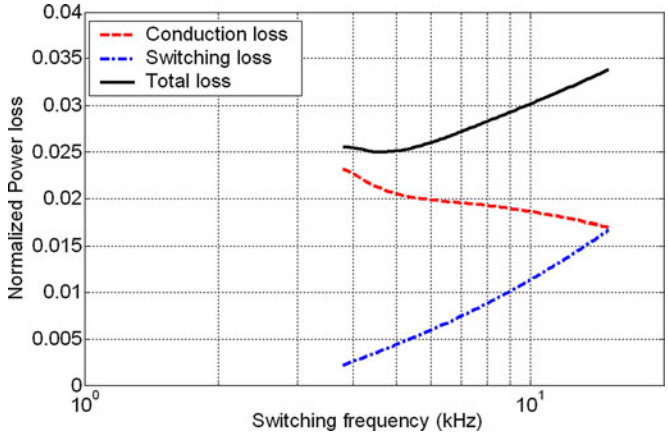

Fig. 17. Power loss versus switching frequency in 3X mode.

where $\Delta V_3 = (V_{\text{in}} - V_{\text{on}}) + V_{C2}(2T_s/3) - V_{C\text{out}}(2T_s/3)$, the constant $K = R_{s3} I_{\text{out}} C_2/(C_{\text{out}} + C_2)$, and the loop capacitance $C_{\text{loop3}} = C_{\text{out}} \times C_2/(C_{\text{out}} + C_2)$.

By equalizing the initial value of the current in the first state and the final value in the third state, the initial current $I(0)$ and the current expression can be solved. For a simplified iteration, the voltage difference in every state can be approximated from half of the capacitor voltage ripples.

The total power loss includes conduction loss, switching loss, and gate drive loss. The conduction loss here refers to the loss dissipated in the semiconductor devices and in the ESR in the passive components. The latter is sometimes separated as the charge/discharge loss, although it is essentially consumed by the loop ESR. It is discussed in [11] that the charging loss is not relevant to the ESR when the switching period and the *RC* time constant satisfy $T_s >> RC$ and the stray inductance is negligible. However, this is not true when the stray inductance is not negligible. The conduction loss can be summed up in (13) for every 1/3 switching cycle

$$P_{\text{con}} = \left(\sum_{j=1}^{3} \frac{V_{\text{on}} \cdot I_{\text{avg},j} + I_{\text{RMS},j}^2 \cdot R_{sj}}{3} \right) + \frac{\left(3I_{\text{out}}^2 + I_{\text{RMS},3}^2 - 2I_{\text{avg},3} \cdot I_{\text{out}}\right) R_{C\text{out}}}{3} \tag{13}$$

where $I_{\text{avg},j}$ and $I_{\text{RMS},j}$ are the average and RMS values of the input current, respectively.

At the end of each switching state, two IGBTs and one diode are turned ON/OFF. The IGBT switching loss is directly proportional to the switching current, given a fixed converter input voltage. The diode reverse recovery current can be expressed as a function of its snap-off current from the datasheet. Therefore, the switching loss is computed in (14) as the integration of the corresponding voltage and current

$$P_{\text{sw}} = V_{\text{ce\_pk}} \cdot f_s \sum_{j=1}^{3} \times \left[\frac{1}{6} I\left(\frac{jTs}{3}\right) \cdot (t_{\text{on}} + t_{\text{off}}) + \frac{1}{2} I_{\text{rr},j} \cdot t_{\text{rr},j} \right]. \tag{14}$$

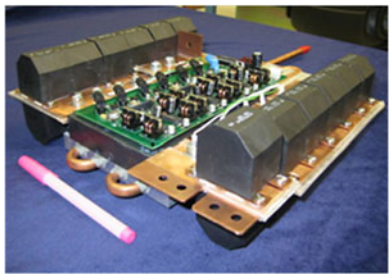

Fig. 18. 55-kW dc-dc multiplier/divider prototype.

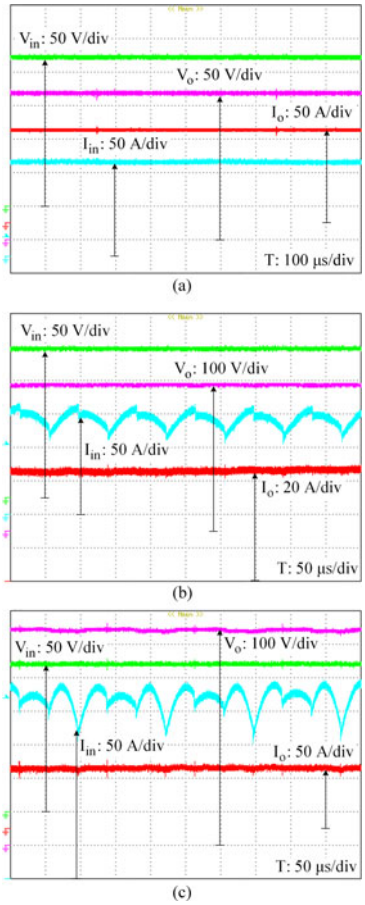

Fig. 19. Experimental waveforms in the steady-state operation. (a) 1X boost mode at 30-kW output. (b) 2X boost mode at 30-kW output. (c) 3X boost mode at 55-kW output.

As one of the guidelines for selecting the switching frequency, the estimated power loss is normalized and plotted in Fig. 17, according to (13) and (14). The circuit parameters are the same as in the next section. The total loss also includes gate drive loss. The base value is 30-kW continuous power at 220-V input voltage. As can be seen, the conduction loss is dominant when the switching frequency is low. As the switching frequency keeps rising, the switching loss becomes dominant. In terms of the overall efficiency, the optimum switching frequency falls in the range of 4∼6 kHz. At the same time, the input current ripple to the battery is another factor to be taken into account

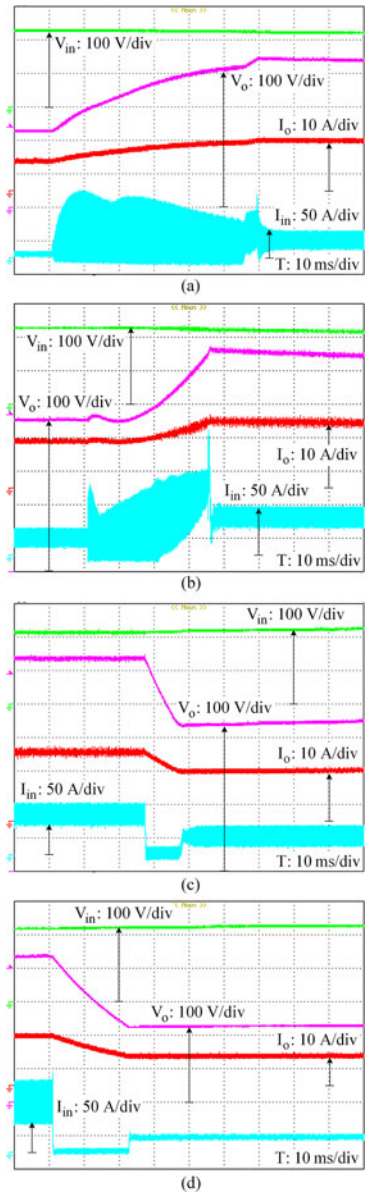

Fig. 20. Experimental waveforms of the *n*X mode transition. (a) Transition from 1X to 2X. (b) Transition from 2X to 3X. (c) Transition from 3X to 2X. (d) Transition from 2X to 1X.

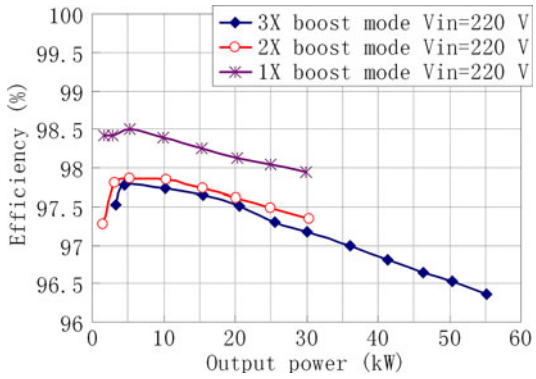

Fig. 21. Measured efficiency of the 55-kW prototype.

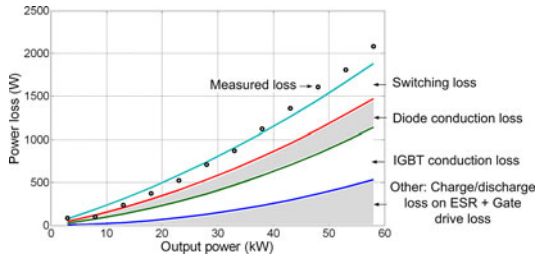

Fig. 22. Power loss breakdown of the 55-kW prototype in 3X mode.

for determining the switching frequency within the desirable efficiency range.

VII. Experimental Results

A 55-kW prototype, as shown in Fig. 18, was built to verify the functionality of the 3X dc-dc converter concept. The switching devices are commercially available 600-V IGBT/IPM modules, which is higher than what is required for the 3X dc-dc converter with 230-V input voltage. In fact, the efficiency of the converter would be higher if a lower (around 400 V) voltage rating module were available. The capacitors for C_1 and C_2 are 500-μF and 240-μF film capacitors, respectively. The output capacitor consists of 40-μF film capacitors in the 3X dc-dc converter and 820-μF capacitors at the inverter dc bus. The duty cycle and frequency control is implemented by one CPLD XC95288XL, which can be readily integrated with the control board for the entire power converter system.

Experimental results in the steady-state and transient operation are shown in Figs. 19 and 20. A total 5-μH ESL in the battery and cable was estimated. The converter operates at 8 kHz in the 3X mode and 12 kHz in the 2X mode. Fig. 19(a) and (b) show the input/output voltage and current waveforms in 1X and 2X modes at their 30-kW peak power. Fig. 19(c) shows the waveforms in 3X mode at the 55-kW peak power. Fig. 20 shows voltage transition waveforms, in which the converter operates at 20 kHz. As can be seen, the transient current was successfully limited below 240 A, the rated current of the converter. Fig. 21 shows the measured efficiency at different output powers in nX mode ($n = 1, 2, 3$). The overall efficiency in the 30-kW continuous power range is over 97%. Fig. 22 gives an estimation of the power loss breakdown in the full power range of the 3X mode, with a comparison to the experimental results. The analysis well predicts the characteristics of the loss with respect to the output power.

Compared to the design of the fixed 3X 1-kW converter in [10], the utilization of parasitic inductance in the proposed variable 3X converter reduces pulse current, the conduction loss, and the capacitance requirement. As a result, a compact size (27.2 cm $\times$ 24.4 cm $\times$8.8 cm) and light weight (5.6 kg) were achieved. Furthermore, the power density of the proposed converter is considerably increased, compared to the power density (30 kW / 3483.55 cm^3 and 30 kW / 6.6 kg) of the dc-dc converter in a commercially mass-production vehicle [16]. The 3.5-kg 212-μH inductor alone contributes significantly to the volume and weight of the traditional boost converter. There is still great potential to make the converter even lighter by replacing the film capacitors with multilayer ceramic capacitors (MLCCs).

VIII. Conclusion

In this paper, an alternative solution has been presented to overcome the demerits of the traditional boost converter for plug-in HEVs. Analysis has shown that a general four-level flying-capacitor dc-dc converter reduces the inductance requirement dramatically. Moreover, a variable 3X dc-dc converter has been proposed that was derived from the four-level dc-dc converter to further minimize the inductance to null for HEVs and PHEVs that require three discrete voltage levels. The experimental results of a 55-kW prototype in steady state and transient operation validated the operating principle and circuit analysis. Compared with the traditional low power switched capacitor dc-dc converters, the variable 3X converter achieves flexible voltage ratios without sacrificing efficiency (>97%) or the component count (only six switching devices and three capacitors) and with low voltage stress (V_{in}) across the switching devices. The transient current is well under control with the aid of the duty cycle control. By advantageously utilizing stray inductance, the variable 3X dc-dc converter achieves high efficiency with high power density. Therefore, it is a promising alternative to the existing boost converter for HEVs and PHEVs.

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