A Multilevel Modular Capacitor-Clamped DC–DC Converter

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***Abstract*—A novel topology of a multilevel modular capacitor-clamped dc–dc converter will be presented in this paper. In contrast to the conventional flying capacitor multilevel dc–dc converter, this new topology is completely modular and requires a simpler gate drive circuit. Moreover, the new topology has many advantageous features such as high frequency operation capability, low input/output current ripple, low ON-state voltage drop, and bidirectional power flow management. This paper discusses the construction and operation of the new converter along with a comparison to a conventional converter. Finally, simulation and experimental results are used to validate the concept of this new topology.**

***Index Terms*—Bidirectional converter, capacitor-clamped converter, dc–dc converter, hybrid electric vehicle, multilevel converter.**

I. Introduction

MULTILEVEL dc–dc converters have become more popular because of their highly efficient power conversion. There are several different types of multilevel dc–dc converters that have been previously developed [1]–[7], [9], [10]. Some of them have bidirectional power handling capability, which is one of the key requirements in future hybrid electric or fuel-cell-powered automobile power systems. Depending on the operation of the converter, most of the capacitor-clamped converters can be grouped into two major categories. Some of the converters originate from the series–parallel converter (SPC) [4]–[7], while the other major category is the flying capacitor multilevel dc–dc converter (FCMDC) [1], [3].

There are several inherent limitations of the SPC circuit. The major drawback is the voltage balancing among the capacitors used in the circuit. This phenomenon is observed in [4]–[7] where all the capacitors are connected in series during the charging period. The number of capacitors used in the circuit depends on the number of levels used, and it is governed by the up/down conversion ratio requirement. Thus, for a five-level converter, there will be five capacitors connected in series during the charging period, which may introduce a capacitor charge unbalance situation. Moreover, the voltage stresses across the switches are not equal. The top-level transistors experience more voltage stress than the bottom-level transistors. For a five-level application, the maximum ratio of voltage stress of the transistors from the top to the bottom level is four. For these two main flaws, the circuit cannot be considered as modular, and modifications need to be introduced for capacitor charge balancing.

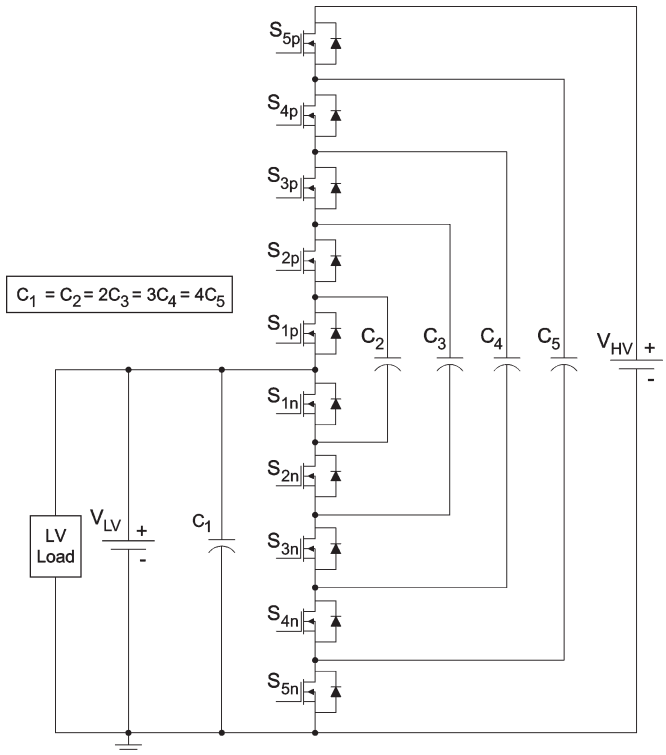

Fig. 1. Schematic of a five-level FCMDC.

The second type of capacitor-clamped converter considered in this paper is the FCMDC converter [3] shown in Fig. 1. The FCMDC circuit shown in [1] and [3] has some potential features to be used in automotive applications such as hybrid electric vehicles to manage the power transfer between different voltage level buses. Therefore, the various characteristics of this converter will be analyzed in detail, and it will be explained why the new topology presented in this paper can meet many key requirements in a hybrid electric or fuel-cell vehicle that cannot be fulfilled using the FCMDC topology. The FCMDC circuit has some limitations. First, this circuit does not have a modular structure. For this reason, the circuit cannot be easily extended to increase/decrease the number of levels, hence

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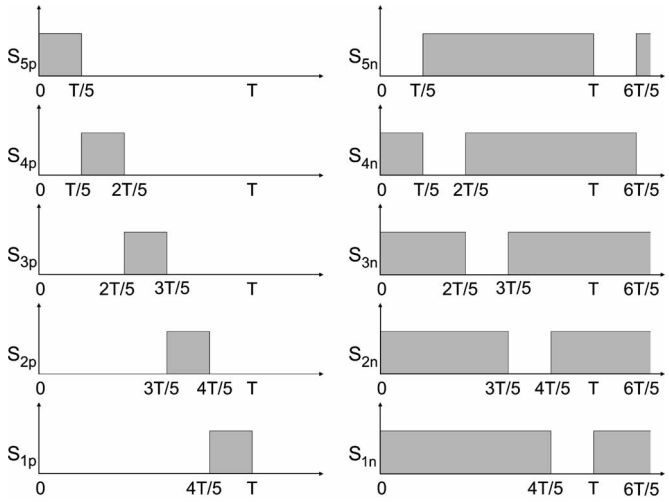

Fig. 2. Switching scheme of the FCMDC circuit.

changing the conversion ratio. The other major limitation is the complicated switching schemes for the different transistors shown in Fig. 2. For the convenience of explaining the operation of the circuit, it is considered that power is transferred from the high voltage (HV) battery to the low voltage battery and associated loads.

During one operating cycle, only one subinterval is associated with the energy extraction from the HV side battery in this converter. During the other subintervals, energy stored in capacitor C_5 is transferred to the other capacitors through the output circuit. Thus, when the conventional converter is designed with a high conversion ratio, one capacitor takes energy from the HV battery for one period over the conversion ratio. This is not a serious issue when the conversion ratio is low. However, when the conversion ratio is high such as 5, only a small timeframe is allowed to transfer the energy from the voltage source to the capacitor, and from the capacitor to the next level capacitors as well. Sometimes it is desirable to operate the circuit at high frequency to reduce the capacitor sizes [3]. However, when the transition time (rise time or fall time) of a transistor is comparable to its ON time $(t_{\rm on})$, the circuit becomes inefficient. For an N-level converter, the ON time for any transistor shrinks to $(1/N)$th of the total time period, and the effective switching frequency is N times the original switching frequency. This increased effective switching will introduce high frequency ripple at the output dc voltage. While charging a battery, this high frequency ripple causes additional heating inside the battery, and this effect is bad for the health of the battery. For these reasons this circuit cannot be operated at high frequency.

The excessive voltage drop across the active switches or diodes inside the converter is another limitation of the FCMDC. This can be seen in Fig. 1. During any subinterval, five transistors/diodes are turned on, and the input/output current flows through these five transistors/diodes. In fact, for an N-level converter, a total number of N transistors/diodes are intended to flow the current, which could add a severe voltage drop across them during high-power applications. Thus, the remedy to this flaw would be to obtain a circuit such that the number of devices in a series path is significantly less. By obtaining a new circuit, the voltage regulation of the converter can be substantially enhanced and losses can be reduced.

TABLE I
DIRECTION OF POWER FLOW AT DIFFERENT BATTERY VOLTAGES

Case	Ratio of battery voltages	Power flow direction	Power flow from high side to low side	Power flow from low side to high side
1	>5	High to Low	Possible	Not possible
2	<5	Low to High	Not possible	Possible

The incapability to withstand a fault in the converter is another major drawback of the FCMDC. To form a five-level converter, ten transistors are required, and if any one of these transistors fails, there is no way to continue the operation of the circuit. Hence, the circuit configuration is nonmodular, so no redundancy can be incorporated in the circuit.

In the proposed application where the converter is responsible for transferring power from a HV battery to a low-voltage battery or vice-versa, the direction of power flow depends on the voltages at the two ends. For a five-level converter, if the voltage at the HV-side battery is more than five times that of the low-voltage battery, then the power is transferred from the HV side to the low-voltage side. By the same token, if the HV-side battery voltage is less than five times of the low voltage battery, then power is transferred from the low- to HV-side battery. This property of power flow indicates the incapability of having a true bidirectional power management system where the power flow direction does not depend on the battery voltages. Table I summarizes the possible cases where a converter with fixed conversion ratio fails to establish bidirectional power management. In automotive applications, the battery voltage at the two ends can vary within a wide range, though power transfer may be required in either direction irrespective of the two end battery voltages. A converter with a variable conversion ratio could solve the problem.

Thus, the limitations of the conventional multilevel flying capacitor converter can be summarized as: 1) nonmodular structure; 2) relatively complicated switching scheme; 3) difficulty in high frequency operation; 4) excessive voltage drop across the switches/diodes; 5) lack of bidirectional power management; and 6) no fault bypass capability.

There are also some other capacitor-clamped or diode-clamped converters such as the neutral-point-clamped (NPC) converter. However, the NPC topology is actually an inverter, and not a dc–dc converter. After a detailed investigation, it was found that many other capacitor-clamped topologies are not ideal for high-power applications, and are more suitable for low-power applications [11].

II. NEW TOPOLOGY

The proposed five-level multilevel modular capacitor-clamped dc–dc converter (MMCCC) shown in Fig. 3 has an

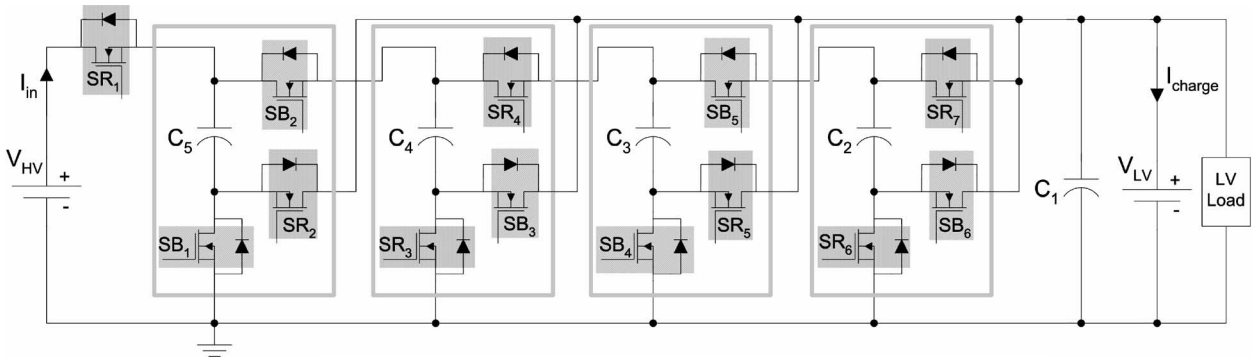

Fig. 3. Five-level MMCCC with four modular blocks.

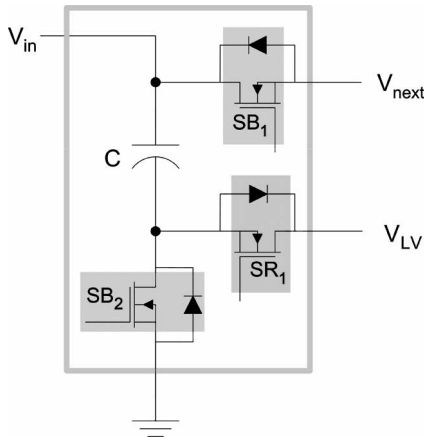

Fig. 4. Modular block of the MMCCC.

inherent modular structure and can be designed to achieve any conversion ratio. Each modular block has one capacitor and three transistors leading to three terminal points. A modular block is shown in Fig. 4. The terminal $V_{\rm in}$ is connected to either the HV battery or to the output of the previous stage. One of the output terminals $V_{\rm next}$ is connected to the input of the next stage. The other output terminal $V_{\rm LB}$ is connected to the low voltage side positive $(+)$ battery terminal.

In an FCMDC with conversion ratio of 5, the total steady state operation takes five subintervals, which is shown in Fig. 2 and Table II. It is seen that only one charge-discharge operation is performed in one subinterval. Thus, the component utilization is limited in this circuit. For an N-level converter, any capacitor except C_1 is utilized during only two subintervals for a complete cycle (one subinterval for charging, one for discharging) and for the remaining $(N-2)$ subintervals in one period, the component is not used. The new converter introduced here can increase the component utilization by performing multiple operations at the same time, which is also shown in Table II.

In Fig. 5, the simplified operational circuit of the MMCCC is shown. To get the new switching scheme, it is initially assumed that the new converter will perform the entire operation in five subintervals, and later it will be shown how these five operations can be done in two subintervals. Fig. 5(a) shows the first subinterval where C_5 is being charged from $V_{\rm HV}$ through the output circuit. In the second subinterval, C_5 will transfer the charge to C_4 through the output circuit, and this operation is shown in Fig. 5(b). During the third subinterval, C_4 releases energy to C_3 through the output circuit as shown in Fig. 5(c). So far, these operations are the same as the conventional FCMDC. Interestingly, during this third subinterval, the charging operation of the first subinterval (C_5 gets charged from $V_{\rm HV}$ through the output circuit) can be performed without perturbing the operation of the entire circuit, which also is shown in Fig. 5(c). Thus in this stage, two operations are performed at the same time, and C_5 gets energy for the second time through the output circuit.

During the fourth subinterval, the same operation of Fig. 5(b) can be performed. In addition to that, C_3 can transfer energy to C_2 through the output circuit without perturbing the entire operation. Thus, two operations can take place at the same time. These operations are shown in Fig. 5(d). In this way, all the steps shown in Fig. 5(a)–(d) are the initialization steps where all the capacitors are being charged and ready to get into the steady state operating conditions.

In the fifth stage shown in Fig. 5(e), C_5 is again energized from $V_{\rm HV}$ and C_4 transfers energy to C_3. C_2 was charged in the previous stage, and now it transfers the energy to the output circuit. Thus, three operations take place at the same time, which are independent of each other. The operations that took place in Fig. 5(d) are repeated again in the sixth step, which is shown in Fig. 5(f). Thus, these two steps shown in Fig. 5(e) and (f) are the steady-state operations of the converter where the fourth step and the sixth step are the same. The simplified diagram shown in Fig. 5(e) is defined as state 1 during steady-state, and the diagram in Fig. 5(f) is the state 2 during steady-state operation. Once all the capacitors are charged after the initialization stage, the circuit enters into the steady-state and state 1 and state 2 will be repeated in every clock cycle.

Out of these six steps, the fifth and sixth step are the two states in the steady state operation of the circuit, and the first four steps are considered as the initialization steps of the converter. From Fig. 5, it is clear that the fourth and the sixth step operations are the same, and considering the fourth step as the state 1, and fifth step as state 2 of steady state, the number of initialization steps could be reduced to three. It is just a matter of convention to define the fifth step as state 1, and not the fourth, and either way, it does not have any impact on the operation of the circuit.

The switching sequence in the new converter works in a simpler way than the conventional converter. As there are only

TABLE II
SWITCHING SCHEMES (STEADY STATE) OF FCMDC AND MMCCC. ↑= CHARGING, ↓= DISCHARGING

FCMDC		MMCCC	
Sub interval No.	Operations	Sub interval No.	Operations
1	$V_{HV} \rightarrow C_5\uparrow + C_1\uparrow$	1	$V_{HV} \rightarrow C_5\uparrow + C_1\uparrow$ $C_4\downarrow \rightarrow C_3\uparrow + C_1\uparrow$ $C_2\downarrow \rightarrow C_1\uparrow$
2	$C_5\downarrow \rightarrow C_4\uparrow + C_1\uparrow$		
3	$C_4\downarrow \rightarrow C_3\uparrow + C_1\uparrow$		
4	$C_3\downarrow \rightarrow C_2\uparrow + C_1\uparrow$	2	$C_5\downarrow \rightarrow C_4\uparrow + C_1\uparrow$ $C_3\downarrow \rightarrow C_2\uparrow + C_1\uparrow$
5	$C_2\downarrow \rightarrow C_1\uparrow$		

two subintervals, two switching states are present in the circuit. Switches SR_1 to SR_7 in Fig. 3 are operated at the same time to achieve state 1; the equivalent circuit is shown in Fig. 5(e). In the same way, switches SB_1 to SB_6 are operated simultaneously to make the steady-state equivalent circuit shown in Fig. 5(f). This new switching pattern is shown in Fig. 6.

The switching scheme of the MMCCC is simpler than the FCMDC topology. In the FCMDC circuit, an N-phase signal generator is needed, where N is the conversion ratio. However, the MMCCC circuit only requires a two-phase signal generator because the circuit has only two operating states in steady-state regardless of the number of levels or conversion ratio. Moreover, when the duty ratio of the converter is required to change (for finer control over the output voltage), it will be more difficult to implement it in a five-phase circuit for the FCMDC. In addition, the five-level FCMDC (shown in Fig. 1) requires ten gate-drive integrated circuits (ICs) to drive ten transistors because bootstrap gate drive circuits cannot be used for this configuration. However, in each module of the MMCCC circuit, three transistors can be driven by two gate drive circuits because two out of these three transistors have a common terminal to create a push-pull configuration (SB_1 and SR_2 in Fig. 3). Thus, the total number of gate drive ICs required in the MMCCC circuit is $(2N-1)$, and the use of bootstrap gate driver ensures correct dead time for the transistors used in the MMCCC circuit.

The simpler switching scheme enables high-speed operation for the new MMCCC circuit. In a conventional FCMDC, the permitted time for charging/discharging of any capacitor depends on the conversion ratio. Thus, for a five-level converter running at frequency f_s, the allowable charging/discharging time is $T_s/5$ ($T_s = 1/f_s$). If this time is the minimum for a complete charging/discharging operation, the switching frequency of the circuit must be less than or equal to f_s. However, this problem is eliminated in the new converter by virtue of the new switching scheme. As there are only two switching states, the switching frequency can be made $2.5f_s$ by keeping the same charging/discharging time $T_s/5$.

Table I shows that a conventional FCMDC has some difficulties in true bidirectional power management because its conversion ratio cannot be changed. To eliminate this problem, the new converter uses one additional level to achieve more voltage at the output side during the up conversion operation. During the down conversion, more power can be transferred from the HV side to the low voltage side by reducing the number of levels to four. Because the circuit is modular, it is possible to change the number of levels by adding or bypassing any redundant levels in the circuit. The duty ratio of the gate drive signals can be reduced to get a fractional conversion ratio to control the current from one bus to the other. This duty ratio reduction technique is essential to control the power flow in bidirectional power management.

The other major advantage of the modular structure is the flexibility to change the conversion ratio. For a five level conversion, four modules are connected in cascade configuration. Thus, the number of modules is $(N-1)$ where N is the conversion ratio. In this way, any number of modules can be connected in cascade and the corresponding conversion ratio can be achieved.

The MMCCC topology is a capacitor-clamped converter, and energy is transferred from one bus to another by capacitors only. The total value of the capacitances used in either FCMDC or MMCCC determines the amount of voltage ripple at the output, and according to [1], the output voltage ripple is an inverse function of the capacitance used in the circuit, which is the same for the MMCCC converter. Moreover, the capacitor charge-discharge profile of the MMCCC topology is the same as the FCMDC topology except the number of subintervals present in the operation. In an FCMDC circuit, the circuit requires the number of subintervals to be equal to the conversion ratio of the circuit. However, all the operations of an FCMDC converter are performed in only two subintervals in an MMCCC converter. Because, the charge-discharge profile is the same in these two converters, the value of the total capacitance used in these circuits are the same provided the same voltage ripple is present at the output.

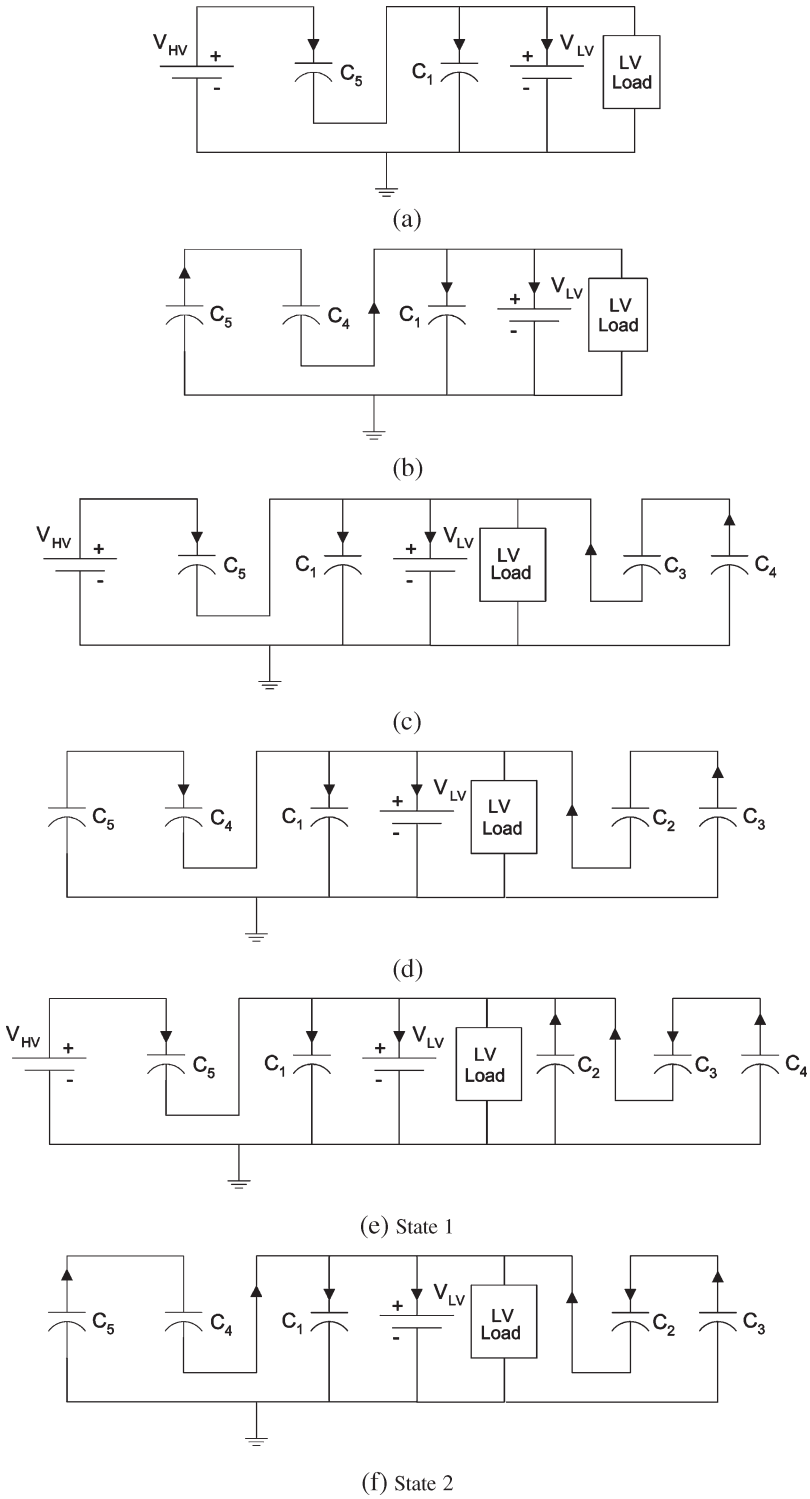

Fig. 5. Simplified diagram of the new converter using the switching scheme of the conventional converter.

The size of the capacitors used in the MMCCC circuit can be made different from the FCMDC topology. In the FCMDC circuit, capacitors used in the different levels have different values, and their values are estimated depending on the voltage stress they experience. On the other hand, the MMCCC topology uses the same capacitance in each module. The main reason is its modularity. Using the same capacitors in each module, the circuit could be made modular, although the capacitors in different modules will experience different voltage stresses. To ensure equal voltage stress across the transistors, capacitors in different modules have to withstand unequal voltage stress.

III. Simulation Results

To compare the performance of the new converter, a six-level converter was simulated in PSIM from Powersim Inc.

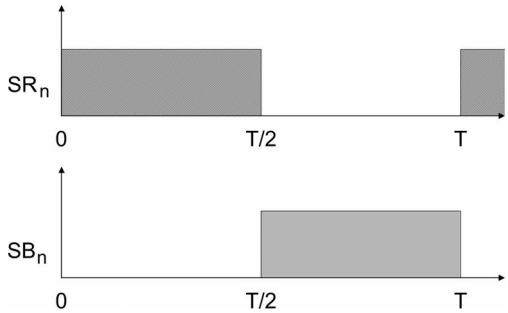

Fig. 6. Gating signal of the switches in the new circuit, i.e., there are only two switching states present in the circuit.

TABLE III
DIFFERENT MODES OF THE SIMULATION

Mode	V_{in} (V)	Output load	Battery voltage
Down conversion	75	1 Ω	NA
Up Conversion	12	30 Ω	NA
Down conversion with battery charging	80	NA	12 V

along with the FCMDC converter. Both were simulated in three modes listed in Table III. During the simulation, the $R_{\rm DS}$ of a MOSFET was assumed as 0.06 Ω, and the equivalent series resistance (ESR) of the capacitors were assumed as 0.1 Ω. As there was no strict guideline to extend the operation of the three-level FCMDC to operate in six-level configuration, the capacitor values were estimated based on the voltage stress they experienced. Thus, for a six-level design, the following capacitor relation was used for the FCMDC converter:

$$C_1 = C_2 = 2C_3 = 3C_4 = 4C_5 = 5C_6.$$

A 1000-μF capacitor was used as C_6, and the other capacitors' values in the FCMDC were determined accordingly. However, to make each module identical in an MMCCC, all the capacitors used in the circuit had the same value of 1000 μF. Thus, the total capacitance in the MMCCC circuit was 6000 μF, and it was 20 000 μF in the FCMDC converter. The experimental results for the MMCCC converter were obtained using the same configuration as the simulation.

Fig. 7(a) shows the output voltage of an FCMDC in down conversion mode. With a 75 V input voltage and a conversion ratio of 6, the output voltage of this converter should be close to 12 V. Fig. 7(b) shows the output voltage of the MMCCC, and clearly it produced an output voltage close to 12 V, which could not be obtained from the conventional FCMDC in this simulation.

Fig. 7(c) shows the input current of the conventional converter, and Fig. 7(d) shows the same for the new converter. This shows that the peak current stress for the new converter is 2.5 times smaller than that of the conventional converter. This feature will ensure higher reliability and the freedom of using smaller-sized transistors.

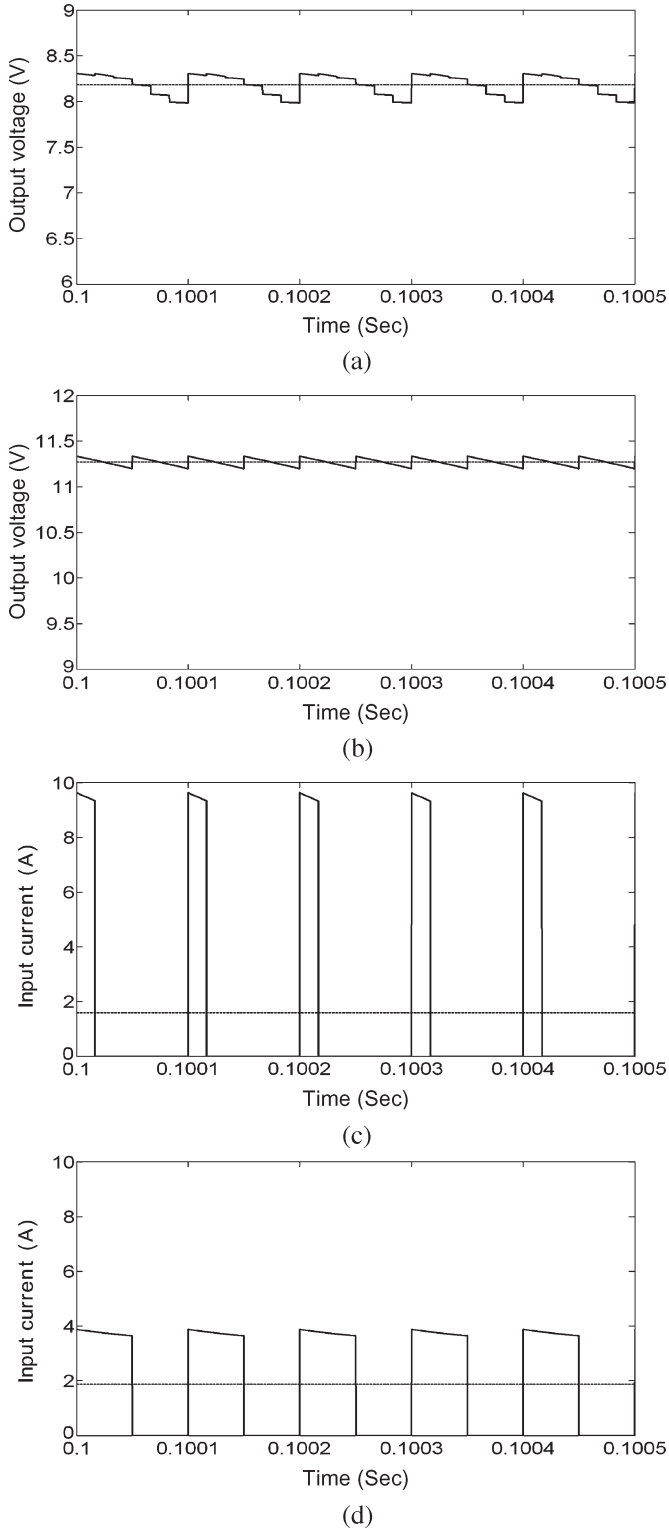

Fig. 7. Converters' simulation results in down-conversion mode ($V_{\rm in} = 75$ V, $R_{\rm load} = 1\ \Omega$). (a) FCMDC. (b) MMCCC. (c) FCMDC. (d) MMCCC.

Fig. 8 shows the simulation results in the up conversion mode. When the low voltage side is energized by a 12-V source and the HV side is loaded by a 30 Ω load, the conventional converter produces an average output of only 37 V, while the new MMCCC produces close to 60 V. They are shown in Fig. 8(a) and (b), respectively. Fig. 8(c) and (d) show the input currents taken from the 12-V source, and the ripple present

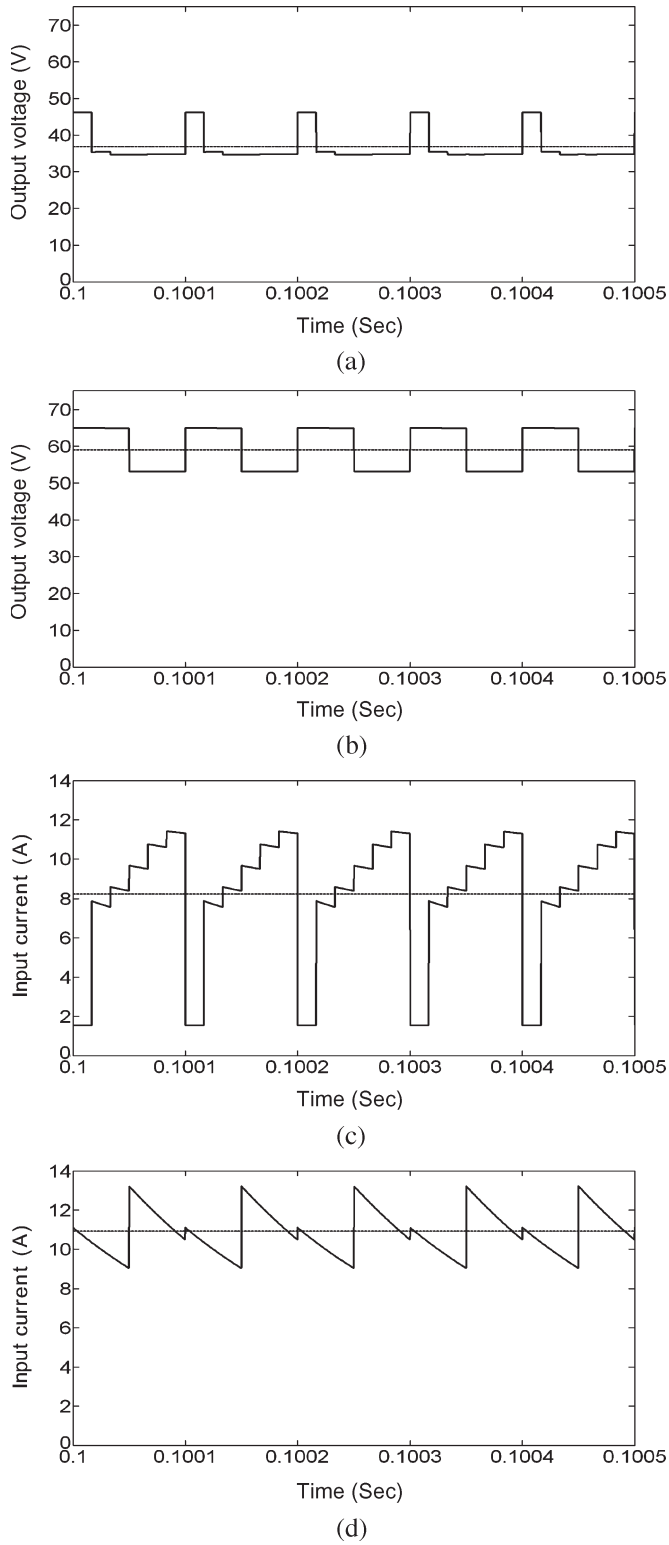

Fig. 8. Converters' simulation results in up-conversion mode ($V_{\rm in} = 12$ V, $R_{\rm load} = 30\ \Omega$). (a) FCMDC. (b) MMCCC. (c) FCMDC. (d) MMCCC.

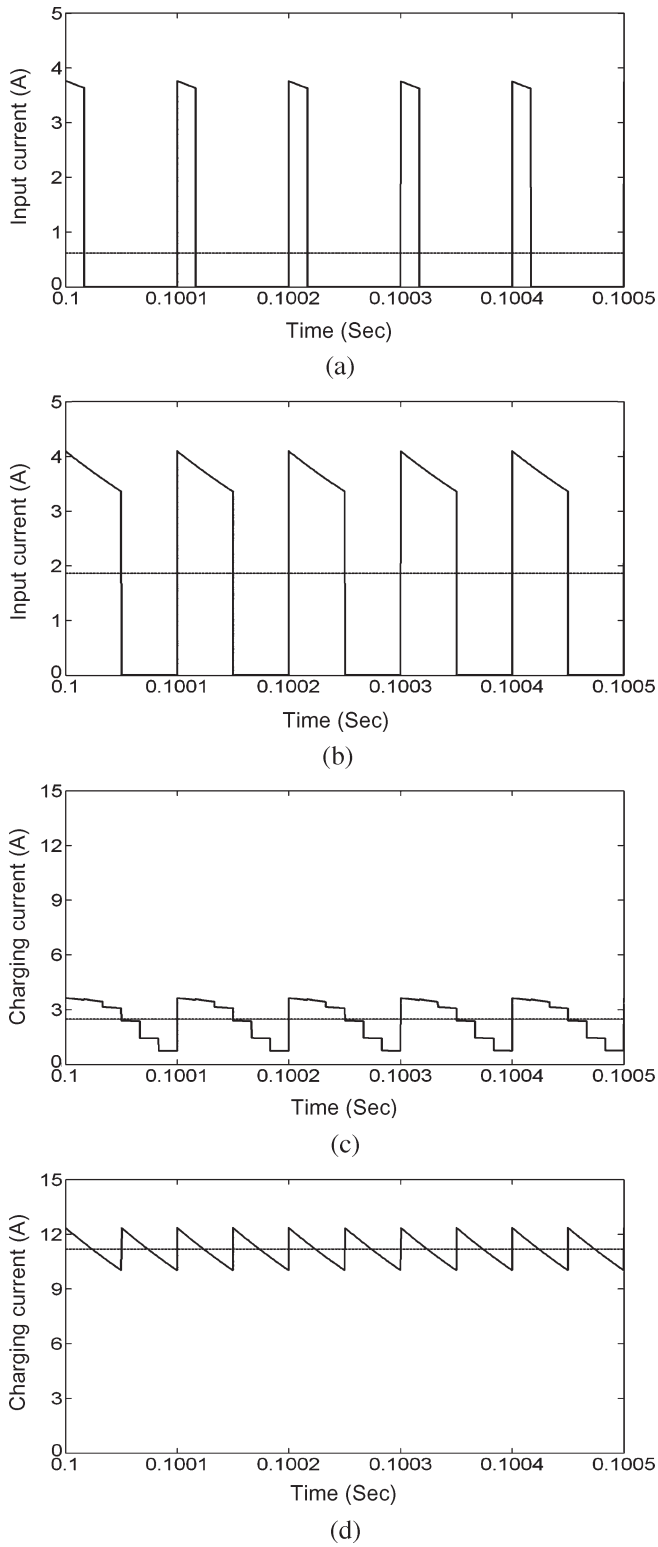

Fig. 9. Simulation results of the converters' battery charging performance in down-conversion mode ($V_{\rm in} = 80$ V). (a) FCMDC. (b) MMCCC. (c) FCMDC. (d) MMCCC.

in the MMCCC is substantially less than the conventional converter. Moreover, it takes more power from the 12-V source and transfers it to the HV side. By virtue of the higher component utilization, the MMCCC can deliver more power than the conventional converter using the same components.

Fig. 9(a)–(d) shows the simulation results in the battery-charging (down conversion) mode. They clearly show that the average output charging current of the MMCCC is substantially higher than the conventional circuit although the input (HV side) peak current is almost the same for both cases.

IV. Features of the New Proposed Topology

A. Advantages

The simulation results and the schematic of the new design explain many of its potential features. The new circuit is modular and requires a simple gate drive circuit. As there are only two switching states present in the circuit, the switching ripple present at the output is always twice the frequency of the gate drive signal, whereas the effective switching frequency is N times of the gate drive signal for an N-level conventional converter. The new converter can be operated at a clock frequency $N/2$ times higher than the FCMDC where N is the conversion ratio. This feature permits the designer to use small-sized capacitors to attain the same output current rating.

The new converter has better voltage regulation compared to the conventional converter. In the up conversion mode, the FCMDC's input current flows through $(N-1)$ series connected transistors and one diode. The situation will be worse when the conventional converter attempts to deliver current from the HV side to the low voltage side. During buck mode of operation, the current flows through $(N-1)$ diodes and only one transistor. Usually, the voltage drop across a diode is higher than the voltage drop across a transistor, and thereby the regulation is limited during this mode. In contrast, the current flows through at most three transistors or diodes at any time in the new converter irrespective of the conversion ratio. The reduced number of series connected devices in the new converter is responsible for less voltage drop and better regulation.

The modular nature of the converter can also provide redundancy in the system. Any module can be operated in active state or in bypass state. In Fig. 3, four active modules are used to achieve a conversion ratio of 5. However, any of these four modules can be operated in bypass state. For example, inside the fourth module from the left, if SR_7 is permanently on and SB_6 and SR_6 are permanently off, this module does not take part in the operation of the converter, and the conversion ratio becomes 4.

Using the redundancy feature, the fault bypass operation can be implemented in the system using a single MMCCC unit. If any fault is detected inside any of the active modules in the system, the corresponding module is bypassed and replaced by another good module which was in bypass state so far. To ensure this operation, there must be some redundant modules available in the system. Moreover, to continue this operation of the converter, the top transistor in each module (such as SB_2 in the leftmost module in Fig. 3) must ensure fault-free operation, meaning this transistor cannot fail. If any of these top transistors fail, it is not possible to continue the operation of the circuit. In addition, the two other transistors in each module are allowed to experience an open circuit fault. In most cases, a damaged MOSFET creates an open circuit fault, and if these two transistors in each module (SB_1 and SR_2) have an open circuit fault, the module can be bypassed by turning on SB_2 permanently.

B. Disadvantages

The new circuit suffers from one limitation. The MMCCC uses more transistors than what is required for the conventional FCMDC with the same conversion ratio. For an N-level design, the conventional converter requires $2N$ transistors whereas the new converter needs $(3N-2)$ transistors. Thus, for a five-level design, the conventional converter needs ten transistors while 13 transistors are needed for the new converter.

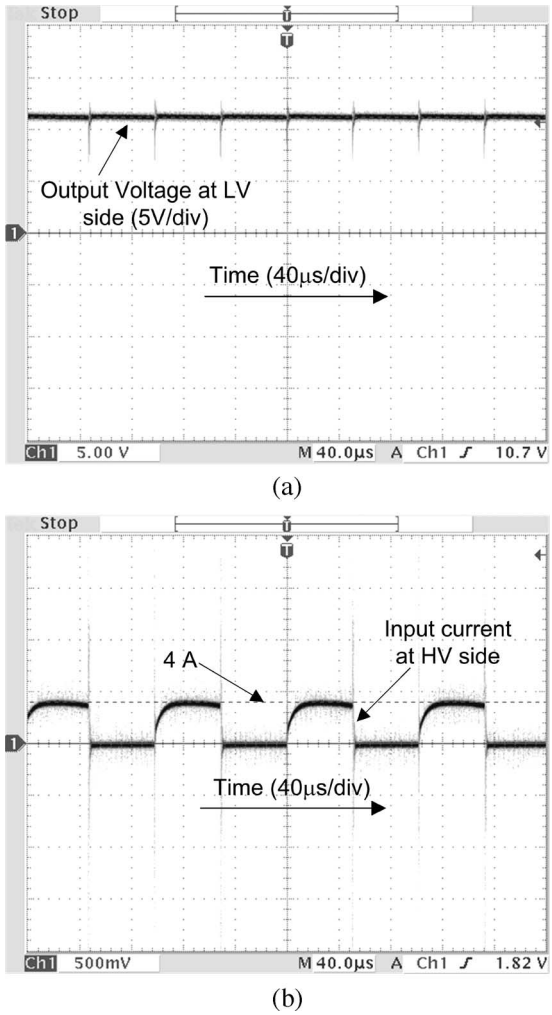

Fig. 10. Experimental results for the down-conversion mode. (a) Output voltage. (b) Input current (1 V = 10 A).

V. Experimental Results

A six-level 500-W prototype of the proposed design has been constructed on a printed circuit board shown in Fig. 14. The circuit was designed for a maximum $V_{\rm HV}$ of 100 V. For a six-level design, five modules are used and each module will have its own gate drive circuit onboard. Inside one module, two bootstrap gate drive circuits (IR2011) have been used to drive three IRFI540N MOSFETs. These MOSFETs have an ON state resistance of 52 mΩ and they are rated at 20 A. An onboard dc–dc converter has been used to drive the top transistor in each module (transistor SB_1 in Fig. 4). General-purpose 1000 μF 100 V electrolytic capacitors having 0.1 Ω ESR have been used in the circuit. A main board has been built in such a way that each module is connected to the main board through a ten-pin header. Thus, if there is a fault in any of the modules, either it can be bypassed by the onboard fault clearing circuit

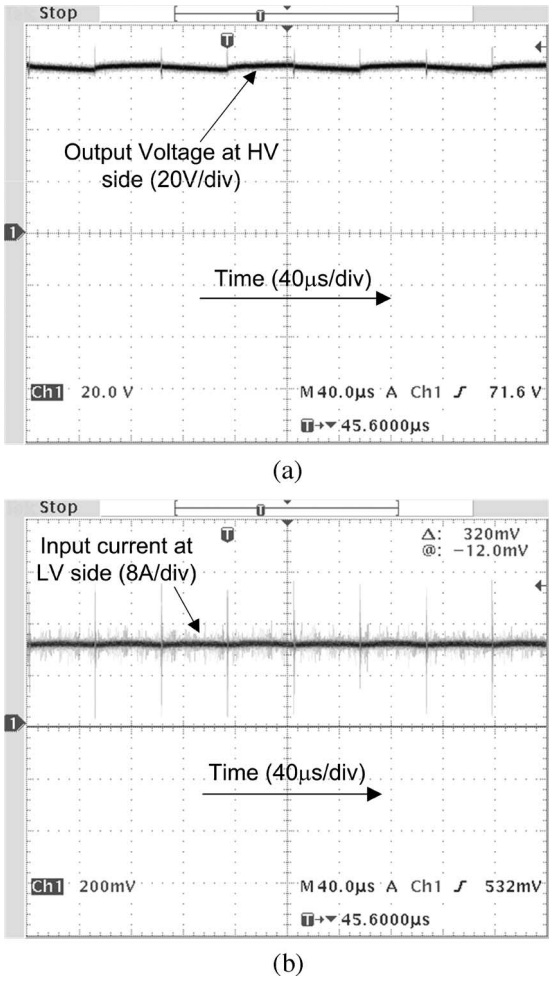

Fig. 11. Experimental results for the up-conversion mode. (a) Output voltage. (b) Input current (100 mV = 4 A).

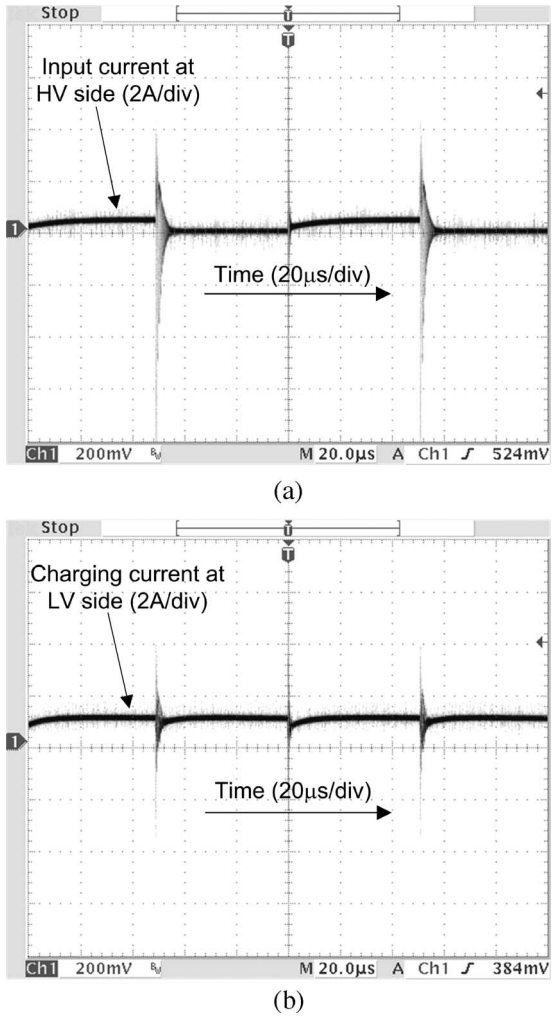

Fig. 12. Experimental results for the battery charging mode. (a) Input current (100 mV = 1 A). (b) Charging current (100 mV = 1 A).

or it can be physically disconnected from the main board and replaced by another good module.

A multimeter has been used to measure all the voltages and currents. Like the simulation, this six-level converter was tested in three steps. In the first step, the down-conversion operation was tested by connecting a 75 V source to the HV side of the converter. A 1 Ω resistive load from a programmable load bank was connected across the output, and the voltage wave shape was recorded. Because of the resistive nature of the load, the current will have the same wave shape like the voltage wave.

Fig. 10(a) shows the output voltage of the MMCCC, and Fig. 10(b) shows the input current wave shape. Thus, the peak input current was found to be 4 A (400 mV drop across a 0.1 Ω resistor), which is the same as that found in the simulations [Fig. 7(d)]. Fig. 11 summarizes the experimental results in the up conversion mode. In this up conversion mode, a 65.3 V output is produced from a 12 V input with 30 Ω loading at the HV side. The output voltage is shown in Fig. 11(a). The input current is shown in Fig. 11(b).

In the battery-charging mode, an 80 V source was connected at the HV side, and the low voltage side of the converter was connected to the battery. Fig. 12(a) shows the input current and Fig. 12(b) shows the output or charging current. For this setup, the maximum charging current to the 12 V battery was only 1.2 A, which is much less than the simulation result. The reason for this low current was the increased battery voltage, which was 13.2 V. In the simulation, the battery voltage was considered constant at 12 V. Between the simulation and experimental figures, there was a difference between the units used in the x-axis. In simulation results, the unit of the time axis was in seconds; however, in the experimental results, the unit was in microseconds.

In the up-conversion and battery charging mode, some differences were observed between the simulation and experimental results. In Fig. 8(b), the simulated output voltage at HV side was a dc voltage varying between two levels of around 55 and 65 V. However, in the experiment, the variation in voltage at the HV node was very small. The reason was that during the experiment, a capacitor having the same value as C_6 was connected at the HV node, and it was responsible for limiting the voltage variation at the HV side. In the simulation, this capacitor was not used. In addition, there was a difference between the ESR (of the capacitors) values used for simulation and experimental results. The actual value of the ESR of the capacitors was much lower than the 0.1 Ω that was assumed in the simulation. For this reason, during the up-conversion mode,

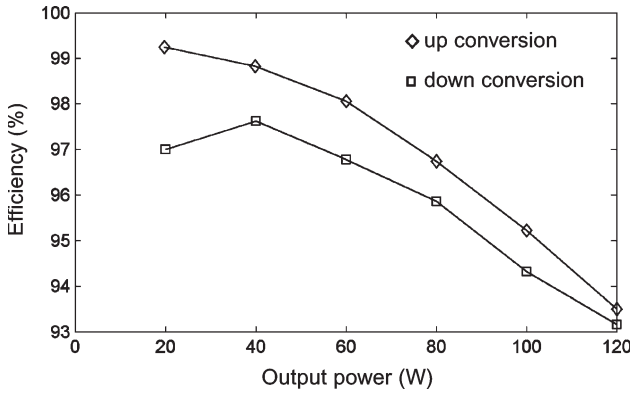

Fig. 13. Efficiency of the MMCCC at different power outputs.

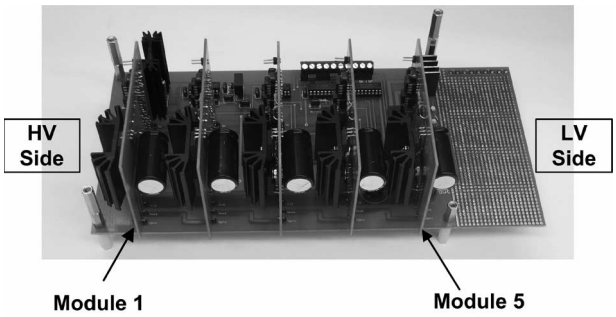

Fig. 14. 500-W six-level prototype.

the input current in the experiment had a smaller ripple than in the simulation.

The converter was tested to measure the efficiency at different operating conditions. Fig. 13 shows the efficiency of the converter at different loading conditions for both up and down conversion mode, and Fig. 14 shows the actual prototype. A maximum efficiency of 99.1% was achieved at 20 W power output (in the up-conversion mode). The relatively higher ON-state resistance (52 mΩ) of the transistors causes the efficiency to drop at higher loading conditions. However, when the converter will be designed for a higher power rating, larger MOSFETs should lead to low ON-state loss and better efficiency at higher output power. Fig. 13 also shows that the MMCCC converter's efficiency at any loading condition is higher in the up-conversion mode than in the down-conversion mode. This happens because in the up-conversion mode, the number of series-connected active (ON) transistors (MOSFET) in one operating cycle is higher than the total number of current-carrying diodes in the current path. However, in the down-conversion mode, the situation is simply opposite. There are more series-connected diodes than the number of active (ON) MOSFETs. Since the voltage drop across the diode is higher than the drop across a MOSFET, the total conduction loss involved in the down-conversion mode was higher than in the up-conversion mode. In both up and down-conversion modes, the switching loss was almost the same, and this is why the efficiency in the up-conversion mode was found higher than in the down-conversion mode.

VI. Conclusion

A new topology of a modular multilevel dc–dc converter has been proposed and validated by both simulation and experimental results. The new converter outperforms some conventional switched capacitor converters by having a more modular construction, high power transfer capability, simpler gate drive circuit requirement, high frequency operation capability, onboard fault bypassing, and bidirectional power management capability. By virtue of the modular topology, the circuit obtains redundancy and the reliability can be increased significantly. The modular nature also introduces the use of one additional level to establish the fault bypassing and bidirectional power flow management. Thus, this converter could be a suitable choice in various applications to establish bidirectional power management between buses having different voltages.

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