Charge Balance Control Schemes for Cascade Multilevel Converter in Hybrid Electric Vehicles

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***Abstract*—This paper presents transformerless multilevel converters as an application for high-power hybrid electric vehicle (HEV) motor drives. Multilevel converters: 1) can generate near-sinusoidal voltages with only fundamental frequency switching; 2) have almost no electromagnetic interference or common-mode voltage; and 3) make an HEV more accessible/safer and open wiring possible for most of an HEV's power system. The cascade inverter is a natural fit for large automotive hybrid electric drives because it uses several levels of dc voltage sources, which would be available from batteries, ultracapacitors, or fuel cells. Simulation and experimental results show how to operate this converter in order to maintain equal charge/discharge rates from the dc sources (batteries, capacitors, or fuel cells) in an HEV.**

***Index Terms*—Cascade inverter, hybrid electric vehicle, motor drive, multilevel converter, multilevel inverter.**

I. Introduction

DESIGNS for heavy duty hybrid electric vehicles (HEVs) that have large electric drives such as tractor trailers, transfer trucks, or military vehicles will require advanced power electronic inverters to meet the high-power demands ($>$ 100 kW) required of them. Development of large electric drive trains for these vehicles will result in increased fuel efficiency, lower emissions and, likely, better vehicle performance (acceleration and braking).

Transformerless multilevel inverters are uniquely suited for this application because of the high VA ratings possible with these inverters [1]. The multilevel voltage-source inverters' unique structure allows them to reach high voltages with low harmonics without the use of transformers or series-connected synchronized-switching devices. The general function of the multilevel inverter is to synthesize a desired voltage from several levels of dc voltages. For this reason, multilevel inverters can easily provide the high power required of a large electric traction drive. For parallel-configured HEVs, a cascaded H-bridges inverter can be used to drive the traction motor from a set of batteries, ultracapacitors, or fuel cells. The use of a cascade inverter also allows the HEV drive to continue to operate even with the failure of one level of the inverter structure [2].

Multilevel inverters also have several advantages with respect to hard-switched two-level pulsewidth-modulation (PWM) adjustable-speed drives (ASDs). Motor damage and failure have been reported by industry as a result of some ASD inverters' high-voltage change rates (dV/dt), which produced a common-mode voltage across the motor windings. High-frequency switching can exacerbate the problem because of the numerous times this common-mode voltage is impressed upon the motor each cycle. The main problems reported have been "motor bearing failure" and "motor winding insulation breakdown" because of circulating currents, dielectric stresses, voltage surge, and corona discharge [3]–[5].

Multilevel inverters overcome these problems because their individual devices have a much lower dV/dt per switching and they operate at high efficiencies because they can switch at a much lower frequency than PWM-controlled inverters.

Three-, four-, and five-level rectifier–inverter drive systems that have used some form of multilevel PWM as a means to control the switching of the rectifier and inverter sections have been investigated in the literature [6]–[10]. Multilevel PWM has lower dV/dt than that experienced in some two-level PWM drives because switching is between several smaller voltage levels. However, switching losses and voltage total harmonic distortion (THD) are still relatively high for some of these proposed schemes.

This paper proposes using fundamental frequency switching at the higher amplitude modulation indexes with different control methods to maintain the charge balance on the inverter dc link devices. At lower amplitude modulation indexes, a unique multilevel PWM technique is employed.

II. Cascaded H-Bridges Structure and Operation

A cascade multilevel inverter consists of a series of H-bridge (single-phase full-bridge) inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from several separate dc sources (SDCSs), which may be obtained from batteries, fuel cells, or ultracapacitors in an HEV. Fig. 1 shows a single-phase structure of a cascade inverter with SDCSs [11]. Each SDCS is connected to a single-phase full-bridge inverter. Each inverter level can generate three different voltage outputs, $+V_{\rm dc}$, 0, and $-V_{\rm dc}$ by connecting the dc source to the ac output side by different combinations of the four switches, S_1, S_2, S_3, and S_4.

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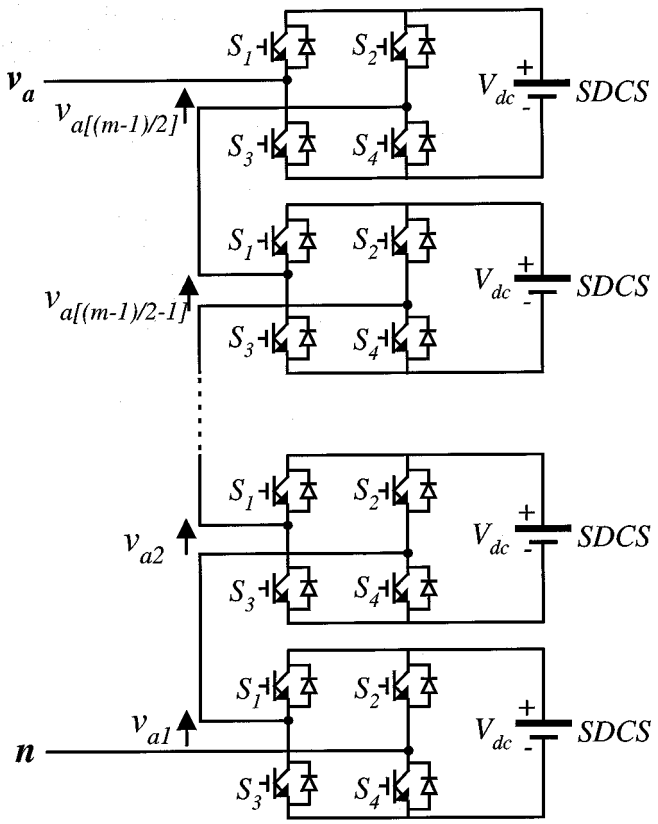

Fig. 1. Single-phase structure of a multilevel cascaded H-bridges inverter.

The ac output of each level's full-bridge inverter is connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels in a cascade inverter is defined by $m = 2s + 1$, where s is the number of dc sources. An example phase voltage waveform for an 11-level cascaded inverter with five SDSCs and five full bridges is shown in Fig. 2. The phase voltage $v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$.

With enough levels, using this fundamental switching technique results in an output voltage of the inverter that is almost sinusoidal. For the 11-1evel example shown in Fig. 2, the waveform has less than 5% THD with each of the H-bridge's active devices switching only at the fundamental frequency. Each H-bridge unit generates a quasi-square waveform by phase shifting its positive and negative phase legs' switching timings. Fig. 2(b) shows the switching timings to generate a quasi-square waveform. Note that each switching device always conducts for 180° (or 1/2 cycle) regardless of the pulsewidth of the quasi-square wave. This switching method makes all of the active devices' current stress equal.

For a stepped waveform such as the one depicted in Fig. 2 with s steps, the Fourier transform for this waveform is as follows:

$$v(\omega t) = \frac{4V_{\rm dc}}{\pi} \sum_n \left[\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)\right] \cdot \frac{\sin(n\omega t)}{n}, \text{where } n = 1, 3, 5, 7, \ldots. \quad (1)$$

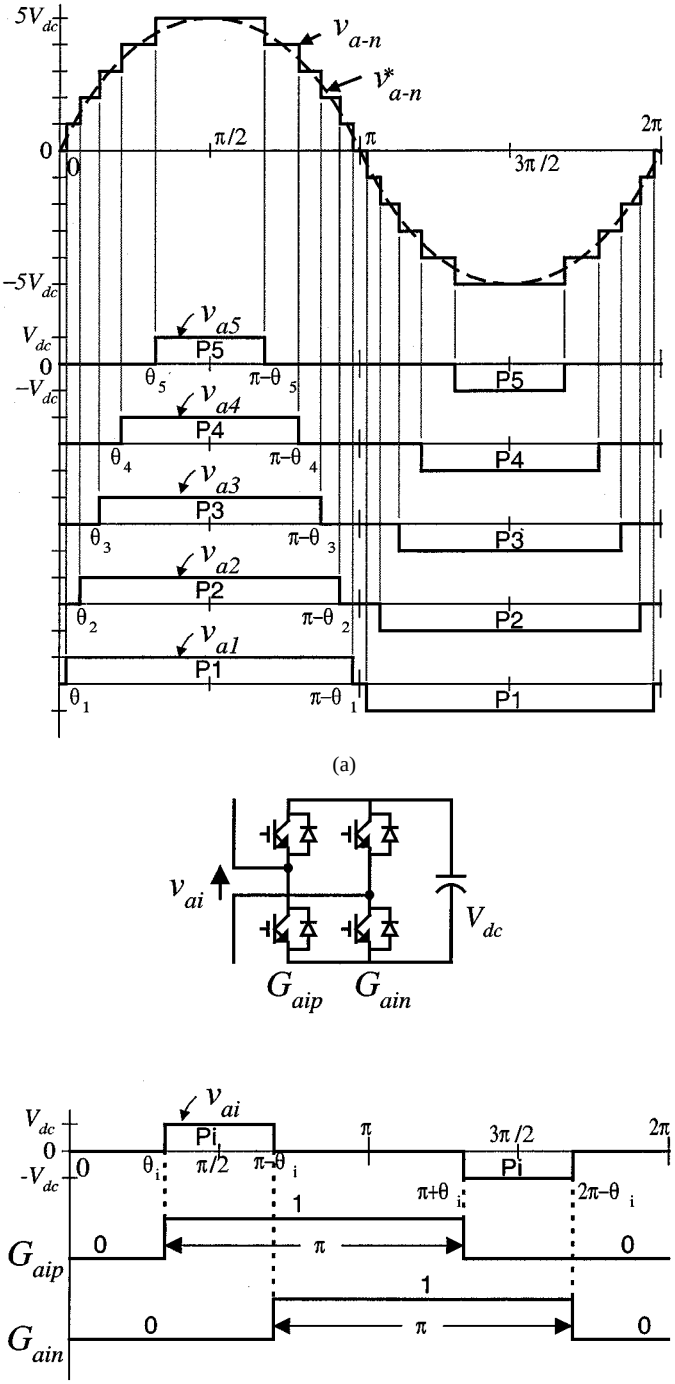

Fig. 2. Waveforms and switching method of the 11-level cascade inverter.

From (1), the magnitudes of the Fourier coefficients when normalized with respect to $V_{\rm dc}$ are as follows:

$$H(n) = \frac{4}{\pi n}\left[\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)\right], \quad \text{where } n = 1, 3, 5, 7, \ldots. \quad (2)$$

The two predominant methods in choosing the switching angles, $\theta_1, \theta_2, \ldots \theta_n$ include: 1) eliminating the lower frequency

dominant harmonics and 2) minimizing the THD. The more popular of the two techniques to reduce THD is to eliminate the lower dominant harmonics and filter the higher residual frequencies. Using this method for the 11-level case in Fig. 2, the 5th, 7th, 11th, and 13th harmonics can be eliminated with the appropriate choice of the conducting angles. One degree of freedom is used so that the magnitude of the output waveform corresponds to the reference amplitude modulation index m_a, which is defined as $V_L^*/V_{L\max}$, where V_L^* is the amplitude command of the inverter output phase voltage and $V_{L\max}$ is the maximum attainable amplitude of the converter, i.e., $V_{L\max} = s \cdot V_{\rm dc}$. The equations from (2) for this case will be (3), as shown at the bottom of the page.

The set of nonlinear transcendental equations (3) can be solved by an iterative method such as the Newton–Raphson method or by using trigonometric identities to expand the $\cos(n\theta)$ terms and then using the theory of resultants to solve a set of polynomial equations [16]. The correct solution to (3) means that the output voltage of the 11-level inverter will not contain the 5th, 7th, 11th, and 13th harmonic components.

The switching angles may also be solved to minimize the THD. The THD for the voltage waveform may be defined as

$$\text{THD}\% = 100 \cdot \sqrt{\left(\frac{[v(t)]_{\rm RMS}}{[v_1(t)]_{\rm RMS}}\right)^2 - 1} \tag{4}$$

where the rms of the cascaded multilevel waveform $v(t)$ with s steps is

$$[v(t)]_{\rm RMS} = V_{\rm dc}\sqrt{s^2 - \frac{2}{\pi}\sum_{k=1}^{s}(2k-1)\,\theta_k} \tag{5}$$

and the fundamental rms value of $v(t)$ is

$$[v_1(t)]_{\rm RMS} = \frac{V_{\rm dc}2\sqrt{2}}{\pi}\sum_{k=1}^{s}\cos(\theta_k). \tag{6}$$

To minimize (4), the partial derivative can be taken with respect each switching angle and set to zero. A generalized formula can be developed by substituting (5) and (6) into (4) and differentiating to determine the partial derivatives. This simplified general formula was then found to be

$$\frac{\partial THD^2}{\partial \theta_n} = (2n-1)\sum_{k=1}^{s}\cos(\theta_k) + \left[2\sum(2k-1)\,\theta_k - \pi s^2\right]\sin(\theta_n) = 0 \tag{7}$$

where n is the nth switching angle. Using (7) for a five-step waveform produces five nonlinear transcendental equations with five variables whose solutions are the angles that minimize the THD.

In comparing the two methods for a five-step inverter (11-level) and the same fundamental frequency magnitude, the THD minimization method yielded a THD of 7.26% and the harmonic elimination yielded a THD of 8.48% without filtering. Because the THD minimization method has only a slight improvement in the THD of the output waveform, the harmonic elimination method is preferred, because some small filters can nearly eliminate most of the leftover high-frequency harmonics. Also, note the THD values shown above include triplen harmonics because the analysis was done for phase voltages. These triplens will not appear in the line–line voltages and the THD would be below 5% in both cases.

Note that the equations above have assumed the ideal case in which the separate dc sources are all equal in magnitude and invariant. This may not be the case in a typical HEV. In the following sections, a description of some control methods to maintain the dc sources to near the same value is described and analysis for when the dc sources have small variations is also shown.

III. Cascaded H-Bridges Structure for HEV Drive

In the parallel HEV configuration, as shown in Fig. 3, the energy storage system, batteries or ultracapacitors, would provide a "power assist" in addition to the internal combustion engine by sending energy through an inverter driving a motor that is mechanically coupled to a summing gear. This parallel configuration can be operated in three modes: 1) as a pure electric vehicle using the electric motor only; 2) as a conventional vehicle using only the internal combustion engine; or 3) using both the engine and the electric motor at the same time. The electric motor can also be used as a generator where it supplies energy to the energy storage system with the cascade converter acting in rectification mode. Note that Fig. 3 also provides for a means of connecting the vehicle to an external charger and using it to charge the batteries as well.

From Fig. 2, note that the duty cycle for each of the voltage levels is different. If this same pattern of duty cycles is used on a motor drive continuously, then the level-1 battery (or other SDCS) is cycled on for a much longer duration than the level-5 battery. This means that the level-1 battery will discharge much sooner than the level-5 battery. However, by using a switching pattern swapping scheme among the various levels every 1/2 cycle as shown in Fig. 4, all batteries will be equally used (discharged) or charged.

The combination of the 180° conducting method [Fig. 2(b)] and the pattern-swapping scheme (Fig. 4) make the cascade inverter's voltage and current stresses the same and helps to maintain the batteries' charge state balanced.

$$\begin{aligned}
\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) &= 0\\
\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) &= 0\\
\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) &= 0\\
\cos(13\theta_1) + \cos(13\theta_2) + \cos(13\theta_3) + \cos(13\theta_4) + \cos(13\theta_5) &= 0\\
\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \cos(\theta_5) &= 5m_a
\end{aligned} \tag{3}$$

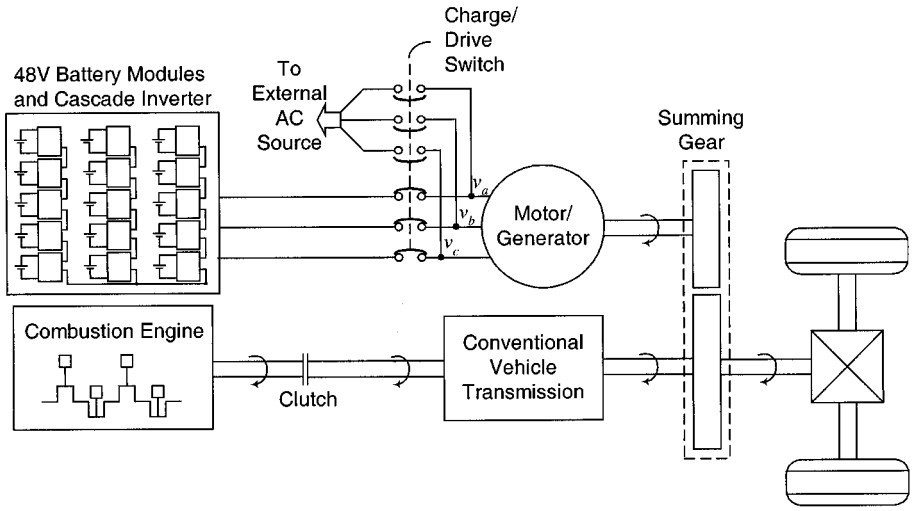

Fig. 3. Parallel-configured HEV using cascaded multilevel converter.

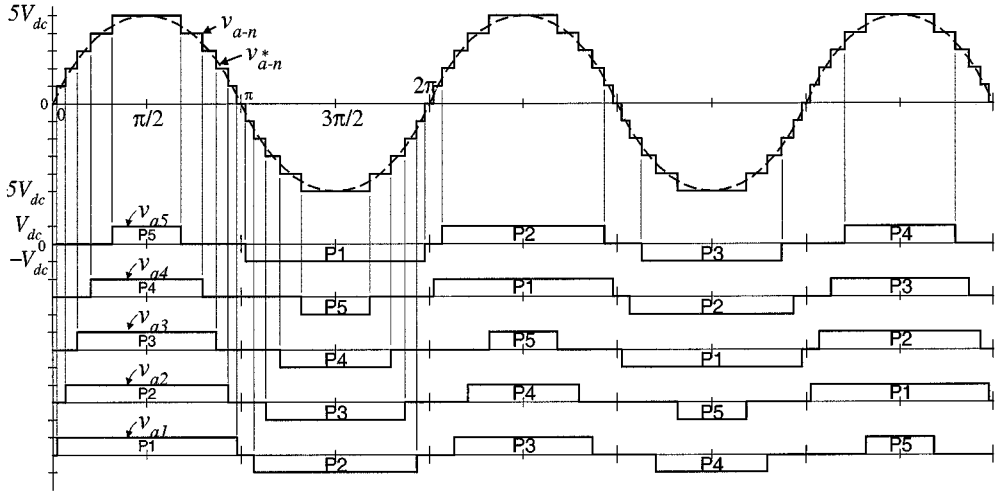

Fig. 4. Switching pattern swapping of the 11-level cascade inverter for balancing battery charge.

Fig. 5 shows the system configuration and control block diagram of an ASD using an 11-level cascade inverter. The duty-cycle lookup table contains switching timings to generate the desired output voltage as shown in Fig. 2. The five switching angles, θ_i ($i = 1$, 2, 3, 4, and 5), are calculated offline to minimize harmonics for each modulation index m_a.

A prototype three-phase 11-level wye-connected cascaded inverter has been built using MOSFETs as the switching devices. A battery bank of 15 SDCSs of 48 Vdc each fed the inverter (five SDCSs per phase). The control of the inverter was via a 32-bit digital signal processor. The switching timing angles θ_i (i =1, 2, 3, 4, and 5), were calculated offline for the following modulation indexes, ($m_a = 0.1, 0.2, \ldots, 1.0$). A table of ten switching patterns corresponding to these modulation indexes was stored in the controller as 1024 states per cycle. A constant voltage/frequency control technique was applied to the motor drive system. As a user interface, a potentiometer was adjusted to apply an external 0–3-V signal to the controller. The 0–3-V signal mapped directly to a 0–60-Hz fundamental frequency for the gate signals sent to the inverter. Also, the switching patterns corresponding to the various modulation indexes were mapped from the 0–3-V external control signal.

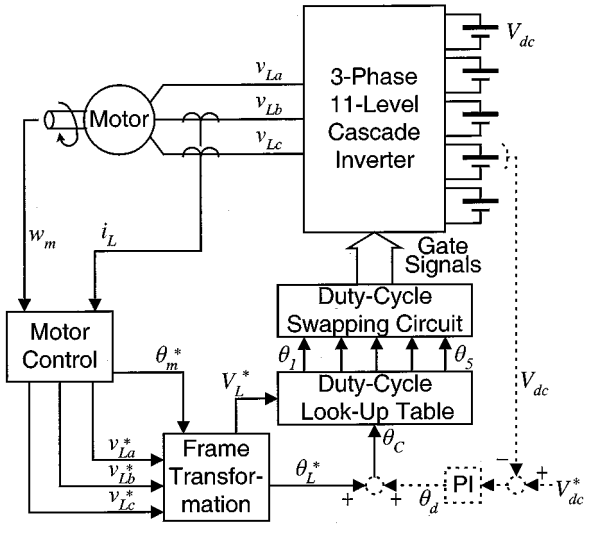

Fig. 5. System configuration of an ASD using the cascade inverter.

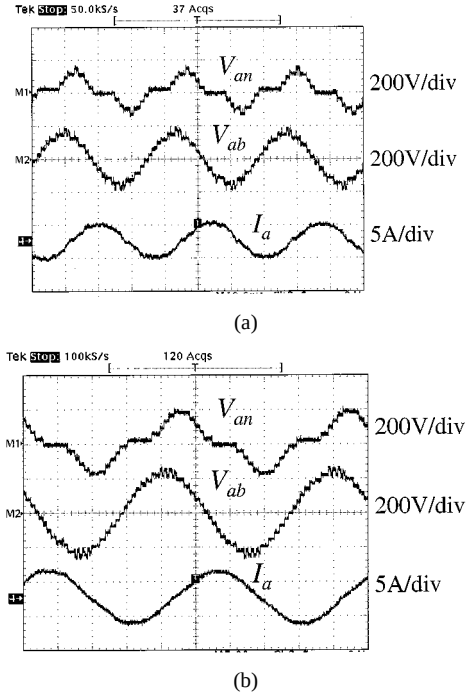

Fig. 6. Experimental waveforms of a battery-fed cascade inverter prototype driving an induction motor at (a) 50% rated speed and (b) 80% rated speed.

Fig. 6 shows experimental waveforms of the 11-level battery-fed cascade inverter prototype driving a 208-V three-phase induction motor at 50% and 80% rated speed using the aforementioned fundamental frequency switching scheme. As can be seen from the waveforms, both the line-line voltage and current are almost sinusoidal. Electromagnetic interference (EMI) and common-mode voltage are also much less than what would result from a two-level PWM inverter because of the inherently low dV/dt (21 times less than a two-level drive) and sinusoidal voltage output.

IV. Multilevel PWM at Low Modulation Indexes

At low modulation indexes ($m_a < 0.5$), use of V/Hz type of control and fundamental frequency switching may result in poor quality waveforms with excessive THD. At these lower modulation indexes, the use of multilevel PWM may be more appropriate [11]. When performing multilevel PWM at low modulation indexes, this allows rotation of the pulses among the various physical levels (H-bridges) of the cascade inverter. A pulse rotation technique similar to the one used for fundamental frequency switching of cascade inverters described in [12] can be used even when a PWM output voltage waveform is desired. Normal carrier-based PWM generates the switching signals, but prior to being sent to the gate drives of the active devices, the signals are sequentially rotated to a different level. The effect is that the output waveform can have a high switching frequency but the individual levels can still switch at a constant switching frequency of 60 Hz if desired.

Example PWM pulses for this type of pulse rotation control are shown in Fig. 7. Pulses (V_{a1}, V_{a2}, and V_{a3}) are shown for three of the five H-bridges that comprise the a phase of the inverter. The line–neutral voltage waveform V_{an} is

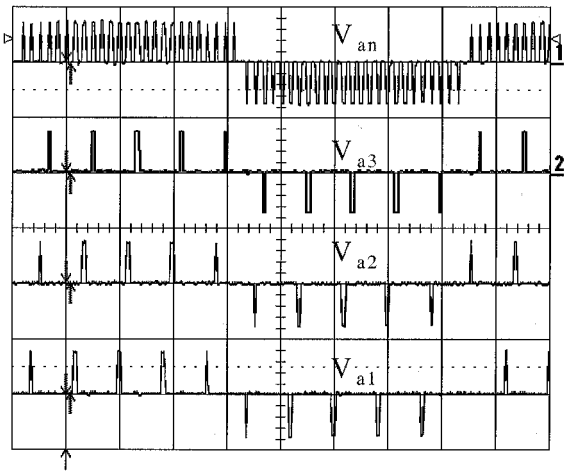

Fig. 7. Pulse rotation in an 11-level prototype cascade inverter (50 V/div, 10 ms/div).

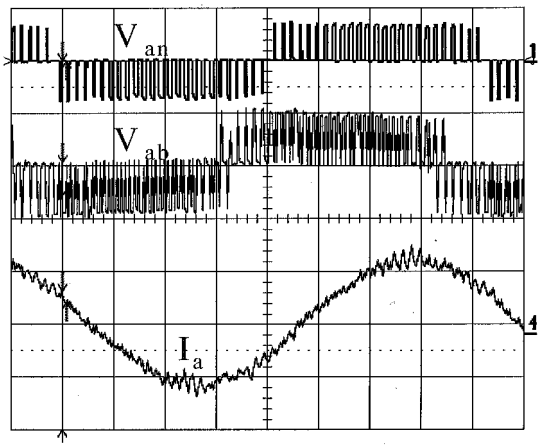

Fig. 8. Cascade inverter waveforms at 12-Hz fundamental frequency operation (50 V/div, 5 A/div, 10 ms/div).

composed of the sum of the pulses from all five H-bridges. While the switching frequency of each individual H-bridge is kept constant at 60 Hz, the effective switching frequency of the phase–neutral voltage is 300 Hz. This technique allows a multilevel cascaded inverter to achieve a quality PWM output waveform at low modulation indexes without resorting to high-frequency switching.

Fig. 8 shows the phase and line voltage and current waveforms for the driven induction motor. For an amplitude modulation index of 0.2 (to run the motor at 1/5 rated speed), the inverter outputs a 12-Hz fundamental frequency voltage waveform that has three levels line–neutral (V_{an}) and three levels line–line (V_{ab}). Fig. 9 shows the same waveforms for operating at an amplitude modulation index of 0.3, or reference frequency of 18 Hz. For this operating condition, the inverter's line–line voltage V_{ab} has five levels.

An important detail to ensure that all the batteries will be equally charged/discharged when performing multilevel PWM is that the number of phase-neutral output voltage pulses for each half cycle of the fundamental frequency waveform should *not* be equal to an integer multiple of the number of H-bridges in one phase of the inverter. Otherwise, each H-bridge would

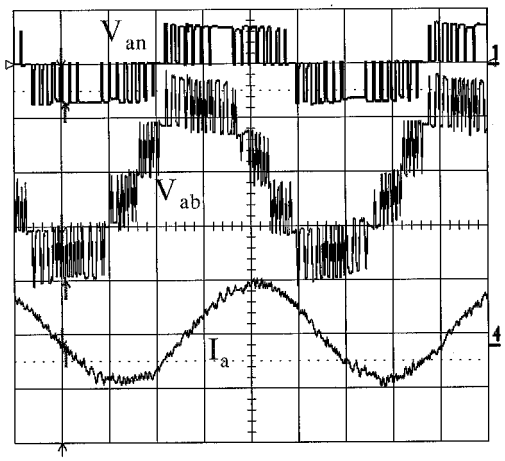

Fig. 9. Cascade inverter waveforms at 18-Hz fundamental frequency operation (50V/div, 5 A/div, 10 ms/div).

generate the same pulsewidths every half cycle, which would lead to different discharge (or charge) rates among the batteries.

V. Variant Voltage-Source Considerations

In most of the present HEV applications, the primary energy storage component is the lead-acid battery. As shown earlier, the duty cycle can be rotated using a set pattern if the batteries have equal magnitudes. However, practical batteries may not have equal charge states even with the charge control scheme outlined previously. In this case, the control would require monitoring each of the battery's charge state separately and assigning the one with the lowest charge the shortest duty cycle and the one with the highest charge the longest duty cycle. In this section, an analysis of the voltage THD and harmonic content is done showing how to sort the order of connection of the separate dc voltage sources (batteries), when the maximum variation of the voltages is $\pm 10\%$. This would mean that a nominal 12-V battery would be at 10.8 V in the nearly discharged state and 13.2 V at a fully charged state. Also, for the following analysis, it was assumed the separate dc sources had values as follows:

$$V_a = [1.10 \quad 1.05 \quad 1.00 \quad 0.95 \quad 0.90]^T. \tag{8}$$

Two methods are considered for determining the switching angles for each level. The first method determines and uses the switching angles assuming the dc sources are all the same. Then, the sources are arranged such that the one with the highest voltage is turned on first and the one with the lowest voltage is turned on last, which is the same order as shown in (8). Even though using the harmonic elimination method, some harmonics will still appear at the lower order harmonics because the angles have not been optimized for the real values of the SDCSs. In addition, the fundamental magnitude will deviate slightly from what it is assumed to be for equal SDCSs.

Using this strategy with the voltage values shown in (8) and for an amplitude modulation index of 1, the THD of the waveform was 7.82%, which was actually *less* than the case where the separate dc sources were identical (8.19%). The harmonic distortion contributed by the lower order harmonics (5th, 7th, 11th, and 13th) was only 0.26%. In addition, the fundamental magnitude increased by 1.7% from its desired value.

Note that the five voltage sources can be arranged in 120 different ways. For the example shown above, the lowest THD did not correspond to the order shown in (8), which is what is desired to help achieve charge equalization. A THD of 7.81% was achieved using the voltages in the following order:

$$V_a = [1.10 \quad 1.00 \quad 1.05 \quad 0.95 \quad 0.90]^T.$$

However, by arranging the voltages from highest to lowest kept the THD within 5% of the value for the optimum (lowest THD) arrangement when this scenario was analyzed for several different combinations of voltage levels and fundamental frequency amplitudes.

The second method also uses the harmonic elimination method, but recalculates the angles taking into account the variances in each of the separate dc sources. Using this method, the lower order harmonics are completely eliminated and the magnitude of the fundamental component will be exactly what is desired. For the same example as used previously, the THD of one voltage phase waveform is 8.49%, which as expected is almost identical to the THD found when the sources were identical (8.48%).

In summary, if the voltage of the separate dc sources is controlled such that the variation is small among the power sources, using the switching angles calculated assuming identical voltage sources is a viable option. In addition, if voltage or charge state of each of the separate dc sources is monitored, the control system should assign the highest duty cycle to the one with the most charge and the lowest duty cycle to the one with the least charge.

VI. Conclusions

A multilevel cascade inverter with separate dc sources has been proposed for use in HEV drives. Simulation and experimental results have shown that, with a control strategy that operates the switches at fundamental frequency, these converters have low output voltage THD and high efficiency and power factor.

In summary, the main advantages of using multilevel converters for hybrid electric drives include the following.

1) They are suitable for large VA-rated and/or high-voltage motor drives.
2) These multilevel converter systems have higher efficiency because the devices can be switched at minimum frequency.
3) Power factor is close to unity for multilevel inverters used as a rectifier to convert generated ac to dc.
4) No EMI problem or common-mode voltage/current problem exists.
5) No charge unbalance problem results when the converters are in either charge mode (rectification) or drive mode (inversion).

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