Start-Up and Dynamic Modeling of the Multilevel Modular Capacitor-Clamped Converter

Faisal H. Khan, *Member, IEEE*, Leon M. Tolbert, *Senior Member, IEEE*, and William E. Webb

***Abstract*—This paper will present the analytical proof of concept of the multilevel modular capacitor-clamped converter (MMCCC). The quantitative analysis of the charge transfer mechanism among the capacitors of the MMCCC explains the start-up and steady-state voltage balancing. Once these capacitor voltages are found for different time intervals, the start-up and steady-state voltages at various nodes of the MMCCC can be obtained. This analysis provides the necessary proof that explains the stable operation of the converter when a load is connected to the low-voltage side of the circuit. In addition, the analysis also shows how the LV side of the converter is $(1/N)$th of the HV side excitation when the conversion ratio of the circuit is *N*. In addition to the analytical and simulation results, experimental results are included to support the analytical proof of concept.**

***Index Terms*—DC–DC power conversion, power capacitors, power conversion, power electronics, power semiconductor switches.**

I. Introduction

CAPACITOR-clamped or switched-capacitor converters are based on capacitive energy transfer mechanisms, and can be designed to operate at very high efficiency. The multilevel modular capacitor-clamped dc–dc converter (MMCCC) presented in [1] had a capacitor-clamped modular architecture unlike many other dc–dc converters based on capacitor-clamped or charge-pump technology [2]–[15]. The MMCCC topology has a bidirectional power management feature, and multiple loads and sources can be simultaneously connected to this converter. MMCCC's various features and applications in hybrid electric and fuel cell automobiles were demonstrated in [16] and [17]. The originality and proof of concept of this topology was verified by several simulation and experimental results in these literatures. As the MMCCC topology is a capacitor-clamped circuit, the proper operation and the capability to produce a certain conversion ratio (CR) can be proven by knowing the various capacitor voltages during the start-up and steady-state operation of the converter.

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The MMCCC is inherently a bidirectional dc–dc converter. For this reason, it does not have a specific input or output. Rather, it has an HV side and a low-voltage (LV) side. If a voltage source of $V_{\rm HV}$ is connected to the HV side, the load connected at the LV side experiences a voltage of $V_{\rm LV}$. On the other hand, a voltage source $V_{\rm LV}$ connected at the LV side produces a load voltage of $V_{\rm HV}$ at the HV side. In both cases, $V_{\rm HV}/V_{\rm LV} = N$, where *N* is the CR of the circuit. The schematic of a five-level MMCCC is shown in Fig. 1.

This paper will provide the analytical derivation of the MMCCC voltage transfer mechanisms. The mathematical expressions rely on the MMCCC circuit's inherent nature to produce a specific CR. In addition, several simulation and experimental results are added to verify the analytical start-up and steady-state voltage expressions derived in this paper.

II. Basic Construction and Operation of the MMCCC

The basic operation of the MMCCC has some similarities with the flying capacitor multilevel dc–dc converter (FCMDC) shown in [2]–[5]. It was presented in [18] that the MMCCC exhibits some of the favorable properties of the FCMDC and the series–parallel converter [6], [7]. The property that achieves equal voltage stress across the transistors was adopted from the FCMDC topology, and the modular construction was adopted from the series–parallel converter. The MMCCC shown in Fig. 1 is a five-level MMCCC, and the circuit has a CR equal to 5. The terminology of voltage levels present in the circuit has been used slightly differently in this paper. Usually, a multilevel dc–dc converter with a CR equal to *N* is defined as an $(N + 1)$-level converter. This convention was adopted from multilevel inverters where zero voltage is a working voltage level in the circuit. However, zero voltage will not be considered as a voltage level for the MMCCC in this paper.

An *N*-level MMCCC circuit requires $(3N - 2)$ transistors, and the method of charge transfer requires two subintervals [1] shown in Fig. 2. Compared to the FCMDC topology, the requirement of only two subintervals, regardless of the CR of the circuit, makes it advantageous from the control point of view. Each transistor will be ON in one of the two subintervals and OFF in the other, which means that the transistors can be separated into two groups that have complementary operations. In the MMCCC shown in Fig. 1, transistors SR1–SR7 are activated in subinterval 1 and SB1–SB6 are activated in subinterval 2.

For ease of understanding, the working principle of the MMCCC is discussed in the down conversion or buck mode in this paper. In a five-level FCMDC, it takes five subintervals to complete the power transfer operation from the input to the output of the circuit. However, in the MMCCC, multiple

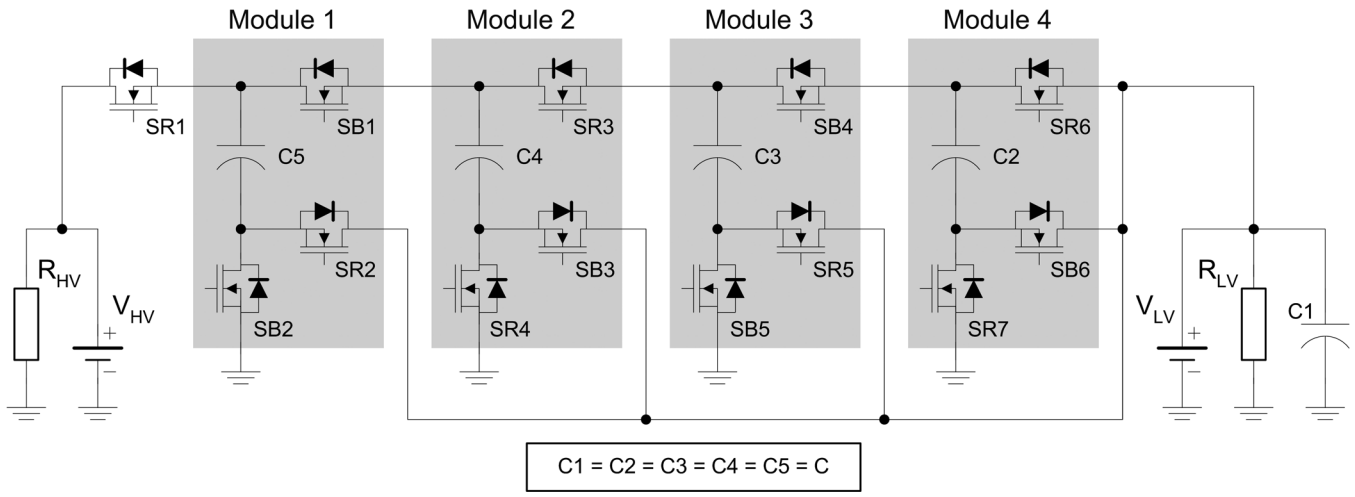


Fig. 1. Schematic of a five-level MMCCC circuit with four modules.

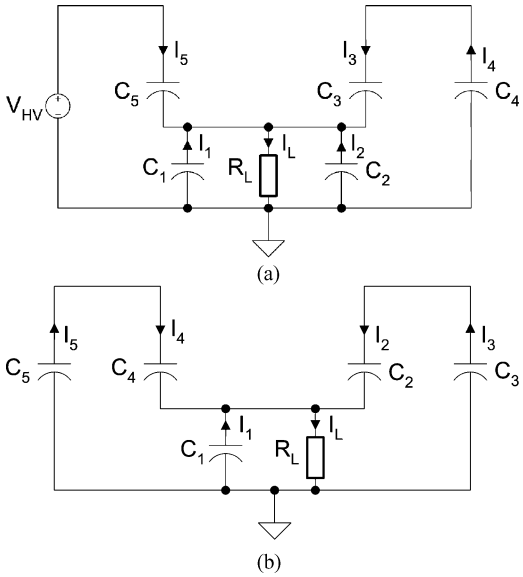


Fig. 2. Steady-state operational diagrams of a five-level MMCCC. (a) Schematic of state 1 or the first subinterval. (b) Schematic of state 2 or the second subinterval.

mutually exclusive charge–discharge operations are executed in only two subintervals. In the first subinterval, C_5 and C_1 are being charged from V_{HV}, and C_4 is discharged through C_3 and C_1. At the same time, C_2 is discharged to C_1. Thus, three operations are executed simultaneously. In the second subinterval, C_5 is discharged to C_4 and C_1, and C_3 is discharged to C_2 and C_1. Thus, a capacitor charged during one subinterval is discharged in the next subinterval. Although, it seems that C_1 is always being charged, and not discharged at any subinterval, the mathematical expression shows otherwise. It will be shown later how in each subinterval, C_1 is being charged for some time, and discharged for the remaining time in the subinterval. The charge–discharge mechanism of various capacitors inside the MMCCC is shown in Table I. In this table, the charge–discharge operation of the MMCCC is also compared with a five-level FCMDC. The detailed operating principle of the MMCCC can be found in [1] and [18].

TABLE I
CHARGE–DISCHARGE OPERATION IN VARIOUS SUBINTERVALS OF AN FCMDC AND MMCCC CONVERTER

FCMDC		MMCCC	
Sub interval no.	Operations	Sub interval no.	Operations
1	$V_{HV\rightarrow} C_5\uparrow + C_1\uparrow$	1	$V_{HV\rightarrow} C_5\uparrow + C_1\uparrow\downarrow$ $C_4\downarrow \rightarrow C_3\uparrow + C_1\uparrow\downarrow$ $C_2\downarrow \rightarrow C_1\uparrow\downarrow$
2	$C_5\downarrow \rightarrow C_4\uparrow + C_1\uparrow$		
3	$C_4\downarrow \rightarrow C_3\uparrow + C_1\uparrow$		
4	$C_3\downarrow \rightarrow C_2\uparrow + C_1\uparrow$	2	$C_5\downarrow \rightarrow C_4\uparrow + C_1\uparrow\downarrow$ $C_3\downarrow \rightarrow C_2\uparrow + C_1\uparrow\downarrow$

The MMCCC circuit uses a hybrid architecture that combines the favorable features of series–parallel converter and FCMDC converter [18]. The modeling technique of various switched-capacitor converters have been discussed in previously published literatures [2], [4], [8], [9], [19]–[28]. The MMCCC modeling technique discussed in the following sections was not adopted from any particular previous derivation; rather, it was influenced by the previous works. The MMCCC circuit has two modes of operations: dynamic state or start-up and the steady state. Two different sets of boundary conditions are applied to deduce the equivalent models of the operational circuit in these two modes. Section III explains how the various capacitors attain steady voltages once the converter is energized. Section IV discusses the voltage variations of the capacitors once a load is connected to the converter.

III. START-UP ANALYSIS OF MMCCC

The MMCCC produces a CR based on the stored and transferred charges among the capacitors. It is required to find the capacitor voltages at different time intervals to prove the concept of the MMCCC topology. The following assumptions were made prior to the actual computational steps: 1) capacitors do not have residual voltages at start up. This ensures the maximum voltage stress across the transistors and makes the analysis in the most conservative manner, and 2) RC $\ll T/2$, where R is the

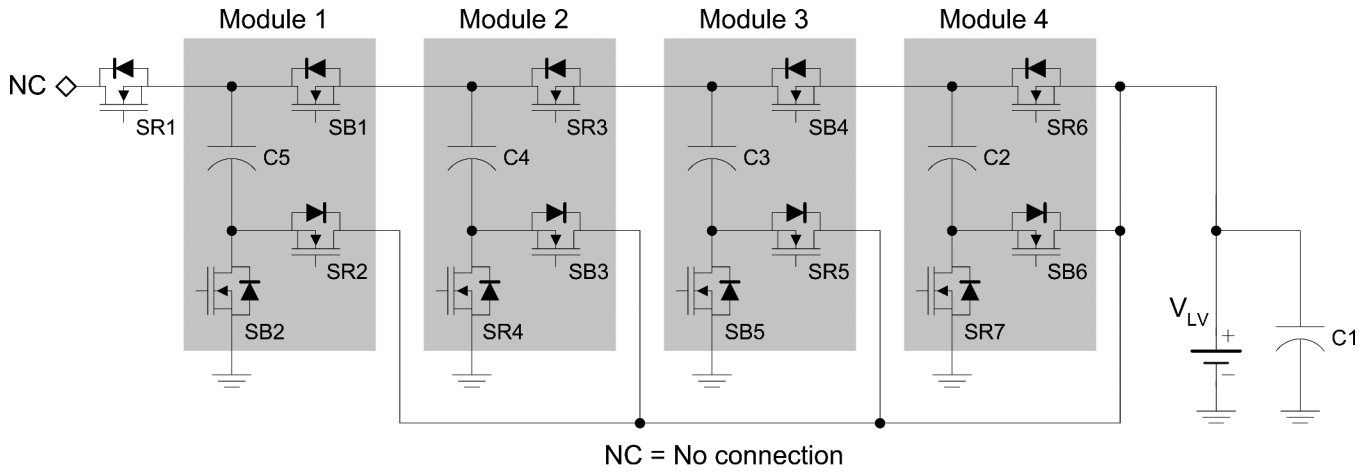


Fig. 3. Start-up arrangement of a five-level MMCCC circuit.

series path resistance of a capacitor charging circuit, C is the capacitance, and T is one switching period.

During start-up, it is also assumed that the converter is working in up-conversion (boost) mode, and the circuit is operating without any load. Once the capacitors obtain the proper operating voltages, the converter starts operating in the steady state, and loads can be connected to it. As the load draws current, there are variations in the capacitor voltages in both sub-intervals of the converter [1]. These variations will depend on the load current, operating frequency, and capacitor sizing. The second part of the analysis works with the steady state capacitor voltages during the two sub-intervals of the converter.

Using its bi-directional power handling capability, the MMCCC can seamlessly work in buck, boost or dual-source mode. To ensure a proper charge balancing during start-up, a voltage source of V_{LV} is connected to the LV side of the converter, and the HV side is left open during the start-up phase. To avoid undesirable voltage stress across the transistors, the HV side is not connected during the first 100 cycles of the start-up state. It will be shown later how the capacitors attain the normal voltages across them within the first 100 cycles of operation. The transistors are operated in sequential steps with the use of a microcontroller. Fig. 3 shows the schematic of the MMCCC with the required arrangement for start-up operation, and Table II shows the required transistor operation for the start-up steps. Step 3 and step 4 in Table II are repeated 100 times to ensure appropriate voltage build up across the capacitors. If the circuit works without any loss or voltage drop across any active or passive devices, a five-level MMCCC will have a $V_{\mathrm{HV}}/V_{\mathrm{LV}}$ ratio of 5. At steady state, the capacitors should have voltages like the following to ensure equal voltage stresses across the transistors:

$$V_{\mathrm{C}_1} = V_{\mathrm{LV}}, \quad V_{\mathrm{C}_2} = V_{\mathrm{LV}}, \quad V_{\mathrm{C}_3} = 2V_{\mathrm{LV}}, \quad V_{\mathrm{C}_4} = 3V_{\mathrm{LV}}, \quad V_{\mathrm{C}_5} = 4V_{\mathrm{LV}}, \quad \text{and} \quad V_{\mathrm{HV}} = 5V_{\mathrm{LV}}.$$

Thus, if the capacitor voltages are found in this form at the end of the modeling, it indicates that the MMCCC circuit can produce the expected CR.

TABLE II
ACTIVE TRANSISTORS AND CAPACITORS IN THE START-UP STEPS

Step	Active transistors	Active capacitors
1	S_{R7}, S_{R6}	C_1, C_2
2	S_{B6}, S_{B5}, S_{B4}	C_1, C_2, C_3
3	S_{R7}, S_{R6}, S_{R5}, S_{R4}, S_{R3}	C_1, C_2, C_3, C_4
4	S_{B6}, S_{B5}, S_{B4}, S_{B3}, S_{B2}, S_{B1}	C_1, C_2, C_3, C_4, C_5
5	S_{R7}, S_{R6}, S_{R5}, S_{R4}, S_{R3}	C_1, C_2, C_3, C_4

A. Step 1 of the Start-Up Process

The operation of this step is shown in Fig. 4(a). In this step, capacitors C_1 and C_2 are connected to the V_{LV} source. Thus, the voltage equations of the capacitors would be

$$V_{\mathrm{C}_1}(t_1) = V_{\mathrm{C}_2}(t_1) = V_{\mathrm{LV}} \tag{1}$$

$$V_{\mathrm{C}_3}(t_1) = V_{\mathrm{C}_4}(t_1) = V_{\mathrm{C}_5}(t_1) = 0. \tag{2}$$

B. Step 2 of the Start-Up Process

This step involves the discharging operation of C_2 and the charging operation of C_3. The operation is shown in Fig. 4(b). Therefore

$$V_{\mathrm{C}_1}(t_2) = V_{\mathrm{LV}} \tag{3}$$

$$V_{\mathrm{C}_2}(t_2) = V_{\mathrm{C}_2}(t_1) + [V_{\mathrm{LV}} + V_{\mathrm{C}_2}(t_1) - V_{\mathrm{C}_3}(t_1)]\frac{\mathrm{C}_3}{\mathrm{C}_2 + \mathrm{C}_3} = 0.5[V_{\mathrm{C}_2}(t_1) + V_{\mathrm{C}_3}(t_1) + V_{\mathrm{LV}}] \tag{4}$$

$$V_{\mathrm{C}_3}(t_2) = V_{\mathrm{C}_3}(t_1) + [V_{\mathrm{LV}} + V_{\mathrm{C}_2}(t_1) - V_{\mathrm{C}_3}(t_1)]\frac{\mathrm{C}_2}{\mathrm{C}_2 + \mathrm{C}_3} = 0.5[V_{\mathrm{C}_2}(t_1) + V_{\mathrm{C}_3}(t_1) + V_{\mathrm{LV}}] \tag{5}$$

$$V_{\mathrm{C}_4}(t_2) = V_{\mathrm{C}_5}(t_2) = 0. \tag{6}$$

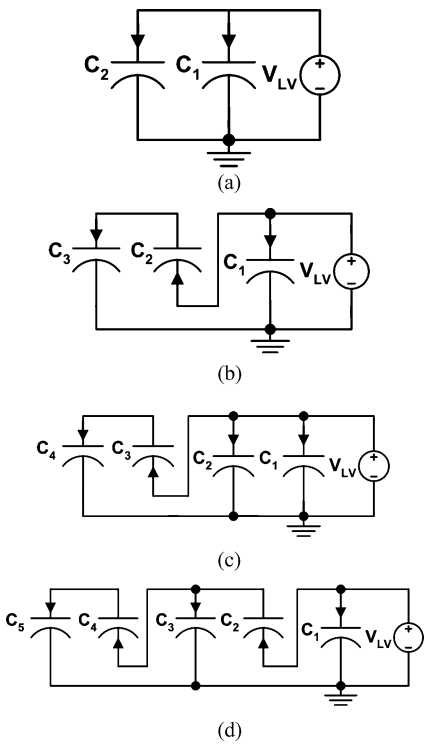


Fig. 4. Schematic diagram of the start-up steps of a five-level MMCCC circuit. (a) Step 1. (b) Step 2. (c) Step 3. (d) Step 4.

C. Step 3 of the Start-Up Process

The operational diagram of this step is shown in Fig. 4(c). In this step, the charge is transferred from C_3 to C_4. C_2 is again connected to V_{LV} as in step 1. Thus, the voltage equations are given as

$$V_{\mathrm{C}_1}(t_3) = V_{\mathrm{C}_2}(t_3) = V_{\mathrm{LV}} \tag{7}$$

$$V_{\mathrm{C}_3}(t_3) = 0.5[V_{\mathrm{C}_3}(t_2) + V_{\mathrm{C}_4}(t_2) - V_{\mathrm{LV}}] \tag{8}$$

$$V_{\mathrm{C}_4}(t_2) = 0.5[V_{\mathrm{C}_3}(t_2) + V_{\mathrm{C}_4}(t_2) + V_{\mathrm{LV}}] \tag{9}$$

$$V_{\mathrm{C}_5}(t_3) = V_{\mathrm{C}_5}(t_2) = 0. \tag{10}$$

D. Step 4 of the Start-Up Process

This step involves the operations that took place in step 2 with an additional charge transfer action from C_4 to C_5. The operational diagram of step 4 is shown in Fig. 4(d), and the voltage equations are given as

$$V_{\mathrm{C}_1}(t_4) = V_{\mathrm{LV}} \tag{11}$$

$$V_{\mathrm{C}_2}(t_4) = 0.5[V_{\mathrm{C}_2}(t_3) + V_{\mathrm{C}_3}(t_3)] - 0.5V_{\mathrm{LV}} \tag{12}$$

$$V_{\mathrm{C}_3}(t_4) = 0.5[V_{\mathrm{C}_2}(t_3) + V_{\mathrm{C}_3}(t_3)] + 0.5V_{\mathrm{LV}} \tag{13}$$

$$V_{\mathrm{C}_4}(t_4) = 0.5[V_{\mathrm{C}_4}(t_3) + V_{\mathrm{C}_5}(t_3)] - 0.5V_{\mathrm{LV}} \tag{14}$$

$$V_{\mathrm{C}_5}(t_4) = 0.5[V_{\mathrm{C}_4}(t_3) + V_{\mathrm{C}_5}(t_3)] + 0.5V_{\mathrm{LV}}. \tag{15}$$

Using (1)–(4), the capacitor voltages at the end of step 2 are

$$X_0 = \begin{bmatrix} V_{\mathrm{C}_1} \\ V_{\mathrm{C}_2} \\ V_{\mathrm{C}_3} \\ V_{\mathrm{C}_4} \\ V_{\mathrm{C}_5} \end{bmatrix} = \begin{bmatrix} V_{\mathrm{LV}} \\ 0 \\ V_{\mathrm{LV}} \\ 0 \\ 0 \end{bmatrix}. \tag{16}$$

The values found from (16) will be used as the initial conditions for step 3, and the voltages at the end of step 3 will be used as the initial voltages for step 4. From the operating principle of the converter, all odd indexed steps become equivalent once the circuit completes the first four steps. This is also true of all even indexed steps. Thus, the circuit is modeled using two repetitive operations described in step 3 and 4. A variable k is defined where k starts from 2. Therefore, the capacitor voltages in any odd and even indexed steps can be generalized using (7)–(10) and (11)–(15), and can be expressed in the following matrix, shown in (17) and (18) at the bottom of this page.

Here, (17) and (18) are in the form $y = Mx + b$ and $z = Ny + d$. After doing the matrix manipulation and expressing the constant factors in terms of V_{C_1}, shown in (19) and (20) at the bottom of the next page, where

$$V_{\mathrm{C}_1}(k) = V_{\mathrm{C}_1}(k+1) = V_{\mathrm{C}_1}(k+n) = V_{\mathrm{LV}}.$$

$$\begin{bmatrix} V_{\mathrm{C}_1}(k+1) \\ V_{\mathrm{C}_2}(k+1) \\ V_{\mathrm{C}_3}(k+1) \\ V_{\mathrm{C}_4}(k+1) \\ V_{\mathrm{C}_5}(k+1) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0.5 & 0.5 & 0 \\ 0 & 0 & 0.5 & 0.5 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{\mathrm{C}_1}(k) \\ V_{\mathrm{C}_2}(k) \\ V_{\mathrm{C}_3}(k) \\ V_{\mathrm{C}_4}(k) \\ V_{\mathrm{C}_5}(k) \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ -0.5 \\ 0.5 \\ 0 \end{bmatrix} V_{\mathrm{LV}} \tag{17}$$

$$\begin{bmatrix} V_{\mathrm{C}_1}(k+2) \\ V_{\mathrm{C}_2}(k+2) \\ V_{\mathrm{C}_3}(k+2) \\ V_{\mathrm{C}_4}(k+2) \\ V_{\mathrm{C}_5}(k+2) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0.5 & 0.5 & 0 & 0 \\ 0 & 0.5 & 0.5 & 0 & 0 \\ 0 & 0 & 0 & 0.5 & 0.5 \\ 0 & 0 & 0 & 0.5 & 0.5 \end{bmatrix} \begin{bmatrix} V_{\mathrm{C}_1}(k+1) \\ V_{\mathrm{C}_2}(k+1) \\ V_{\mathrm{C}_3}(k+1) \\ V_{\mathrm{C}_4}(k+1) \\ V_{\mathrm{C}_5}(k+1) \end{bmatrix} + \begin{bmatrix} 1 \\ -0.5 \\ 0.5 \\ -0.5 \\ 0.5 \end{bmatrix} V_{\mathrm{LV}}. \tag{18}$$

After n iterations, the final capacitor voltage vector can be given by

$$f = (CA)^n X_0 \tag{21a}$$

where X_0 is the capacitor voltage matrix at the end of step 2 found in (16). Using MATLAB

$$(CA)^n = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 2 & 0 & 0 & 0 & 0 \\ 3 & 0 & 0 & 0 & 0 \\ 4 & 0 & 0 & 0 & 0 \end{bmatrix}, \qquad \text{where } n = 100 \tag{21b}$$

and the final capacitor voltage matrix f can be calculated using (21a) and (21b). Thus,

$$f = \begin{bmatrix} 1 \\ 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} V_{\mathrm{LV}}. \tag{22}$$

The start-up gating sequence is operated at a speed of 10 000 steps/s, which is equal to the switching frequency (10 kHz) of the converter at steady state. Thus, after 100 iterations or 10 ms

$$\begin{aligned} V_{\mathrm{C}_1} &= 1V_{\mathrm{LV}} \\ V_{\mathrm{C}_2} &= 1V_{\mathrm{LV}} \\ V_{\mathrm{C}_3} &= 2V_{\mathrm{LV}} \\ V_{\mathrm{C}_4} &= 3V_{\mathrm{LV}} \\ V_{\mathrm{C}_5} &= 4V_{\mathrm{LV}}. \end{aligned} \tag{23}$$

The analytical derivation presented in this section explains the start-up operation of a five-level MMCCC circuit. In Fig. 2, the two subintervals of the circuit in steady state are shown. In the first subinterval, C_5 and C_1 are connected in series and across V_{HV}. If there is no loss in the circuit or any load connected at the output, the total voltage across the series connected circuit of C_5 and C_1 should be 5 V_{LV}, as shown in (23). In addition, there is another current path composed of $\mathrm{C}_4, \mathrm{C}_3$, and C_1. In Fig. 2, during state 1, C_4 is connected across the series combination of C_3 and C_1. Equation (23) shows that the voltage across C_4 (3 V_{LV}) is equal to the summation of voltages across C_1 (1 V_{LV}) and C_3 (2 V_{LV}). Moreover, C_2 is connected across C_1, and their voltages are also matched. Therefore, the voltages across the capacitors during state 1 are matched to each other.

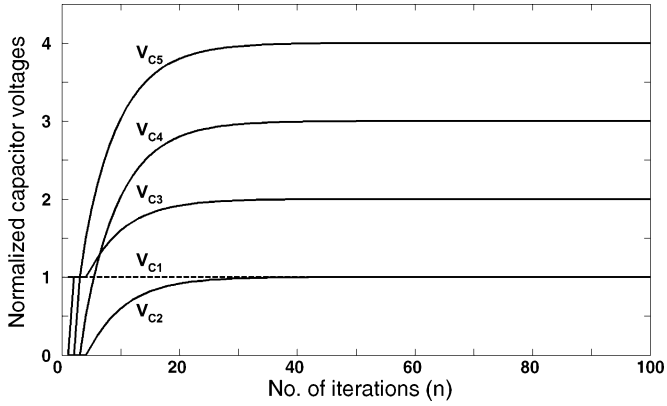


Fig. 5. Analytically derived capacitor voltage variations with iterations. At $n = 40$, all voltages have reached steady state for all practical purposes. Voltage magnitudes are normalized to V_{LV}. Each iteration takes 100 μs.

In state 2, C_5 is connected across the series circuit of C_4 and C_1. These voltages are also matched and can be seen in (23). In the same way, C_3 is connected across the series circuit of C_2 and C_1, and the voltage across C_3 (2 V_{LV}) is the same as the total voltage across C_1 and C_2 ($V_{\mathrm{LV}} + V_{\mathrm{LV}} = 2V_{\mathrm{LV}}$). Therefore, the capacitor voltages in state 2 are also matched, and the load can be connected either at HV side or LV side. Once a load is connected at either side, the load current will discharge the capacitors, and charge transfer will take place either from a voltage source (V_{LV} or V_{HV}) to a capacitor or from one capacitor to another. In this case, the steady-state capacitor voltages will be different from the values stated in (23), and the analysis is shown in the next section.

The values of different capacitor voltages in (21a) were plotted for different values of n varying in the range of 1 to 100, as shown in Fig. 5. Two charge transfer operations in odd and even indexed steps [shown in (19) and (20)] take place in one clock cycle (for one value of n), and Fig. 5 shows the capacitor voltages at the end of the even indexed step (second subinterval) in each clock cycle. It is also seen that, for all practical purposes, the capacitor voltages reach steady state after 40 iterations. To verify the start-up operation using the technique presented in

$$\begin{bmatrix} V_{\mathrm{C}_1}(k+1) \\ V_{\mathrm{C}_2}(k+1) \\ V_{\mathrm{C}_3}(k+1) \\ V_{\mathrm{C}_4}(k+1) \\ V_{\mathrm{C}_5}(k+1) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -0.5 & 0 & 0.5 & 0.5 & 0 \\ 0.5 & 0 & 0.5 & 0.5 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{\mathrm{C}_1}(k) \\ V_{\mathrm{C}_2}(k) \\ V_{\mathrm{C}_3}(k) \\ V_{\mathrm{C}_4}(k) \\ V_{\mathrm{C}_5}(k) \end{bmatrix} = A \begin{bmatrix} V_{\mathrm{C}_1}(k) \\ V_{\mathrm{C}_2}(k) \\ V_{\mathrm{C}_3}(k) \\ V_{\mathrm{C}_4}(k) \\ V_{\mathrm{C}_5}(k) \end{bmatrix} = AX_0 \tag{19}$$

$$\begin{bmatrix} V_{\mathrm{C}_1}(k+2) \\ V_{\mathrm{C}_2}(k+2) \\ V_{\mathrm{C}_3}(k+2) \\ V_{\mathrm{C}_4}(k+2) \\ V_{\mathrm{C}_5}(k+2) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ -0.5 & 0.5 & 0.5 & 0 & 0 \\ 0.5 & 0.5 & 0.5 & 0 & 0 \\ -0.5 & 0 & 0 & 0.5 & 0.5 \\ 0.5 & 0 & 0 & 0.5 & 0.5 \end{bmatrix} \begin{bmatrix} V_{\mathrm{C}_1}(k+1) \\ V_{\mathrm{C}_2}(k+1) \\ V_{\mathrm{C}_3}(k+1) \\ V_{\mathrm{C}_4}(k+1) \\ V_{\mathrm{C}_5}(k+1) \end{bmatrix} = C \begin{bmatrix} V_{\mathrm{C}_1}(k+1) \\ V_{\mathrm{C}_2}(k+1) \\ V_{\mathrm{C}_3}(k+1) \\ V_{\mathrm{C}_4}(k+1) \\ V_{\mathrm{C}_5}(k+1) \end{bmatrix} \tag{20}$$

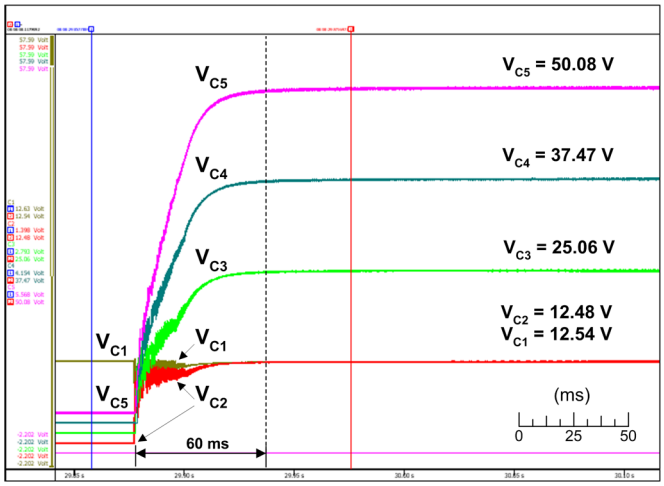


Fig. 6. Experimental results of the capacitor voltages in the MMCCC during the start up period.

this paper, a five-level MMCCC prototype has been constructed on a printed circuit board. The circuit was designed for a maximum $V_{\rm HV}$ of 220 V. For a five-level design, four modules are used with each module having its own gate drive stages. Inside one module, two bootstrap gate drive circuits (IR2110) have been used to drive three IXFR120N20 MOSFETs. These MOSFETs have an ON resistance of 0.017 Ω at 25 °C, and are rated at 200 V, 105 A. General-purpose 4500-μF (3 × 1500 μF) 200-V electrolytic capacitors having an equivalent series resistance (ESR) of 0.04 Ω have been used. An LDS-Nicolet Vision XP multichannel data acquisition system and a Lecroy Waverunner high sampling digital oscilloscope were used to record the capacitor voltages $V_{\rm C_1}$, $V_{\rm C_2}$, $V_{\rm C_3}$, $V_{\rm C_4}$, and $V_{\rm C_5}$, which are shown in Fig. 6.

While comparing Figs. 5 and 6, the capacitor voltages were normalized to 1 $V_{\rm LV}$ in Fig. 5, and a 12.63-V source was used as $V_{\rm LV}$ in the experiment. The voltage across $\rm C_5$ reaches to 50.08 V after 0.06 s in the experiment; however, theoretically, it should reach to 50.52 V (4 $V_{\rm LV}$) within 0.01 s. Because many of the nonideal quantities such as drain-source resistance $\rm R_{DS}$ of the MOSFETs, capacitor ESR, and switching losses were not included in the model, the time required to establish the proper capacitor voltages was longer than the analytically computed values. However, the experimental capacitor voltages were very close to the analytically computed values. The comparison between the analytical and experimental values, and corresponding percentage of error are summarized in Table III.

TABLE III
COMPARISON BETWEEN THE ANALYTICAL AND EXPERIMENTAL START-UP VOLTAGES ACROSS THE CAPACITORS IN THE MMCCC

$V_{\rm LV}$ = 12.63 V			
Parameter	Analytical value (V)	Experimental value (V)	% Error
V_{C1}	1 $V_{\rm LV}$ = 12.63	12.54	0.71
V_{C2}	1 $V_{\rm LV}$ = 12.63	12.48	1.19
V_{C3}	2 $V_{\rm LV}$ = 25.26	25.06	0.79
V_{C4}	3 $V_{\rm LV}$ = 37.89	37.47	1.11
V_{C5}	4 $V_{\rm LV}$ = 50.52	50.08	0.87

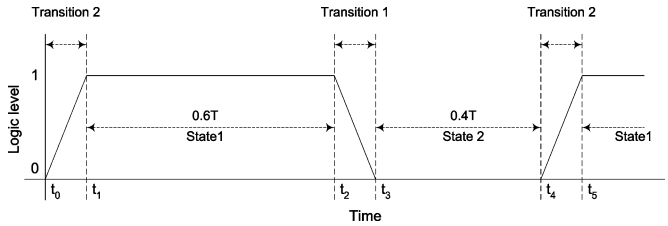


Fig. 7. Transition state timing diagram of a five-level MMCCC.

IV. STEADY-STATE ANALYSIS OF MMCCC

Section III presents the step-by-step start-up switching scheme that can ensure safe operating voltage of the transistors in the circuit. After 100 cycles, the capacitor voltages reach the values shown in (23). During this time, the load was not connected at the output, and the source $V_{\rm LV}$ was connected at the LV side to balance the capacitor voltages. Therefore, the values found from (23) will be used as the initial conditions of the steady-state operation of the circuit. During steady-state operation, the MMCCC circuit operates in the two states shown in Fig. 2(a) and (b). Based on these operating states, the operation of the MMCCC circuit can be divided into four operating zones. They are: 1) state 1; 2) transition 1 (from state 1 to state 2); 3) state 2; and 4) transition 2 (from state 2 to state 1). These different zones are shown in Fig. 7. The transition states are very small compared to state 1 and state 2. Provided that the converter has a stable operating condition, voltage and current equations at t_4 and t_5 would be the same as t_0 and t_1, respectively, after one clock cycle.

In a five-level converter, there are three current paths in state 1 (V_E–$\rm C_5$–$\rm C_1$, $\rm C_4$–$\rm C_3$–$\rm C_1$, and $\rm C_2$–$\rm C_1$), and two current paths in state 2 ($\rm C_5$–$\rm C_4$–$\rm C_1$ and $\rm C_3$–$\rm C_2$–$\rm C_1$), as shown in Fig. 8. The amount of ripple present at node 1 or at the output depends on how much the capacitors are discharged, and the discharge amount depends on how long the capacitors are connected to the load. Therefore, to keep the ripple component equal in these two subintervals or states, the duration of state 1 is 1.5 times the duration of state 2 considering the increased number of current paths present during state 1. Thus, for a five-level conversion, (t_2–t_1) is 1.5 times (t_4–t_3). As a result, (t_2–t_1) = 0.6T and (t_4–t_3) = 0.4T, where T is the time period of one cycle. The reason for choosing these time intervals has been explained in [1]. For the proposed design, T is 100 μs for an operating frequency of 10 kHz.

V. ANALYTICAL MODELING

A. Current and Voltage Equations in State 1

At time $t = t_1$, the MMCCC circuit is on the verge of state 1, as shown in Fig. 7. Four constant offsets $\delta_1, \delta_3, \delta_4$, and δ_5 are added to the capacitor voltages estimated at the beginning of state 1 to include the effect of load current. Using the

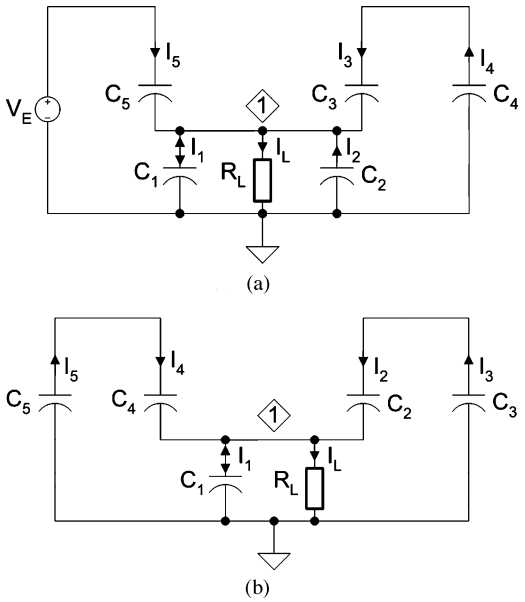


Fig. 8. Redefined steady-state diagrams with load connected at the LV side. (a) State 1. (b) State 2.

voltages found from the start-up analysis and considering several constant deviations during steady state

$$V_{C_5}(t_1) = 0.8E + \delta_5 \tag{24}$$

$$V_{C_4}(t_1) = 0.6E + \delta_4 \tag{25}$$

$$V_{C_3}(t_1) = 0.4E + \delta_3 \tag{26}$$

$$V_{C_2}(t_1) = V_{C_1}(t_1) = 0.2E + \delta_1 \tag{27}$$

where, E is the voltage amplitude of the source V_E shown in Fig. 8(a), and the following equations can be used as boundary conditions derived from this figure. These boundary conditions are not global, and are valid during state 1 only. Therefore

$$E = V_{C_5} + V_{C_1} \tag{28}$$

thus, $\delta_5 + \delta_1 = 0$ from (24) and (27)

$$V_{C_4} = V_{C_3} + V_{C_2} \tag{29}$$

thus, $\delta_4 + \delta_3 + \delta_1$ from (25)–(27)

$$\text{and} \qquad I_1 + I_2 + I_4 + I_5 = I_L \tag{30}$$

from Fig. 8(a).

Depending on the direction of current and the capacitor voltages, the following equations could be written at the end of state 1 (at $t = t_2$):

$$V_{C_5} = 0.8E + \delta_5 + \frac{I_5 0.6T}{C} \tag{31}$$

$$V_{C_4} = 0.6E + \delta_4 - \frac{I_4 0.6T}{C} \tag{32}$$

$$V_{C_3} = 0.4E + \delta_3 + \frac{I_4 0.6T}{C} \tag{33}$$

$$V_{C_1} = V_{C_2} = 0.2E + \delta_1 - \frac{I_1 0.6T}{C} \tag{34}$$

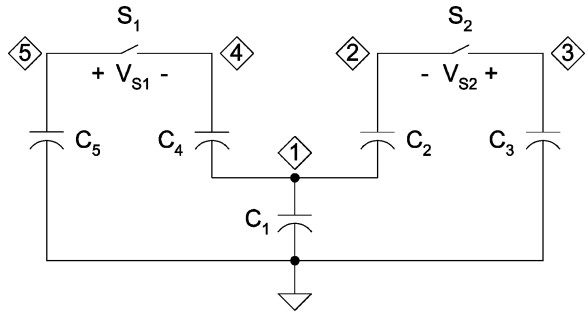


Fig. 9. Schematic diagram of transition 1 operation.

where $C_1 = C_2 = C_3 = C_4 = C_5 = C$, and $I_3 = I_4$ and $I_1 = I_2$. Here, I_1, I_4, and I_5 are the average currents during this subinterval.

To satisfy the boundary condition (28), and using (31) and (34)

$$I_5 = I_1 (\text{as } \delta_5 + \delta_1 = 0).$$

In the same way, using the boundary condition (29), and values from (32) and (34)

$$I_1 = 2I_4 \text{ as } \delta_4 = \delta_3 + \delta_1. \tag{35}$$

Using (30),

$$I_1 = I_2 = I_5 = \frac{2I_L}{7} \tag{36}$$

and using (35),

$$I_4 = \frac{I_L}{7}. \tag{37}$$

Using (31)–(37),

$$V_{C_5}(t_2) = 0.8E + \delta_5 + \frac{6\Delta}{35} \tag{38}$$

$$V_{C_4}(t_2) = 0.6E + \delta_4 - \frac{3\Delta}{35} \tag{39}$$

$$V_{C_3}(t_2) = 0.4E + \delta_3 - \frac{3\Delta}{35} \tag{40}$$

$$V_{C_1}(t_2) = V_{C_2} = 0.2E + \delta_1 - \frac{6\Delta}{35} \tag{41}$$

where $\Delta = I_L T/C$.

Now, there will be a transition from state 1 to state 2 at $t = t_2$, and it will continue until $t = t_3$. This transition is shown in Fig. 9. After this transition, the converter will be transformed from the circuit shown in Fig. 8(a) to that shown in Fig. 8(b). Therefore, the capacitor voltages found at the end of state 1 will be the inputs in transition 1, and the voltages found at the end of transition 1 will be used as the inputs in state 2.

B. Current and Voltage Equations in Transition 1

During the transition process, all five capacitors participate in the charge transfer process simultaneously. However, for the convenience of the analysis, it is assumed that this operation takes place in several steps. These steps are such that the effect

of interconnecting multiple capacitors simultaneously would be the same as connecting them sequentially. Fig. 9 explains the sequential capacitor switching in a transition state. This transition is analyzed with the help of two switches S_1 and S_2. It is assumed that S_1 is turned on first, and then S_2. For the convenience of the analysis, the capacitor voltage at the beginning of this transition state are defined as V_{C_1}, V_{C_2}, V_{C_3}, V_{C_4}, and V_{C_5} rather than using the exact values found in (38)–(41). Two intermediate variables V_{S_1} and V_{S_2} are defined such that

$$V_{S_1} = V_{C_5} - (V_{C_4} + V_{C_1}) \tag{42}$$

and

$$V_{S_2} = V_{C_3} - (V_{C_2} + V_{C_1}). \tag{43}$$

When S_1 is closed and S_2 is open, C_5 will be discharged, and will transfer some of its charge to C_4 and C_1. Thus, there will be a voltage drop across C_5, and the change in V_{C_5} is

$$d(V_{C_5}) = V_{S_1} \frac{C_{5eq}}{C_{5eq} + C}$$

where C_{5eq} is the capacitance connected at terminal 5 in Fig. 9 or the capacitance seen by C_5. Thus, $d(V_{C_5}) = V_{S_1}\,(0.5C/(0.5C + C)) = V_{S_1}/3$.

Due to this operation, the change in the voltage at node 4 is

$$d(V_4) = V_{S_1} \frac{C}{C_{5eq} + C} = \frac{2V_{S_1}}{3}.$$

Change in the voltage of $C_4 = d(V_{C_4}) = d(V_4)\,(C_1/C_1 + C_4) = \frac{V_{S_1}}{3}$.

In the same way, $d(V_{C_1}) = V_{S_1}/3$.

Thus, the new capacitor voltages are

$$V'_{C_5} = V_{C_5} - d(V_{C_5}) = V_{C_5} - \frac{V_{S_1}}{3} \tag{44}$$

$$V'_{C_4} = V_{C_4} - d(V_{C_4}) = V_{C_4} - \frac{V_{S_1}}{3} \tag{45}$$

$$V'_{C_1} = V_{C_1} - d(V_{C_1}) = V_{C_1} - \frac{V_{S_1}}{3}. \tag{46}$$

When S_2 is turned on, there occurs some charge transfer among the capacitors, and as a result, the voltages of the capacitors change. Using the same method as described previously

$$V_{C_1}(t_3) = 0.2E + \frac{3\Delta}{70} + \frac{1}{4}\delta_5. \tag{47}$$

In the same way

$$V_{C_2}(t_3) = 0.2E - \frac{9\Delta}{140} - \frac{1}{8}\delta_5 + \frac{1}{2}\delta_4 \tag{48}$$

$$V_{C_3}(t_3) = 0.4E - \frac{3\Delta}{140} + \frac{1}{8}\delta_5 + \frac{1}{2}\delta_4 \tag{49}$$

$$V_{C_4}(t_3) = 0.6E + \frac{3\Delta}{140} + \frac{3}{8}\delta_5 + \frac{1}{2}\delta_4 \tag{50}$$

and

$$V_{C_5}(t_3) = 0.8E + \frac{9\Delta}{140} + \frac{5}{8}\delta 5 + \frac{1}{2}\delta 4. \tag{51}$$

Using the same method followed in state 1 and transition 1, the capacitor voltages at the end of transition 2 can be obtained, and they are summarized as follows:

$$V_{C_1}(t_5) = V_{C_2}(t_5) = 0.2E + \frac{\Delta}{245} - \frac{3}{28}\delta 5 \tag{52}$$

$$V_{C_3}(t_5) = 0.4E + \frac{19\Delta}{980} + \frac{17}{56}\delta 5 + \frac{1}{2}\delta 4 \tag{53}$$

$$V_{C_4}(t_5) = 0.6E + \frac{23\Delta}{980} + \frac{11}{56}\delta 5 + \frac{1}{2}\delta 4 \tag{54}$$

$$V_{C_5}(t_5) = 0.8E - \frac{\Delta}{245} + \frac{3}{28}\delta 5. \tag{55}$$

After transition 2, the capacitor voltages should be equal to what they were at the beginning of state 1, if the capacitor voltages are to be balanced over each cycle. Equations (52)–(55) show the values of the five capacitor voltages at $t = t_5$. Starting at t_1, the converter completes a cycle at t_5, and thus, the capacitor voltages found at t_5 should be the same as they were at t_1.

Therefore, by comparing (24)–(27) and (52)–(55), we obtain

$$\delta 5 = -\frac{4\Delta}{875}, \qquad \delta 4 = \frac{79\Delta}{1750}, \qquad \delta 3 = \frac{71\Delta}{1750}, \qquad \text{and}$$
$$\delta 1 = \frac{4\Delta}{875}. \tag{56}$$

Now, the calculated values of $\delta_1, \delta_3, \delta_4$, and δ_5 can be proven accurate if they satisfy the initial constraints that were made in state 1. To check this

$$\delta_5 + \delta_1 = -\frac{4\Delta}{875} + \frac{4\Delta}{875} = 0$$

which satisfies (28), $\delta_4 - \delta_3 - \delta_1 = \frac{79\Delta}{1750} - \frac{71\Delta}{1750} - \frac{4\Delta}{875} = 0$ and which satisfies (29).

Thus, the calculated values of δ_4 and δ_3 are consistent. Therefore, using the computed values of $\delta_5, \delta_4, \delta_3$, and δ_1, the capacitor voltages at the beginning of state 1 are

$$V_{C_5} = 0.8E - \frac{4\Delta}{875} \tag{57}$$

$$V_{C_4} = 0.6E + \frac{79\Delta}{1750} \tag{58}$$

$$V_{C_3} = 0.4E + \frac{71\Delta}{1750} \tag{59}$$

$$V_{C_1} = V_{C_2} = 0.2E + \frac{4\Delta}{875}. \tag{60}$$

Here, the load voltage is V_{C_1}, and from the preceding voltage expressions, the load voltages at different time intervals are listed as following:

$$V_{C_1}(t_1) = 0.2E + \frac{4\Delta}{875} \tag{61}$$

$$V_{C_1}(t_2) = 0.2E - \frac{146\Delta}{875} \tag{62}$$

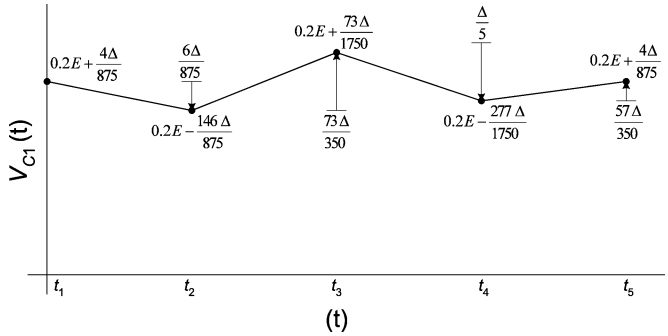


Fig. 10. Analytically calculated values of V_{C_1} and its variations at different time intervals.

$$V_{C_1}(t_3) = 0.2E + \frac{73\Delta}{1750} \tag{63}$$

$$V_{C_1}(t_4) = 0.2E - \frac{277\Delta}{1750} \tag{64}$$

$$V_{C_1}(t_5) = 0.2E + \frac{4\Delta}{875}. \tag{65}$$

Using the values found from (61)–(65), the load voltages at different time intervals were plotted in Fig. 10, and the voltage ripples were also estimated. It was found that at the end of state 1, the voltage ripple was $6\Delta/35$, and during transition 1, the ripple was $-(73\Delta/350)$. During state 2, the voltage ripple was $\Delta/5$, and during transition 2, the ripple was $-(57\Delta/350)$. Thus, over one full cycle, the total ripple is zero $[(6\Delta/35)-(73\Delta/350)+\Delta/5-(57\Delta/350)=0]$. Fig. 10 also shows these ripple components at different times. Note that the voltage quantities plotted in Fig. 10 are not to scale.

These computational steps prove that the MMCCC obtains a stable operation when the load is connected to it. The capacitor voltages found from (57)–(60) are the steady-state values of them. If the converter starts with these capacitor voltages at the beginning of state 1, after one complete cycle, the capacitor voltages will return to these values. This steady-state operating point will be shifted due to a change in load because the term Δ is a function of load current. However, for different loading conditions, the values of δ_1–δ_5 will be different, and after one cycle, the converter will have the same capacitor voltages that it had at the beginning of state 1 during the new loading condition.

VI. Experimental Verification

A. Voltage Ripple Across the Load

To verify the voltage expression from the analytical derivation, the MMCCC was tested with different loading conditions. Fig. 11 shows the experimental voltage across C_1 for a loading condition described in Table IV. This experimental voltage ripple measured across C_1 is found to be consistent with the simulated waveform, and the comparison is shown in Table IV. The maximum percentage of error was 2.3%, which indicates that the analytical model is accurate in estimating the LV side voltage.

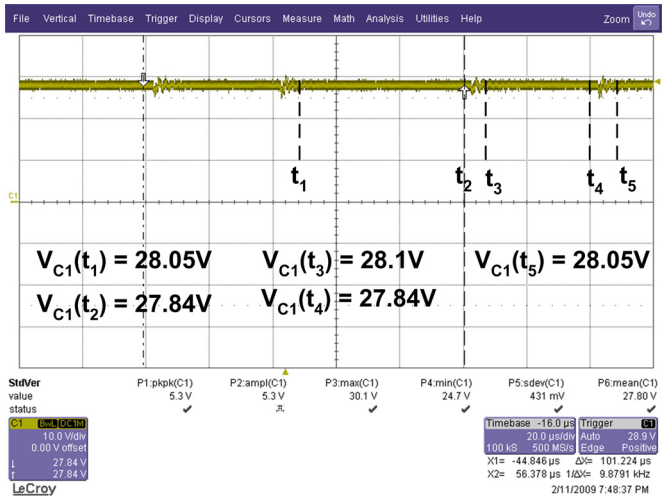


Fig. 11. Experimental values of V_{C_1} and its variations at different time intervals.

TABLE IV
Experimental Setup for Measuring V_{C_1}, and the Comparison Between Analytical and Experimental Results

Experimental setup			
Parameters	Value		
Operating mode	Down conversion		
V_{HV} (V_E)	142.67 V		
V_{LV}	28.05 V		
I_L	10.02 A		
C	4.5 mF		
f	10 kHz		
T	100 µs		
Δ	0.223		
Analytical vs. experimental results			
Parameters	Analytical value (V)	Experimental value (V)	Percentage of error (%)
V_{C1} (t_1)	28.54	28.05	1.7
V_{C1} (t_2)	28.50	27.84	2.3
V_{C1} (t_3)	28.54	28.10	1.6
V_{C1} (t_4)	28.50	27.84	2.3
V_{C1} (t_5)	28.54	28.05	1.7

B. Effect of Unequal Capacitors

The other useful feature of the MMCCC is the capability of producing an accurate CR even with some variation in the capacitances of the capacitors used in the modules. Although the mathematical model has been derived assuming equal capacitance in every module, the MMCCC's operation remains unaffected when capacitors of different values are used. This allows the MMCCC to use capacitor components that do not have tight manufacturing tolerances. A simulation in PSIM was performed to verify this, and three sets of data for V_{C_1} were recorded for various combinations of the capacitors. These combinations are shown in Table V, and the simulation results are displayed in Fig. 12. This simulation shows that the MMCCC can produce the same CR for various capacitance mismatches in the circuit. The simulation also shows that the ripple component across C_1 is a function of the total capacitance in the circuit; case 3 produces the largest ripple and the total capacitance was 4.1 mF, whereas it was 5 mF in both case 1 and case 2. Another

TABLE V
CAPACITOR VALUES IN DIFFERENT CASES TO VERIFY MMCCC'S CAPABILITY TO PRODUCE THE SAME CR WITH UNEQUAL CAPACITANCES AT DIFFERENT LEVELS

Parameters	Values in case 1	Values in case 2	Values in case 3
C_1	1C	1C	0.8C
C_2	1C	1.3C	1.3C
C_3	1C	1.2C	0.5C
C_4	1C	0.7C	0.5C
C_5	1C	0.8C	1C
Total capacitance in the circuit	5C	5C	4.1C
Average V_{LV}	44.275 V	44.27 V	44.247 V
Operating mode	Down conversion	Down conversion	Down conversion
V_{HV}	225 V	225 V	225 V
CR	5.08	5.08	5.09

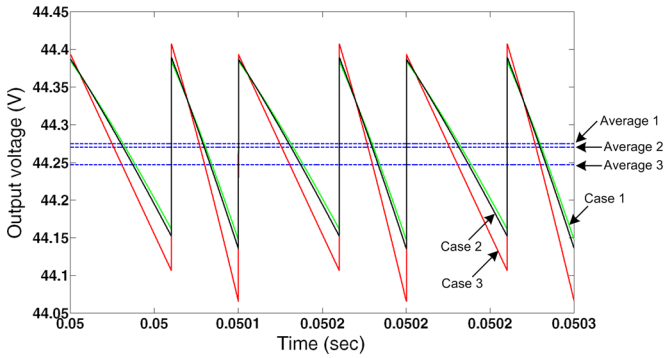


Fig. 12. Simulation results of the voltage across C_1 for different combinations of capacitances used in the circuit.

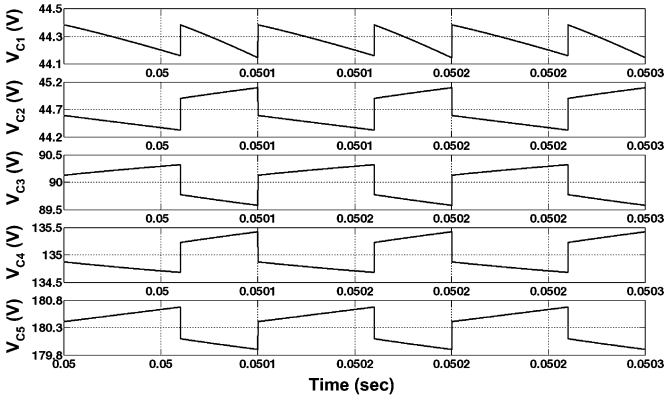


Fig. 13. Simulation results of the voltages across the capacitors of the MMCCC with the loading condition described in Table V.

simulation was performed to investigate the impact of loading on the various capacitor voltages, and the results are shown in Fig. 13. This figure shows the various capacitor voltages with time, and the loading condition stated in Table IV was used to generate these plots.

TABLE VI
INPUT AND OUTPUT VOLTAGES OF THE MMCCC WITH A CONSTANT IMPEDANCE LOAD CONNECTED AT THE LV SIDE

R_L = 2.8 Ω, Operating mode: Down conversion (buck mode)		
V_{in} (V_{HV})	V_{out} (V_{LV})	CR
21.04	4.02	5.23
41.12	8.09	5.09
60.95	12.02	5.07
81.17	15.97	5.08
100.60	19.75	5.09
120.93	23.76	5.09
140.44	27.60	5.09
160.03	31.56	5.07

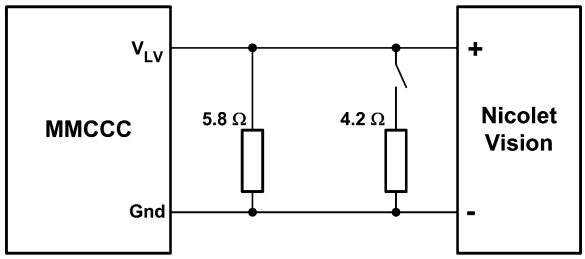


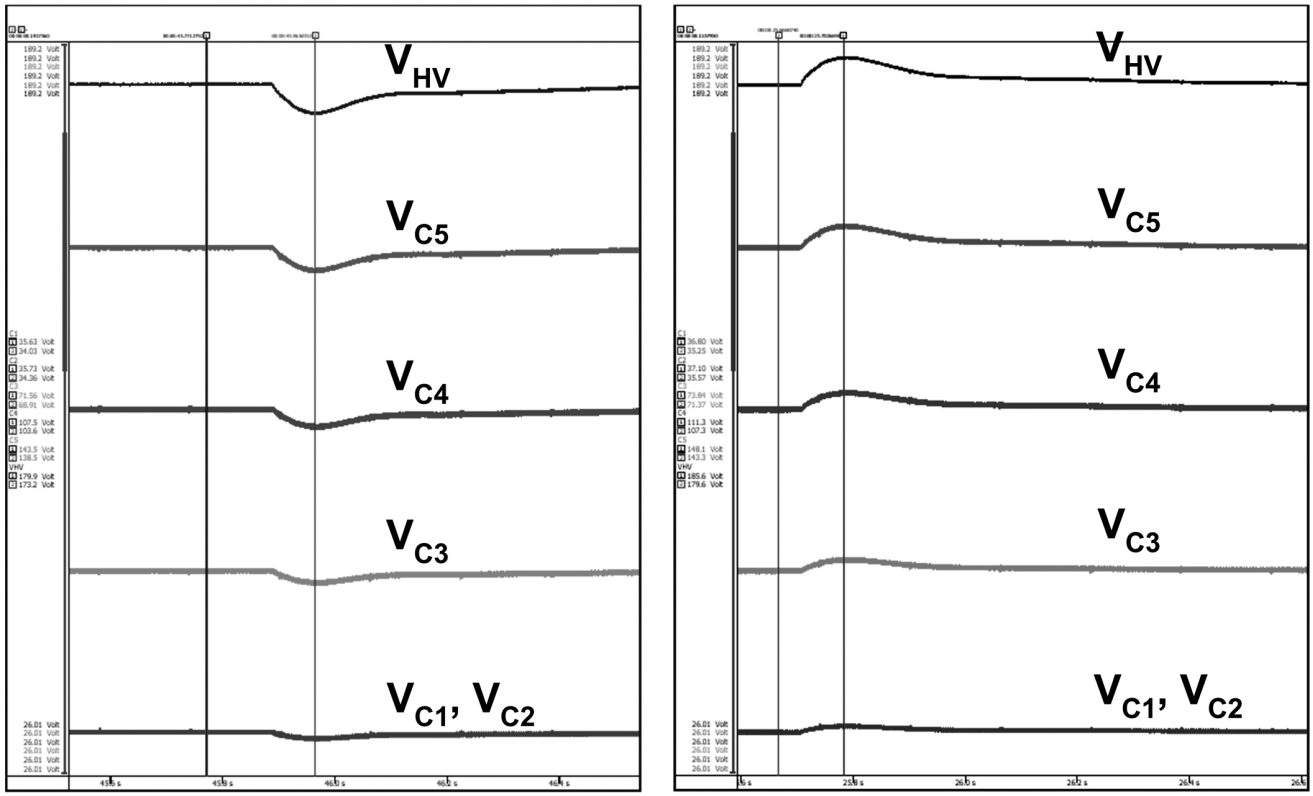
Fig. 14. Test schematic to characterize the impact of step load variation at the capacitor voltages in the MMCCC circuit.

C. Input–Output Voltage Relation

The MMCCC circuit was tested in down conversion (buck) mode by applying various input voltages with a 2.8-Ω load connected at the LV side. This test was performed to verify the consistency in the CR of the converter during input voltage variation. Because the circuit does not have any voltage control scheme, it maintains an integer CR, and therefore, the output varies linearly with the input. These experimental results are summarized in Table VI, which shows that the converter produced a consistent CR of five except for very LV output conditions.

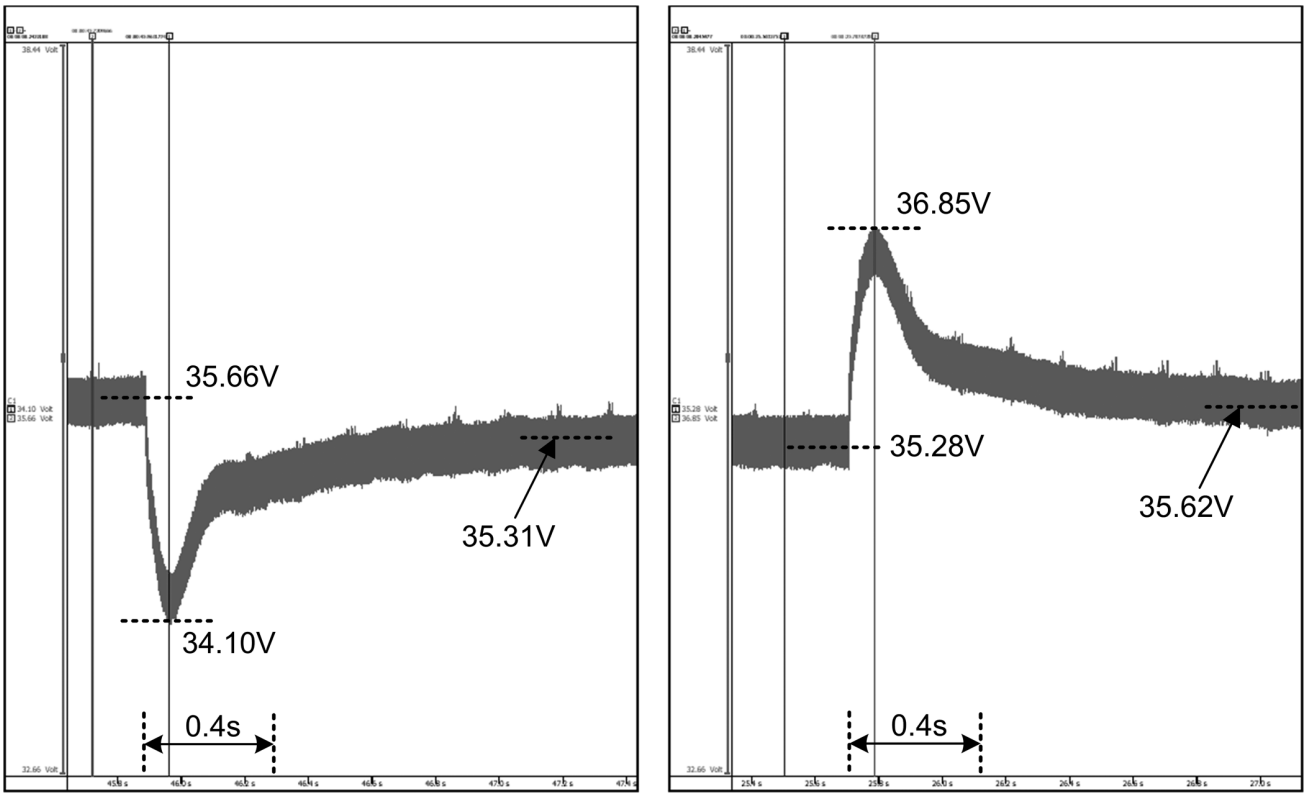
D. Impact of Step Load Change

When a dc–dc converter experiences a step load variation at the output, a temporary voltage variation occurs across the load. The variation may prolong for a considerable amount of time depending on the control scheme used in the circuit. In the MMCCC discussed in this paper, there was no control circuit used, as the circuit is intended to produce constant CR regardless of the input voltage variation. The MMCCC circuit was stressed by a step load change at the LV side, and the voltage variations across the various capacitors were observed and recorded. The schematic shown in Fig. 14 was used to characterize this step load variation and a Nicolet Vision data analyzer was used to capture the voltage variation across the capacitors. With one resistive load (5.8 Ω) connected at the output, the power consumption was 229.4 W. The power consumption was abruptly elevated to 510.7 W by adding a 4.2 Ω load into the circuit. Fig. 15 shows the step ON and step OFF load changes across the capacitors of the MMCCC. This figure also shows that the greatest impact is experienced by C_5, and the smallest voltage variation is observed at C_1 during both step ON and step OFF load



(a) (b)

Fig. 15. Experimental results for the capacitor voltages during a step load change. (a) Step ON. (b) Step OFF.



(a) (b)

Fig. 16. Experimental results for the voltage fluctuations at the LV side (V_{C_1}) of the MMCCC during step load change. (a) Step ON. (b) Step OFF.

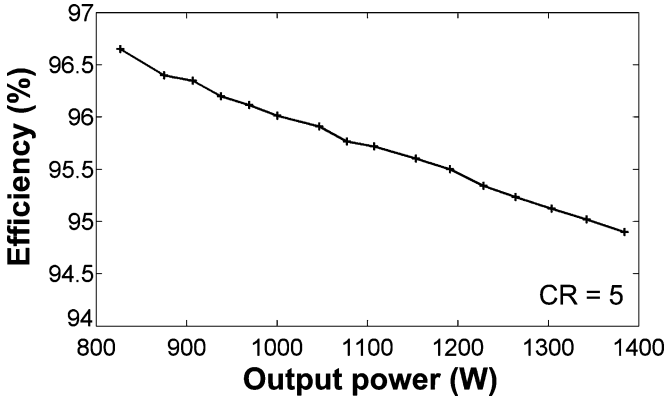


Fig. 17. Experimental efficiency for a 5-kW MMCCC at different loading conditions.

changes. However, the ratio of voltage variation and steady-state voltage across a capacitor is comparable for all capacitors.

The impact of a step load change at the LV side was investigated further, which is shown in Fig. 16. At 229.4 W output, the LV side voltage was 35.66 V, and it decreased to 34.10 V immediately after the additional load was connected to the circuit. The voltage variation is 4.37% of the steady-state value, and the voltage returned to the previous voltage within 0.4 s. Similar behavior occurs during a step OFF transient, and the voltage variation was 4.45%. Differences were observed between the steady-state values before and after the step load change took place. This is expected from the MMCCC circuit without any voltage regulation where the steady-state output voltage decreases with increased output power.

E. Efficiency of the MMCCC

The charge/discharge operation of the MMCCC has similarities with the FCMDC. Thus, a well-constructed MMCCC with proper current traces and appropriate components should be as efficient as an FCMDC. Fig. 17 shows the efficiency profile of a 5-kW MMCCC. The maximum efficiency obtained from this circuit is 96.5%, and efficiency decays with increased load. It was found that the 5-kW MMCCC circuit suffered from voltage drops across the current paths used in the circuit, and this explains why the conduction loss in the circuit starts to dominate at higher output levels. By using fast gate driving circuits, suitable MOSFETs, and adequate current paths, the efficiency level could be extended to the 97%–98% level for the MMCCC. A well-designed FCMDC can achieve efficiency in the range of 96%–98% for various operating conditions [2].

VII. Conclusion

A detailed analytical approach to calculate the capacitor voltages, as well as load voltage of the MMCCC, has been presented. Because the circuit is based on capacitor-clamped topology, the capacitor voltages at various time intervals defines the load voltage for any variation in the load impedance or input voltage, and thereby, the CR of the circuit can be determined. The analysis determines the stability of the load voltage during load variations and the amount of voltage ripple present at the output. The start-up analysis was simplified by reducing one variable from the equation, and the final capacitor voltages were obtained using eigenvalue–eigenvector decomposition. In addition, an average current/charge model was developed, and all the capacitor voltages at various time instants were derived. It was shown how the capacitors exhibit charge balancing among themselves through the steady-state model of the circuit. Finally, the analytical start-up and steady-state quantities were verified by experimental results and analysis.

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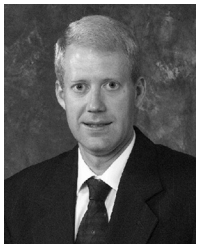

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