Multiple-Load–Source Integration in a Multilevel Modular Capacitor-Clamped DC–DC Converter Featuring Fault Tolerant Capability

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***Abstract*—A multilevel modular capacitor-clamped dc–dc converter (MMCCC) will be presented in this paper with some of its advantageous features. By virtue of the modular nature of the converter, it is possible to integrate multiple loads and sources with the converter at the same time. The modular construction of the MMCCC topology provides autotransformer-like taps in the circuit, and depending on the conversion ratio of the converter, it becomes possible to connect several dc sources and loads at these taps. The modularity of the new converter is not limited to only this dc transformer (auto) like operation, but also provides redundancy and fault bypass capability in the circuit. Using the modularity feature, some redundant modules can be operated in bypass state, and during some faults, these redundant modules can be used to replace a faulty module to maintain an uninterrupted operation. Moreover, by obtaining a flexible conversion ratio, the MMCCC converter can transfer power in both directions. Thus, this MMCCC topology could be a solution to establish a power management system among multiple sources and loads having different operating voltages.**

***Index Terms*—DC–DC power conversion, power capacitors, power conversion, power electronics, power MOSFETs, power semiconductor switches.**

I. Introduction

In AUTOMOTIVE applications, a high-efficiency bidirectional dc–dc converter is a key element to provide the power for the electrical drive train in future hybrid electric or fuel cell automobiles [1]–[11]. A bidirectional capacitor-clamped dc–dc converter is a potential candidate in this application for many advantageous features. One of the major advantages of the capacitor-clamped converter is that it can attain very high efficiency even at partial loads [12]–[19], whereas efficiency drops significantly at partial loads for classical dc–dc converters with an inductive energy transfer mechanism [20]–[22]. There are several different types of multilevel dc–dc converters that have been developed previously [16]–[19], [23]–[27]. The flying capacitor multilevel converter shown in [28] has some potential features to be used in high-power integration that can facilitate multiple dc sources to integrate into the system [29]. Several other approaches to integrate multiple dc sources using multilevel and other topologies of dc–dc converters have been presented in [30] and [31].

A modular circuit is advantageous over a nonmodular structure for several reasons. If the circuit is modular, it is possible to distribute the total power handling capability among multiple modules used in the circuit; therefore, low voltage/current stress is experienced by individual semiconductor devices in the circuit. In addition, a modular circuit incorporates redundancy in the system that yields some fault tolerance properties of the circuit. Using the modularity, it is possible to localize any fault in the system, and the affected module can be bypassed and another good module activated, and thus, a continuity of operation can be maintained. Moreover, the faulty module can be physically removed from the system, and can be repaired or replaced by another module. This feature can facilitate easier maintenance and can obtain higher mean time between failures (MTBFs).

This paper will present some new features of the multilevel modular capacitor-clamped dc–dc converter (MMCCC) that was presented in [28]. One of the key features of the MMCCC topology is that the circuit can be considered as a dc autotransformer having multiple taps where each module provides one intermediate voltage node. Using this feature of the circuit, it becomes possible to simultaneously connect several dc voltage sources having different magnitudes. Thus, the converter may satisfy the need for a power management unit for a system with more than two voltage sources and loads. Moreover, it will also be shown how multiple loads can be connected across the voltage nodes so that several voltage outputs can be obtained from the circuit simultaneously. In Sections II–V, the MMCCC topology and the multiple load/source integration technique will be presented along with simulation and experimental results. Section III will explain the dc autotransformer action of the converter. Section VI will present the redundancy and fault bypass feature of the converter.

II. MMCCC Topology

The five-level MMCCC shown in Fig. 1 has an inherent modular structure and can be designed to achieve any conversion ratio (CR) [28]. Each modular block has one capacitor and three transistors, leading to three terminal points. A modular block is shown in Fig. 2. The terminal $V_{\rm in}$ is connected to either the high-voltage battery or the output of the previous stage. One of the output terminals $V_{\rm next}$ is connected to the input of the

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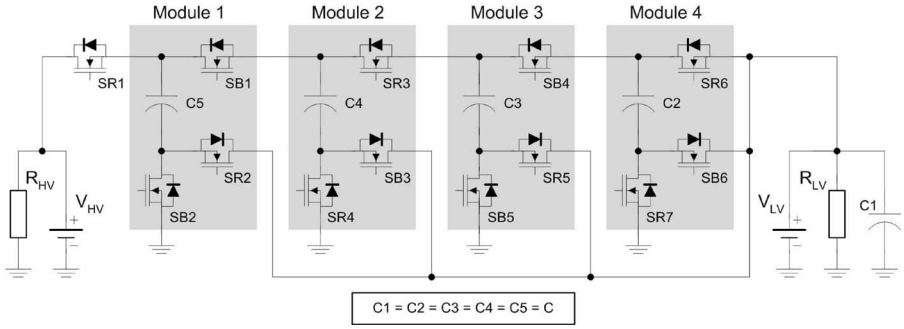


Fig. 1. Schematic of a five-level MMCCC circuit with four modules.

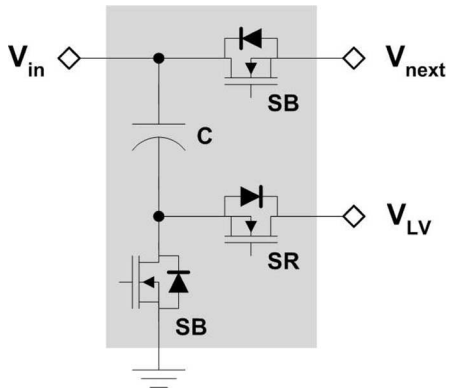


Fig. 2. Schematic of one module of the MMCCC circuit.

TABLE I
SWITCHING SCHEMES OF FCMDC AND MMCCC CIRCUITS

FCMDC		MMCCC	
Sub interval No.	Operations	Sub interval No.	Operations
1	$V_{HV} \rightarrow C_5\uparrow + C_1\uparrow\downarrow$	1	$V_{HV} \rightarrow C_5\uparrow + C_1\uparrow\downarrow$ $C_4\downarrow \rightarrow C_3\uparrow + C_1\uparrow\downarrow$ $C_2\downarrow \rightarrow C_1\uparrow\downarrow$
2	$C_5\downarrow \rightarrow C_4\uparrow + C_1\uparrow\downarrow$		
3	$C_4\downarrow \rightarrow C_3\uparrow + C_1\uparrow\downarrow$		
4	$C_3\downarrow \rightarrow C_2\uparrow + C_1\uparrow\downarrow$	2	$C_5\downarrow \rightarrow C_4\uparrow + C_1\uparrow\downarrow$ $C_3\downarrow \rightarrow C_2\uparrow + C_1\uparrow\downarrow$
5	$C_2\downarrow \rightarrow C_1\uparrow\downarrow$		

↑ = chaging, ↓ = discharging.

next stage. The other output terminal $V_{\rm LV}$ is connected to the low-voltage side + battery terminal or load.

In a flying capacitor multilevel dc–dc converter (FCMDC) with CR of 5, the total operation takes five subintervals [28], [32], and this is shown in Table I. Only one charge–discharge operation is performed in one subinterval. Thus, the component utilization becomes limited in this circuit. For an N-level FCMDC circuit, any capacitor except C_1 is utilized during only two subintervals for a complete cycle (one subinterval for charging, one for discharging) and for the remaining three subintervals in one period, the component is not used. The MMCCC topology can increase the component utilization by performing multiple operations at the same time, which is shown in Table I. In spite of having more transistors for a certain CR, the MMCCC circuit offers better component utilization compared to the FCMDC converter [33].

The switching sequence in the MMCCC circuit works in a simpler way than the FCMDC converter. As there are only two subintervals, two switching states are present in the circuit. Switches $\rm SR_1$–$\rm SR_7$ in Fig. 1 are operated at the same time to achieve state 1. In the same way, switches $\rm SB_1$–$\rm SB_6$ are operated simultaneously to make state 2. The equivalent circuit diagrams that show capacitor charging–discharging operation during these subintervals are shown in Fig. 3, and the switching operations are summarized in Table I. The gate signal sequence to drive the MOSFETs is shown in Fig. 4, and the detail operation of the MMCCC topology can be found in [28] and [32].

III. MULTIPLE-SOURCE INTEGRATION

There are several existing topologies that allow the integration of multiple sources to a dc–dc converter simultaneously [30], [31]. The modular nature of the MMCCC converter creates intermediate voltage nodes at module interconnection points. These intermediate voltage nodes can be used to simultaneously integrate multiple voltage sources to build a power management system among various voltage sources. The five-level MMCCC circuit shown in Fig. 1 has four modules, and every module's input port creates a voltage node in the circuit. Fig. 5 shows a six-level MMCCC converter, and analytically computed voltage levels generated at nodes 1–6 are shown. This figure shows that each node produces a dc voltage with an ac voltage swing superimposed on it. The amplitude of the ac voltage swing is equal to $1V_{\rm LV}$ or V_6. The voltages at different nodes are summarized in Table II.

Using this time-varying nature of these node voltages, some additional voltage sources can be connected at these nodes, and this operation is shown in Fig. 6. Inherently, the MMCCC circuit is a bidirectional converter, and it can be used to manage the power flow between $V_{\rm HV}$ and $V_{\rm LV}$ (Fig. 1) by controlling the CR of the circuit, and the number of active levels present in the circuit governs the CR. The added functionality of the multiple-source integration can facilitate a system to integrate up to seven voltage sources for a six-level converter; which means five additional voltage sources at nodes 1–5 can be connected. This feature may be used to integrate various kinds of energy sources, such as solar cell, fuel cell, battery, etc., having different voltages in the same system.

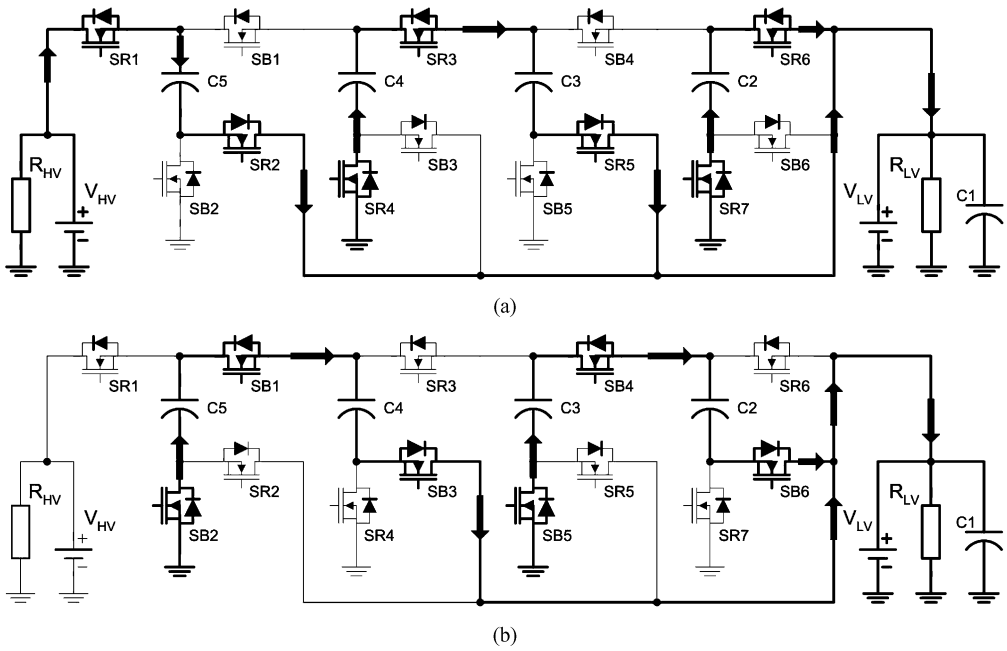


Fig. 3. Charge–discharge operation of the MMCCC converter in different subintervals. (a) State 1. (b) State 2. Converter is operating in down-conversion (buck) mode.

Table II shows the calculated values of the time-varying voltages at different nodes of the six-level MMCCC circuit for the two states present in the circuit. At state 1, the voltage at node 2 is $4V_{\rm LV}$, and during state 2, the voltage is $5V_{\rm LV}$. Thus, if an external voltage source of amplitude $4V_{\rm LV}$ is connected to node 2, it will contribute power along with $V_{\rm HV}$ to the low-voltage side of the converter during state 1. During state 2, the voltage at node 2 becomes $5V_{\rm LV}$, which is higher than the external source voltage; thus, the converter will not draw any power from the external source connected at this node. In the same way, four other voltage sources can be connected at nodes 1, 3–5.

While connecting multiple sources in the system, one issue needs to be considered to keep the ripple component present at the load voltage within a specific range. The origin of the ripple voltage at the LV-side output lies in the time-decayed voltages across the capacitors when they are subjected to provide load current. If the capacitors are discharged to provide a large load current, the voltage across them drops at a higher rate, and the ripple voltage increases. To reduce ripple in the output voltage, multiple stacked-capacitor branches are connected in parallel in each subinterval in an MMCCC converter, and it was shown in [28] and [32] how these parallel current paths exist in each subinterval of the MMCCC operation.

The ripple component at the output depends on how many parallel current paths are present in any subinterval. Capacitors inside the MMCCC converter act as energy storage, and more number of parallel paths ensure greater current delivering ability for a certain voltage ripple. This is why less number of parallel paths generate greater voltage ripple for a certain load current. However, the number of parallel current paths in each subinterval depends on the CR of the circuit, and they are the same in each subinterval when the CR is an even number [28], [32]. As an example, two parallel current paths exist in both subintervals

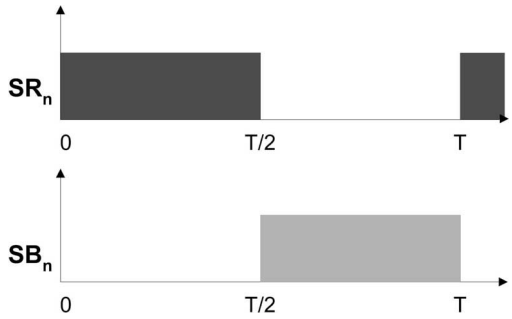


Fig. 4. Two gate driving signals for the MMCCC converter.

in a four-level MMCCC converter, and the ripple component present in the output voltage is the same in each subinterval. On the other hand, three parallel current paths exist in state 1 and two paths exist in state 2 for a five-level MMCCC converter. Fig. 7(a) shows the three current paths in state 1 for a five-level configuration, and these paths are I_5, I_3 (or I_4), and I_2. In state 2, two current paths exist, and they are I_5 (or I_4) and I_3 (or I_2). The current through C_1 is not considered here because C_1 is charged and discharged in the same subinterval and all other capacitors have only one operation (charge or discharge) in each subinterval. The current paths for a four-level configuration are shown in Fig. 7(c) and (d).

When a voltage source is connected to $V_{\rm HV}$, and a load is connected to $V_{\rm LV}$, the current flow from $V_{\rm HV}$ in each subinterval depends on the number of parallel paths active in each subinterval. Thus, when the MMCCC converter works with an even CR, the discharge rate of the capacitors have the same value during both subintervals, and the ripple voltage at the LV side is the minimum. However, when the CR is odd, the number of paralleled current paths are not equal, and the numbers are three

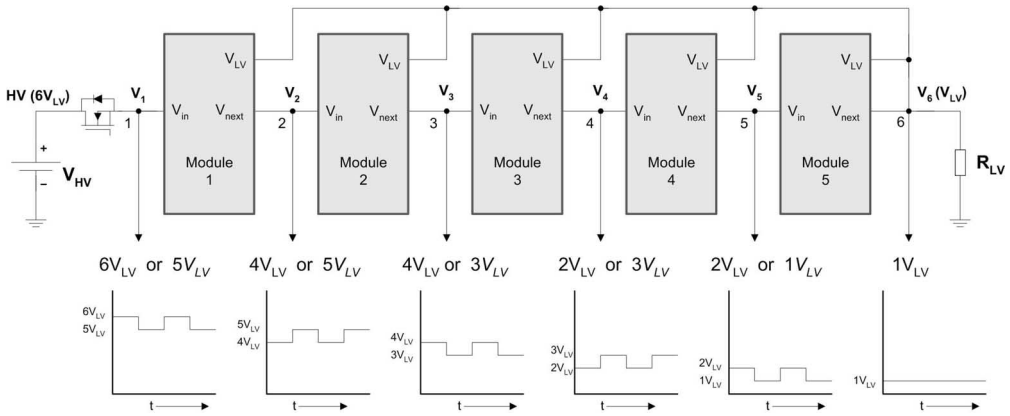


Fig. 5. Schematic of a six-level MMCCC converter with intermediate node voltages labeled. The bottom part shows the calculated voltages at those nodes.

TABLE II
TIME-VARYING NODE VOLTAGES OF A SIX-LEVEL MMCCC CIRCUIT

State	Active Switches	V_1	V_2	V_3	V_4	V_5	V_6
1	S_{R1}- S_{R7}	$6V_{LV}$	$4V_{LV}$	$4V_{LV}$	$2V_{LV}$	$2V_{LV}$	$1V_{LV}$
2	S_{B1}- S_{B6}	$5V_{LV}$	$5V_{LV}$	$3V_{LV}$	$3V_{LV}$	$1V_{LV}$	$1V_{LV}$

(3) and two (2) consecutively in a five-level MMCCC circuit in alternate subintervals. To keep the ripple components matched in each subinterval, the duty ratio in each subinterval needs to be adjusted. For an odd CR with a value n, the number of parallel current paths is $(n+1)/2$ in subinterval 1, and it is $(n-1)/2$ in subinterval 2. The amount of ripple at the output in each subinterval is proportional to the ratio of the number of paralleled current paths and the time duration of the subinterval. For this reason, when the converter delivers current with a higher number of parallel paths, it can maintain the allowed ripple voltage for longer time duration. On the other hand, fewer paralleled paths maintain the ripple specification for shorter time duration. Thus, the ratio of time durations of subinterval 1 and 2 should be $(n+1)$:$(n-1)$. If this ratio is not maintained, the ripple component at the load cannot be maintained at the minimum level, and they will be unequal in different subintervals. Fig. 8(a) shows the simulated output voltage of a five-level converter when the ratio of these durations is 1:1. When the ratio is made 3:2, it produces significantly smaller ripple, and this is shown in Fig. 8(b). The ripple voltage (p–p) in the first case is 632.2 mV, and it is only 168.2 mV for the later case. These simulation results are obtained by applying a 70-V source at the HV side and a 1-Ω load connected at the LV side of a five-level MMCCC converter.

The correlation of the ripple component with the CR discussed in the preceding section is responsible for defining two subsets of voltage nodes that can be used to integrate voltage sources in the MMCCC converter. When the converter is operating with an even CR and a source is connected at $V_{\rm HV}$, the durations of subintervals 1 and 2 are same. Now, if another voltage source is connected at V_2, it will provide power to the LV side with equal number of paralleled current paths in each subinterval. Thus, the current drawn from V_2 will have the same phase with $V_{\rm HV}$. The effective number of modules between this source and load at $V_{\rm LV}$ is 3 because the source connected at V_2 contributes current only when this node voltage becomes close to $4V_{\rm LV}$. Therefore, the ripple component at the LV side remains the same after connecting V_2 into the system, and the current shared by V_2 is in phase with the current provided by $V_{\rm HV}$.

Now, if a voltage source is connected at V_3, the effective number of modules between V_3 and the LV side becomes 2. If V_3 would be the only voltage source connected in the system, the duty ratio of subintervals 1 and 2 are required to change because of an odd CR effective in the circuit. As long as $V_{\rm HV}$ and V_2 are already connected in the system, and the CR is even, any voltage source will increase the load voltage ripple if it is connected at V_1, V_3, or V_5 node. For the same reason, if a voltage source is connected at V_1 only, the effective CR would be odd, and the duty ratios of the subintervals are needed to be adjusted. After doing that, voltage sources can be connected at V_3, or V_5, and the load ripple quantity would be unaffected.

Thus, when the converter works with an even CR, voltage sources can be connected simultaneously at $V_{\rm HV}, V_2, V_4$, and $V_{\rm LV}$. On the other hand, sources can be connected simultaneously at V_1, V_3, and V_5 with an odd CR effective in the circuit. However, sources from these two groups can be used in a mixed operation if the increase in the LV-side ripple voltage is ignored.

A conventional dc–dc converter typically connects one load and one source, and bidirectional dc–dc converters can have loads and sources at both ends. Future applications such as hybrid electric or fuel-cell automobiles may involve multiple sources in the system, such as engine generator, batteries of different voltage levels, supercapacitors, photovoltaic cells, etc. The MMCCC converter facilitates multiple intermediate voltage nodes, and multiple sources and loads could be simultaneously connected to the converter at these intermediate nodes. When the MMCCC converter is already connected to a source, the voltages at these nodes are automatically defined by the location of the node. If an additional source needs to be connected, it should be close to the voltage at the node where it needs to be connected. In Fig. 5, if the circuit is powered by $V_{\rm HV}$, any other available voltage source of amplitude $4V_{\rm LV}$ can be connected at node 2. In the same way, a voltage source of amplitude $3V_{\rm LV}$ could be

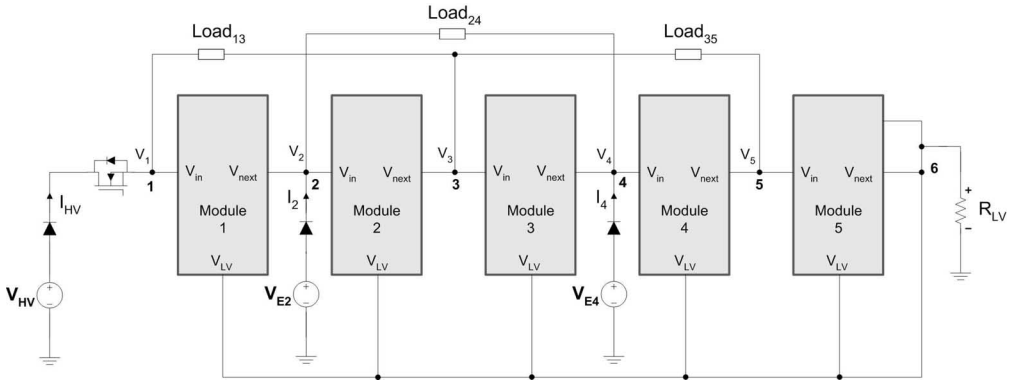


Fig. 6. Schematic of the voltage source and load integration in the MMCCC converter.

connected at node 3, and a $2V_{\rm LV}$ source can be connected at node 4. In addition, two other voltage sources could be connected to the system at nodes 5 and 6.

IV. Multiple-Load Integration

The other advantage of this integration feature is the ability to connect multiple loads at the same time. Fig. 5 shows the no-load voltages at different nodes of the MMCCC circuit. Nodes 1–5 generate time-varying voltages; however, a dc load cannot be connected between any of these nodes and ground. This figure also shows that the time-varying voltage at nodes 1, 3, and 5 have the same phase. This is true for nodes 2 and 4 also. Thus, it is possible to connect a load in various ways between these in-phase nodes. Fig. 6 shows how loads can be connected between nodes (1, 3), (2, 4), and (3, 5) to obtain a constant dc voltage across the loads. The voltage across the load connected between node 6 and ground is $1V_{\rm LV}$ and the voltage difference between two adjacent in-phase nodes is $2V_{\rm LV}$. In the same way, the voltage difference between nodes 1 and 5 is $4V_{\rm LV}$. Thus, it is possible to connect multiple loads of $1V_{\rm LV}$, $2V_{\rm LV}$, and $4V_{\rm LV}$ simultaneously in a six-level MMCCC circuit. This feature adds the flexibility to integrate multiple loads simultaneously and it is not required for any efficiency improvement.

Multiple-load integration feature is especially useful for future hybrid or fuel-cell automobile power architecture where electrical loads of multiple voltage levels will be present [4], and a power management system will be essential to mitigate the demands for various loads. The MMCCC converter thus gains the momentum to work as a power management system by offering the integration of multiple loads and sources simultaneously for future automobiles.

V. Experimental Results

To verify the concept of integrating multiple loads and sources in the circuit, an experimental setup was made, and the schematic in Fig. 6 was followed. A 500-W six-level MMCCC prototype shown in Fig. 9 was used. The circuit has five (5) modules, and each module has three IRFI540N MOSFETs and one 1000 μF capacitor. One bootstrap MOSFET gate driver and one single MOSFET gate driver are used inside each module to drive these MOSFETs. The switching frequency of the circuit is 10 kHz.

Three bench-top power supplies were used as $V_{\rm HV}$, V_{E2}, and V_{E4}. One 3-Ω load was used as $R_{\rm LV}$, and two 24-Ω loads were used as $\rm Load_{24}$ and $\rm Load_{35}$. In addition, one 48-Ω resistor was used as a load connected between nodes 1 and 5. The main input voltage $V_{\rm HV}$ was kept at 75 V. Fig. 10(a) shows the no-load voltages at HV (the cathode terminal of the diode connected to $V_{\rm HV}$), V_1 and V_2 nodes. Fig. 10(b) shows the voltages recorded at V_3, V_4, V_5, and $V_{\rm LV}$ nodes. These voltages have the same variations in phase and magnitude found in the calculation (shown in Fig. 5). The voltages at nodes 1–5 have a swing of $1V_{\rm LV}$. Thus, the voltage at node 5 varies between 12.3 and 25 V. There was a small voltage swing of 1.4 V found at the HV node, although it was supposed to be a constant value of 75 V obtained from $V_{\rm HV}$. This voltage was measured at the converter board and not across the power supply terminals. Due to the voltage drop across the current sampling resistor and wire stray inductance, a small ripple was observed at this voltage input port of the converter.

Figs. 11 and 12 show how three sources connected to the converter can share the total load current simultaneously. For this experiment, a 3-Ω resistive load was connected across the $V_{\rm LV}$ node and ground. This power sharing operation was tested in two steps. In the first step, $V_{\rm E2}$ was kept less than 48 V and $V_{\rm E4}$ was kept less than 24 V. During this time, there was no power flow from these two sources, and this is shown in Fig. 11(a). In this step, $V_{\rm HV}$ was kept at 75.8 V. When $V_{\rm E2}$ is increased to go beyond 48 V level, it starts to share the power delivered to the output side, and this is shown in Fig. 11(b). When $V_{\rm E2}$ reaches 52 V, it delivers the entire power to the load and no current is drawn from the $V_{\rm HV}$ source. This is shown in Fig. 11(c). If $V_{\rm HV}$ is removed from the system, $V_{\rm E2}$ can provide the total power to the load with a voltage lower than 52 V. This time V_2 (before connecting $V_{\rm E2}$) decreases due to the absence of any current injected by $V_{\rm HV}$, and a lower $V_{\rm E2}$ ($\sim$50 V) is required to flow the same current to the load as when $V_{\rm HV}$ was present.

In the second case, $V_{\rm E4}$ was used to share the load current. Fig. 12(a) shows the situation when the magnitude of $V_{\rm E4}$ was raised to 26.75 V so that it starts to share the load current with $V_{\rm E2}$. This time, $V_{\rm HV}$ and $V_{\rm E2}$ were kept the same as they were in case 1. When $V_{\rm E4}$ was raised to 30.7 V, it provided the entire power to the load, and power delivered by $V_{\rm HV}$ and $V_{\rm E2}$ became zero. This is shown in Fig. 12(b). However, if $V_{\rm HV}$ and $V_{\rm E2}$ are

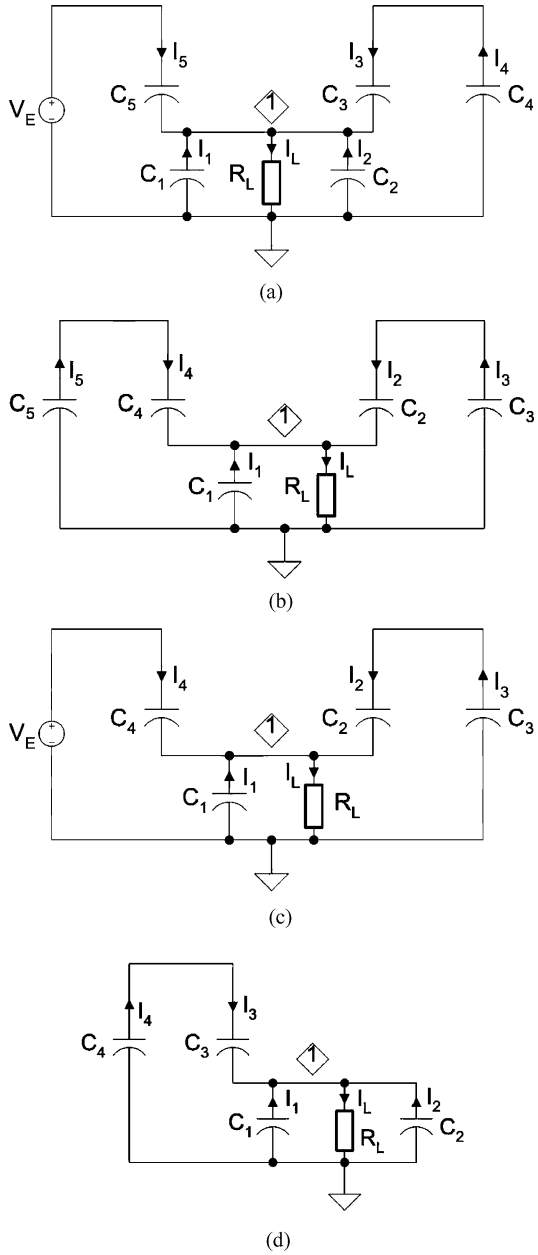


Fig. 7. Equivalent circuit diagram of the MMCCC converter with different number of parallel paths for odd and even CRs. (a) State 1 diagram with CR = 5. (b) State 2 diagram with CR = 5. (c) State 1 diagram with CR = 4. (d) State 2 diagram with CR = 4.

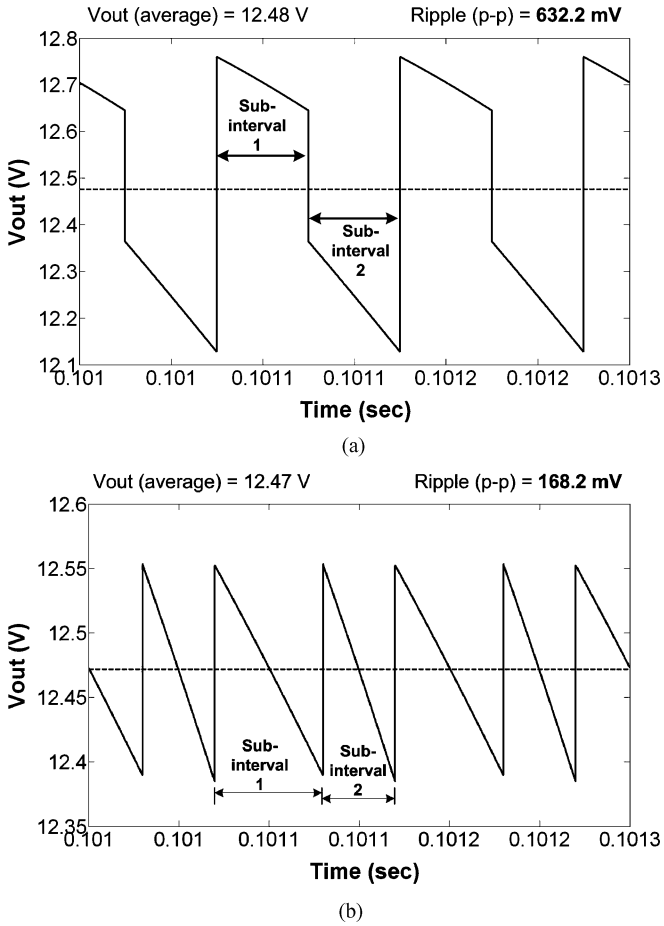


Fig. 8. Simulated output voltage ripple of a five-level MMCCC converter for different ratios of state 1 and state 2 time durations. (a) Output voltage ripple when both subintervals have same durations. (b) Output voltage ripple when the ratio of time durations of state 1 and state 2 is 3:2.

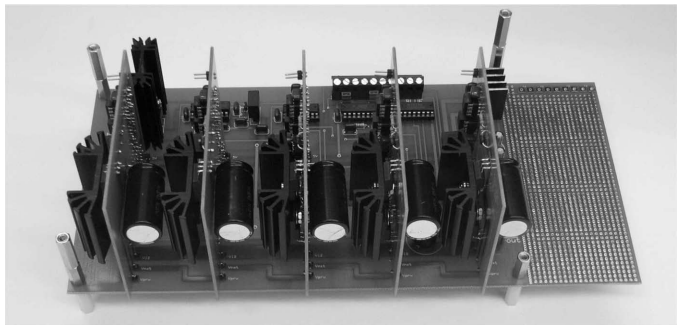
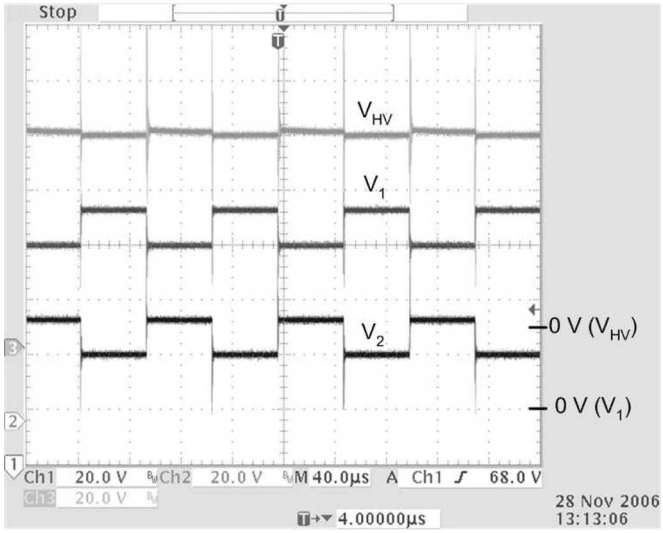


Fig. 9. Experimental 500-W six-level MMCCC converter proof of concept.

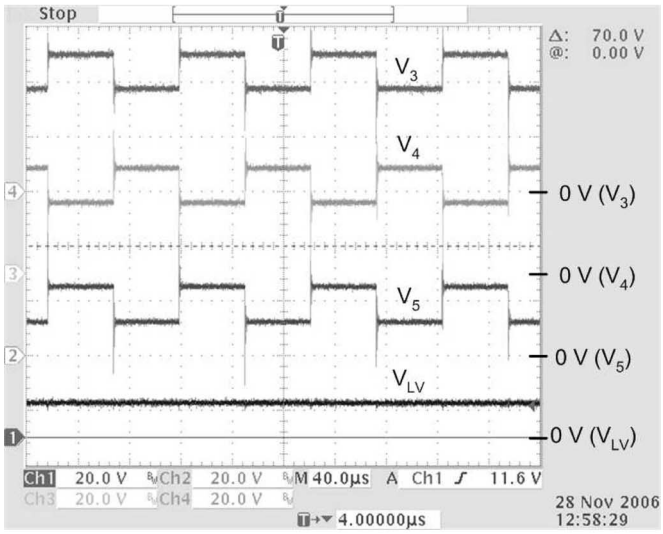
removed from the system, $V_{\mathrm{E}4}$ can deliver the total power with a voltage less than 30.7 V. When the magnitude of $V_{\mathrm{E}2}$ and $V_{\mathrm{E}4}$ were reduced, V_{HV} was back in operation, and all of these three dc sources shared the load current. This is shown in Fig. 12(c).

Fig. 13 explains the multiple-load integration method in the system. Voltages V_{35} and V_{LV} are shown in Fig. 13(a), and it can be seen that the voltage across Load_{35} is almost $2V_{\mathrm{LV}}$. Fig. 13(b) shows the load voltages across R_{LV} and Load_{24} (24 Ω). Similar to Load_{35}, Load_{24} also experiences a voltage of approximately $2V_{\mathrm{LV}}$. In Fig. 13(c), the load voltage R_{LV} and voltage across Load_{15} (48 Ω) are shown, and voltage across Load_{15} was found to be almost four times V_{LV}. These experiments prove that three different kinds of loads having voltages $1V_{\mathrm{LV}}$, $2V_{\mathrm{LV}}$, and $4V_{\mathrm{LV}}$ can be connected simultaneously in the MMCCC circuit.

The efficiency of a switched capacitor circuit depends on several factors such as number of levels (CR), $R_{\mathrm{DS}}(\mathrm{ON})$ of the MOSFETs, the equivalent series resistance (ESR) of the capacitors, and the load current. The efficiency is a function of output impedance (R_O) and load impedance (R_L) for a Fibonacci converter presented in [15], where $\eta = [1/(1 + R_O/R_L)]$. Thus, efficiency can be significantly improved by decreasing the output impedance of the converter that requires the use of low



(a)

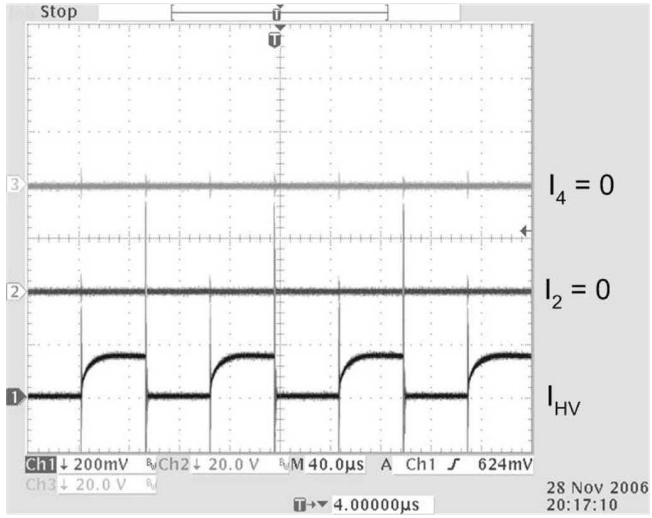


(b)

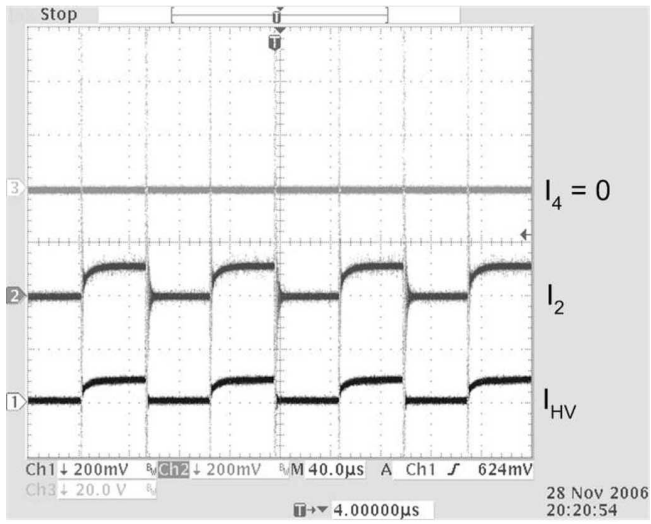
Fig. 10. Node voltages in experimental six-level MMCCC at no-load condition. (a) Voltages $V_{\rm HV}$, V_1, and V_2. (b) Voltages V_3, V_4, V_5, and $V_{\rm LV}$. The converter was operated in down-conversion mode. All voltages are scaled to 20 V/division.

$R_{\rm DS}({\rm ON})$ MOSFETs and capacitors with lower ESR. Usually, the ESR has an inverse relationship with the capacitance [14], and the electrolytic capacitors used for a high-power MMCCC circuit offers very low ESR, which is in the range of milliohms. Recently, MOSFETs can offer very low $R_{\rm DS}({\rm ON})$ that could be even less than 10 mΩ. By paralleling capacitors and MOSFETs, the output impedance of the circuit can be reduced further.

The series–parallel converter discussed in [12] presents an analytical approach to calculate the efficiency of the converter, and the efficiency is defined as a function of the number of capacitors used in the circuit and the ratio of the output and input voltage of the converter. The experimental results presented in [12] shows the maximum efficiency of the converter that is 87.3%, and the $R_{\rm DS}({\rm ON})$ of the MOSFETs is 0.25 Ω. Typically, the $R_{\rm DS}({\rm ON})$ of this magnitude is the greatest source of power losses in the



(a)



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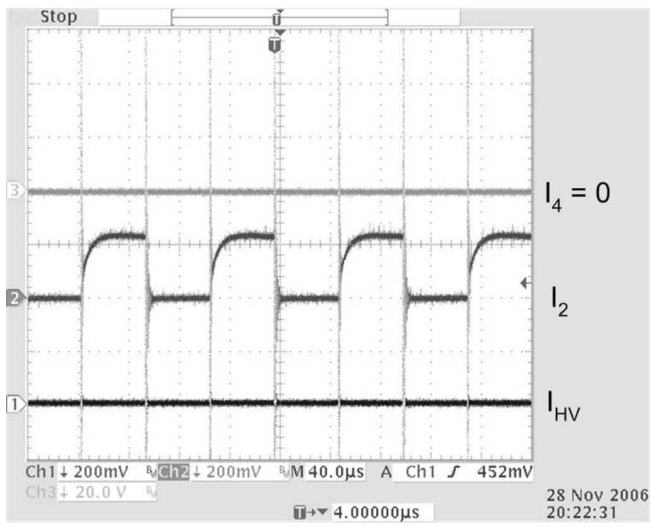
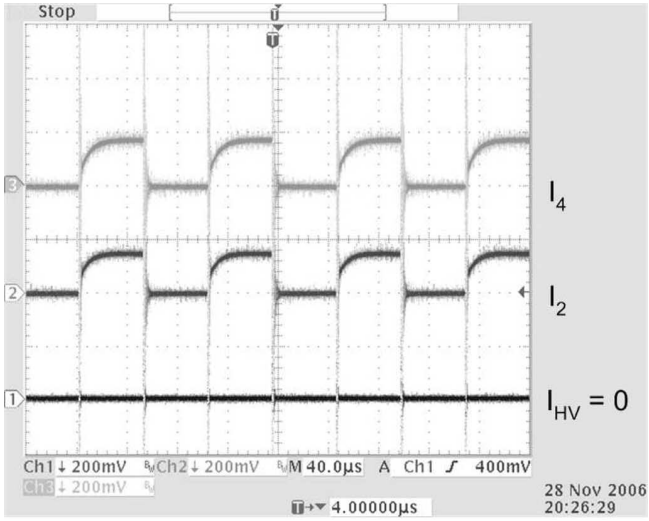


(c)

Fig. 11. Experimental input currents (2 A/division) shared by three sources ($V_{\rm HV}$, $V_{\rm E2}$, and $V_{\rm E4}$ in Fig. 6). (a) Total current is provided by $V_{\rm HV}$ (75.8 V). (b) Current is shared by $V_{\rm HV}$ and $V_{\rm E2}$ (51.8 V). (c) Total current is provided by $V_{\rm E2}$ (52 V) only.



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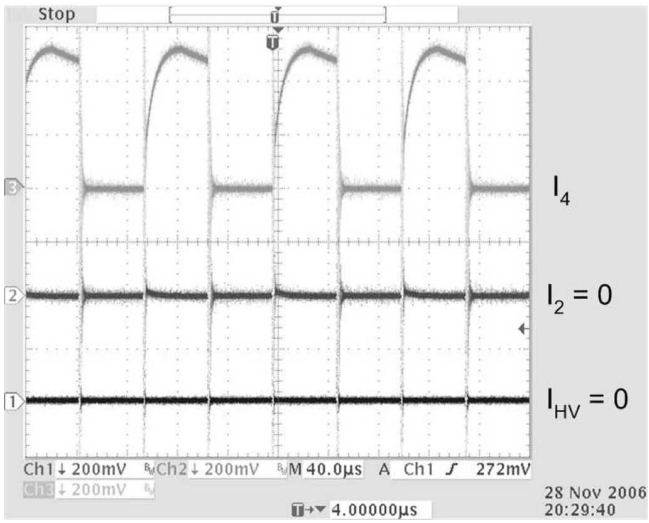

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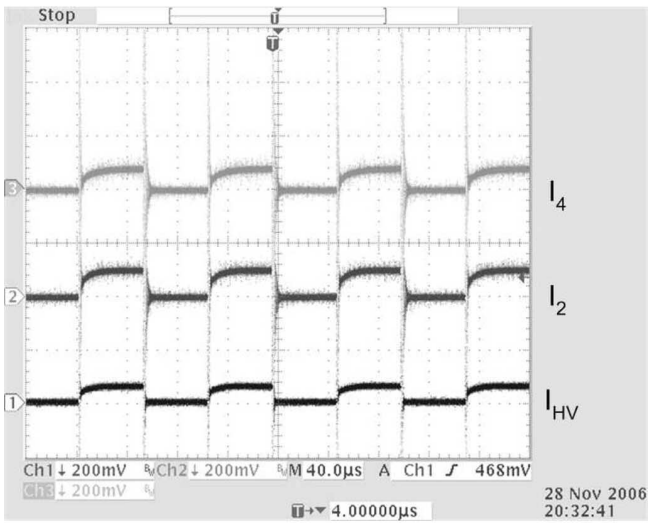
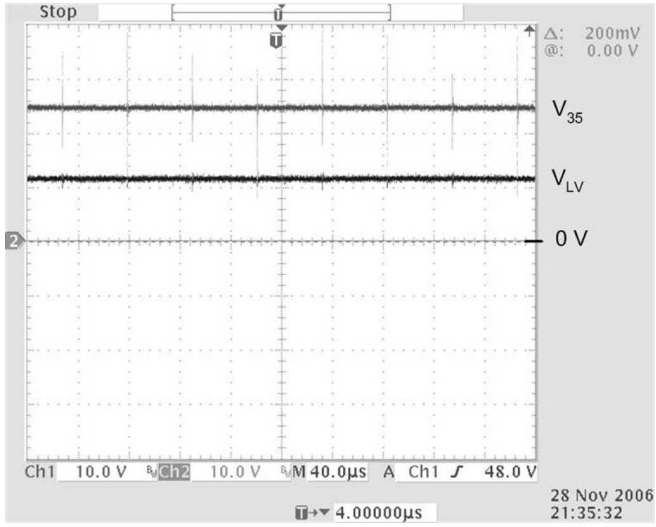


(c)

Fig. 12. Input currents (2 A/division) shared by three sources ($V_{\mathrm{H}V}$, $V_{\mathrm{E}2}$, and $V_{\mathrm{E}4}$ in Fig. 6). (a) Current is shared by $V_{\mathrm{E}2}$ (52 V) and $V_{\mathrm{E}4}$ (26.75 V). (b) Total current is provided by $V_{\mathrm{E}4}$ (30.7 V) only. (c) Total current is shared by $V_{\mathrm{H}V}$ (75.9 V), $V_{\mathrm{E}2}$ (51.2 V), and $V_{\mathrm{E}4}$ (26.07 V).



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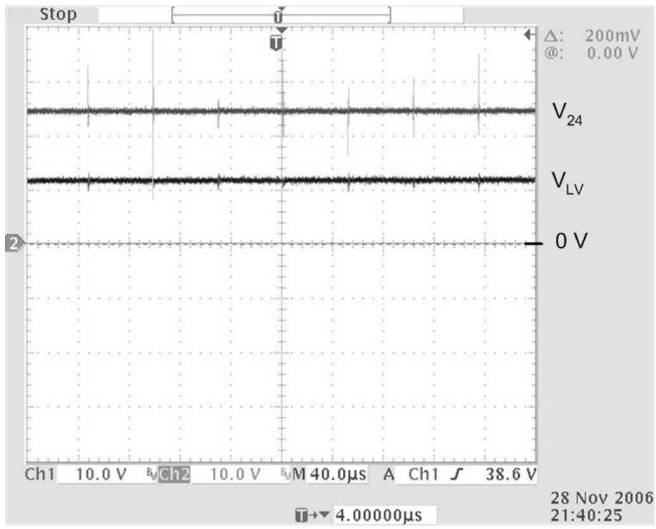

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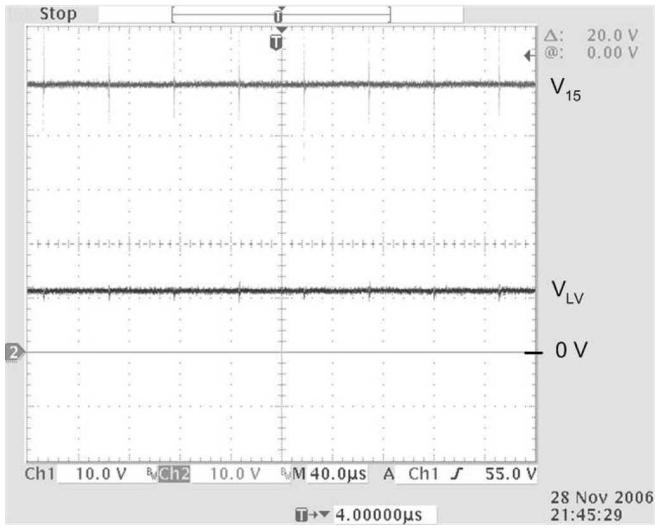
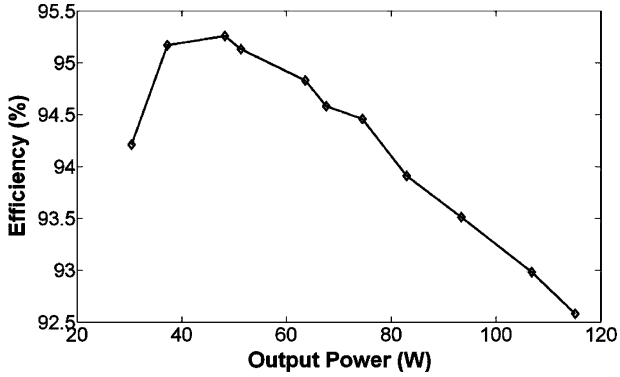


(c)

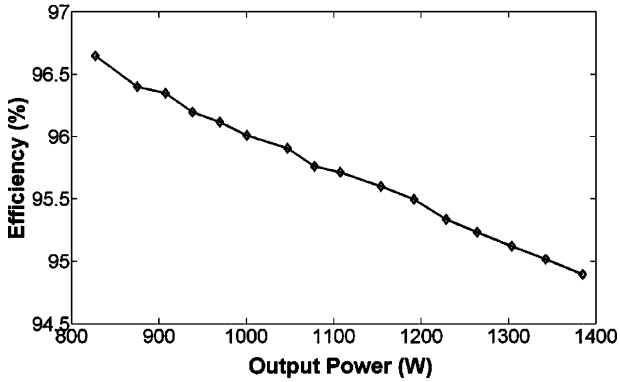
Fig. 13. Experimental load voltages connected between intermediate nodes. (a) V_{LV} and V_{35}; and V_{35} is two times V_{LV}. (b) V_{24} and V_{LV}. (c) V_{15} and V_{LV}; and V_{15} is four times V_{LV}. All voltages are scaled to 10 V/division.

circuit, and the efficiency can be significantly improved by using MOSFETs with very low $R_{\mathrm{DS}}(\mathrm{ON})$. The capacitor-clamped converter presented in [16] thus achieves efficiency as high as 98% at low power output.

It was discussed in [32] how the MMCCC converter achieves the voltage-clamping features of an FCMDC and charge equalization features of a series–parallel converter. Thus, by considering the issues of these two converter types, the efficiency can be improved even for high output power. The 500-W six-level MMCCC circuit was tested for efficiency measurements, and the test results are shown in Fig. 14(a). The efficiency of a 5-kW prototype presented in [33] is shown in Fig. 14(b) for various loading conditions. A maximum efficiency of 96.5% can be achieved for the 5-kW version. However, the efficiency of a dc–dc converter greatly depends on the topology as well as the design of the converter construction. The practical design involves the choice of components, gate drive circuits, printed circuit board (PCB) layout, sizing of current carrying conductors, etc. In addition, switched-capacitor circuits typically offer lower efficiency at higher output power [15], and the efficiency greatly varies with the output voltage ripple [16]. The current-carrying conductors in both MMCCC prototypes suffered from considerable voltage drops at high current levels, and they significantly reduced the efficiency at higher output power levels. A well-designed prototype of an MMCCC circuit should offer efficiency as high as 96% at full-load, and even higher at partial loads.



(a)



(b)

Fig. 14. Efficiency of the MMCCC converter at different loading conditions. (a) Efficiency of the 500-W prototype. (b) Efficiency of the 5-kW prototype.

VI. Redundancy and Fault Bypass Capability

To take the full advantage of the modular structure, some redundancy is introduced in the MMCCC circuit. This unique feature of the MMCCC topology enables an uninterrupted operation when there are certain kinds of faults in the modules. When transistor SB_1 in Fig. 1 is permanently ON and the other two transistors are permanently OFF, the module works as a bypass module. In this condition, the module does not participate in the operation of the converter and simply bypasses the current through itself. During the normal operation that is defined as the active state, all three transistors in a module are controlled by the proper gate-driving signals. Thus, any module can be operated in either active state or bypass state by activating appropriate control signals in a module.

To get some level of redundancy in the system, some modules are operated in bypass state and the remaining modules work in active states. When a fault is detected inside any of the active modules, the main board control circuit detects the location of the fault and sends a signal to the faulty module, and therefore, bypasses the module. However, to keep the CR unchanged, the control circuit engages one of the redundant modules, which was in bypass state so far. As a result, an uninterrupted operation can be confirmed. The level of redundancy is application-specific, and the number of redundant levels can be as many as needed. Nevertheless, a module cannot be bypassed if the bypass transistor (S_{B1} in Fig. 1) experiences an open circuit fault; the converter stops operating in this fault situation. In addition, if there is a sustained short circuit fault (which is a rare occurrence in MOSFETs) with the other two transistors inside a module, the circuit also fails to operate. In spite of these two limitations, the MMCCC converter offers better reliability compared to the FCMDC converter because the FCMDC converter fails to operate if there is any open- or short-circuit fault with any of the transistors inside the circuit.

Fig. 15 explains the redundancy and fault bypass operation, and shows how the converter can withstand a fault and continue its normal operation. A three-level converter with two redundant modules is shown in Fig. 15. During normal operation, modules 1 and 2 work as active modules, and modules 3 and 4 work as bypass modules, as shown in Fig. 15(a). Fig. 15(b) shows a situation where a fault has occurred in module 2. To keep the CR unchanged, the converter needs two active modules in the system. This time, the control circuit detects the location of the fault and bypasses module 2. Then, it engages module 3 in active state, which was in bypass state so far, as shown in Fig. 15(c). From this moment, modules 1 and 3 work as active modules, and modules 2 and 4 work as bypass modules. At this point, the present state of the circuit is capable of handling one more fault that can be bypassed using module 4.

Using the redundancy feature, true bidirectional power management can also be established in the circuit. Thus, it is possible to increase or decrease the number of levels and thus the CR [33]. When a multilevel converter is used to transfer power between two voltage sources, the direction of power flow

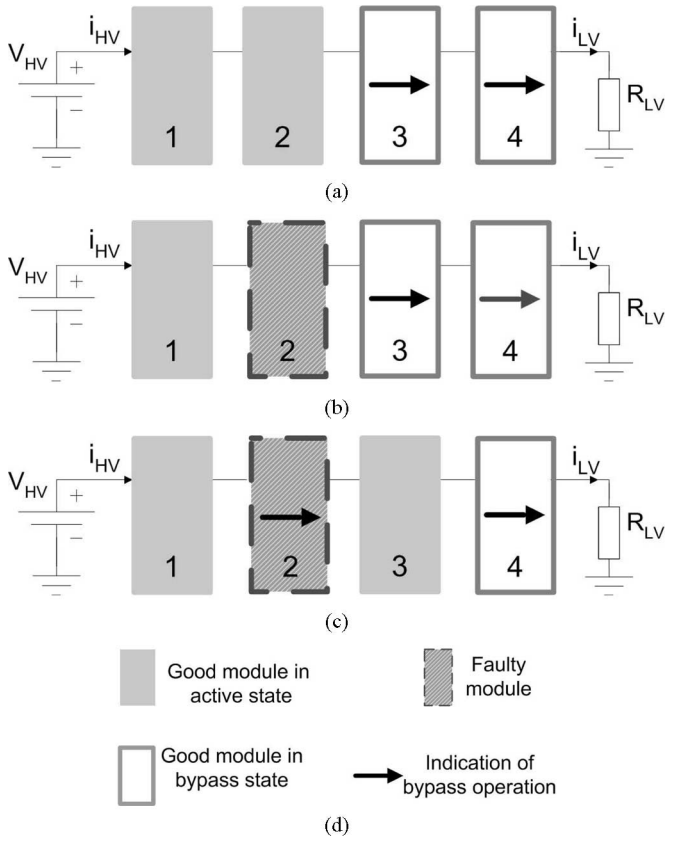


Fig. 15. Redundancy and fault withstand capability of the converter. (a) Three-level converter running at normal operating mode with two redundant modules (3 and 4). (b) Fault occurred in module 2. (c) Module 2 went into bypass mode and replaced by module 3.

is governed by the ratio of the two voltage sources (RVSs) and the CR. Unlike the RVS, the CR is usually an integer value for capacitor-clamped converters, and when the CR is greater than the RVS, the low-voltage source transfers power to the high-voltage source. On the other hand, a CR lesser than the RVS will force the converter to transfer power from the high-voltage side to low-voltage side. However, depending on the battery condition, RVS may change; and for a fixed CR, the power flow may change its direction, even if it is not desired. In this situation, a variable CR could solve this problem, and in the MMCCC circuit, the CR value can be changed by adding or subtracting a level in the system. Thus, a four-level converter can be operated in either a three- or a five-level configuration only if it has redundant levels available, and true bidirectional power management can be established. For a finer control on the CR, the duty ratio of the gate drive signal may be changed, and it becomes possible to get a more precise control of the current.

VII. Conclusion

A new topology of modular multilevel dc–dc converter has been proposed, and the multiple-load–source integration technique has been presented and verified through experiments. The test results show that several voltage sources can be connected to the different nodes of the circuit, and the load power requirement can be mitigated by those voltage sources in a combined fashion. Thus, it becomes possible to achieve CRs of multiple integer values from the circuit, and a complete power management protocol can be established among various voltage sources. Moreover, the circuit can generate different load voltages simultaneously, and this feature makes it possible to obtain various output voltages from a wide input voltage range. Thus, this feature helps to consider the MMCCC converter as a dc autotransformer having multiple taps to connect multiple loads and dc sources at the same time.

In addition to this feature, the modular nature of the MMCCC topology can be successfully used to obtain redundancy and fault bypassing capability in the system. This feature can increase the reliability of the system, and decreases the downtime of the converter. Moreover, the circuit is capable of bidirectional power handling. Thus, all these features make the MMCCC topology a suitable candidate in various applications.

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