

Development of a 55 kW 3X DC-DC Converter for HEV Systems

Wei Qian and Fang Z. Peng

Department of Electrical and Computer Engineering
Michigan State University
East Lansing, MI, USA, 48824
qianwei@egr.msu.edu

Leon M. Tolbert

Electrical Engineering and Computer Science
University of Tennessee
Knoxville, TN, USA, 37996

Abstract—The design of a 55 kW 3X dc-dc converter is presented for hybrid electric vehicle (HEV) traction drives. It can interface the battery with the inverter dc bus with three output/input voltage ratios and have smooth transition in voltage ratio changes. By making use of the parasitic inductance, the size and weight of the converter are significantly reduced. Its magnetic-less feature and high efficiency provide the great potential for the very high temperature operation. The circuit parameter design and the circuit modeling are provided. Experimental results are given to verify the analysis and design concepts.

Keywords- DC-DC power conversion; multilevel converter; pulse width modulation; voltage multipliers; voltage dividers.

I. INTRODUCTION

A typical Plug-in HEV drive train consists of a battery, a power converter and a traction motor to drive the vehicle. In most commercial HEV systems, the power converter is a bidirectional dc-dc converter plus an inverter. The dc-dc converter interfaces the battery and the inverter with variable dc bus voltages, so that the inverter can always operate at its optimum operating point. In the traditional dc-dc converters, the magnetic components are employed. They are bulky, heavy, costly, and always one of the hottest parts in the system. Hence, with the trend of higher coolant temperatures, those converters already hit the limit of obtaining high efficiency while reducing the size and weight. Further, as temperature goes up over 250 °C, the permeability of the magnetic materials declines drastically. So the magnetic components are unstable and are prone to get saturated, not to mention the upper limit of the winding insulation. With the technical development of wide bandgap devices and multi-layer ceramic capacitor (MLCCs), the ever-higher temperature components will be available expect the magnetic cores. Especially, the technology of MLCC enables low ESR and thus high ripple current capacity in a compact package. Some commercially available MLCCs present very unique temperature characteristics. They can handle even higher ripple current at elevated temperature, thanks to the material property and manufacture process. So it becomes possible to eventually eliminate the need for forced cooling for the magnetic-less dc-dc converters.

The magnetic-less property and high efficiency make the multilevel dc-dc converter a promising candidate for the very

high temperature applications. However, the main concern of the existing multilevel dc-dc converters is their constrained output voltage range for a given input. So [1] proposes a 3X dc-dc converter that realized three different output/input voltage ratios with the minimum components count (semiconductor devices and capacitors). The voltage stress is also the lowest compared to other multilevel dc-dc converters. As in some commercial HEVs, by the combination of the discrete voltage ratios from the dc-dc converter and the continuous control of the modulation index of the inverter, it is sufficient to operate the inverter in its efficient operation range. As a result, the drive train can be rated properly to accommodate the high voltage demand for the high speed range of the vehicle. This paper will focus on some design issues for the 55 kW dc-dc converter.

II. BASIC OPERATION PRINCIPLE

The 3X dc-dc converter represented in Fig.1 employs the same topology as in [2]; however, with three different PWM methods, the voltage ratio V_{out}/V_{in} can be 1, 2 and 3 in steady state. Because of its bi-directional nature, the converter can be viewed as a multiplier or a divider based on the definition of source and load.

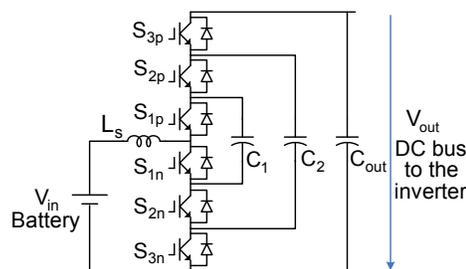


Fig 1. Topology of the 3X dc-dc converter

To achieve the voltage ratio of 1, namely 1X, the converter always operates in one switching state as shown in Fig.2, with all the switches (IGBTs with freewheeling diodes) except S_{1n} always turned on. Thus, the output is directly fed by the input. When the desired ratio is 2, the converter alternates with 1/2 duty ratio between two switching states I and II illustrated in Figs.3 (a) and (b). In state I, the capacitor C_1 is connected to the battery; in state II, C_1 is in series with the battery to connect with C_2 and C_{out} . Consequently, the voltage ratio will be kept to

2X. In the same manner, in 3X mode, the converter circulates from switching states I, II to III as shown in Figs.4 (a), (b) and (c), with 1/3 duty ratio per state. After these three states, the

capacitor voltages will be balanced automatically and the output voltage is three times the input voltage.

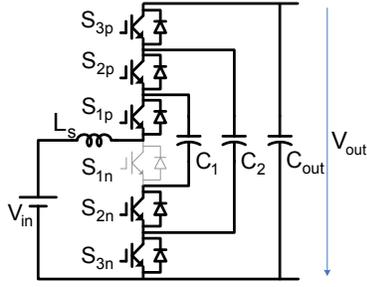
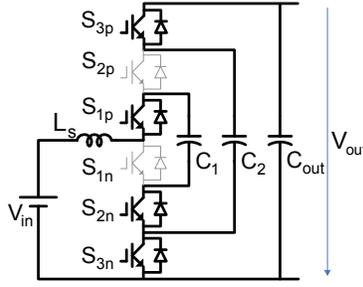
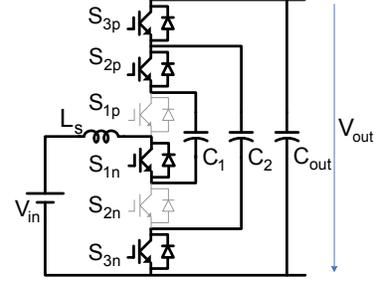


Fig 2. Switching patterns for 1X mode

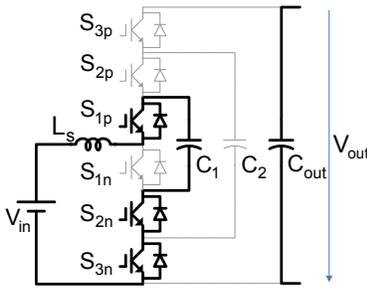


(a)

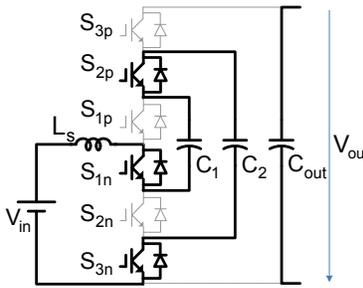


(b)

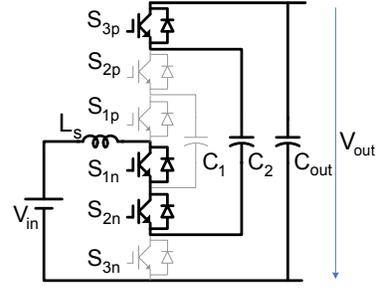
Fig 3. Switching patterns for 2X mode: (a) Switching state I. (b) Switching state II.



(a)



(b)



(c)

Fig 4. Switching patterns for 3X mode. (a) Switching state I. (b) Switching state II. (c) Switching state III.

III. CAPACITOR PARAMETER DESIGN

The converter is desired to output 30 kW continuous power and 55 kW peak power. For C_2 and C_{out} , there are less output voltage ripples in 2X mode than in 3X mode, so the latter is picked for capacitance calculation. Ignoring the power loss for simplification, the average output current I_o equals $I_{in}/3$ in 3X mode. The converter output voltage ripple is constrained to 5%, and the ripples for the other capacitors are 15% with respect to the input voltage. In the practical system, the dc-dc converter output shares the dc link capacitor C_{dc} with the inverter. C_{out} acts as temporary energy storage to decouple the parasitic inductance between the converter output C_{out} and the inverter dc bus capacitor C_{dc} . So the equivalent output capacitance for the converter is C_{out} plus C_{dc} . The minimum capacitance requirement is calculated as:

$$C_1 = \frac{\int_0^{\frac{1}{3}T_s} i_{in} dt}{V_{in} \times 15\%} = \frac{\frac{1}{3}T_s \times I_{in}}{V_{in} \times 15\%} \quad (1)$$

$$C_2 = \frac{\int_0^{\frac{1}{3}T_s} i_{in} dt}{2V_{in} \times 15\%} = \frac{\frac{1}{3}T_s \times I_{in}}{2V_{in} \times 15\%} \quad (2)$$

$$C_{out} + C_{dc} = \frac{\int_0^{\frac{2}{3}T_s} i_o dt}{3V_{in} \times 5\%} = \frac{\frac{2}{3}T_s \times I_{in} / 3}{3V_{in} \times 5\%} \quad (3)$$

The required current capacity is determined by comparing the RMS current in both 2X and 3X modes.

A. 2X mode

Since the RMS of ripple current is relatively small, the RMS current going through the capacitor C_1 in 2X mode can be simplified as:

$$I_{c1(RMS)} = \sqrt{\frac{(I_{in})^2 \times \frac{T_s}{2} \times 2}{T_s}} = I_{in} \quad (4)$$

In the 2X mode, the capacitors C_2 , C_{out} and the inverter dc link capacitor are paralleled to supply the load with the output current, which equals $I_{in}/2$. Only in half the switching cycle, they all got refueled by half the input current. So the RMS current through these three capacitors in 2X mode is:

$$(I_{c2} + I_{c_{out}} + I_{c_{dc}})_{(RMS)} = \sqrt{\frac{(I_{in}/2)^2 \times \frac{T_s}{2} \times 2}{T_s}} = I_{in} / 2 \quad (5)$$

B. 3X mode

Similarly, the capacitor C_1 (as well as C_2) is charged in 1/3 switching cycle, discharged in another 1/3 cycle and disconnected in the rest cycle. Their RMS current can be expressed as:

$$I_{c1(RMS)} = I_{c2(RMS)} = \sqrt{\frac{I_{in}^2 \times \frac{T_s}{3} \times 2}{T_s}} = \sqrt{\frac{2}{3}} I_{in} \quad (6)$$

Based on the discharge current of I_o in 2/3 cycle and the charge current of $(I_{in} - I_o)$ in the rest cycle, the RMS current through C_{out} and C_{dc} is:

$$(I_{Cout} + I_{Cdc})_{(RMS)} = \sqrt{\frac{(I_{in}/3)^2 \times \frac{2T_s}{3} + (2I_{in}/3)^2 \times \frac{T_s}{3}}{T_s}} = \frac{\sqrt{2}}{3} I_{in} \quad (7)$$

IV. THE MINIMUM REQUIREMENT AND EFFECT OF THE PARASITIC INDUCTANCE

Provided sufficient capacitance, the voltage differences in the steady state are small, so the current through the switches is relatively small. However, during the transition when the output voltage ratio changes between V_{in} and $2V_{in}$, or between $2V_{in}$ and $3V_{in}$, the large voltage differences can lead to high transient current through the devices. Therefore, a variable PWM duty ratio and high switching frequency control is proposed in [1] to limit the inrush current. Besides, there is some parasitic inductance in the battery and in the cable connecting the converter to the battery. The parasitic inductance in the circuit plays an important role in smoothing the transition. To estimate the minimum parasitic inductance requirement at given maximum switching frequency, assume the voltage across C_1 and C_2 are constant in each short switching period T_{tr} . The transient switching frequency f_{tr} is designed as 20 kHz in this converter. The maximum allowable current variation rate is set as 80% of the current rating of the switching device. Based on the detail transient PWM control methods in [1], consider two worst cases of highest transient currents among all the transition modes:

A. $V_{out}: 1V_{in} \rightarrow 2V_{in}$

During the transition, the capacitors C_2 and C_{out} are charged up to $2V_{in}$ gradually from the initial voltage $1V_{in}$. Assume that the aforementioned inductor current is continuous and define the duty ratio D as the duration when C_{out} is charged by the addition of C_1 and the battery over the entire switching period T_s . There are two active switching states (DT_{tr}) and one freewheeling state $((1/2-D)T_{tr})$ between them as described in [1]. In the active switching states, the switching patterns are the same as those in the 2X steady state as shown in Figs. 3(a) and (b), except that the duty ratio D increases gradually. The input current variation can be calculated according to the active switching states II, the switching pattern of which is illustrated in Fig. 3(b):

$$\begin{aligned} \Delta i_{Ls} &= \frac{V_{Ls} \times DT_{tr}}{L_s} \\ &= \frac{(V_{in} + V_{c1} - V_o)DT_{tr}}{L_s} \\ &= \frac{V_{in}(1-2D)DT_{tr}}{L_s(1-D)} \leq I_{rated} \times 80\% \end{aligned} \quad (8)$$

where $V_o = V_{in}/(1-D)$, (Duty ratio D : from 0 to 1/2)
 $\Delta i_{Ls \max}$ occurs at $D=0.29$ in the above function.

B. $V_{out}: 2V_{in} \rightarrow 3V_{in}$

In the same way, the current variation in the 2X to 3X transition is computed using the active switching state III, the switching pattern of which is shown in Fig. 4(c)

$$\Delta i_{Ls} = \frac{(V_{in} + V_{c2} - V_o)DT_{tr}}{L_s} = \frac{V_{in}(1-3D)DT_{tr}}{L_s(2/3-D)} \leq I_{rated} \times 80\% \quad (9)$$

Where, $V_o = V_{in}/(2/3-D)$, (D: from 1/6 to 1/3)

$\Delta i_{Ls \max}$ occurs at $D=0.2$ in the above function.

In comparison of the two cases, the minimum inductance requirement can be got based on the input voltage and the switching frequency. It is 4.1 μH at 230 V and 20 kHz in this system. In practice, a lower parasitic inductance than the calculation is tolerated because the voltages of the capacitors C_1 and C_2 are observed a little drop given the transient inrush current and finite capacitance. The requirement of parasitic inductance can be further reduced by increasing the switching frequency in the transition. The equivalent series inductance (ESL) of the battery varies with the number of cells in series. A rule of thumb for the parasitic inductance is 1 μH per 1 meter conductor. Plus, in some HEVs, the battery is placed about 2~3 meters away from the converter. So the total inductance would be enough; otherwise, a small air core inductor can be added when parasitic inductance is not enough for the large voltage difference and the adopted devices can not achieve sufficiently high switching frequency. In fact, the presence of the parasitic inductance significantly reduces the capacitance requirement. It restricts the inrush current otherwise faced in a pure RC charge/discharge circuit even in steady state. A smoother input current results in less conduction loss.

V. CIRCUIT MODELING AND POWER LOSS ANALYSIS

Unlike the traditional converter, the multilevel dc-dc converter has unique efficiency characteristics. For instance, when the current is unidirectional in each switching state, the switching power loss is lower at the lower switching frequency; however, the capacitor charging/discharging power loss becomes higher. In other words, a higher switching frequency may not necessarily lead to higher system power loss. Likewise, while the conduction loss drops with larger stray inductance, the switching loss rises with the higher switching current. Thus, it is very necessary to theoretically investigate the efficiency profiles associated with the operation frequency and circuit parameters.

A few assumptions are made for the power loss analysis:

1) To simplify the calculation, the saturation voltage V_{on} of the IGBT and diode in the series loop is modeled as constant voltage source, though there is some variation resulted from the conducting current.

2) The load current is assumed as constant dc. It is applicable since the output voltage has very small ripples.

3) The dead time is ignored when modeling the input current and capacitor voltage.

4) The ESR variation with respect to current and frequency is ignored.

The switching loss is directly proportional to the switching current given a fixed converter input voltage. The conduction loss here refers to the loss dissipated on the semiconductor devices (IGBTs with diodes) and on the equivalent series resistance (ESR) in the charging/discharging loop. The latter is sometimes termed as the charge/discharge loss, though it is essentially consumed by the ESR of the semiconductor devices. It is discussed in [5] that the charging loss is irrelative to the ESR when the switching period and the RC time constant satisfy $T_s \gg RC$. However, it differs when the stray inductance is not negligible.

The nX steady state operation modes can be modeled as N equivalent circuits. Take the 3X mode for instance. The equivalent circuits are illustrated in Fig 5. In Fig 5 (a), when C_1 is charged by the battery, the input current can be solved as:

$$i = e^{-\alpha_1 t} \left[I(0) \cos \omega_1 t + (C_1 \Delta V_1 \frac{\alpha_1^2 + \omega_1^2}{\omega_1} - \frac{\alpha_1 I(0)}{\omega_1}) \sin \omega_1 t \right] \quad (10)$$

$(t = 0 \sim \frac{T_s}{3})$

where $I(0)$ is the initial input current through the lumped ESL in the charging loop. The initial voltage difference is:

$$\Delta V_1 = (V_{in} - V_{on}) - V_{c1}(0) \quad (11)$$

The input current in the second state when charging C_2 as shown in Fig 5 (b) is:

$$i = e^{-\alpha_2 (t - \frac{T_s}{3})} \left[I(\frac{T_s}{3}) \cos \omega_2 (t - \frac{T_s}{3}) + (C_{loop2} \Delta V_2 \frac{\alpha_2^2 + \omega_2^2}{\omega_2} - \frac{\alpha_2 \times I(\frac{T_s}{3})}{\omega_2}) \sin \omega_2 (t - \frac{T_s}{3}) \right] \quad (12)$$

$(t = \frac{T_s}{3} \sim \frac{2T_s}{3})$

where,

$$\Delta V_2 = (V_{in} - V_{on}) + V_{c1}(\frac{T_s}{3}) - V_{c2}(\frac{T_s}{3}) \quad (13)$$

$$C_{loop2} = \frac{C_1 \times C_2}{C_1 + C_2} \quad (14)$$

In the first two states, it is easy to estimate the conduction loss consumed in the output loop when the output capacitor supports the load. For charging the output capacitor as shown in Fig 5(c), the current can be expressed as a function of both initial input current and load current:

$$i = e^{-\alpha_3 (t - \frac{2T_s}{3})} \left\{ \left(I(\frac{2T_s}{3}) - \frac{C_2 I_{load}}{C_2 + C_{out}} \right) \cos \omega_3 (t - \frac{2T_s}{3}) + [C_{loop3} (\Delta V_3 - K) (\alpha_3^2 + \omega_3^2) - \alpha_3 \left(I(\frac{2T_s}{3}) - \frac{C_2 I_{load}}{C_2 + C_{out}} \right)] \frac{1}{\omega_3} \times \sin \omega_3 (t - \frac{2T_s}{3}) \right\} + \frac{C_2}{C_{out} + C_2} I_{load}$$

$(t = \frac{2T_s}{3} \sim T_s)$ (15)

where,

$$\Delta V_3 = (V_{in} - V_{on}) + V_{c2}(\frac{2T_s}{3}) - V_{c_{out}}(\frac{2T_s}{3}) \quad (16)$$

$$K = R_{load} I_{load} \frac{C_2}{C_{out} + C_2} \quad (17)$$

$$C_{loop3} = \frac{C_{out} \times C_2}{C_{out} + C_2} \quad (18)$$

As can be found, when the load current is zero, the third switching state complies with a generalized model extracted from the preceding two states:

$$i = e^{-\alpha_i (t - t_0)} \left[I(t_0) \cos \omega_i (t - t_0) + (C_{loopi} \Delta V_i \frac{\alpha_i^2 + \omega_i^2}{\omega_i} - \frac{\alpha_i \times I(t_0)}{\omega_i}) \sin \omega_i (t - t_0) \right] \quad (19)$$

$$(t = t_0 \sim t_0 + \frac{T_s}{3})$$

$$\alpha_i = R_{si} / 2L_s \quad (20)$$

$$\omega_i = \sqrt{\frac{1}{L_s C_{loopi}} - (\frac{R_{si}}{2L_s})^2} \quad (i = 1, 2, 3) \quad (21)$$

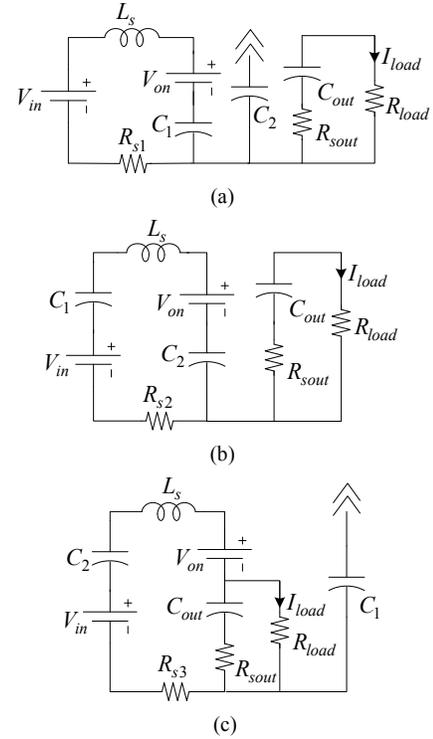


Fig 5. Equivalent circuit for the 3X mode: (a) Switching state I. (b) Switching state II. (c) Switching state III

The power loss can be calculated numerically based on the above circuit modeling. In addition, the generalized model is applicable to some other multilevel dc-dc converters. The resonance frequency in each switching state can be found from the equivalent loop capacitance and the estimated ESL. Then the switching device can be switched at zero current or very low current. Consequently, the converter may be able to operate at a very high switching frequency.

VI. CALCULATION AND EXPERIMENTAL RESULTS

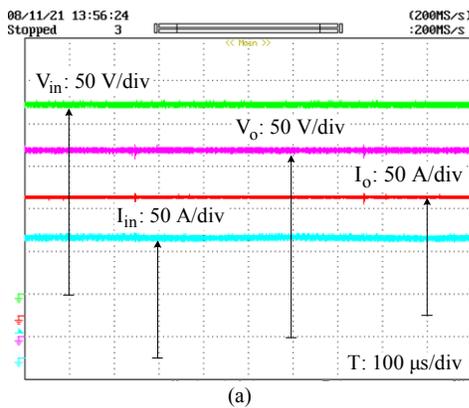
The prototype of the 55 kW dc-dc converter is shown in Fig 6. Its dimension is $27.2 \times 24.4 \times 8.8$ cm³ and its weight is around 5.6 kg. The switching devices used were integrated in

an IPM module PM600CLA600. The capacitors C_1 and C_2 were 500 μF film capacitors FFV34H0506K and 240 μF film capacitors FFV36A0206K respectively. The output capacitor is 40 μF FFV36A0206K. In the steady state operation experiment, the converter is loaded with another dc-dc converter as an electronic load. The dc bus capacitor C_{dc} between these two converters are 820 μF . The converter operates at 8 kHz in 3X mode and 12 kHz in 2X mode in steady state and it worked at 20 kHz during the transition. The complex logic for the duty ratio and frequency control in steady state and transient operation was implemented by one CPLD XC95288XL.

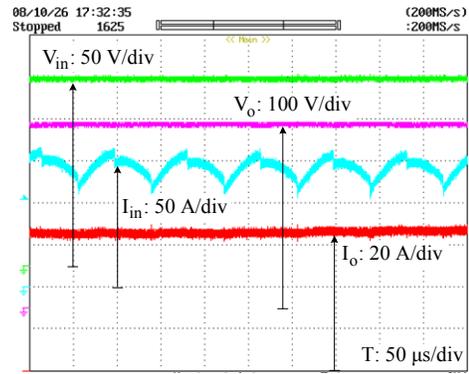


Fig 6. The 55 kW dc-dc converter prototype

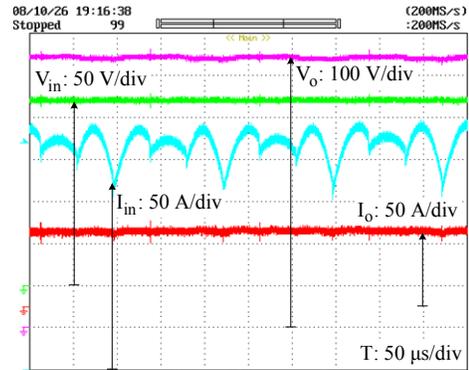
Fig 7 shows some waveforms in the steady state and operation. Fig 7 (a) and (b) are the input/output voltage and current waveforms in 2X and 1X modes at their 30 kW peak power. Fig 7(c) shows the corresponding waveforms in 3X mode at the 55 kW peak power. The output/input voltage ratio is a little lower than nX because of the device voltage stress and dead time as discussed in [6]. Fig 8 shows the converter performance during voltage ratio change transition, in which the converter is loaded with a 30 Ω resistive load. In all cases the transient current is well limited within the rated current. The minimized inrush current and the fast transition make the transient temperature rise of the components almost unobservable. Hence, the transient PWM and frequency control prolongs the lifetime and enhances reliability of the converter.



(a)

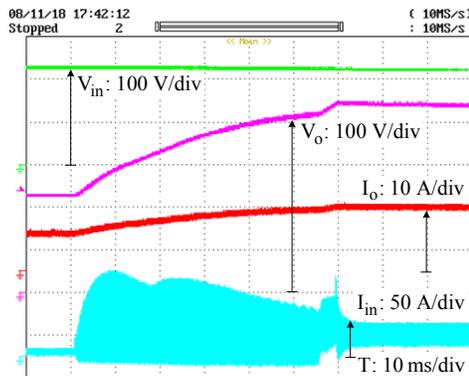


(b)

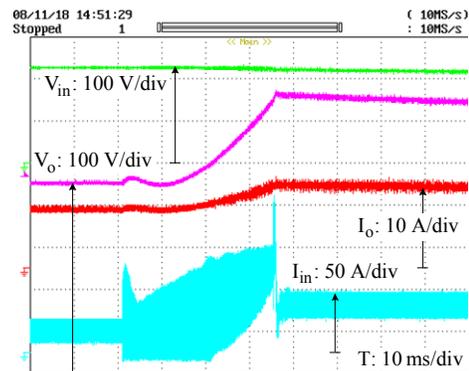


(c)

Fig 7. The experimental waveforms in steady state operation: (a) 1X boost mode at 30 kW output. (b) 2X boost mode at 30 kW output. (c) 3X boost mode at 55 kW output.



(a)



(b)

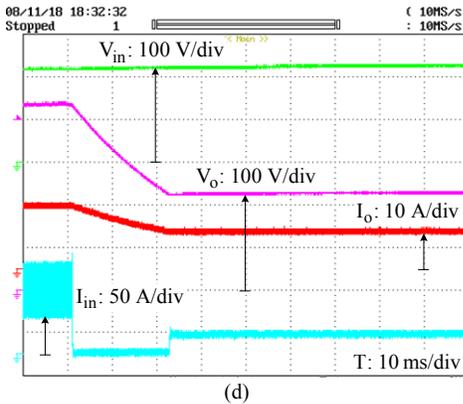
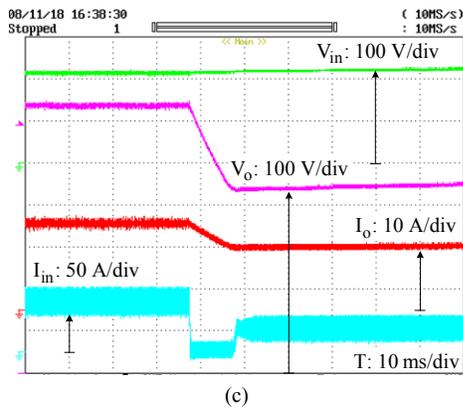


Fig 8. The experimental waveforms of the nX mode transition: (a) Transition from 1X to 2X. (b) Transition from 2X to 3X. (c) Transition from 3X to 2X. (d) Transition from 2X to 1X.

The calculated power loss breakdown is plotted in Fig 9 using the proposed circuit model. The input power is 30 kW and the input voltage is 230 V in the 3X mode. The ESL is simulated by an air-core inductor wound by litz wire in the experiment. The measured ESL from the inductor and the cable is approximately 3.6 μH . The total loss includes the conduction loss, switching loss and the gate drive power loss. As can be seen, the conduction loss is the dominant power loss when the switching frequency is low. It goes down with the increment of the switching frequency and gradually gets stable as the switching frequency reaches 5 kHz. As the switching frequency keeps rising, the switching loss becomes dominant at very high frequency. Fig 10 compares the calculated and measured efficiency with respect to different frequency. The estimation errors stems from the modeling assumptions, parasitic parameters, and the calculated initial condition in each switching state. The optimal switching frequency is related to the capacitance and parasitic inductance in the designed circuit. It can be seen from the experimental results that it falls in the range of 4–6 kHz for this prototype. However, the input current ripple is considerably larger at lower frequency. So the operation frequency should also be selected taking into account the current ripple.

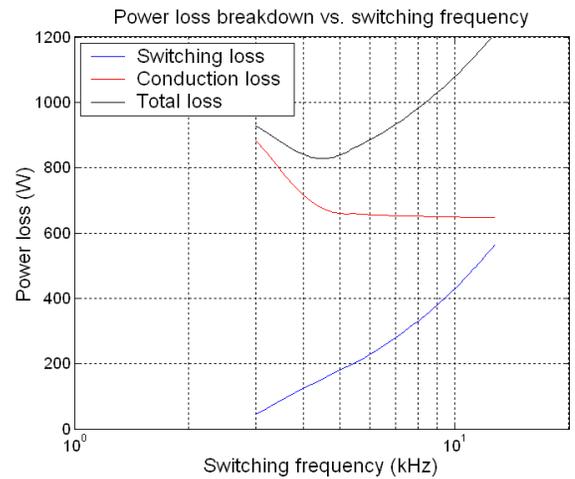


Fig 9. Calculated power loss breakdown vs. switching frequency at 30 kW in 3X mode.

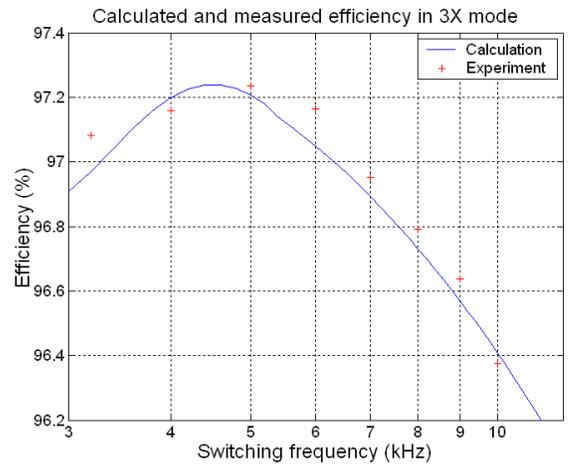


Fig 10. Calculated and measured efficiency with different switching frequency input power in 3X mode

VII. CONCLUSION

The analysis and design of a 55 kW 3X dc-dc converter are presented. The converter implemented three variable output/input voltage ratios with the minimum component count and the lowest voltage stress across the switching devices. The existence of parasitic inductance, along with the transient PWM and frequency control, limits the transient current. The parasitic inductance also helps reduce the conduction loss and the capacitance requirement. Thereby the compact size and light weight are achieved. The circuit model is built to evaluate the efficiency profiles related to the operation frequency and circuit parameters. The experimental results in steady state and transient operation validate the principle and design rules. The efficiency testing results verifies the circuit modeling and power loss analysis.

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