4H- and 6H- Silicon Carbide in Power MOSFET Design

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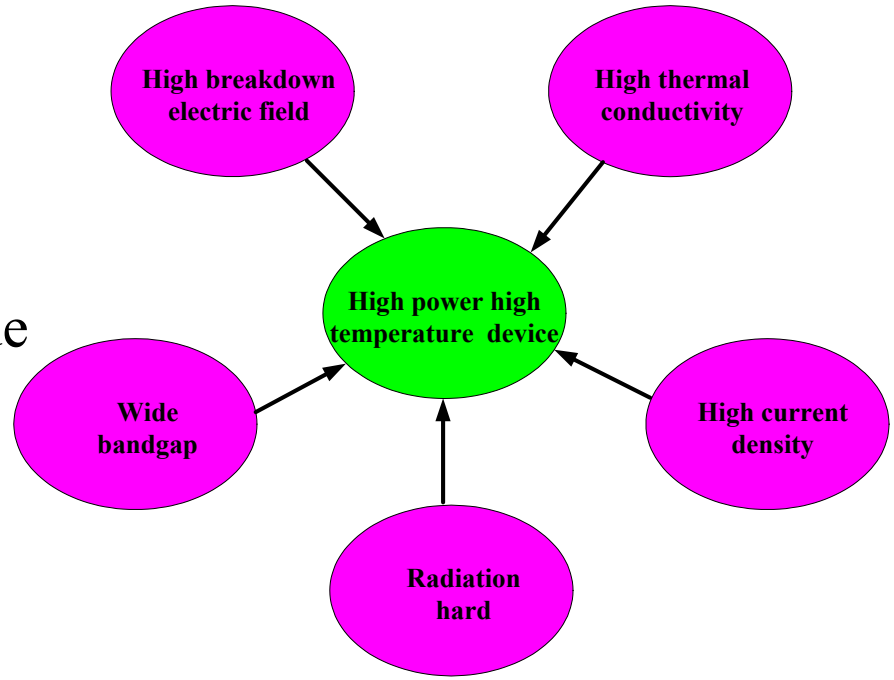
April 7, 2004

Agenda

- Overview of silicon carbide
- Comparison of Si and SiC MOSFET
- Vertical power MOSFET model
- A proposed device structure
- MOSFET temperature model
- Results
- Conclusions

Why SiC?

- Large band gap and high melting point enable high temperature device operations
- Large break down field enable the fabrication of smaller and compact high voltage power devices
- Requires smaller cooling system due to High thermal conductivity
- Extremely radiation hard
- Shows excellent reverse recovery characteristics
- Excellent mechanical properties make SiC ideal for MEMS applications



Why Not Silicon?

- Smaller band gap and low melting point enable medium range of temperature device operations
- Due to lower thermal conductivity, requires larger cooling system
- Smaller electric breakdown field limit the device size and voltage
- Shows high leakage current

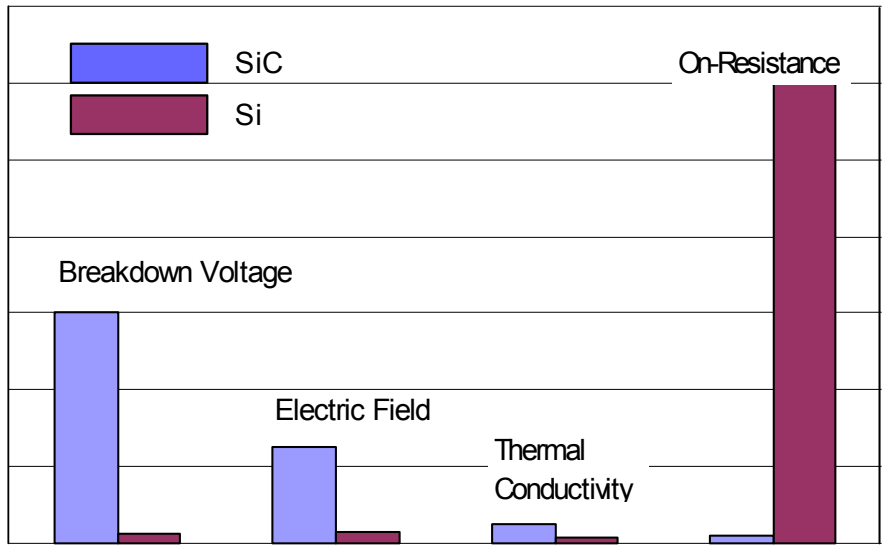


Fig: Comparison of Si and SiC properties

Physical & Electrical Properties of SiC

Properties	Si	6H-SiC	4H-SiC
Bandgap(eV)	1.11	3.0	3.26
Dielectric const.	11.8	9.7	10
Breakdown field (V/cm)	$6x10^5$	$3.5x10^6$	$3.5x10^6$
Saturated drift velocity (cm/sec)	$1x10^7$	$2x10^7$	$2x10^7$
Electron mobility (in bulk) (cm^2/V-sec)	1350	370	720^a 650^c
Hole mobility (in bulk) (cm^2/V-sec)	450	95	120
Thermal conductivity (W/cm-^{o}K)	1.5	4.9	4.9
Melting point (^{o}C)	1420	2830	2830
Hardness (kg/mm^2)	1000	-	2310

a=along a-axis, c=along c-axis

Comparison of Wide Bandgap Materials

- SiC is unique because of its native oxide is SiO_2 , therefore easy to fabricate field effect device
- Though Diamond has the best material properties, it is not suitable for conventional electronic device fabrication.
- It is very difficult to form oxide in GaN, it is suitable for opto-electronics devices

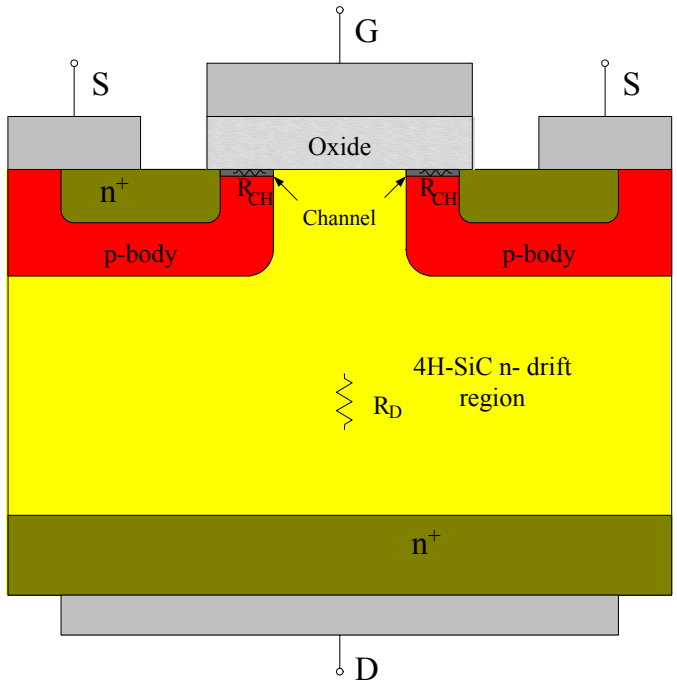
Properties	4H-SiC	GaN	Diamond
Lattice constant (Å)	3.073 a 10.053 c	4.51	3.57
Thermal expansion ($x10^{-6}$) ^oC	-	5.6	0.08
Density (g/cm^3)	-	-	3.51
Melting point (^oC)	2830	-	4000
Bandgap (eV)	3.26	3.45	5.45
Saturated electron velocity ($x10^7$ cm/s)	2.0	2.2	2.7
Mobility (cm^2/V-s) Electron Hole	 780 50	 1250 250	 2200 1600
Breakdown Voltage ($x10^5$ V/cm)	30	>50	100
Dielectric constant	9.66	11	5.5
Resistivity (Ω-cm)	-	10^{10}	10^{13}
Thermal conductivity (W/cm.K)	4.9	1.3	20
Hardness (kg/mm^2)	2130 a	-	10000

Power MOSFET design considerations

- Specific on-resistance has to be kept as low as possible
- Breakdown voltage has to increase as design requirements
- Low specific on-resistance reduces power losses and increases efficiency
- Specific on-resistance increases with the increase of the breakdown voltage
- A design trade-off has to be made between the specific on-resistance and the voltage rating

$$V_{Br} = \frac{\varepsilon . E_c^2}{2.q.N_d}$$

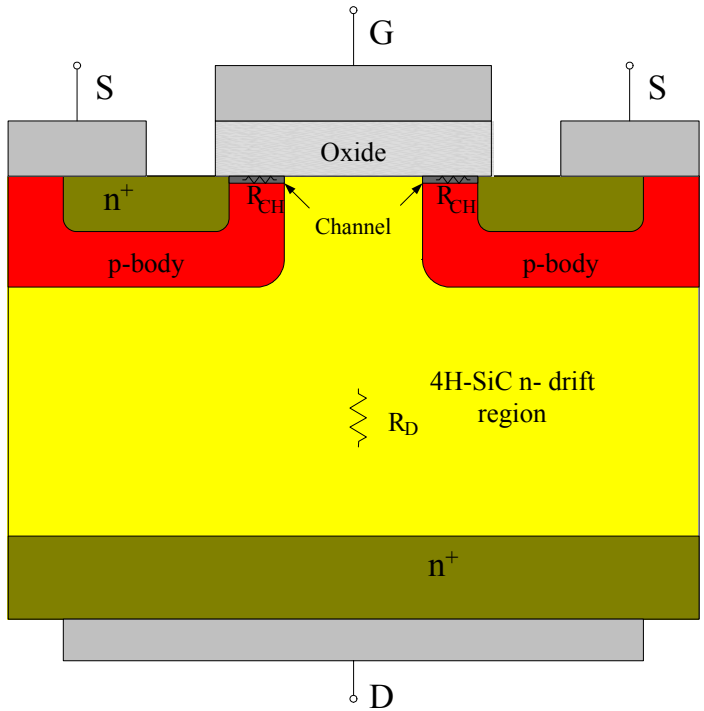
$$R_{on-sp} = \frac{4V_{Br}^2}{\varepsilon . E_c^3 . \mu_n}$$



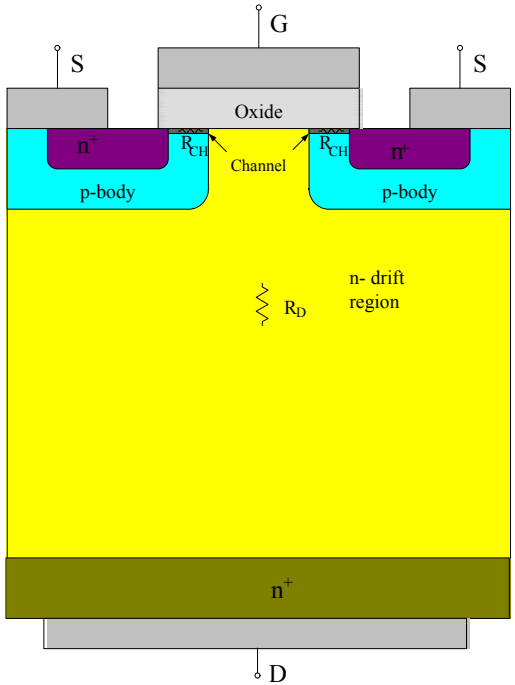
Power MOSFET design considerations (contd.)

- SiC devices demonstrate one-hundredth times lower specific on-resistance and ten times higher breakdown voltage than the silicon devices for the same device dimensions
- Drift region thickness is ten times lower in silicon carbide compared to silicon device for same voltage rating
- Mass and volume of heat sink is 15-20% smaller in case of silicon carbide

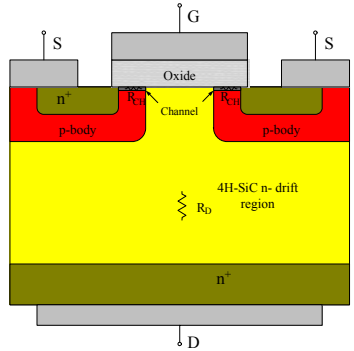
$$W_{drift} \approx \frac{2V_{Br}}{E_c}$$



Comparison of Si & SiC Power MOSFETs



Si-MOSFET



SiC-MOSFET & Heat sink

Heat sink for Si devices

	Silicon	Silicon-Carbide
On-Resistance	100 m.Ω/cm^2	1 m.Ω/cm^2
Drift Region Thickness	100 μm	10 μm
Operating Temperature	150ºC	500ºC
Heat Sink Volume & Mass	100%	80-85%
Device size	100%	50%

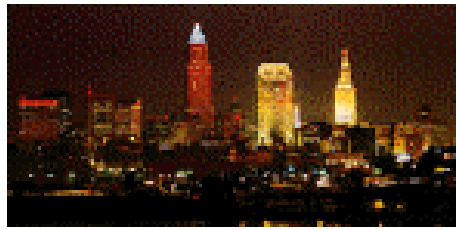
Analog VLSI and Devices Laboratory

Future power electronics w*ill be* SiC !

Today's Technology	Advantages of Silicon Carbide	Payoff
Large energy losses	Reduce loss by 10x	Large improvement in efficiency
Limited voltage and power level	Increase power 10^3x	Simplify use in electrical grid
Low operating temperature (< 150ºC)	Increase range to 500ºC	New applications; eliminate massive heat sinks
Large heat sinks & filters	Reduce size/weight by 3x	Lightweight, compact systems

Potential applications of SiC electronics

Automotive



Utility

Space-craft

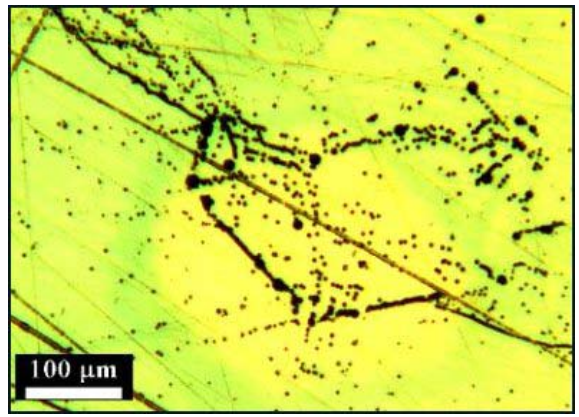
Mining

Nuclear power

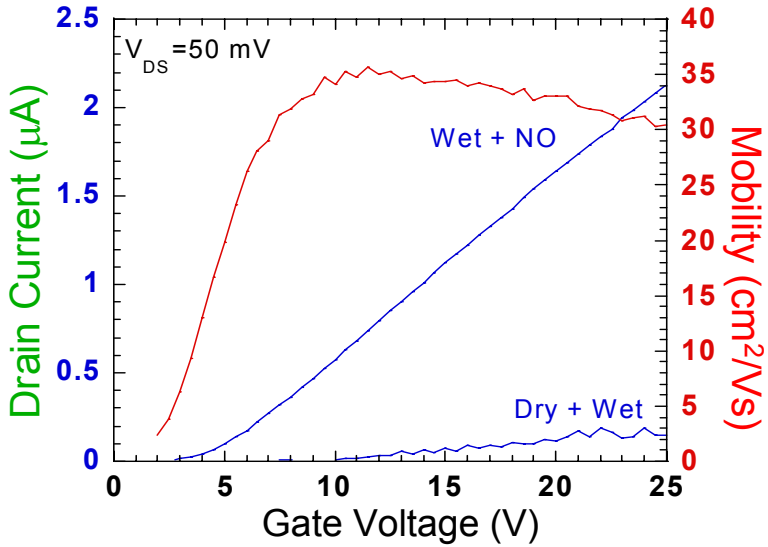
Aircraft

Limitations of SiC

- Higher defect densities due to micropipes and dislocations in the crystal orientations
- Material processing and device fabrication require high temperature process (1000-1700°C)
- Device quality SiC wafer is very costly
- High interface state densities
- Low inversion layer mobility
- Power MOSFETs in SiC are not commercially available

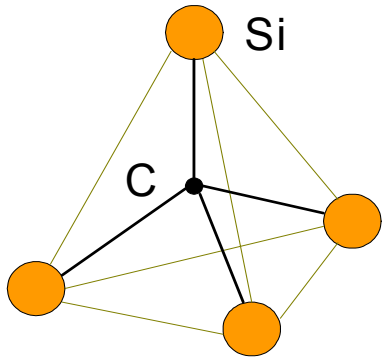


Micropipes defects

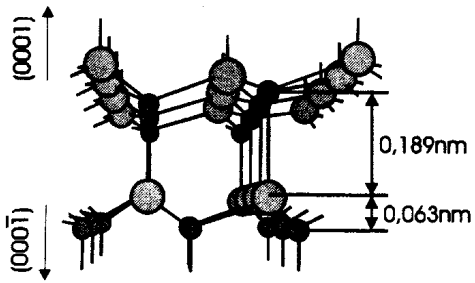


Atomic structure

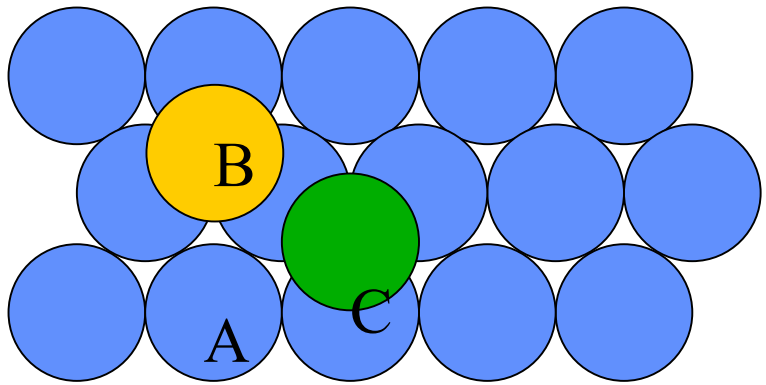
- SiC are made by arrangement of covalently bonded tetrahedral Si and C atoms
- 50% carbon atoms and 50 % silicon atoms
- SiC has more than 100 known polytypes
- Polytype refers to a family of material which has common stoichiometric



Tetragonal bonding between carbon and silicon atoms



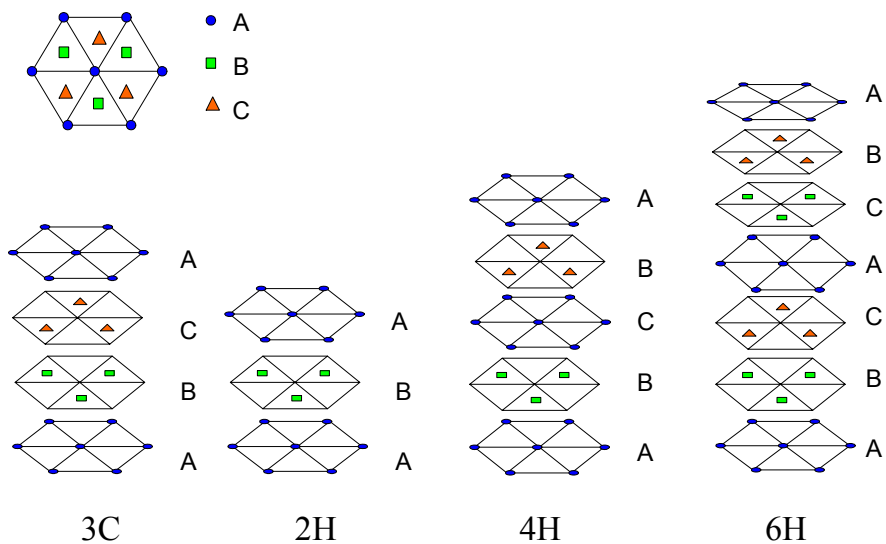
Locations of Si (light) and C atoms (dark) in SiC



Site locations for C atoms in (0001) plan

Atomic structure (contd.)

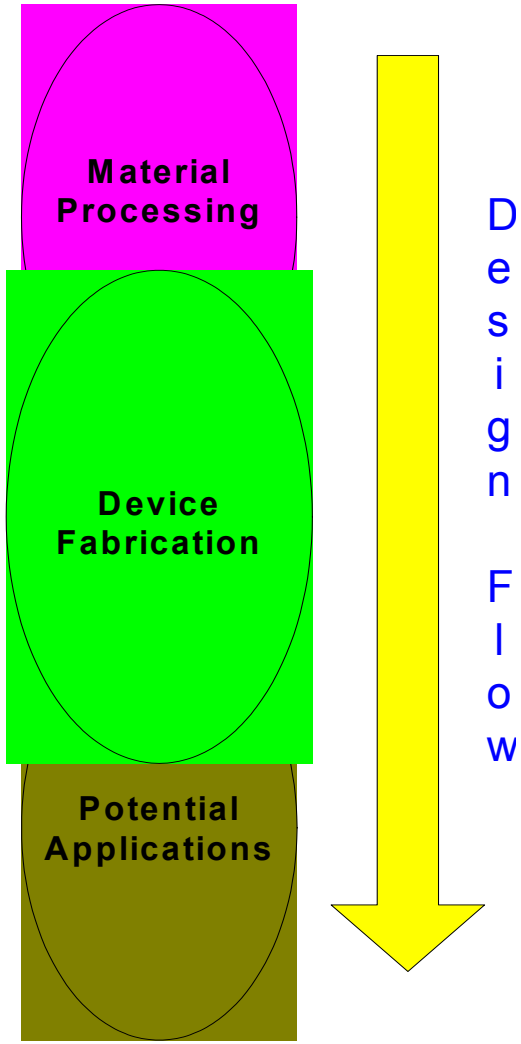
- The arrangement of SiC bi-layers is same in 2-D but differs in by stacking sequence in 3-D
- 3 commonly used polytypes:
  - **3C-SiC**: Cubic structure, Zinc-blend, ABCABC….
  - **4H-SiC**: Hexagonal close packed, ABCBABCB…
  - **6H-SiC**: Hexagonal close packed, ABCACBABCAC…



Stacking sequences for four different SiC polytypes

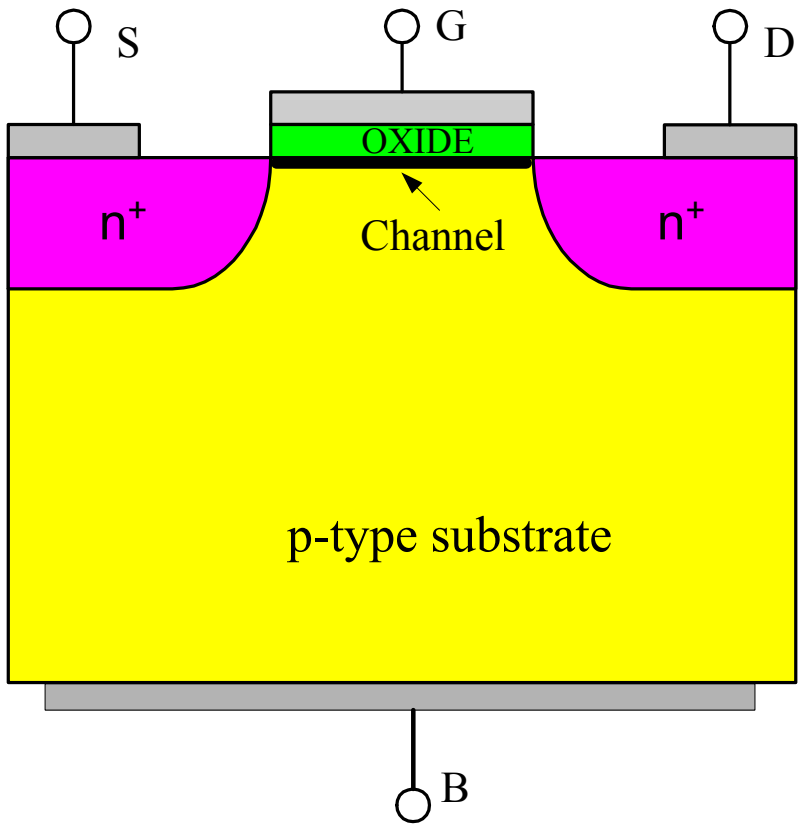
Device fabrication:the pathway to success

- Material Processing
  - Epitaxial Growth
  - Dopant Activation
  - Interface Engineering
- Device Fabrication
- Applications
  - Circuit Design
  - System Integration



Drawback of lateral structure for power application

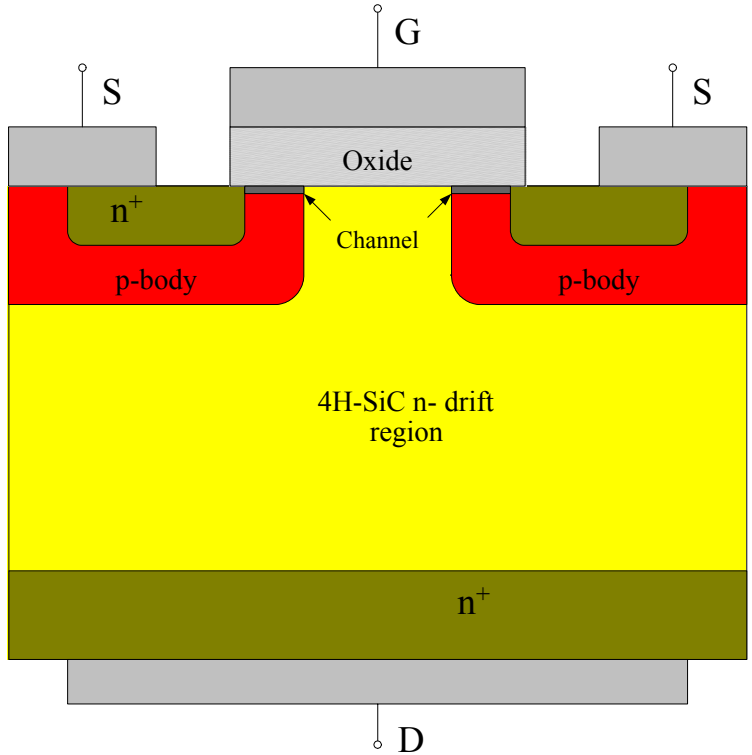
- Power MOSFETs have to handle high voltages and high currents
- Lateral structure is not suitable for power application
- Current flows laterally through the channel below the gate oxide
- No drift region available to hold large voltage
- No option is available for forward blocking capability
- Required large W to get large W/L ratio to increase the current capacity



Lateral MOSFET Structure

Vertical MOSFET for high voltage and high power

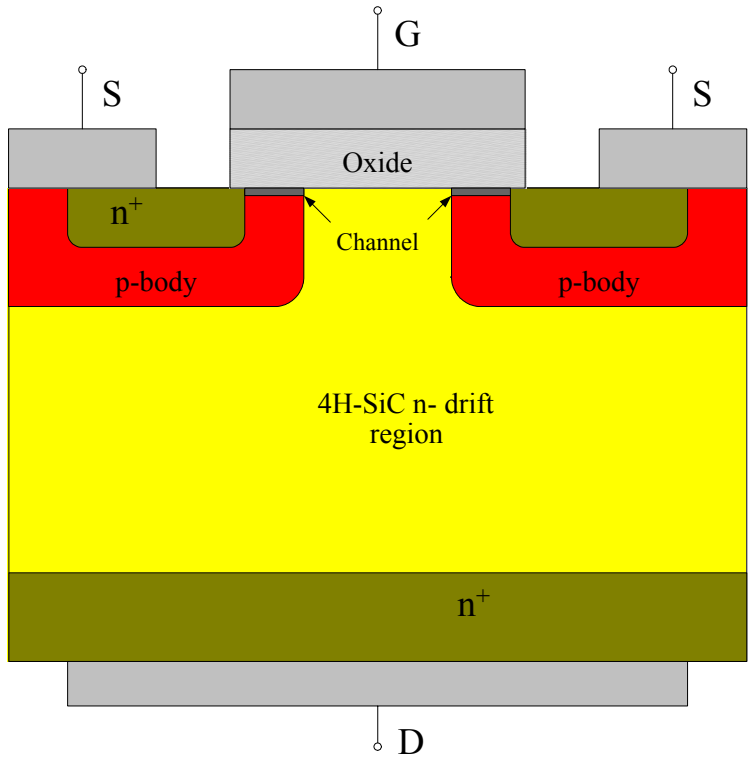
- Source and drain are made on top and bottom of the wafer respectively
- Current flows vertically from drain to source through drift and channel region
- Drift region supports most of the applied drain voltage
- Channel region provides the current gain
- p-n junction between p-body and n-drift region provides forward blocking capability



Vertical MOSFET Structure

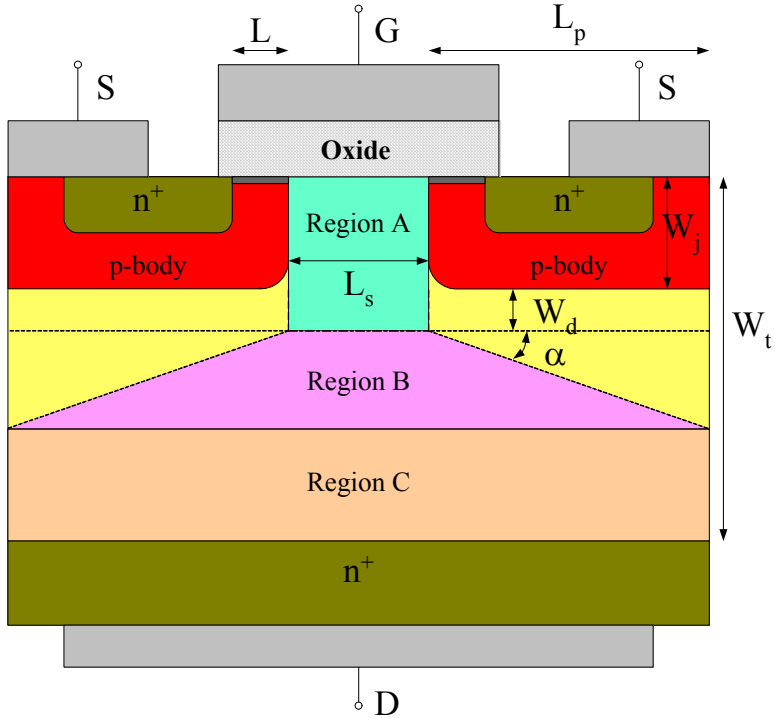
Vertical MOSFET for high voltage and high power

- P-bodies can be made either round or hexagonal shaped to get large W
- Length L can be made very small
- For same die area, W/L ratio is higher compared to lateral MOSFET
- Drift region doping can be adjusted to get high breakdown voltage with low on-resistance
- 4H-SiC is suitable for vertical structure due to higher mobility in vertical direction



Modeling of vertical DIMOS structure

- For analysis the structure is divided into two regions: (i) the channel region, and (ii) the drift region
- Channel forms in the *p*-body below the gate oxide where gate voltage controls the channel currents
- Drain current is divided into two channel currents in two *p*-bodies on both sides
- Drift region begins at the drain and ends at the channel near the oxide layer

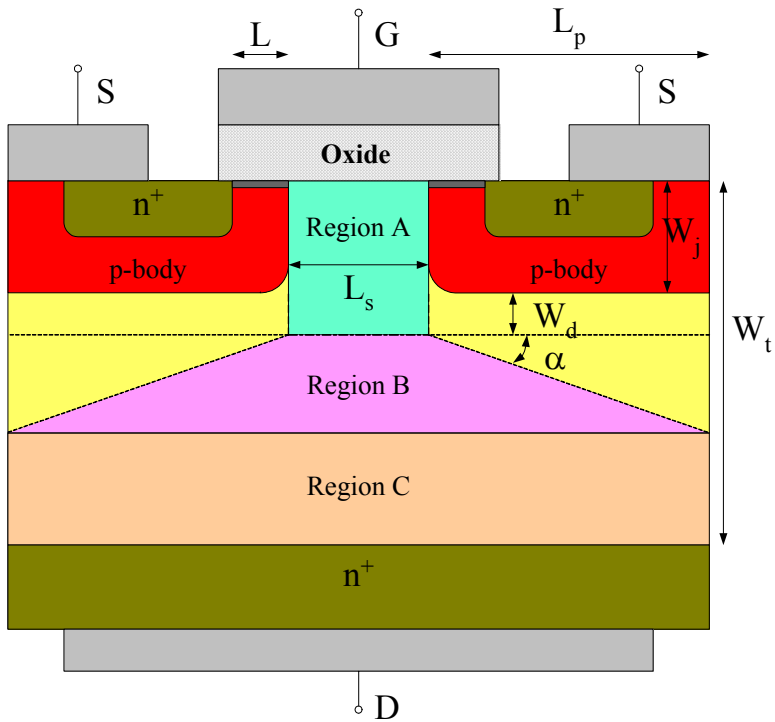


Cross-section details of VDIMOS structure used in the model

M Hasanuzzaman, S.K. Islam, L. Tolbert, and Burak Ozpineci,"Model Simulation and Verification of a Vertical Double Implanted (DIMOS) Transistor in 4H-SiC", *proceedings of the IASTED international conference*, February 24-26, 2003, Palm Spring, CA.

Modeling of vertical DIMOS structure (contd.)

- Drift region is divided into three regions
- Region A: an accumulation region between the *p*-bodies with small cross-section
- Region B: a drift region with varying cross-section
- Region C: a drift region with constant cross-section
- Current voltage relations for channel region and three drift regions have been developed



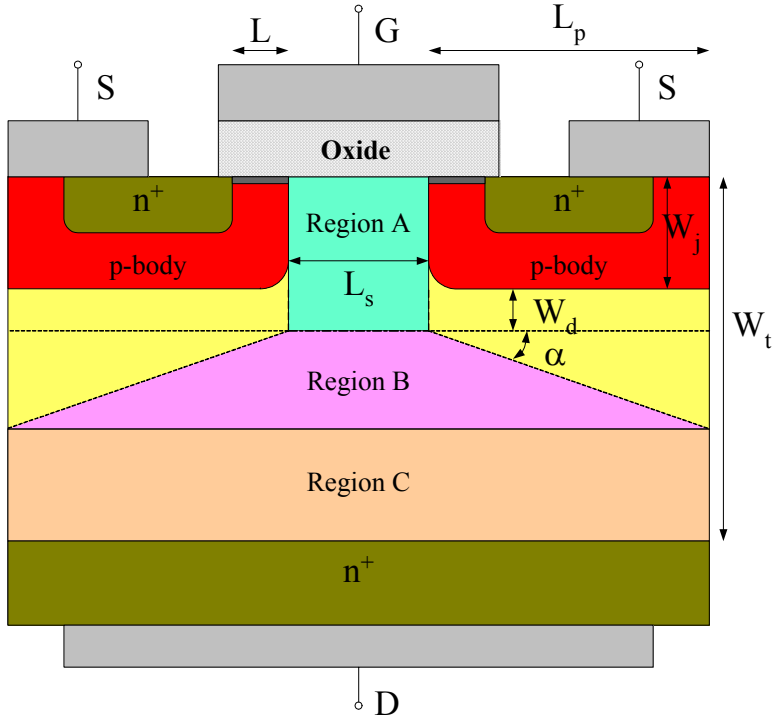
Modeling of vertical DIMOS structure (contd.)

Channel Current

$$I_{ch} = \frac{W\mu_{neff}}{2L\left[1+(\mu_{neff}/2v_{sat}L)V_{ch}\right]}V_{ch}\left[2C_{ox}(V_{GS}-V_T)-(C_{ox}+C_{do})V_{ch}\right]$$

- Where $C_{ox}+C_{do}$ is the total capacitance of the oxide and the body depletion
- Current increases with the decrease of channel length and increase in channel width and voltage
- Gate voltage controls the channel current
- At saturation, channel current is given by,

$$I_{ch(sat)} = Wv_{sat}C_{ox}(V_{GS}-V_T)$$



Modeling of vertical DIMOS structure (contd.)

Drift Region Voltage

Total drift region voltage is the sum of the voltages of the three regions,

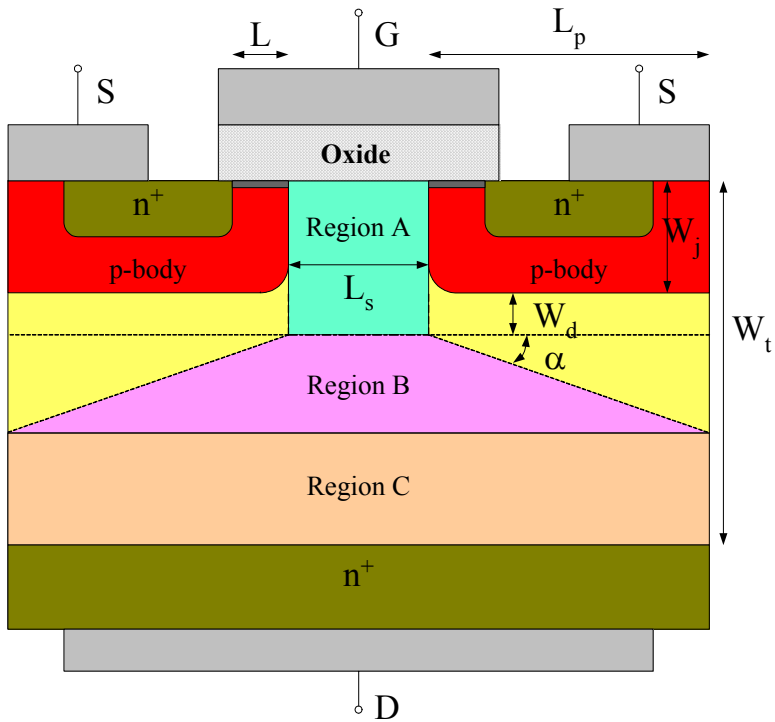
$$V_{drift} = V_A + V_B + V_C$$

Where,

$$V_A = \int_0^{W_j+W_d} E_y\,dy = \frac{I_D(W_j + W_d)}{W(L_s q N_d \mu_n) - I_D / E_C}$$

$$V_B = \frac{I_D}{WqN_d\mu_n \cot\alpha} \log\left[\frac{WqN_d\mu_n(L_s + 2L_P) - I_D/E_C}{WqN_d L_s \mu_n - I_D/E_C}\right]$$

$$V_C = \frac{I_D\left(W_t - W_j - W_d - L_P \tan\alpha\right)}{WqN_d\mu_n(L_S + 2L_P) - I_D/E_c}$$



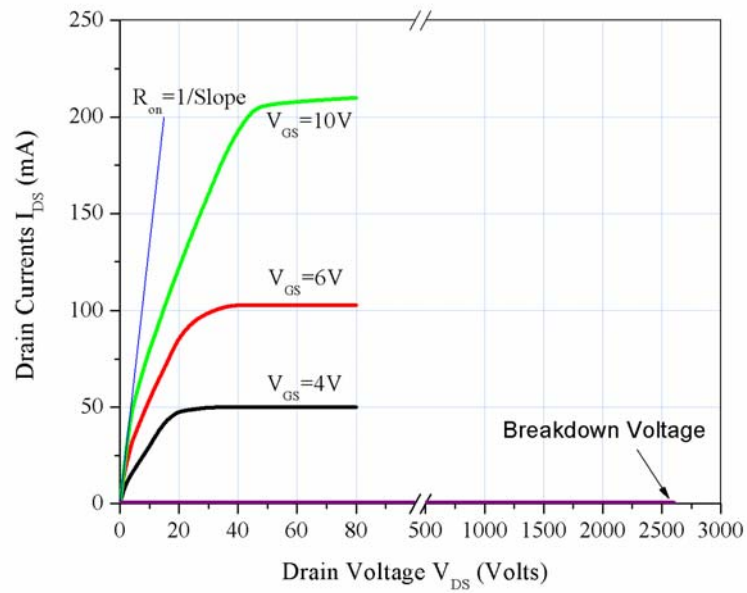
Results from the analytical model

- Voltage and current equations are solved numerically because of the implicit nature of the two sets of equations
- The parameter values of 4H-SiC are used to evaluate the drain currents
- A number of output characteristics are obtained for different gate voltages

$L = 1\ \mu m$,	$W_t = 25\ \mu m$
$L_p = 15\ \mu m$,	$W_j = 5\ \mu m$
$L_s = 18\ \mu m$	$V_T = 1V$

$\mu_{n\text{-}SiC} = 40\ cm^2/V.s$, $t_{ox} = 500$ Å

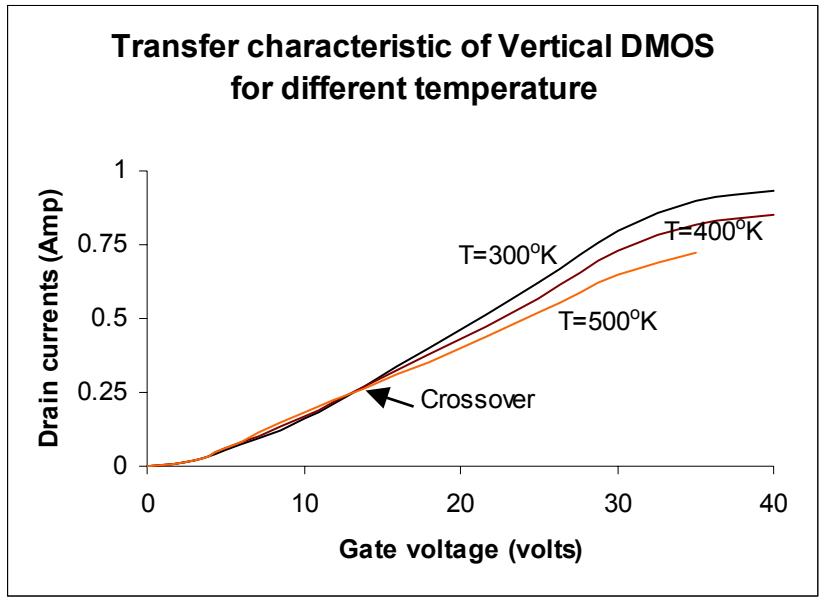
$\varepsilon_{ox} = 3.9 \times 8.854 \times 10^{-12}$ F/cm



Output Characteristics of vertical DIMOS with 4H-SiC parameters

Results of analytical model(contd.)

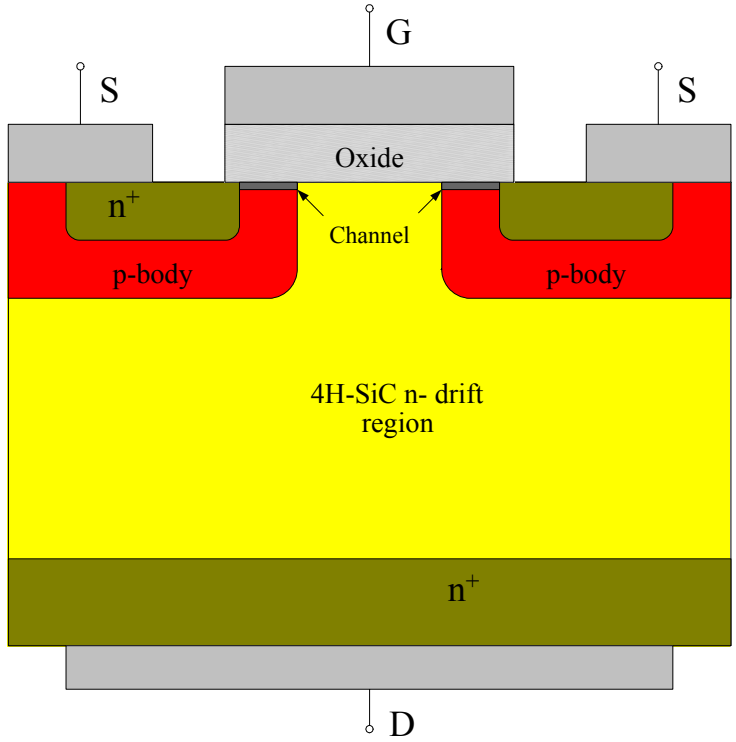
- Effects of impurity concentrations of drift region and narrow *p*-body spacing regions have been observed
- Gate loses its control over the drain current if velocity saturation occurs before the drain pinches off
- Larger *p*-body separation reduces the quasi-saturation effect
- Lower impurity concentrations increase the quasi-saturation effect
- Transfer characteristics show a clear crossover with temperature variation at a gate voltage of 15V



Transfer Characteristics of VDIMOS with 4H-SiC parameters

Model verification using ATLAS simulations

- Vertical MOSFET structure in 4H-SiC is proposed to verify the analytical model
- *n*-Drift is doped lightly ($4.2 \times 10^{15} cm^{-3}$) to hold the desired breakdown voltage
- *n*+ regions are doped ($1.5 \times 10^{20} cm^{-3}$) with Nitrogen
- *p*-body is formed by Aluminum implantations ($4 \times 10^{17} cm^{-3}$)
- *p*-bodies are separated by 20μm
- Oxide thickness is 500Å
- Drift region thickness is 20μm



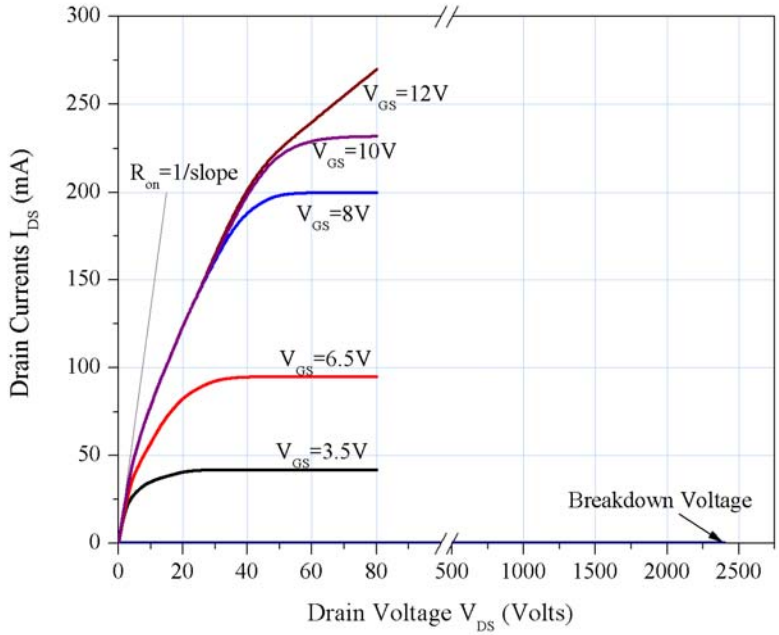
Vertical MOSFET Structure in 4H-SiC

Device dimensions for the proposed 4H-SiC DIMOS

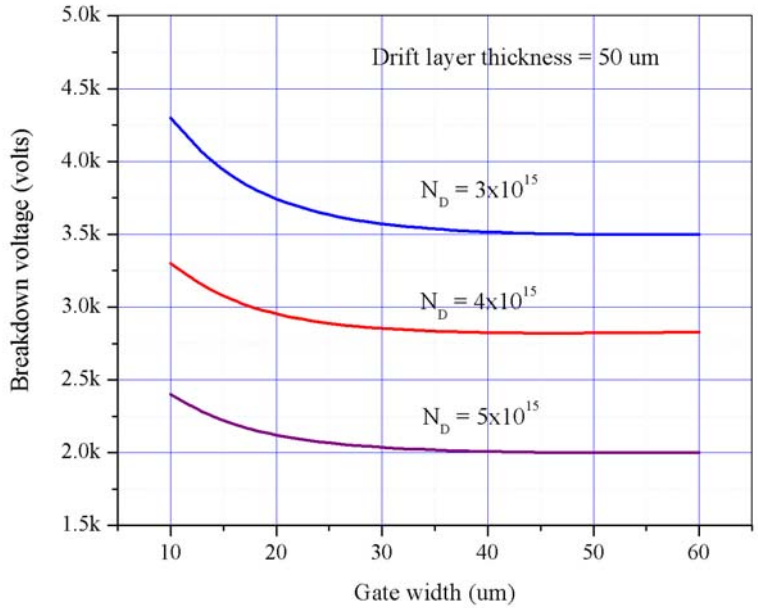
Device dimensions		Doping		
		Region	Doping level	Impurity
Channel width	400 μm	n-drift	$4x10^{15}cm^{-3}$	Nitrogen
Channel length	1 μm	p-bodies	$4x10^{17}cm^{-3}$	Aluminum
Oxide thickness	500 Å	n+ region	$(1.5x10^{20}cm^{-3})$	Nitrogen
p-bodies separation	20 μm			
Epilayer thickness	25 μm			

Simulation results using ATLAS device simulator

	Analytical model	ATLAS simulations
Drain currents	**220 mA at V_{GS}=10V**	**232 mA at V_{GS}=10V**
Specific on-resistance	**54 mΩ.cm²**	**60 mΩ.cm²**
Breakdown voltage	**2.6kV**	**2.3kV**



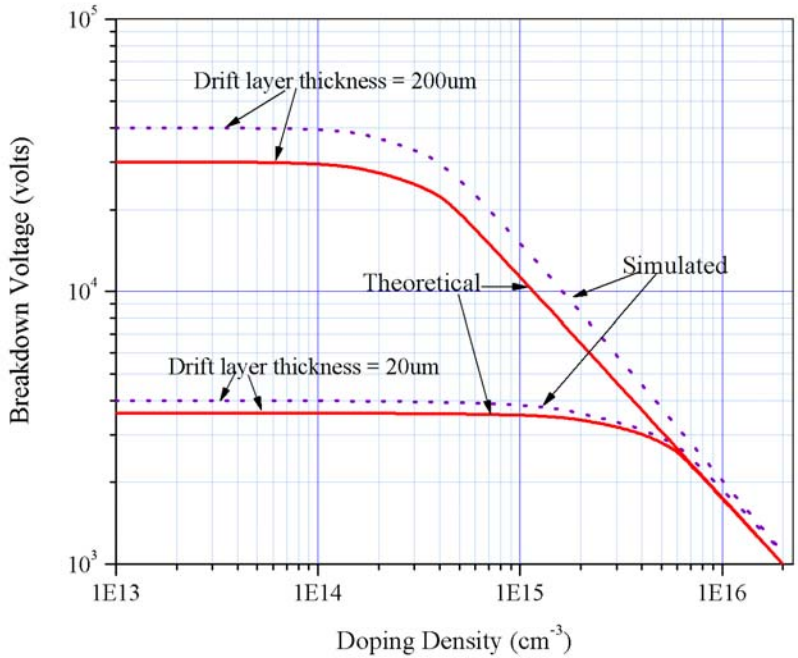
Output characteristics from ATLAS simulator



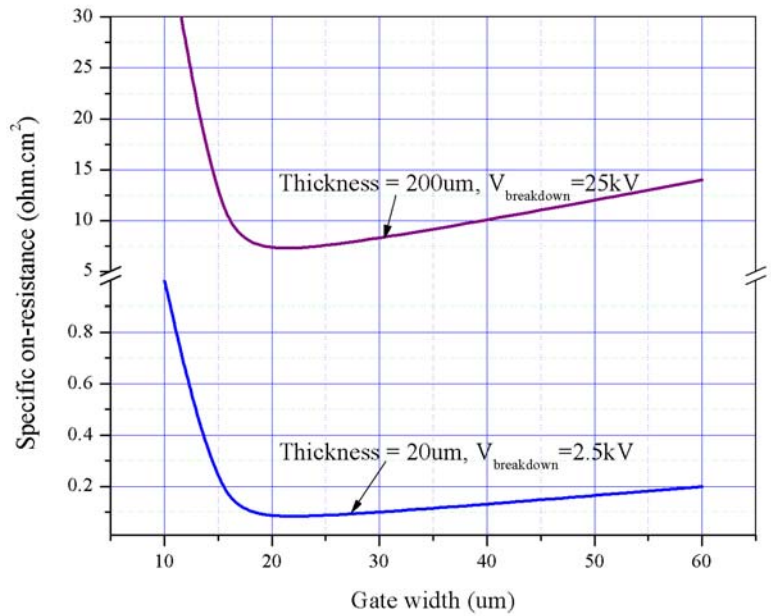
Breakdown voltage variation with gate length

Simulation results using ATLAS device simulator (contd.)

- Optimum gate width of 20 μm is obtained for minimum specific on-resistance
- A good agreement between the theoretical and the simulated values of breakdown voltage
- Specific on-resistance values are in the same magnitude compared to the recently published values
- Clear quasi-saturation effect has been observed in ATLAS simulation
- Good agreement between the analytical model and the proposed device structure



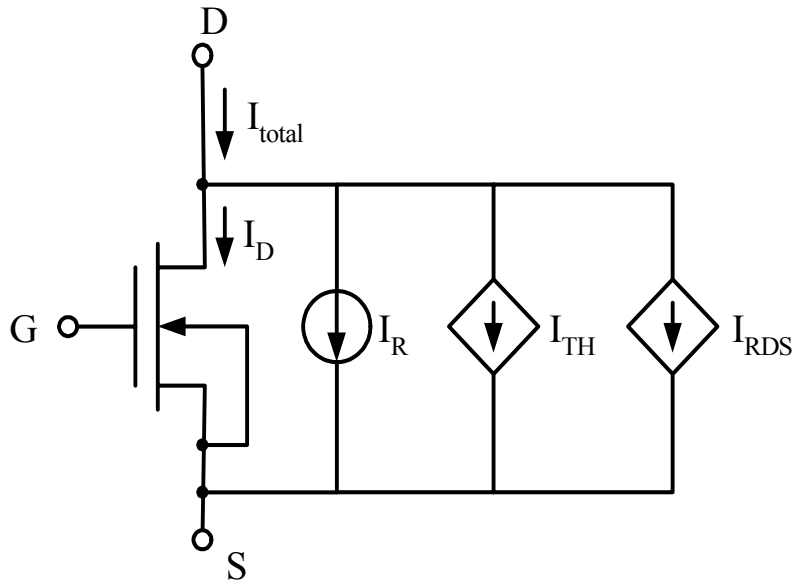
Comparison of theoretical and simulated values of breakdown voltages with drift layer thickness as a parameter



Variation of specific on-resistance with gate width

Temperature modeling for lateral MOSFET

- I_D = MOSFET channel current, at room temperature
- I_R = Body leakage current
- I_{TH} = Current change due to the threshold voltage change
- I_{RDS} = Current change due to the change of drain and source contact region resistance
- I_D is kept constant over the temperature variation
- The compensating currents incorporate the change in the MOSFET's current



MOSFET model with temperature compensation

*M. Hasanuzzaman, S.K. Islam and L.M. Tolbert, "Effects of temperature variation (300°-600° K) in MOSFET modeling in 6H silicon carbide", Solid State Electronics, Vol 48/1 pp 125-132, 2004

Temperature modeling for lateral MOSFET(contd.)

Total Drain Current

$$I_{total} = I_D + I_R + I_{TH} + I_{RDS}$$

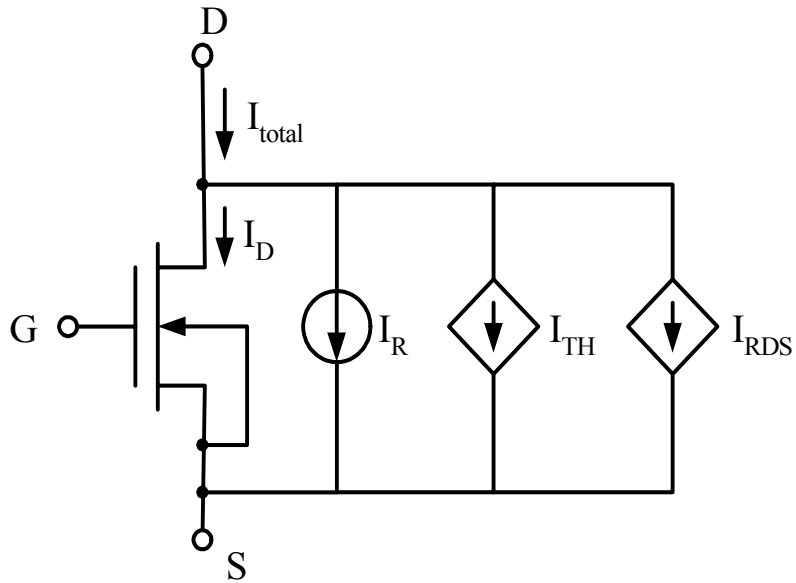
Where,

$$I_D = \frac{W}{L}\mu_n C_{ox}\left[\left(V_{GS} - V_{TH}\right) - V_{DS}/2\right]V_{DS}$$

$$I_R = qA\frac{D_n n_i^2}{L_n N_A}\alpha A T^3 \exp\left\{-\frac{E_g}{kT}\right\}$$

$$I_{TH} = \frac{W}{L}\mu_n C_{ox}\left[V'_{TH} - V_{TH}\right]V_{DS}$$

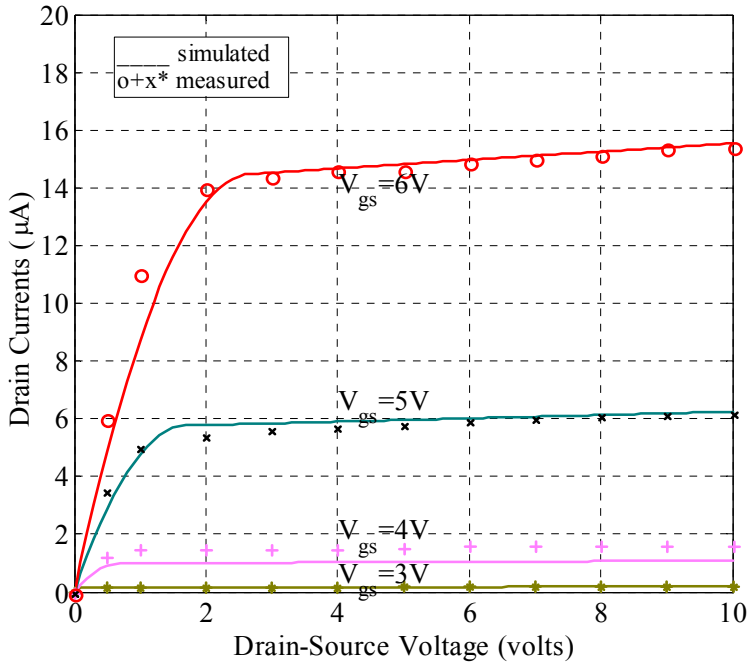
$$I_{RDS} = \beta\left(\frac{1}{R'_{DS}} - \frac{1}{R_{DS}}\right)V_{DS}$$



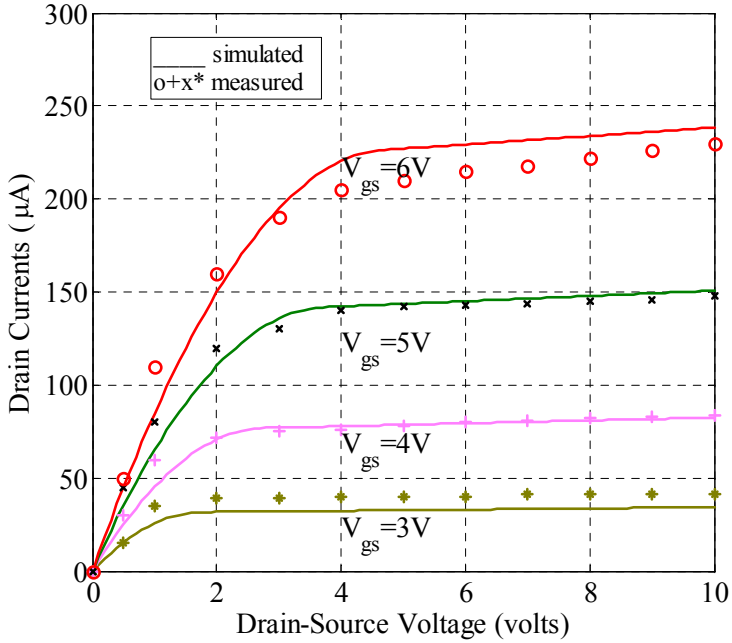
MOSFET model with temperature compensation

Results of temperature model in 6H-SiC

- The model simulations match perfectly with the measured data at 300°K
- The simulations at 600°K match reasonably with the measured data with minor discrepancies
- At 300°K, the drain current is 15μA, whereas it rises to 235μA at 600°K for a gate voltage V_{GS}= 6V



Output characteristics for simulated and measured data at 300°K



Output characteristics for simulated and measured data at 600°K

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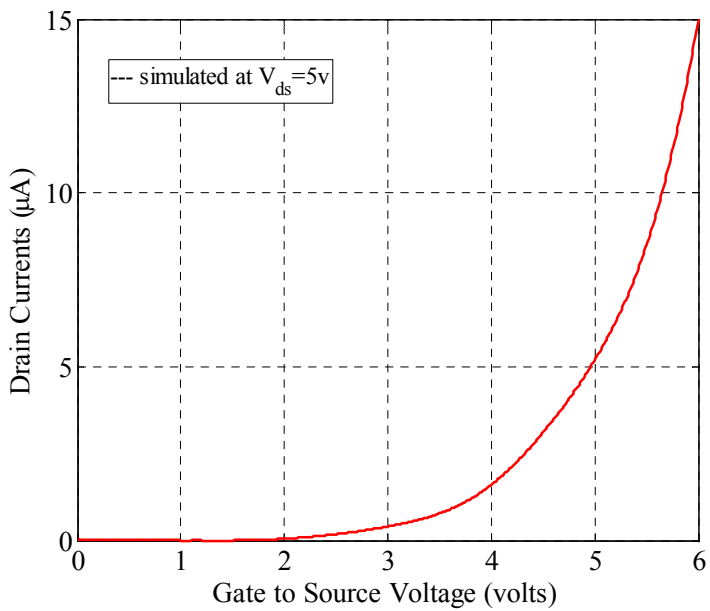
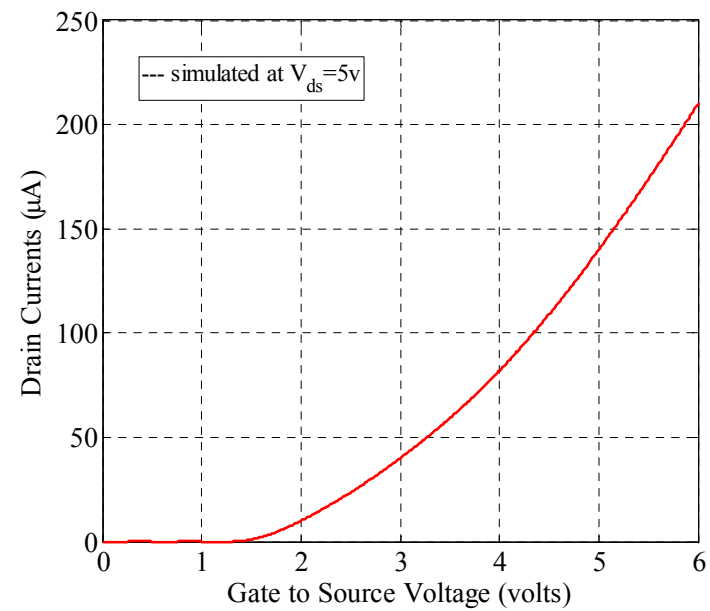
Results of temperature model in 6H-SiC (contd.)

Contribution of the compensating currents to the total current change

Temperature (°K)	Total Current change (μA)	Due to I_{TH}	Due to I_R	Due to I_{RDS}
400	**45**	**90%**	**2%**	**8%**
500	**116**	**85%**	**6%**	**9%**
600	**220**	**78%**	**15%**	**7%**



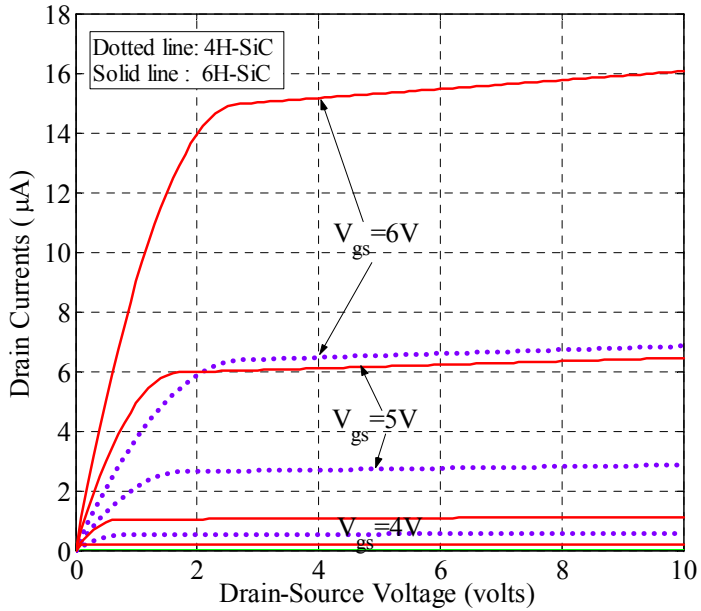
Transfer characteristics simulated at drain-source voltage V_{DS}=5V, temperature 300°K



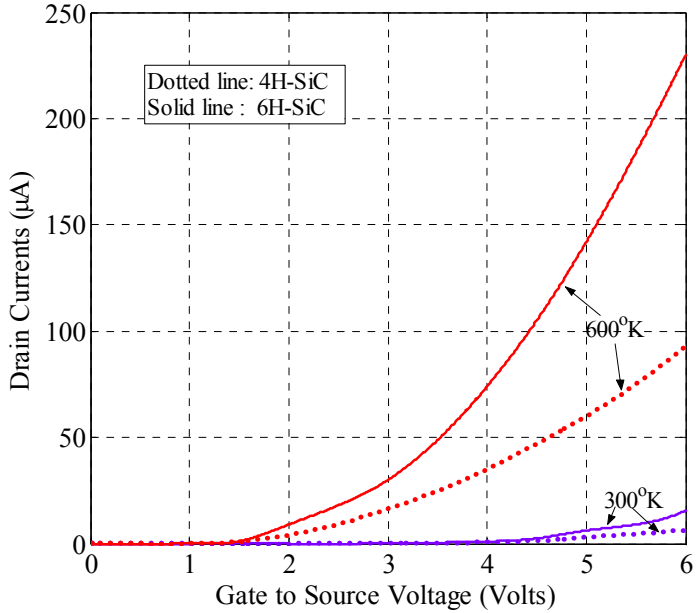
Transfer characteristics simulated at drain-source voltage V_{DS}=5V, temperature 600°K

Results of temperature model in 4H- & 6H-SiC

- Drain currents of 6H-SiC MOSFET are greater than their 4H-SiC counterparts by a factor of approximately 2.5
- Higher mobility of 6H-SiC (≅100 cm^2/V.sec) results in higher drain current of 6H-SiC MOSFET compared to 4H-SiC MOSFETs
- Simulation results show a better performance for 6H-SiC MOSFETs



Output characteristics of 4H- & 6H-SiC lateral MOSFET at 300°K



Transfer characteristics of 4H- & 6H-SiC lateral MOSFET

*M. Hasanuzzaman, S.K. Islam and L.M. Tolbert, "Temperature Dependency of MOSFET Device Characteristics in 4H- and 6H-Silicon Carbide (SiC)" ", to be presented in ISDRS'2003

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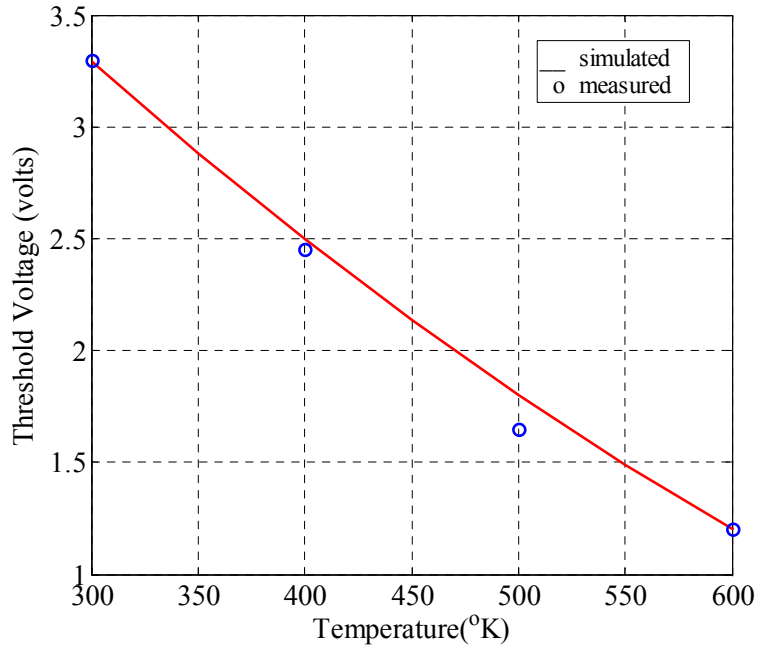
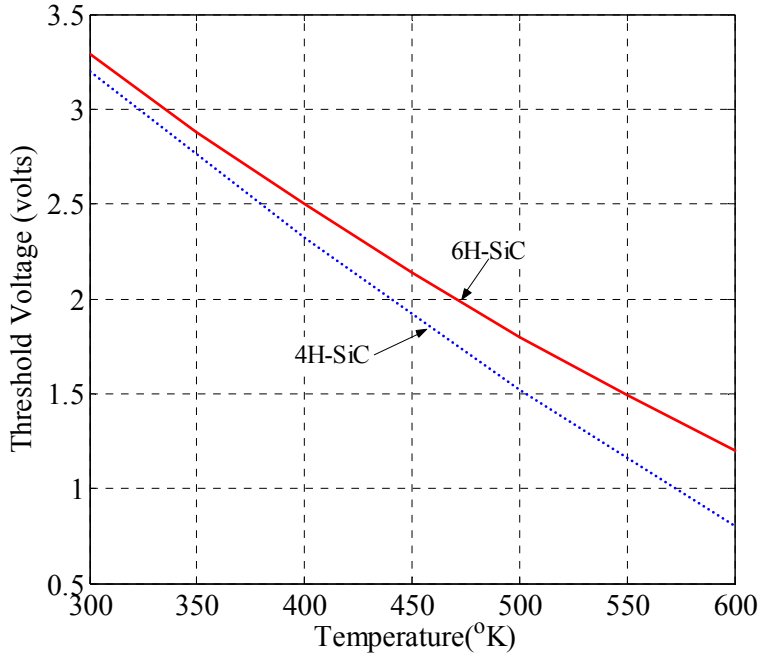
Results of temperature model in 4H- & 6H-SiC

- Threshold voltage changes from 3.2V at 300°K to 1.2V at 600°K
- Simulated values of the threshold voltages matches with the measured data
- Variation of threshold voltage for 4H-SiC is predicted using the model



Threshold voltages obtained from simulation and measurement for different temperature



Threshold voltage variation of 4H- & 6H-SiC lateral MOSFET with temperature

Conclusions

- Silicon carbide is better alternate material for high power and high temperature device application
- An analytical model for vertical DIMOS in 4H-SiC is developed
- A device structure is proposed to verify the model
- A temperature model for lateral MOSFET is developed
- Simulation with MOSFET temperature model is carried out for 4H- and 6H-SiC materials

Thanks!!