4H- and 6H- Silicon Carbide in Power MOSFET Design

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Agenda

- Overview of silicon carbide
- Comparison of Si and SiC MOSFET
- Vertical power MOSFET model
- A proposed device structure
- MOSFET temperature model
- Results
- Conclusions
Why SiC?

- Large band gap and high melting point enable high temperature device operations
- Large break down field enable the fabrication of smaller and compact high voltage power devices
- Requires smaller cooling system due to High thermal conductivity
- Extremely radiation hard
- Shows excellent reverse recovery characteristics
- Excellent mechanical properties make SiC ideal for MEMS applications
Why Not Silicon?

- Smaller band gap and low melting point enable medium range of temperature device operations
- Due to lower thermal conductivity, requires larger cooling system
- Smaller electric breakdown field limit the device size and voltage
- Shows high leakage current

**Fig:** Comparison of Si and SiC properties
# Physical & Electrical Properties of SiC

<table>
<thead>
<tr>
<th>Properties</th>
<th>Si</th>
<th>6H-SiC</th>
<th>4H-SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap (eV)</td>
<td>1.11</td>
<td>3.0</td>
<td>3.26</td>
</tr>
<tr>
<td>Dielectric const.</td>
<td>11.8</td>
<td>9.7</td>
<td>10</td>
</tr>
<tr>
<td>Breakdown field (V/cm)</td>
<td>6x10^5</td>
<td>3.5x10^6</td>
<td>3.5x10^6</td>
</tr>
<tr>
<td>Saturated drift velocity (cm/sec)</td>
<td>1x10^7</td>
<td>2x10^7</td>
<td>2x10^7</td>
</tr>
<tr>
<td>Electron mobility (in bulk) (cm^2/V-sec)</td>
<td>1350</td>
<td>370</td>
<td>720(^a) 650(^c)</td>
</tr>
<tr>
<td>Hole mobility (in bulk) (cm^2/V-sec)</td>
<td>450</td>
<td>95</td>
<td>120</td>
</tr>
<tr>
<td>Thermal conductivity (W/cm^2-K)</td>
<td>1.5</td>
<td>4.9</td>
<td>4.9</td>
</tr>
<tr>
<td>Melting point (°C)</td>
<td>1420</td>
<td>2830</td>
<td>2830</td>
</tr>
<tr>
<td>Hardness (kg/mm^2)</td>
<td>1000</td>
<td>-</td>
<td>2310</td>
</tr>
</tbody>
</table>

\(^a\) along a-axis, \(^c\) along c-axis
Comparison of Wide Bandgap Materials

SiC is unique because of its native oxide is SiO₂, therefore easy to fabricate field effect device.

Though Diamond has the best material properties, it is not suitable for conventional electronic device fabrication.

It is very difficult to form oxide in GaN, it is suitable for opto-electronics devices.

<table>
<thead>
<tr>
<th>Properties</th>
<th>4H-SiC</th>
<th>GaN</th>
<th>Diamond</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lattice constant (Å)</td>
<td>3.073 a 10.053 c</td>
<td>4.51</td>
<td>3.57</td>
</tr>
<tr>
<td>Thermal expansion (x10⁻⁶) °C</td>
<td>-</td>
<td>5.6</td>
<td>0.08</td>
</tr>
<tr>
<td>Density (g/cm³)</td>
<td>-</td>
<td>-</td>
<td>3.51</td>
</tr>
<tr>
<td>Melting point (°C)</td>
<td>2830</td>
<td>-</td>
<td>4000</td>
</tr>
<tr>
<td>Bandgap (eV)</td>
<td>3.26</td>
<td>3.45</td>
<td>5.45</td>
</tr>
<tr>
<td>Saturated electron velocity (x10⁷ cm/s)</td>
<td>2.0</td>
<td>2.2</td>
<td>2.7</td>
</tr>
<tr>
<td>Mobility (cm²/V-s)</td>
<td>780 50</td>
<td>1250 250</td>
<td>2200 1600</td>
</tr>
<tr>
<td>Electron Hole</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Breakdown Voltage (x10⁵ V/cm)</td>
<td>30</td>
<td>&gt;50</td>
<td>100</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>9.66</td>
<td>11</td>
<td>5.5</td>
</tr>
<tr>
<td>Resistivity (Ω-cm)</td>
<td>-</td>
<td>10¹⁰</td>
<td>10¹³</td>
</tr>
<tr>
<td>Thermal conductivity (W/cm.K)</td>
<td>4.9</td>
<td>1.3</td>
<td>20</td>
</tr>
<tr>
<td>Hardness (kg/mm²)</td>
<td>2130 a</td>
<td>-</td>
<td>10000</td>
</tr>
</tbody>
</table>
Specific on-resistance has to be kept as low as possible

Breakdown voltage has to increase as design requirements

Low specific on-resistance reduces power losses and increases efficiency

Specific on-resistance increases with the increase of the breakdown voltage

A design trade-off has to be made between the specific on-resistance and the voltage rating

\[ V_{Br} = \frac{\varepsilon E_c^2}{2qN_d} \]

\[ R_{on-sp} = \frac{4V_{Br}^2}{\varepsilon E_c^3 \mu_n} \]


Power MOSFET design considerations (contd.)

- SiC devices demonstrate one-hundredth times lower specific on-resistance and ten times higher breakdown voltage than the silicon devices for the same device dimensions.
- Drift region thickness is ten times lower in silicon carbide compared to silicon device for same voltage rating.
- Mass and volume of heat sink is 15-20% smaller in case of silicon carbide.
Comparison of Si & SiC Power MOSFETs

Si-MOSFET

SiC-MOSFET & Heat sink

Heat sink for Si devices

<table>
<thead>
<tr>
<th></th>
<th>Silicon</th>
<th>Silicon-Carbide</th>
</tr>
</thead>
<tbody>
<tr>
<td>On-Resistance</td>
<td>100 m.Ω/cm²</td>
<td>1 m.Ω/cm²</td>
</tr>
<tr>
<td>Drift Region Thickness</td>
<td>100 µm</td>
<td>10 µm</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>150°C</td>
<td>500°C</td>
</tr>
<tr>
<td>Heat Sink Volume &amp; Mass</td>
<td>100%</td>
<td>80-85%</td>
</tr>
<tr>
<td>Device size</td>
<td>100%</td>
<td>50%</td>
</tr>
</tbody>
</table>
**Future power electronics will be SiC!**

<table>
<thead>
<tr>
<th>Today’s Technology</th>
<th>Advantages of Silicon Carbide</th>
<th>Payoff</th>
</tr>
</thead>
<tbody>
<tr>
<td>Large energy losses</td>
<td>Reduce loss by 10x</td>
<td>Large improvement in efficiency</td>
</tr>
<tr>
<td>Limited voltage and power level</td>
<td>Increase power $10^3$x</td>
<td>Simplify use in electrical grid</td>
</tr>
<tr>
<td>Low operating temperature (&lt; 150ºC)</td>
<td>Increase range to 500ºC</td>
<td>New applications; eliminate massive heat sinks</td>
</tr>
<tr>
<td>Large heat sinks &amp; filters</td>
<td>Reduce size/weight by 3x</td>
<td>Lightweight, compact systems</td>
</tr>
</tbody>
</table>
Potential applications of SiC electronics

Automotive

Utility

Space-craft

Mining

Nuclear power

Aircraft

Analog VLSI and Devices Laboratory
Limitations of SiC

- Higher defect densities due to micropipes and dislocations in the crystal orientations
- Material processing and device fabrication require high temperature process (1000-1700°C)
- Device quality SiC wafer is very costly
- High interface state densities
- Low inversion layer mobility
- Power MOSFETs in SiC are not commercially available
SiC are made by arrangement of covalently bonded tetrahedral Si and C atoms

50% carbon atoms and 50% silicon atoms

SiC has more than 100 known polytypes

Polytype refers to a family of material which has common stoichiometric
The arrangement of SiC bi-layers is same in 2-D but differs in by stacking sequence in 3-D

3 commonly used polytypes:

- **3C-SiC**: Cubic structure, Zinc-blend, ABCABC….
- **4H-SiC**: Hexagonal close packed, ABCBABCBCB…
- **6H-SiC**: Hexagonal close packed, ABCACBABCAC…

Stacking sequences for four different SiC polytypes
Device fabrication: the pathway to success

- Material Processing
  - Epitaxial Growth
  - Dopant Activation
  - Interface Engineering
- Device Fabrication
- Applications
  - Circuit Design
  - System Integration
Drawback of lateral structure for power application

- Power MOSFETs have to handle high voltages and high currents
- Lateral structure is not suitable for power application
- Current flows laterally through the channel below the gate oxide
- No drift region available to hold large voltage
- No option is available for forward blocking capability
- Required large W to get large W/L ratio to increase the current capacity
Vertical MOSFET for high voltage and high power

- Source and drain are made on top and bottom of the wafer respectively.
- Current flows vertically from drain to source through drift and channel region.
- Drift region supports most of the applied drain voltage.
- Channel region provides the current gain.
- p-n junction between p-body and n-drift region provides forward blocking capability.

Vertical MOSFET Structure
Vertical MOSFET for high voltage and high power

- P-bodies can be made either round or hexagonal shaped to get large W
- Length L can be made very small
- For same die area, W/L ratio is higher compared to lateral MOSFET
- Drift region doping can be adjusted to get high breakdown voltage with low on-resistance
- 4H-SiC is suitable for vertical structure due to higher mobility in vertical direction
Modeling of vertical DIMOS structure

- For analysis the structure is divided into two regions: (i) the channel region, and (ii) the drift region
- Channel forms in the p-body below the gate oxide where gate voltage controls the channel currents
- Drain current is divided into two channel currents in two p-bodies on both sides
- Drift region begins at the drain and ends at the channel near the oxide layer

Cross-section details of VDIMOS structure used in the model

Modeling of vertical DIMOS structure (contd.)

- Drift region is divided into three regions
  - Region A: an accumulation region between the $p$-bodies with small cross-section
  - Region B: a drift region with varying cross-section
  - Region C: a drift region with constant cross-section
- Current voltage relations for channel region and three drift regions have been developed
Modeling of vertical DIMOS structure (contd.)

**Channel Current**

\[ I_{ch} = \frac{W \mu_{\text{neff}}}{2L[1 + (\mu_{\text{neff}} / 2V_{\text{sat}})V_{ch}]} \left[ 2C_{ox}(V_{GS} - V_T) - (C_{ox} + C_{do})V_{ch} \right] \]

- Where \( C_{ox} + C_{do} \) is the total capacitance of the oxide and the body depletion

- Current increases with the decrease of channel length and increase in channel width and voltage

- Gate voltage controls the channel current

- At saturation, channel current is given by,

\[ I_{ch(sat)} = W \mu_{\text{sat}} C_{ox} (V_{GS} - V_{T}) \]
Modeling of vertical DIMOS structure (contd.)

Drift Region Voltage

Total drift region voltage is the sum of the voltages of the three regions,

\[ V_{\text{drift}} = V_A + V_B + V_C \]

Where,

\[ V_A = \int_{0}^{W_j+W_d} E_y dy = \frac{I_D (W_j + W_d)}{W (L_s qN_d \mu_n) - I_D / E_C} \]

\[ V_B = \frac{I_D}{WqN_d \mu_n \cot \alpha} \log \left[ \frac{WqN_d \mu_n (L_s + 2L_p) - I_D / E_C}{WqN_d L_s \mu_n - I_D / E_C} \right] \]

\[ V_C = \frac{I_D (W_t - W_j - W_d - L_p \tan \alpha)}{WqN_d \mu_n (L_s + 2L_p) - I_D / E_C} \]
Results from the analytical model

- Voltage and current equations are solved numerically because of the implicit nature of the two sets of equations.

- The parameter values of 4H-SiC are used to evaluate the drain currents.

- A number of output characteristics are obtained for different gate voltages.

\[ \mu_{\text{n-SiC}} = 40 \text{ cm}^2/\text{V.s}, \quad t_{\text{ox}} = 500 \text{ Å} \]
\[ \varepsilon_{\text{ox}} = 3.9 \times 10^{-12} \text{ F/cm} \]

- \( L = 1 \mu\text{m}, \quad W_t = 25 \mu\text{m} \)
- \( L_p = 15 \mu\text{m}, \quad W_j = 5 \mu\text{m} \)
- \( L_s = 18 \mu\text{m} \quad V_T = 1\text{V} \)

Output Characteristics of vertical DIMOS with 4H-SiC parameters
Results of analytical model (contd.)

- Effects of impurity concentrations of drift region and narrow $p$-body spacing regions have been observed.
- Gate loses its control over the drain current if velocity saturation occurs before the drain pinches off.
- Larger $p$-body separation reduces the quasi-saturation effect.
- Lower impurity concentrations increase the quasi-saturation effect.
- Transfer characteristics show a clear crossover with temperature variation at a gate voltage of 15V.

Transfer Characteristics of VDIMOS with 4H-SiC parameters.
Model verification using ATLAS simulations

- Vertical MOSFET structure in 4H-SiC is proposed to verify the analytical model

- $n$-Drift is doped lightly ($4.2 \times 10^{15} \text{cm}^{-3}$) to hold the desired breakdown voltage

- $n^+$ regions are doped ($1.5 \times 10^{20} \text{cm}^{-3}$) with Nitrogen

- $p$-body is formed by Aluminum implantations ($4 \times 10^{17} \text{cm}^{-3}$)

- $p$-bodies are separated by $20 \mu\text{m}$

- Oxide thickness is $500 \AA$

- Drift region thickness is $20 \mu\text{m}$
## Device dimensions for the proposed 4H-SiC DIMOS

<table>
<thead>
<tr>
<th>Device dimensions</th>
<th>Doping</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Region</td>
</tr>
<tr>
<td>Channel width</td>
<td>400 µm</td>
</tr>
<tr>
<td>Channel length</td>
<td>1 µm</td>
</tr>
<tr>
<td>Oxide thickness</td>
<td>500 Å</td>
</tr>
<tr>
<td>p-bodies separation</td>
<td>20 µm</td>
</tr>
<tr>
<td>Epilayer thickness</td>
<td>25 µm</td>
</tr>
</tbody>
</table>
Simulation results using ATLAS device simulator

<table>
<thead>
<tr>
<th></th>
<th>Analytical model</th>
<th>ATLAS simulations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain currents</td>
<td>220 mA at $V_{GS}=10V$</td>
<td>232 mA at $V_{GS}=10V$</td>
</tr>
<tr>
<td>Specific on-resistance</td>
<td>54 mΩ.cm²</td>
<td>60 mΩ.cm²</td>
</tr>
<tr>
<td>Breakdown voltage</td>
<td>2.6kV</td>
<td>2.3kV</td>
</tr>
</tbody>
</table>

Output characteristics from ATLAS simulator

Breakdown voltage variation with gate length
Simulation results using ATLAS device simulator (contd.)

- Optimum gate width of 20 µm is obtained for minimum specific on-resistance
- A good agreement between the theoretical and the simulated values of breakdown voltage
- Specific on-resistance values are in the same magnitude compared to the recently published values
- Clear quasi-saturation effect has been observed in ATLAS simulation
- Good agreement between the analytical model and the proposed device structure

Comparison of theoretical and simulated values of breakdown voltages with drift layer thickness as a parameter

Variation of specific on-resistance with gate width
Temperature modeling for lateral MOSFET

- $I_D = \text{MOSFET channel current, at room temperature}$
- $I_R = \text{Body leakage current}$
- $I_{TH} = \text{Current change due to the threshold voltage change}$
- $I_{RDS} = \text{Current change due to the change of drain and source contact region resistance}$
- $I_D$ is kept constant over the temperature variation
- The compensating currents incorporate the change in the MOSFET's current

Total Drain Current

\[ I_{\text{total}} = I_D + I_R + I_{TH} + I_{RDS} \]

Where,

\[ I_D = \frac{W}{L} \mu_n C_{ox} \left[ \left( V_{GS} - V_{TH} \right) - V_{DS} / 2 \right] V_{DS} \]

\[ I_R = qA \frac{D_n n_i^2}{L_n N_A} \alpha A T^3 \exp \left\{ - \frac{E_g}{kT} \right\} \]

\[ I_{TH} = \frac{W}{L} \mu_n C_{ox} \left[ V'_{TH} - V_{TH} \right] V_{DS} \]

\[ I_{RDS} = \beta \left( \frac{1}{R'_{DS}} - \frac{1}{R_{DS}} \right) V_{DS} \]

MOSFET model with temperature compensation
Results of temperature model in 6H-SiC

- The model simulations match perfectly with the measured data at 300ºK.
- The simulations at 600ºK match reasonably with the measured data with minor discrepancies.
- At 300ºK, the drain current is 15µA, whereas it rises to 235µA at 600ºK for a gate voltage $V_{GS} = 6V$.

![Output characteristics for simulated and measured data at 300ºK](image1.png)

![Output characteristics for simulated and measured data at 600ºK](image2.png)
Results of temperature model in 6H-SiC (contd.)

Contribution of the compensating currents to the total current change

<table>
<thead>
<tr>
<th>Temperature (°K)</th>
<th>Total Current change (µA)</th>
<th>Due to $I_{TH}$</th>
<th>Due to $I_R$</th>
<th>Due to $I_{RDS}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>400</td>
<td>45</td>
<td>90%</td>
<td>2%</td>
<td>8%</td>
</tr>
<tr>
<td>500</td>
<td>116</td>
<td>85%</td>
<td>6%</td>
<td>9%</td>
</tr>
<tr>
<td>600</td>
<td>220</td>
<td>78%</td>
<td>15%</td>
<td>7%</td>
</tr>
</tbody>
</table>

Transfer characteristics simulated at drain-source voltage $V_{DS}=5V$, temperature 300°K

Transfer characteristics simulated at drain-source voltage $V_{DS}=5V$, temperature 600°K

--- simulated at $V_{ds}=5v$
Results of temperature model in 4H- & 6H-SiC

- Drain currents of 6H-SiC MOSFET are greater than their 4H-SiC counterparts by a factor of approximately 2.5
- Higher mobility of 6H-SiC ($\approx$100 cm$^2$/V.sec) results in higher drain current of 6H-SiC MOSFET compared to 4H-SiC MOSFETs
- Simulation results show a better performance for 6H-SiC MOSFETs

Output characteristics of 4H- & 6H-SiC lateral MOSFET at 300°C

Transfer characteristics of 4H- & 6H-SiC lateral MOSFET

Results of temperature model in 4H- & 6H-SiC

- Threshold voltage changes from 3.2V at 300°K to 1.2V at 600°K
- Simulated values of the threshold voltages matches with the measured data
- Variation of threshold voltage for 4H-SiC is predicted using the model

Threshold voltages obtained from simulation and measurement for different temperature

Threshold voltage variation of 4H- & 6H-SiC lateral MOSFET with temperature
Conclusions

- Silicon carbide is better alternate material for high power and high temperature device application
- An analytical model for vertical DIMOS in 4H-SiC is developed
- A device structure is proposed to verify the model
- A temperature model for lateral MOSFET is developed
- Simulation with MOSFET temperature model is carried out for 4H- and 6H-SiC materials
Thanks!!