Split-Phase Control

LTSpice Simulation

![Graph showing voltage output (V_out) against current output (I_out) for different load conditions. The graph includes three load conditions: 50 \mu F, 1 m\Omega; 500 \mu F, 100 m\Omega, and 5 \mu F, 1 m\Omega. The graph also includes markers for different load conditions: R_{SSL}, R_{FSL}, and Current Loaded, Split-Phase.]
Complete Soft Charging

FCML and SC Buck
Types of Capacitors
Ceramic Capacitor Impedance and Resistance

Capacitor data sources

- Murata Simsurfing
- TDK SEAT
MLCC

- Capacitor codes, e.g. X7R or C0G standardized to define stability over temperature
  - **Class-II**: Codes begin with X, Y, or Z (e.g. X7R, Y5V)

- **Class-I**: Codes begin with [CBLAMPRSTVU] (e.g. C0G, NPO)
2.2μF, 50V X7R (Class-II) 0603 footprint

Remaining: 7.2% at full voltage
10nF, 50V C0G (Class-I) 0603 footprint

DC Bias [V]

Frequency [Hz]

Capacitance [pF]

Impedance [ohm]

Resistance [ohm]
10nF, 50V X7R (Class-II) 0603 footprint
10nF, 50V C0G (Class-I) varied footprint
Same 0603 Footprint

![Graph showing impedance vs frequency for 2.2μF X5R and 10nF C0G capacitors.]

- **2.2μF X5R**
- **10nF C0G**
Table II

<table>
<thead>
<tr>
<th>Component</th>
<th>Dielectric</th>
<th>Manufacturer</th>
<th>Part Number</th>
<th>$V_{dc}$</th>
<th>$C_{n}$</th>
<th>N(parallel)</th>
<th>$C_{tot}$</th>
<th>DF</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{cal}$</td>
<td>C0G</td>
<td>TDK</td>
<td>CAA572C0G22J204J640LH</td>
<td>650 V</td>
<td>200 nF</td>
<td>2</td>
<td>400 nF</td>
<td>$&lt; 0.02 %$</td>
</tr>
<tr>
<td>$C_{ref}$</td>
<td>C0G</td>
<td>TDK</td>
<td>C5750C0G2A154J230KE</td>
<td>100 V</td>
<td>150 nF</td>
<td>32</td>
<td>4.8 $\mu$F</td>
<td>$&lt; 0.03 %$</td>
</tr>
<tr>
<td>$C_{DUT}$</td>
<td>X7R</td>
<td>Knowles Syfer</td>
<td>2220Y1K00474KETWS2</td>
<td>1 kV</td>
<td>470 nF</td>
<td>1</td>
<td>470 nF</td>
<td>$&gt; 0.71 %$</td>
</tr>
</tbody>
</table>

Fig. 6. $U - Q$ hysteresis recorded at 50 Hz for a range of excitation voltages for (a) the calibration capacitor, which shows no hysteresis and has a constant $C_Q = C_0$ at all voltages, and (b) the DUT, which exhibits increasing hysteresis and losses with increasing excitation voltage. $C_Q$ highlighted for $U_{ac} = 270$ Vrms. Measured $U - Q$ curves are identical at 50 Hz and 100 Hz.

$C_{oss}$ Hysteresis

Fig. 15. Losses per cycle versus normalized, by (8), $dV/dt$ for the three studied devices and two additional “extreme performance” devices. The red outline around the TPH3202LS results indicates applied voltages under 300 V and $\beta = 1.46$ in (8). All recorded measurements are included here. There are no measurements for the TPH3202LS 30 MHz $\phi_2$, as the $\phi_2$ wave generator could not be tuned to maintain ZVS with the TPH3202LS device and $C_{REF}$ in parallel.
Transistor Structure and Material

SiC

Si Superjunction

Si

Fig. 4: $C_{OSS}$ losses for three devices from 1-35 MHz.

Fig. 6: Silicon superjunction $C_{OSS}$ loss data.