High Side Signal Ground

- Gate driver chip must implement $v_{gs}$ waveforms
- Issue: source of $Q_2$ is not grounded
Generating Floating Supply

- Isolated supplies sometimes used; Isolated DC-DC, batteries
- Bootstrap concept: capacitor can be charged when $V_s$ is low, then switched
UCC27211a Internal Diagram
Cascaded Bootstrapping

<table>
<thead>
<tr>
<th>Drive Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Direct Drive</td>
<td>Easiest high-side application the MOSFET and can be driven directly by the PWM controller or by a ground referenced driver, but it must meet two conditions, as follows: $V_{CC} &lt; V_{GS,\text{MAX}}$ and $V_{DC} &lt; V_{CC} - V_{GS,\text{Miller}}$.</td>
</tr>
<tr>
<td>Floating Supply Gate Drive</td>
<td>Cost impact of isolated supply is significant. Opto-coupler tends to be relatively expensive, limited in bandwidth, and noise sensitive.</td>
</tr>
<tr>
<td>Transformer Coupled Drive</td>
<td>Gives full gate control for an indefinite period of time, but is somewhat limited in switching performance. This can be improved with added complexity.</td>
</tr>
<tr>
<td>Charge Pump Drive</td>
<td>The turn-on times tend to be long for switching applications. Inefficiencies in the voltage multiplication circuit may require more than low stages of pumping.</td>
</tr>
<tr>
<td>Bootstrap Drive</td>
<td>Simple and inexpensive with limitations; such as, the duty cycle and on-time are both constrained by the need to refresh the bootstrap capacitor. Requires level shift, with the associated difficulties.</td>
</tr>
</tbody>
</table>
Half Bridge Loop Inductance

Parasitic inductances of input loop explicitly shown:

Even better: minimize area of the high frequency loop, thereby minimizing its inductance

Addition of bypass capacitor confines the pulsating current to a smaller loop:

high frequency currents are shunted through capacitor instead of input source
Bridge Layout
Effect of Loop Inductance

$$L_{\text{loop}} = 1.6\text{nH}$$

$$L_{\text{loop}} = 0.4\text{nH}$$

D Reusch, “Optimizing PCB Layout”
Half Bridge Layout: Another Example

D. Reusch & J Strydom, “Understanding the Effect of PCB Layout on Circuit Performance in a High-Frequency Gallium-Nitride-Based Point of Load Converter”
Layout Impact Measurements

- Smallest Loop Area results in
  - Smaller overvoltage
  - Lower switching loss

D. Reusch & J Strydom, "Understanding the Effect of PCB Layout on Circuit Performance in a High-Frequency Gallium-Nitride-Based Point of Load Converter"
Sinusoidal Analysis (Ch 19)

Fundamentals of Power Electronics (2nd Ed)
Ch 22 in 3rd Ed.

$n_p(t)$ - component of $v_p$ at $f_s$

$$v_p(t) = v_g$$

will lose exact $f/s$ information
- can check current polarity for possible AVS

$$i_p(t)$$

even more fundamental dominated
due to low pass characteristics of
the toroid

$$E_{in}$$

e.g. for SRC
$$E_{in} = \frac{5v}{3} + \frac{1}{3} + \frac{2v}{n^2} \approx 2v$$
Sinusoidal Analysis: Comments

- Generally most accurate when operating near resonance with a high $Q$
- Effective quality factor $Q_e$ depends not only on resonant tank, but also on loading
- Analysis neglects switching intervals; can only predict where ZVS cannot be obtained
AC Link Waveforms

\[ V_g \]  
\[ i_g \]  
\[ V_p^+ \]  
\[ i_p^+ \]  
\[ v_p^- \]  
\[ i_s^+ \]  
\[ v_s^- \]  
\[ i_{out}^+ \]  
\[ V_{out}^- \]  

DC Average

Ac waveforms
fundamental Harmonic

DC Average

\[ v_p(t) \rightarrow \text{full/actual signal} \]
\[ v_{p1}(t) \rightarrow \text{fundamental Harmonic} \]
\[ V_{p1} \cos(\omega t + \phi_{v_0}) \]