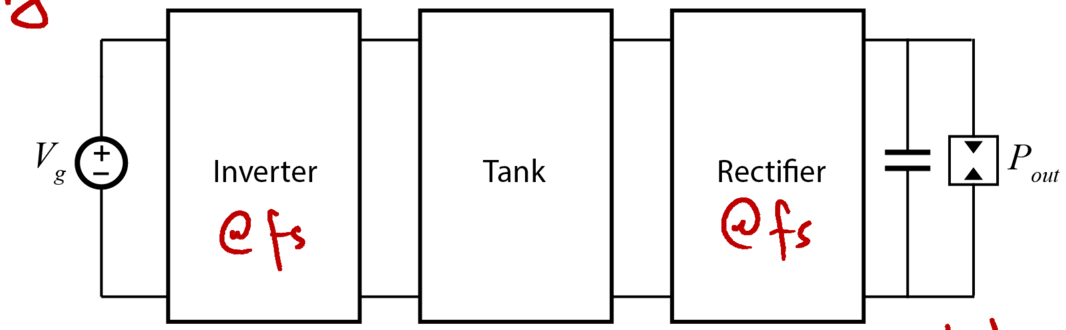
Midterm Project

- Select a (dc-dc) converter steady-state hardware design problem
- Detail
  - Application specification
  - Performance specification
    - should advance on SotA; near-optimal design
  - Design parameters
- Apply techniques from class
  - Design using MATLAB
  - Validate through simulation (PLECs/Spice)
- Should result in prototype-ready paper design
- Finalize scope by October 4th
  - 5 pts, text entry or pdf
  - Briefly describe application, performance spec, and design parameters
- Report Due October 18th
  - Narrative of analysis and results
  - Clear but minimally "wordy"
  - IEEE format (though incomplete content w.r.t. review and explanation)
- Class presentations thereafter

Symmetric Converters

HW #3 solution
Applies symmetry

AC-link Topologies



DC + ripple

waveforms ac-only @ fs

DC + ripple

Converter waveforms exhibit defined symmetry

- All waveforms are periodic about fs
- ac waveforms have half-period antisymmetry
- dc waveforms have half-period symmetry

without symmetry, using Augmented SS

$$\tilde{x}(T_s) = \left(\prod_{i=n_i}^{1} e^{\hat{A}_i t_i}\right)\tilde{x}(0)$$

n_i = number of switching intervals in one period

$$\tilde{X}_{ss} \rightarrow \mathrm{null}\left(I - \prod_{i=n_i}^{1} e^{\hat{A}_i t_i}\right)$$

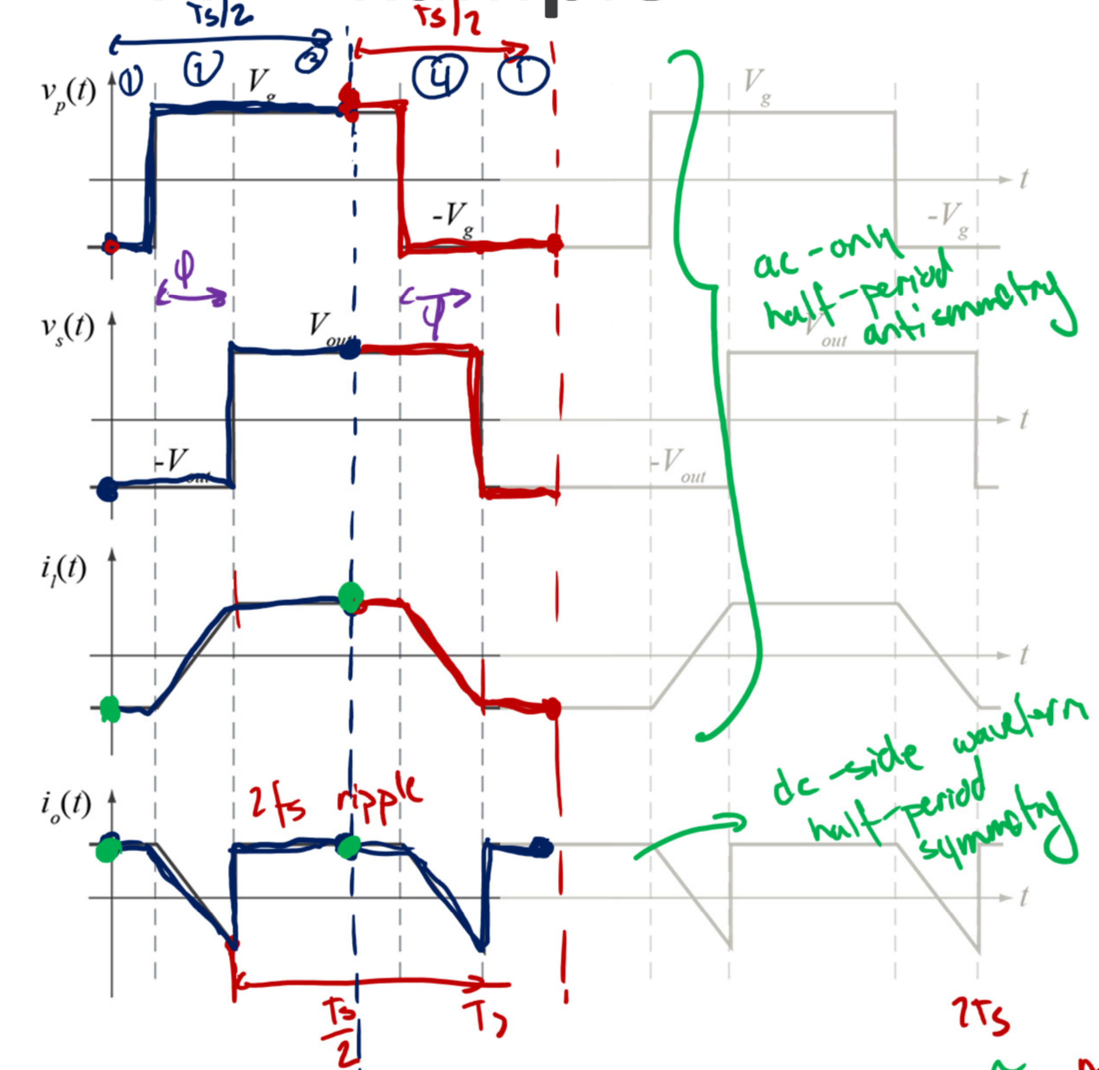
using symmetry arguments:

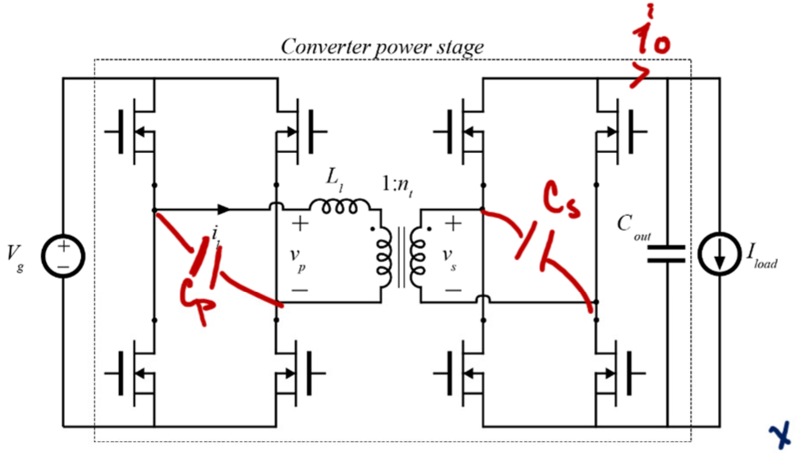
$$\tilde{x}(T_s/2) = \left(I_{HC}\prod_{i=\frac{n_i}{2}}^{1} e^{\hat{A}_i t_i}\right)\tilde{x}(0)$$

$$x(t) = \begin{bmatrix} x_{DC} \\ x_{AC} \end{bmatrix} \rightarrow I_{HC} = \begin{bmatrix} I & \emptyset \\ \emptyset & -I \end{bmatrix}$$

$$\tilde{X}_{ss} \rightarrow \mathrm{null}\left(I - I_{HC}\prod_{i=\frac{n_i}{2}}^{1} e^{\hat{A}_i t_i}\right)$$

DAB Example





$$x = \begin{bmatrix} v_p \\ v_s \\ i_L \\ v_{out} \end{bmatrix}$$

for this DAB

w/out symmetry

$$\Phi = e^{\tilde{A}_4 t_4} e^{\hat{A}_3 t_3} e^{\tilde{A}_2 t_2} e^{\tilde{A}_1 t_1}$$

$$x(T_s) = \Phi\, x(0)$$

$$X_{ss} \rightarrow \text{null}(I - \Phi)$$

half-cycle symmetry

$$\Phi_H = e^{\tilde{A}_2 t_2} e^{\tilde{A}_1 t_1}, \quad I_{Hc} = \begin{array}{c} \begin{array}{ccccc} v_p & v_s & i_L & v_o & B \end{array} \\ \begin{bmatrix} -1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \end{array}$$

$$X_{ss} \rightarrow \text{null}(I - I_{Hc}\Phi_H)$$

$$\tilde{A}_i = \begin{array}{c c} & \begin{array}{cc} n_s & 1 \end{array} \\ \begin{array}{c} n_s \\ 1 \end{array} & \begin{bmatrix} A_i & B_u \\ 0 & 0 \end{bmatrix} \end{array}$$

Note: this implies control possible about $2 \cdot f_s$

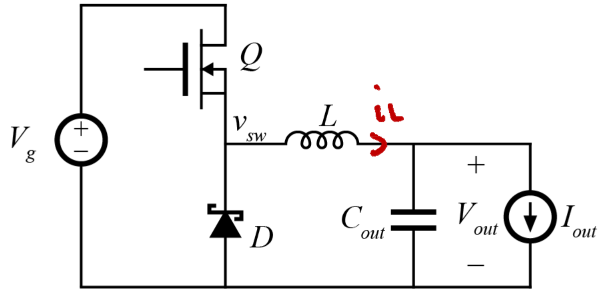
State-dependent Switching

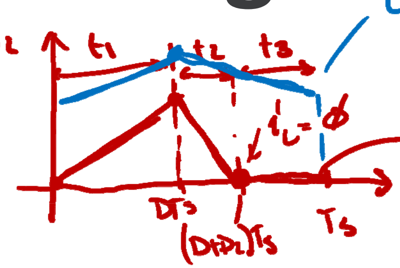
$t_1 \to$ defined by external modulation signal

ccm $\quad t_2 = T_s - t_1$

$$x(T_s) = e^{A_2 t_2} e^{A_1 t_1} x(0)$$

DCM Buck





DCM: $t_1 \to$ same

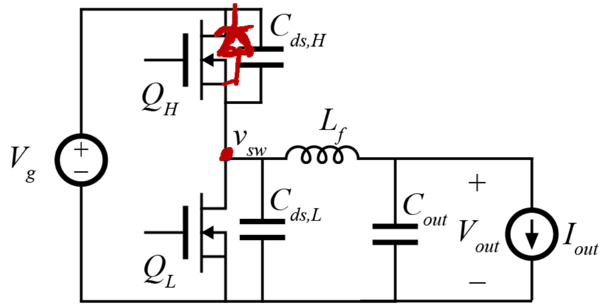
$t_2 \to$ defined by $i_L(t) > \phi$

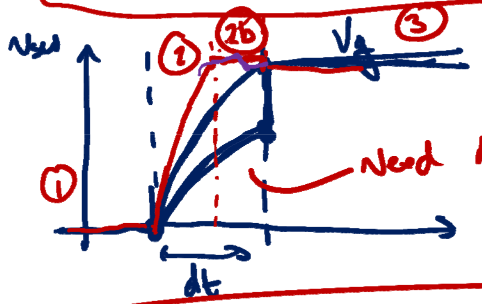
$t_3 \to T_s - t_1 - t_2$

$$x(T_s) = e^{\tilde{A}_3 t_3} e^{\tilde{A}_2 t_2^*} e^{A_1 t_1} x(0)$$

Neither · Diode ON · FET ON

ZVS Buck

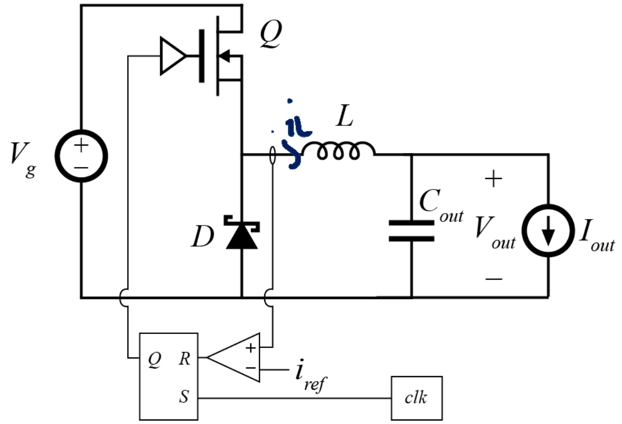


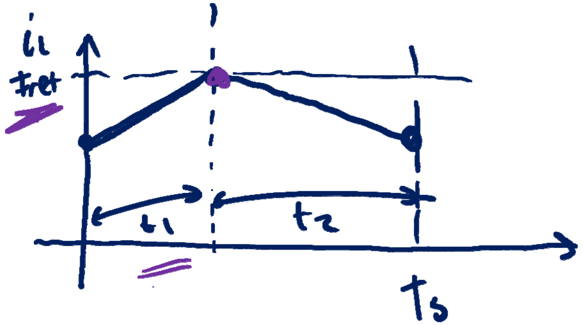


t_{2b}

Need Add'l interval if we overshoot ZVS

CPM Buck





$t_1 \to$ whatever time it takes to get $i_L(t) = I_{ref}$

$t_2 \to T_s - t_1$