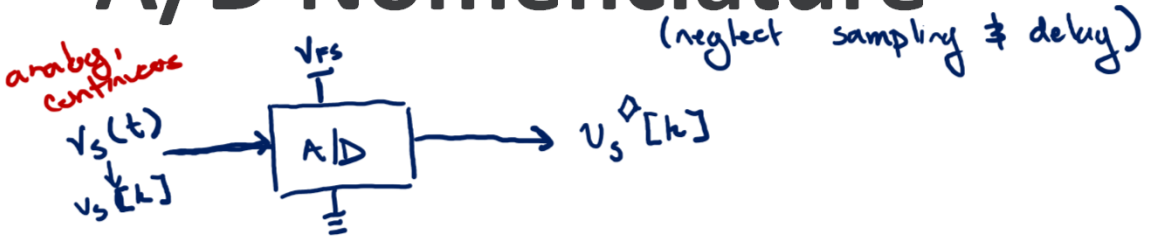
A/D Nomenclature



(neglect sampling & delay)

$Q_{A/D}[\cdot]$ → A/D Quantization Characteristic

when not saturated

$$Q_{A/D}[\cdot] \equiv q_{v_s}^{A/D} \cdot \tilde{v}_s[k] \equiv Q_{A/D}[v_s[k]]$$

$\wedge_{A/D}$ = # of bits of A/D

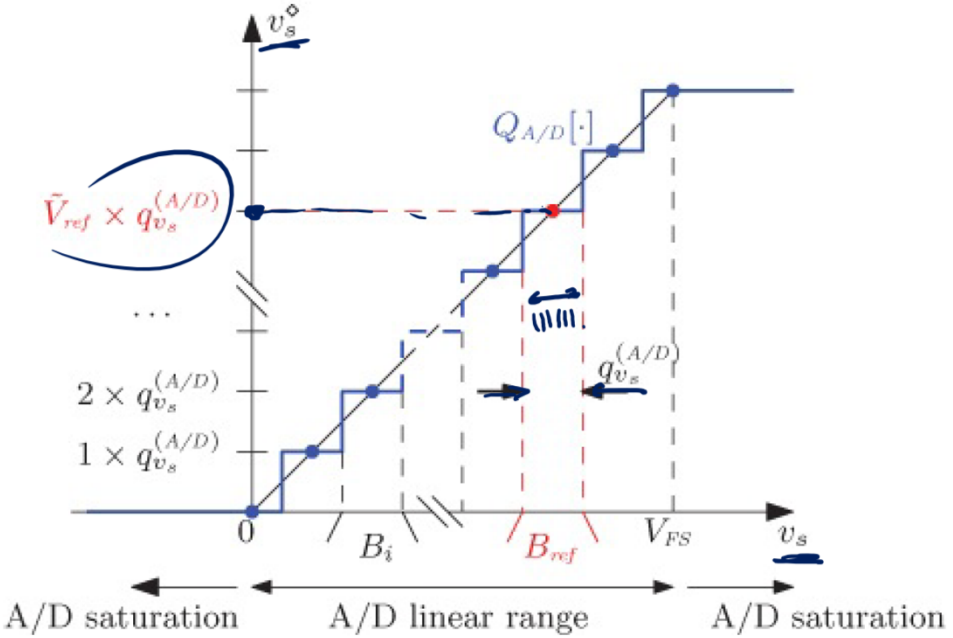
$q_{v_s}^{A/D}$ = quantization resolution of v_s due to A/D [volts/bin]

common case $q_{v_s}^{A/D} = \frac{V_{FS}}{2^{\wedge_{A/D}}}$

$\tilde{v}_s[k]$ = integer number representing A/D bin
(actual binary encoded number out of A/D)

$v_s^{\diamond}[k]$ = equivalent quantized value [volts]

$$v_s^{\diamond}[k] = \tilde{v}_s[k] \cdot q_{v_s}^{A/D}$$



$\tilde{v}_s[k] \in \mathbb{Z}^+$ $\quad 0 \leq \tilde{v}_s[k] \leq 2^{\wedge_{A/D}}$

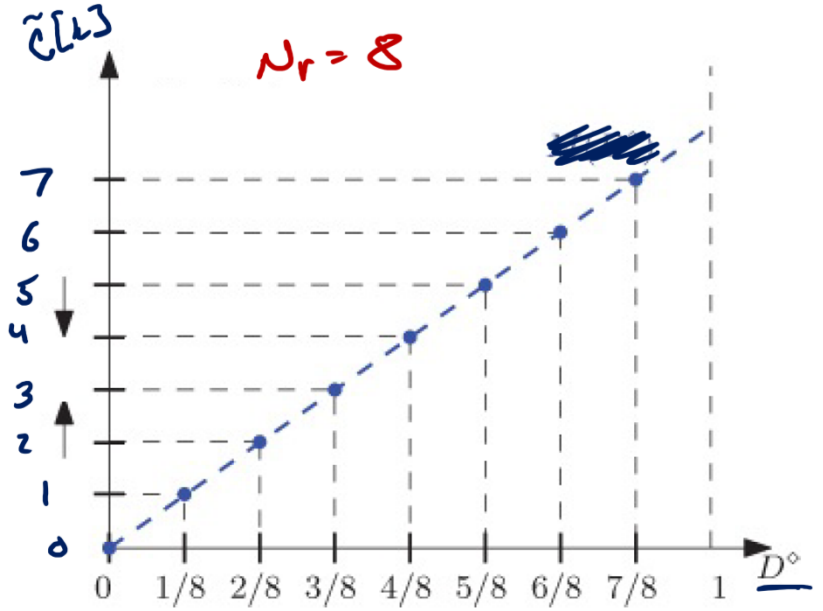
PWM Nomenclature

PWM clock is T_{clk}

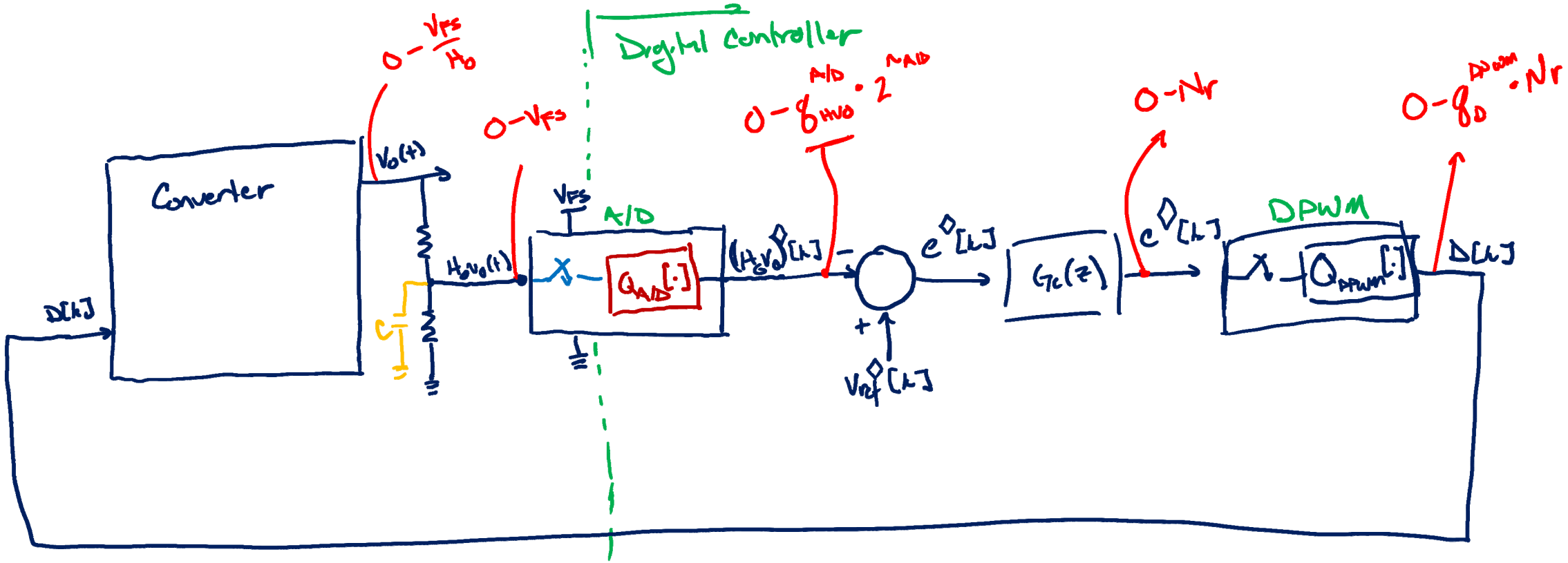
$$T_{clk} = \frac{T_s}{N_r}$$

N_r = number of clocks per period T_s
& maximum value of PWM counter (sawtooth)

$$f_{\circ}^{PWM} = \frac{1}{N_r}$$



Digital Loop Resolution Limits



Assume $G_c(z)$ has an integral component

steady-state occurs when $e^{\Diamond}[k] = 0$

PWM Quantization

$N_r = 8$

In steady-state, before any quantization

$$M(D) = \frac{V_o}{V_g} = D \text{ for Buck} = \frac{1}{1-D} \text{ for Boost}$$

with DPWM quantization

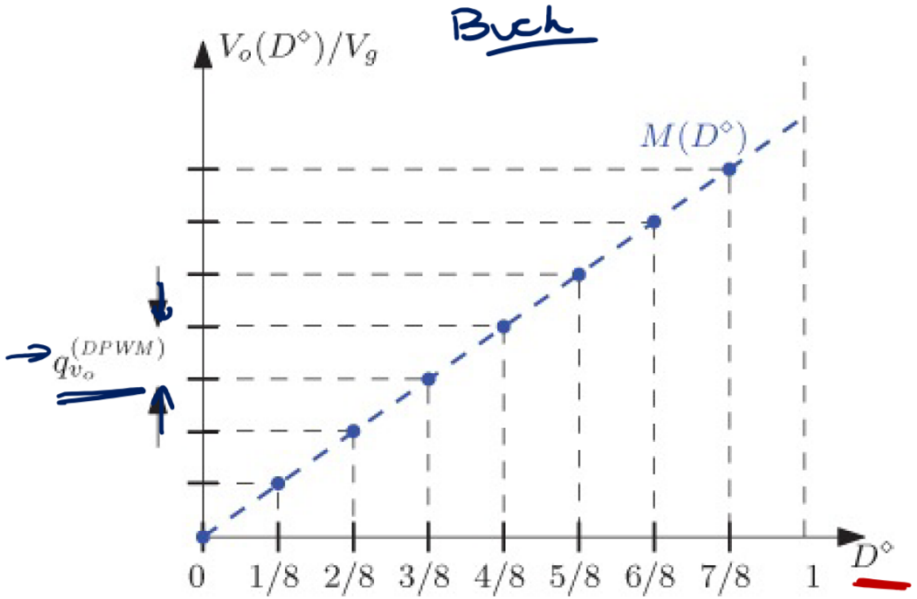
$$M(D^\diamond) = \frac{V_o(D^\diamond)}{V_g}$$

$$V_o(D^\diamond) = M(D^\diamond) V_g$$

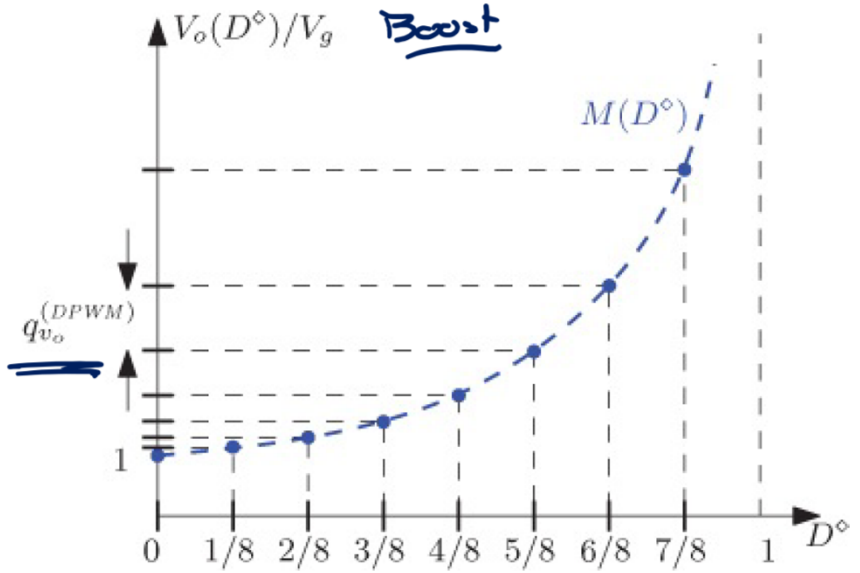
In general, DPWM results in a quantization of steady-state output voltage

$$q_{v_o}^{DPWM} = \left.\frac{\partial M}{\partial D}\right|_{D^\diamond} \cdot V_g \cdot \frac{1}{N_r}$$

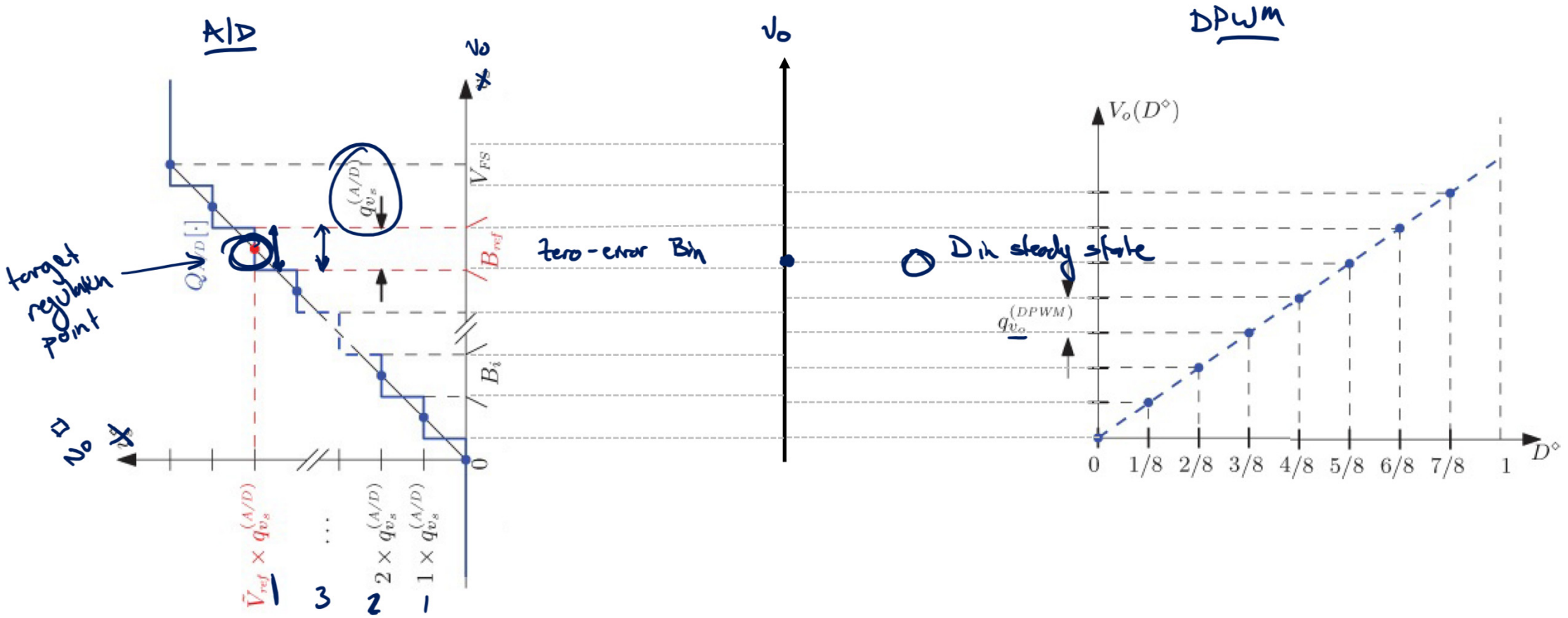
Buck



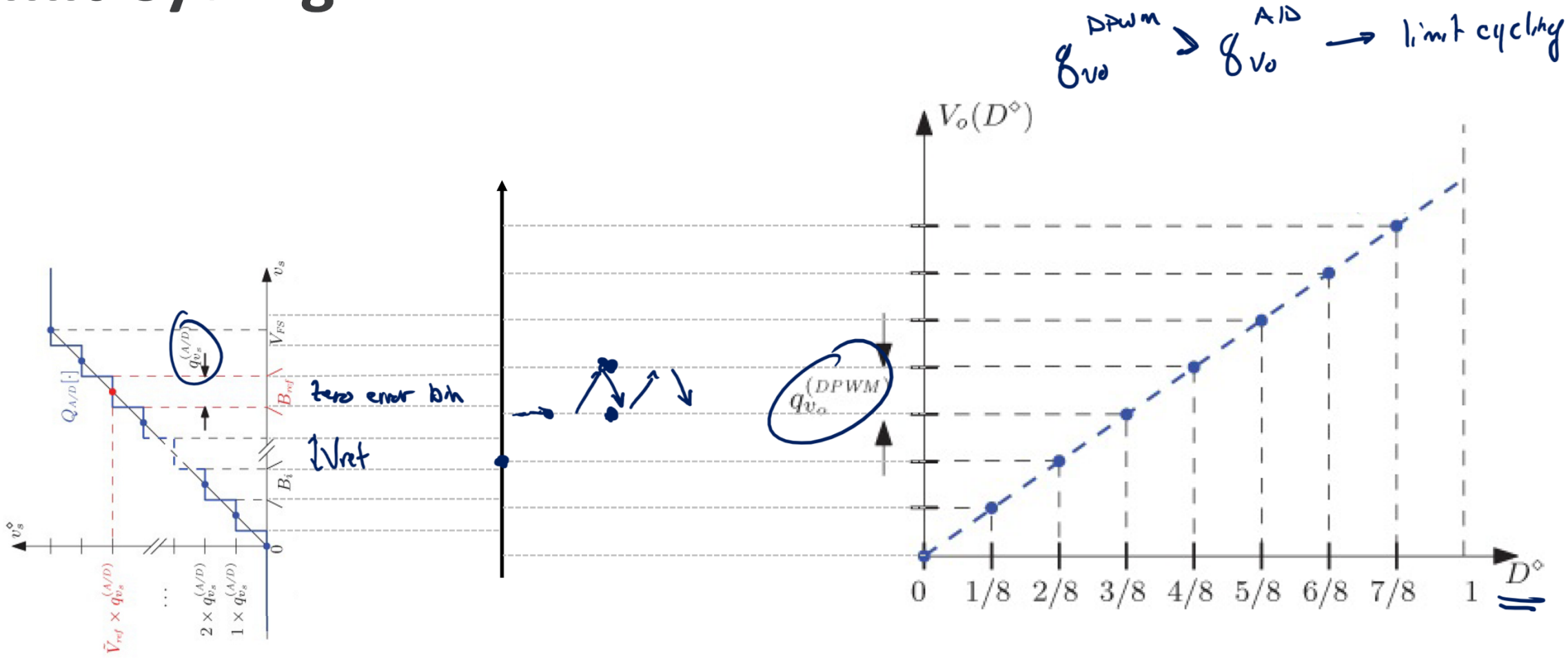
Boost



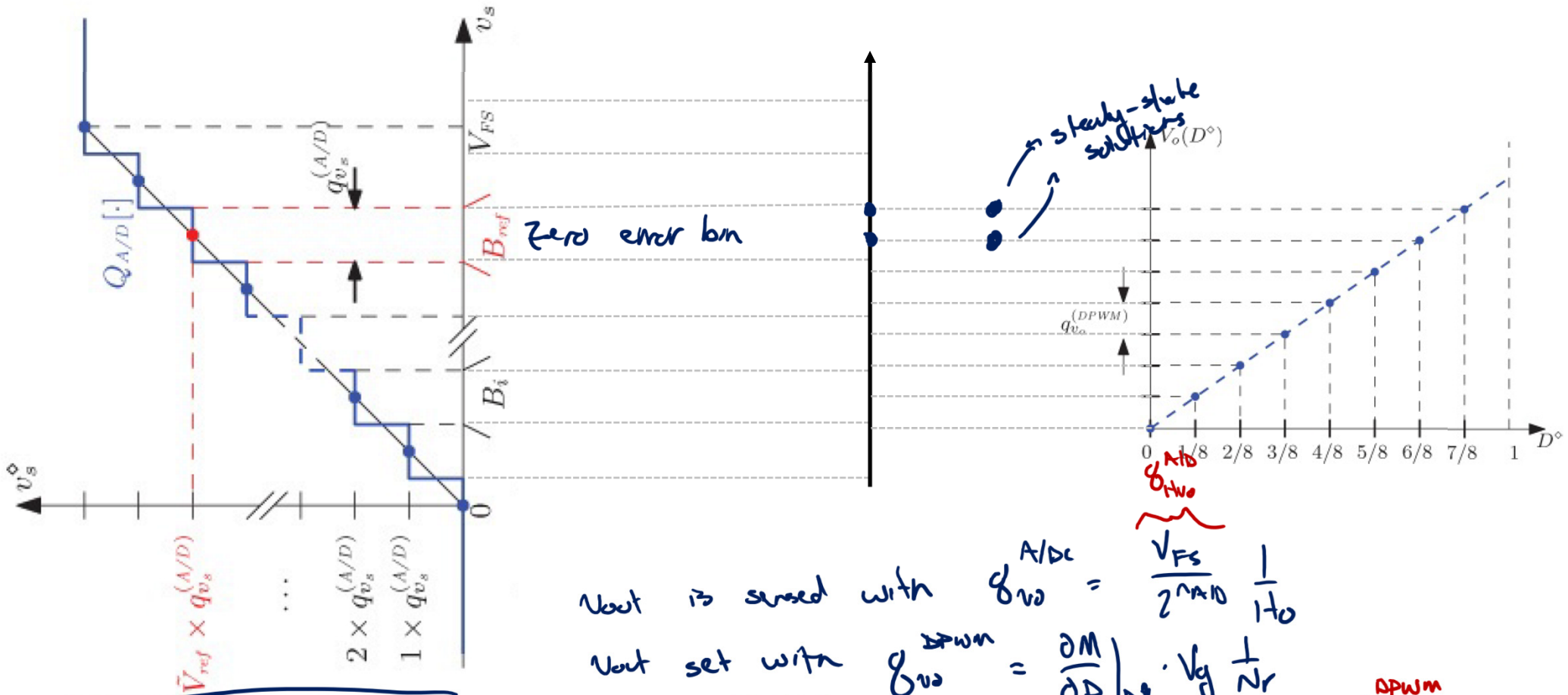
Limit Cycling



Limit Cycling



Limit Cycling

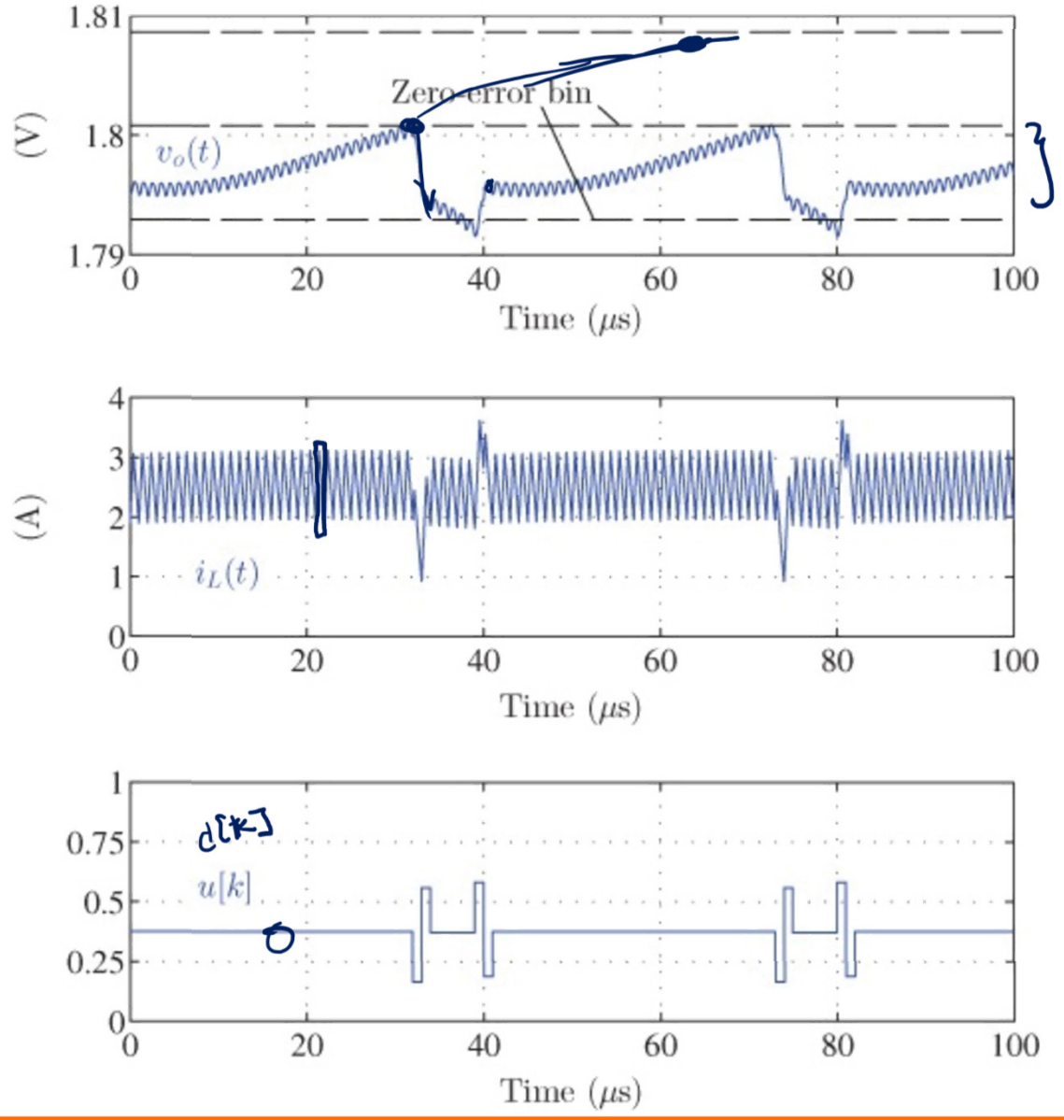


V_{out} is sensed with $q_{v_o}^{A/Dc} = \frac{V_{FS}}{2^{nA/D}} \frac{1}{H_0}$

V_{out} set with $q_{v_o}^{DPWM} = \frac{\partial M}{\partial D}\Big|_{D^\diamond} \cdot V_g \frac{1}{N_T} \rightarrow q_D^{DPWM}$

if $q_{v_o}^{DPWM} < q_{v_o}^{A/D}$ → No limit cycling

Example Waveforms



low frequency oscillation between adjacent duty cycle bins

Fig 5.10