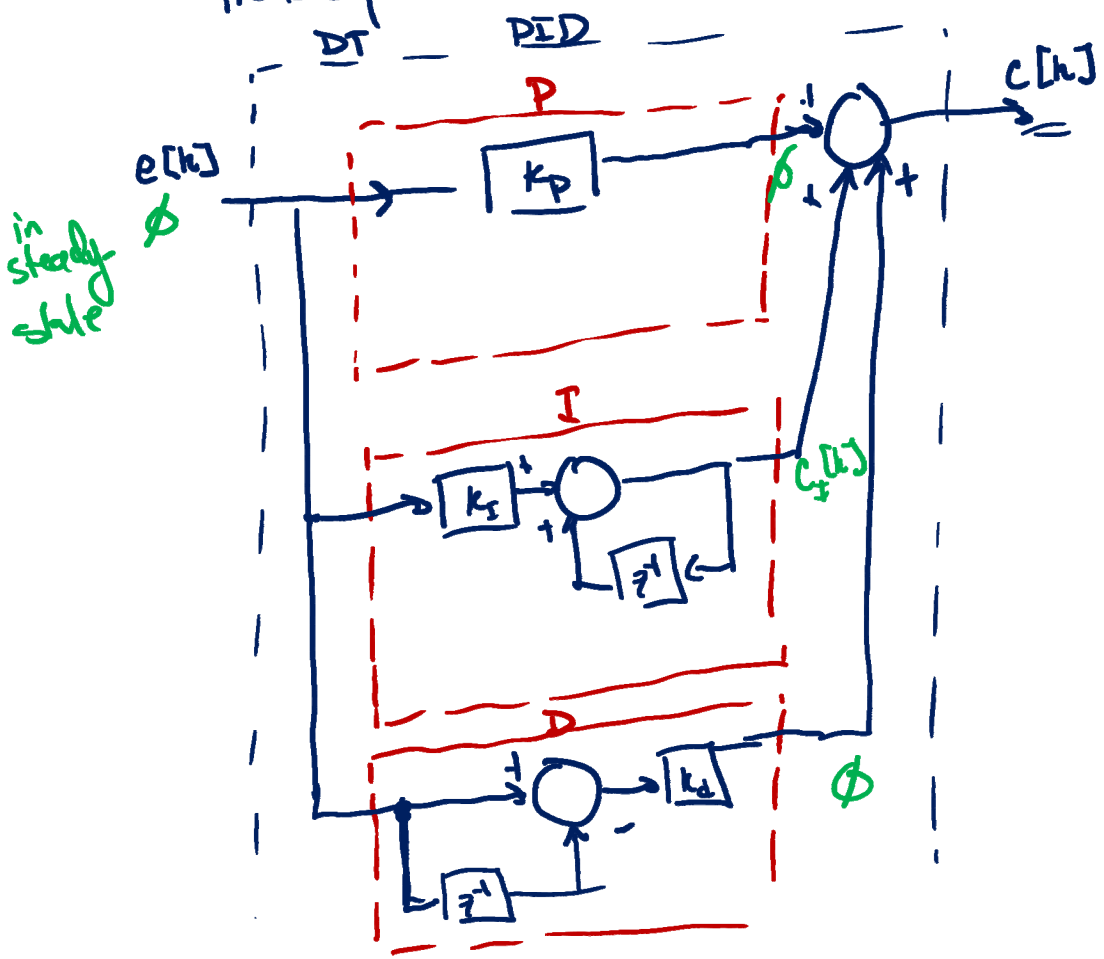
Final Project

- Select a dc-dc converter and application, design a closed-loop digital controller
- Detail
  - Converter Design (brief, may leverage midterm)
  - Target performance (both large and small-signal)
    - should be aggressive
  - Design and final implementation
- Design must include
  - Realistic ADC/DPWM models (sampling, delay, quantization)
  - At least one additional nonlinearity (Nonlinear controller, GSS, etc.)
  - At least one technique from an IEEE publication not directly discussed in class
- Validation must include
  - Direct comparison between small-signal prediction and large-signal performance
  - Testing over conditions motivating valid operation in a realistic use case
- Apply techniques from class
- Should result in prototype-ready paper design
- Validate through simulation (PLECs/Simulink)
- Presentations Nov 25th
- Report Due December 2nd
  - Narrative of analysis and results
  - Clear but minimally “wordy”
  - IEEE format (though incomplete content w.r.t. review and explanation)

Integral Gain Limitations

Previously assumed $G_c(z)$ had an integral component



In steady-state, only integral component dictates output

$$C[k] = f(C_I[k])$$

In steady-state

$$C[k] = k_I \underbrace{\sum_{n=-\infty}^{k} e[n]}_{\text{some integer}}$$

If $k_I > 1$, some values of C[k] are inaccessible

if $k_I \leq 1$, full DPWM resolution accessible in steady-state

Limit Cycling Conclusions

Conditions on g_{vo}^{DPWM} -vs.- $g_{vo}^{A/D}$ & on k_I are neither necessary nor sufficient to guarantee no limit cycling

Not necessary → some bits have a steady-state DC solution even if $g_{vo}^{DPWM} > g_{vo}^{A/D}$; just not all bits will.

Not sufficient → dynamic effects may still result in limit cycling

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Does it Matter?

If $n_{A/D}$ & N_r are very large, we may not care

What can be done?

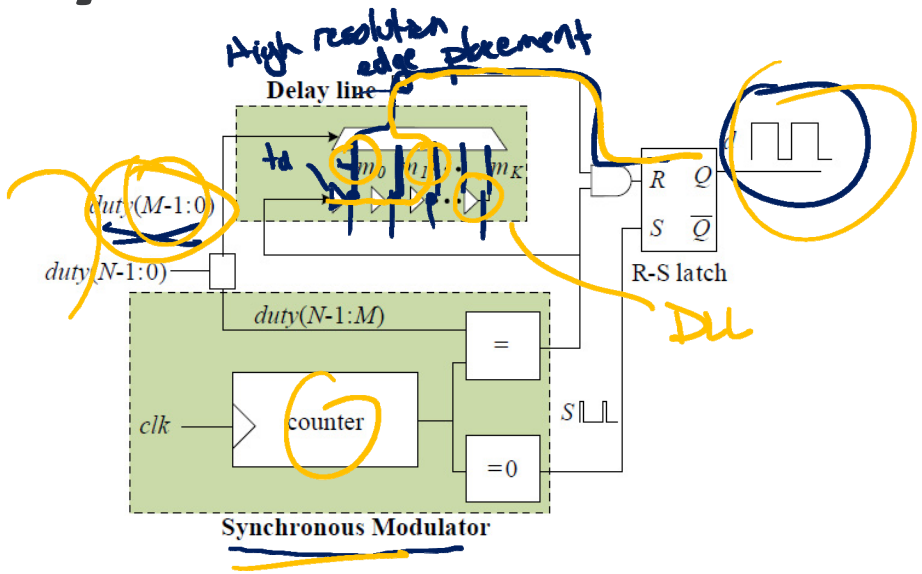
(0) Increase DPWM resolution by increasing $f_{clk} = \frac{1}{T_{clk}}$ → ↑ N_r

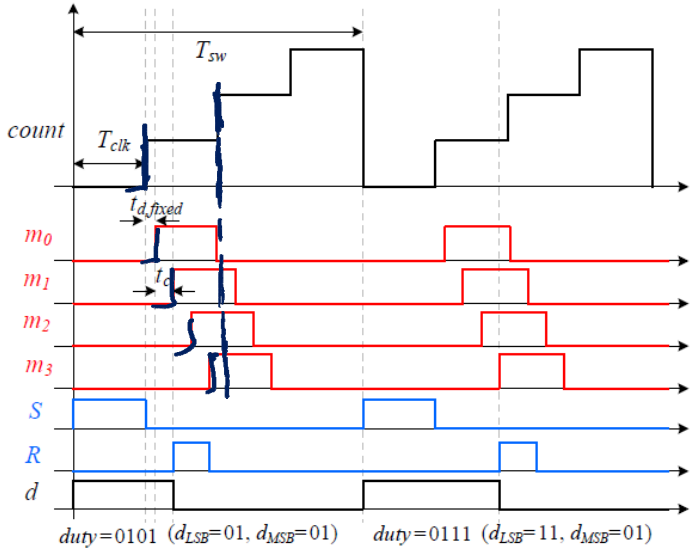
(1) Drop ADC resolution (↓ $n_{A/D}$)

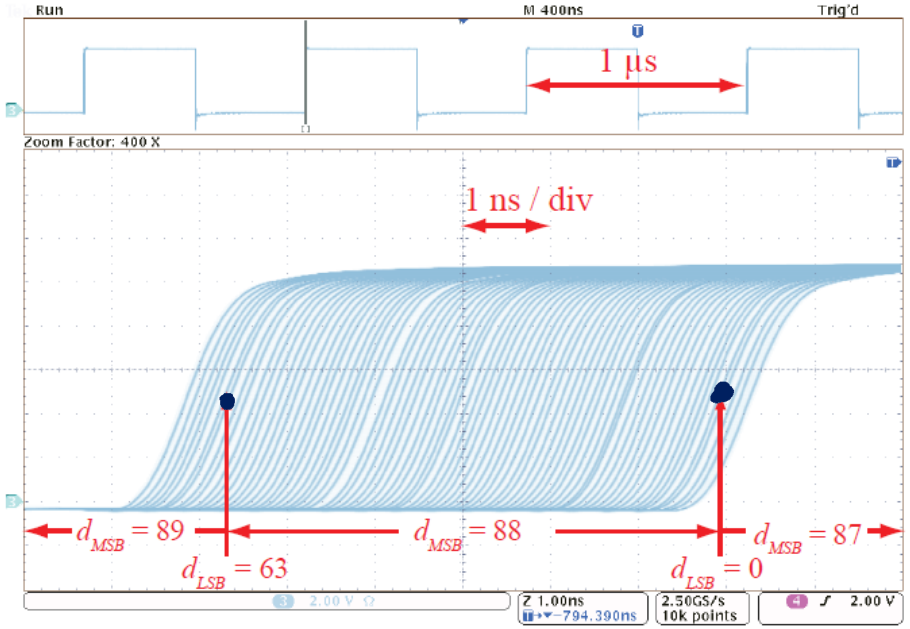
(2) Drop f_s to allow higher N_r → Requires redesign of passive elements, etc.

(3) Next couple slides on alternate DPWMs

Hybrid DPWM


Delay line
m_0 m_1 m_K
duty(M-1:0)
duty(N-1:0)
R Q
S $\overline{Q}$
R-S latch
duty(N-1:M)
=
clk
counter
=0
S
Synchronous Modulator


T_{sw}
count
T_{clk}
$t_{d,fixed}$
m_0
m_1
m_2
m_3
S
R
d
duty=0101 (d_{LSB}=01, d_{MSB}=01)
duty=0111 (d_{LSB}=11, d_{MSB}=01)


Run
M 400ns
Trig'd
1 µs
Zoom Factor: 400 X
1 ns / div
d_{MSB} = 89
d_{LSB} = 63
d_{MSB} = 88
d_{MSB} = 87
d_{LSB} = 0
2.00 V
Z 1.00ns
-794.390ns
2.50GS/s
10k points
2.00 V