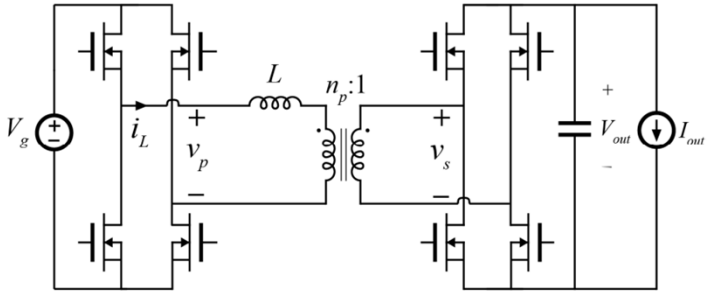
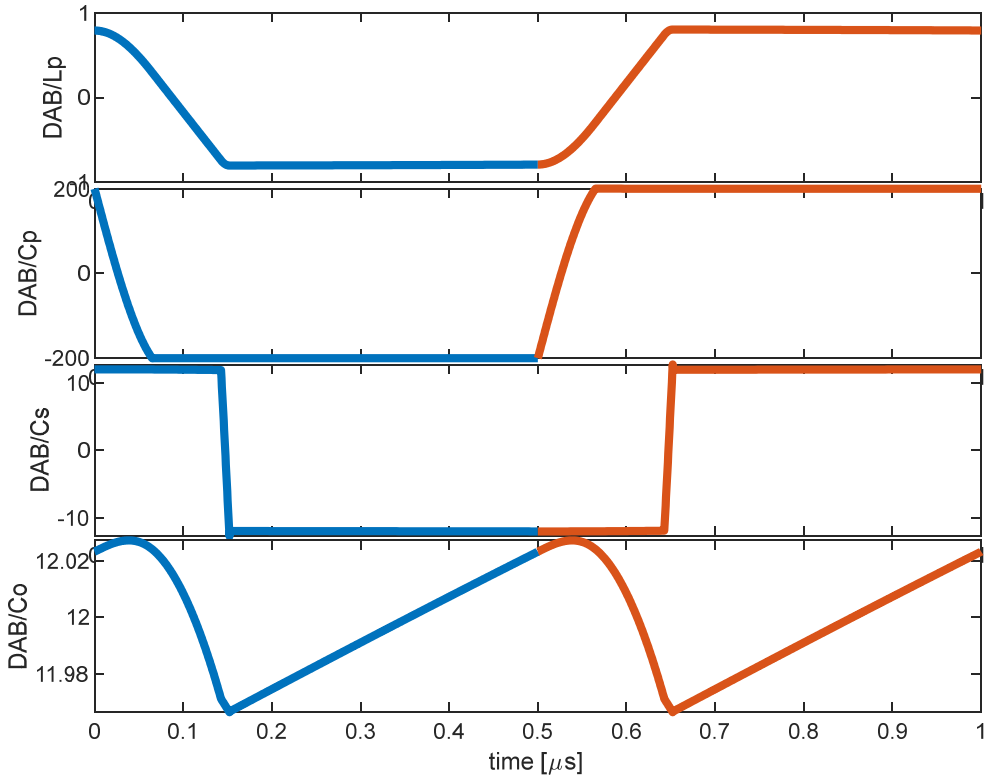
Example Design



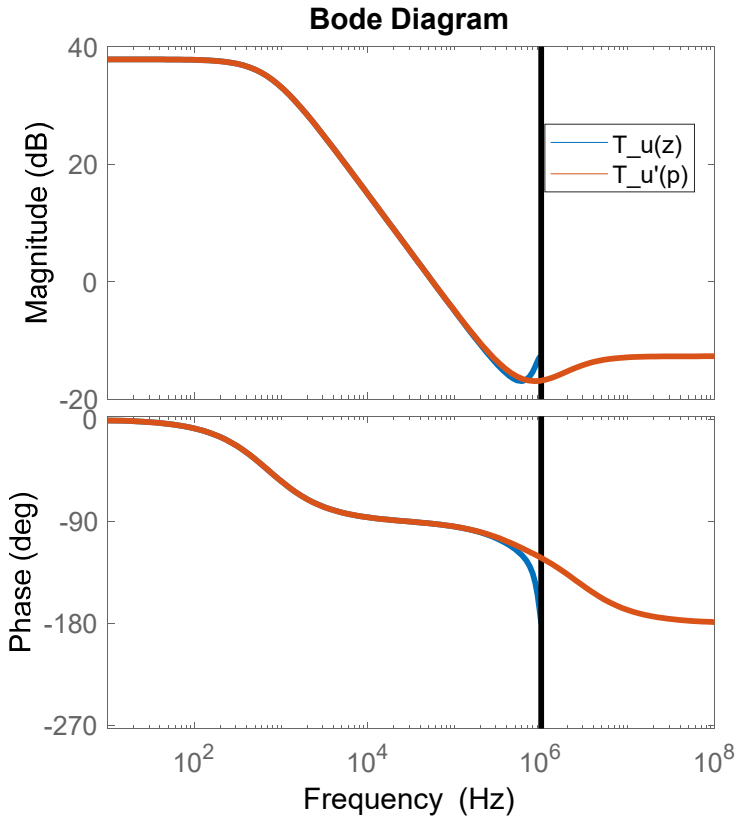


Plant Model

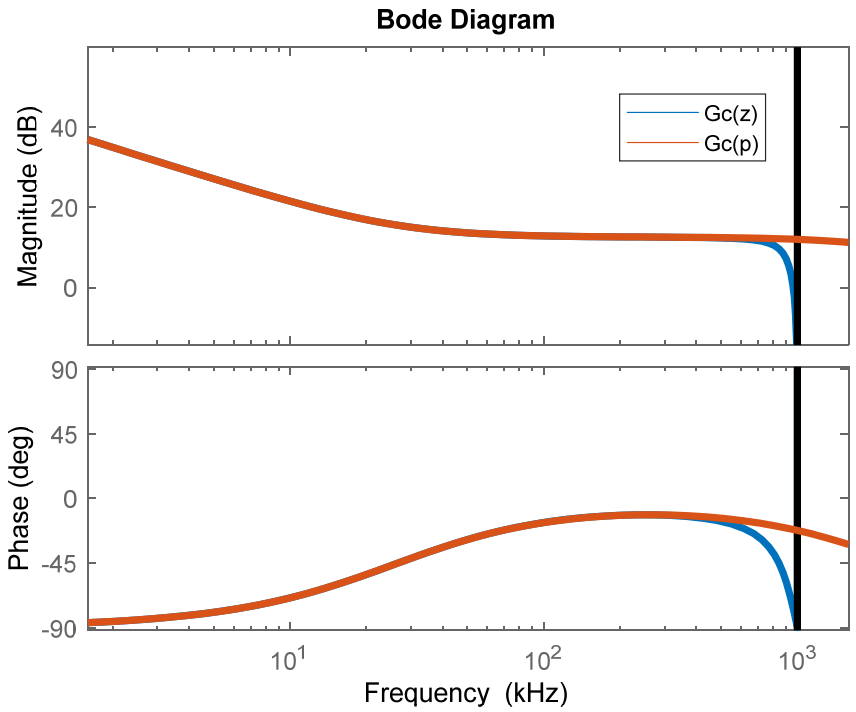
ADC and PWM Model

Loop Gain

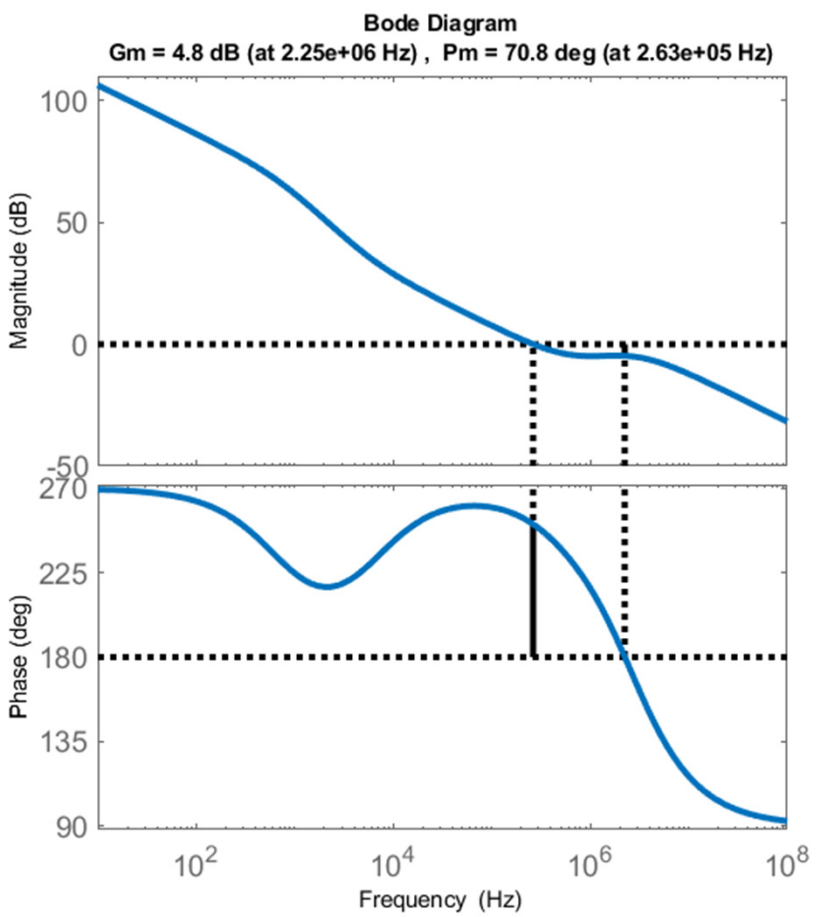
Compensator Design

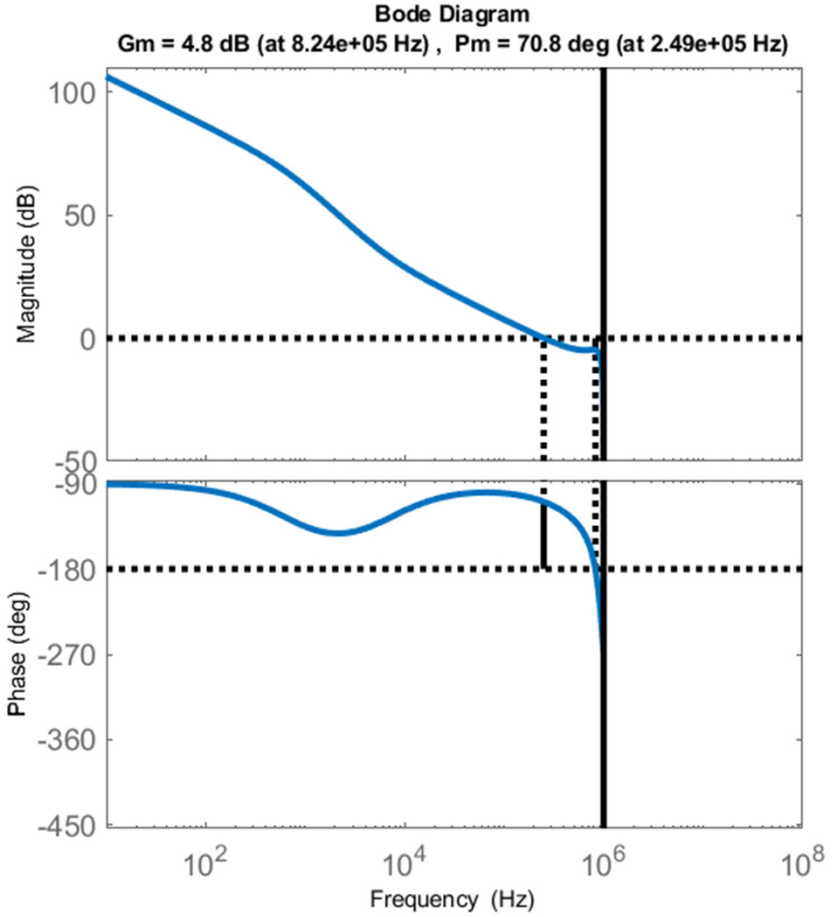


Compensator Digital Implementation

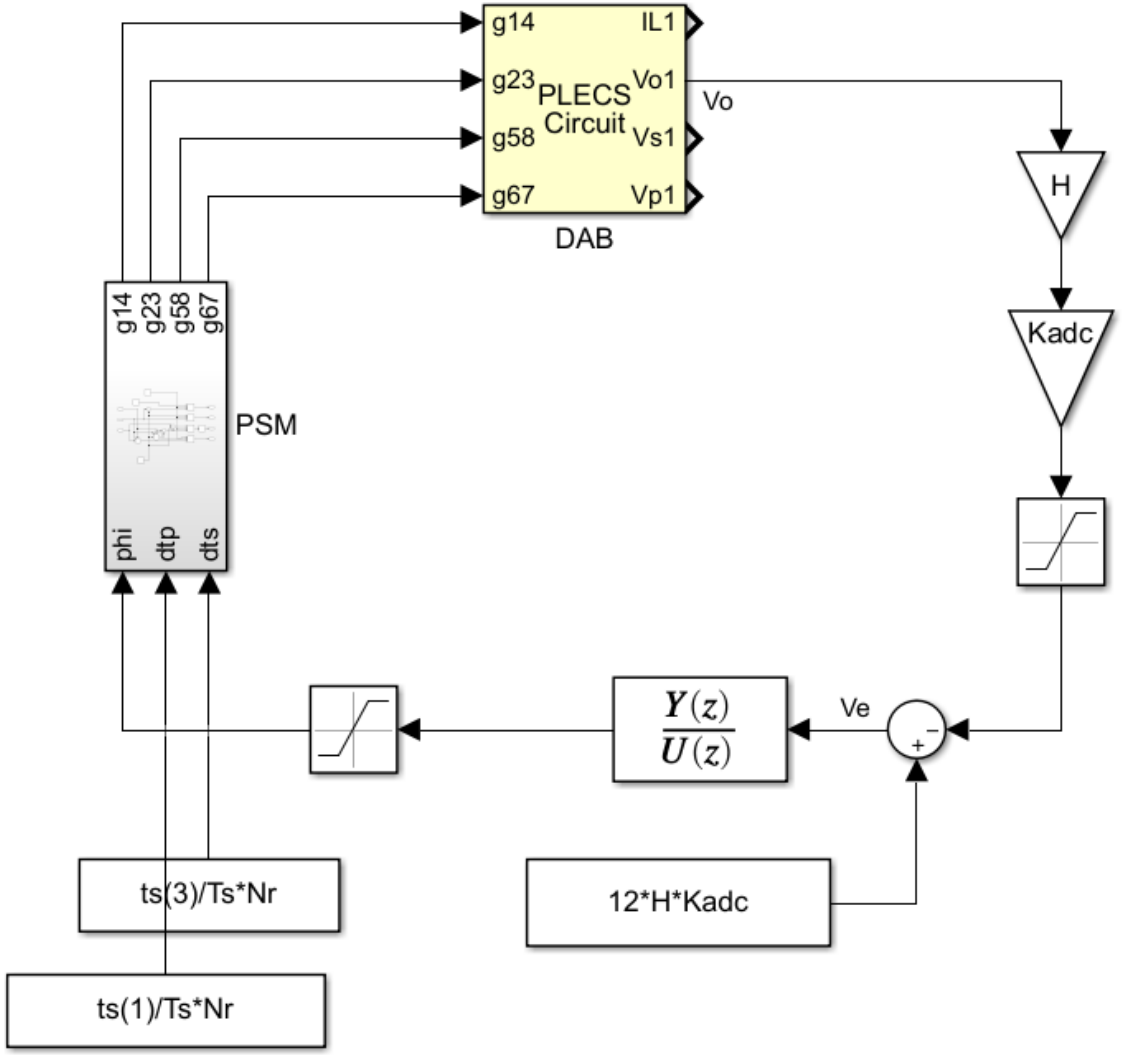


Compensated Loop Gain

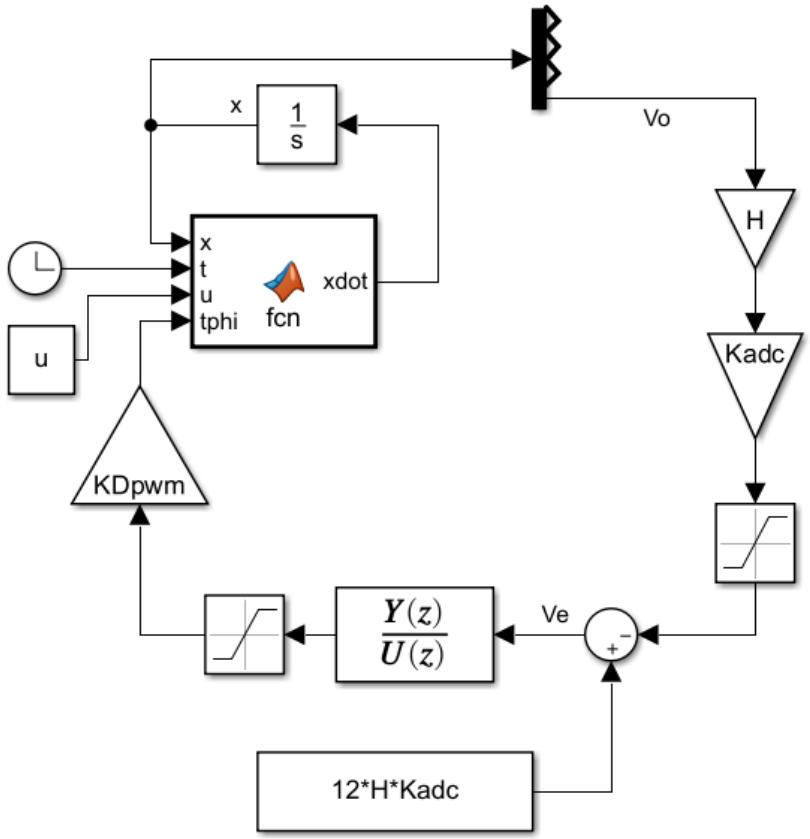




Simulation (Large Signal)

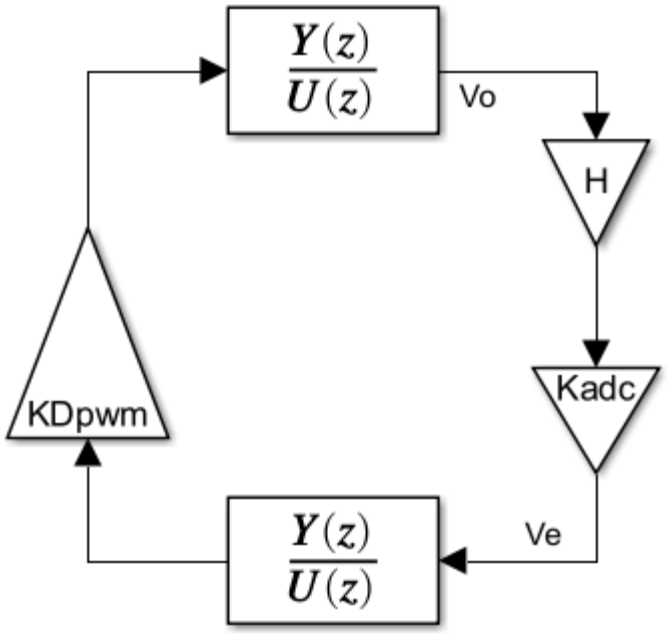


Alternative Simulation (Large Signal)

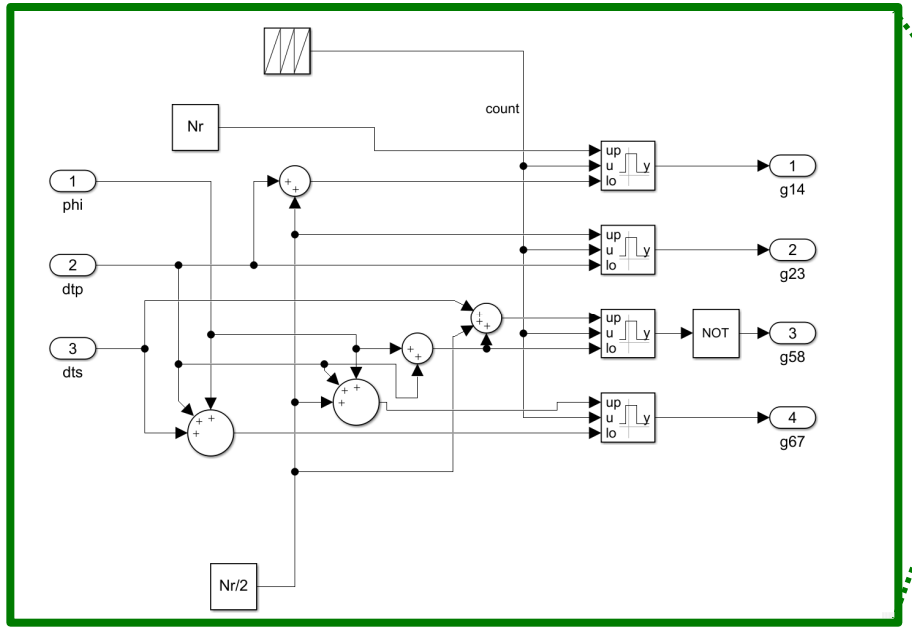


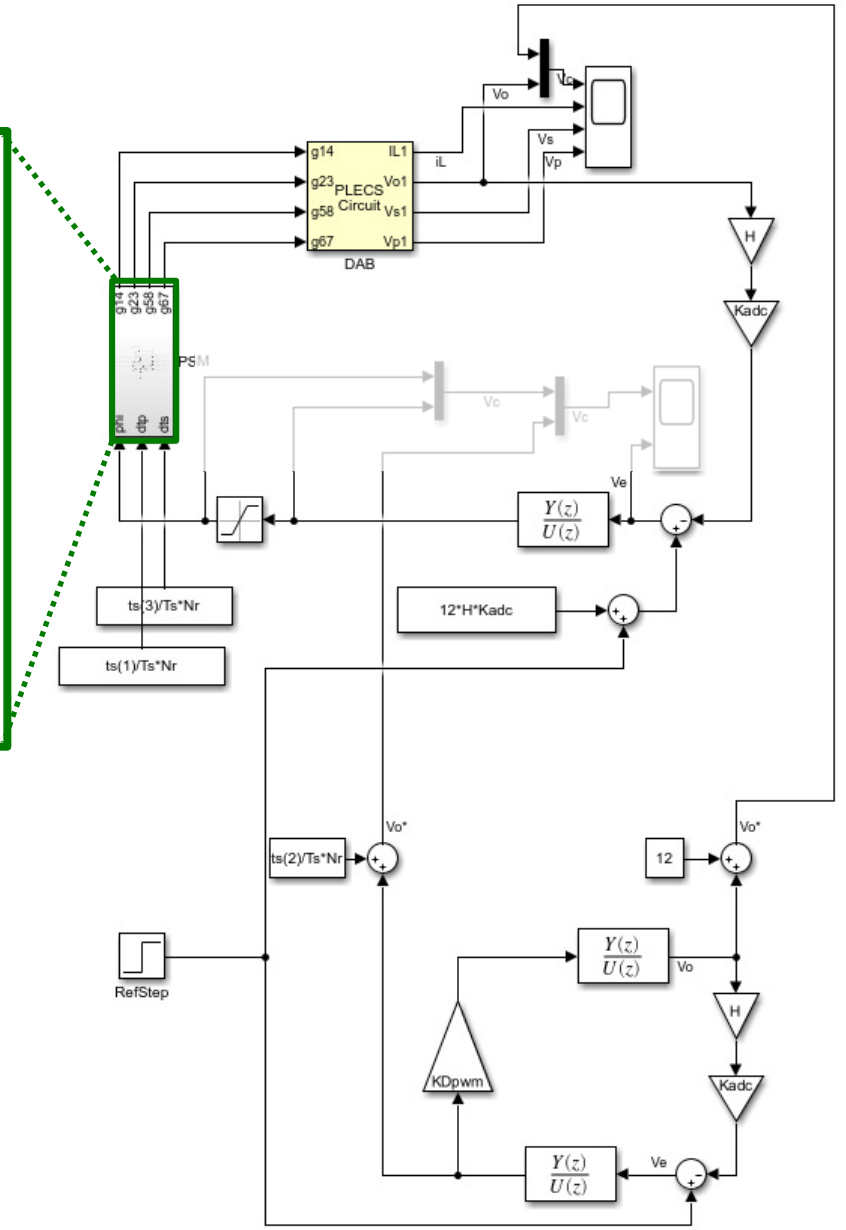

```
function xdot = fcn(x, t,
    u,tphi, A1, A2, B1, B2, Ts)

tp = mod(t,Ts);

if(tp<tphi)
    xdot = A1*x + B1*u;
else
    xdot = A2*x+B2*u;
end
```

Simulation (Small Signal)

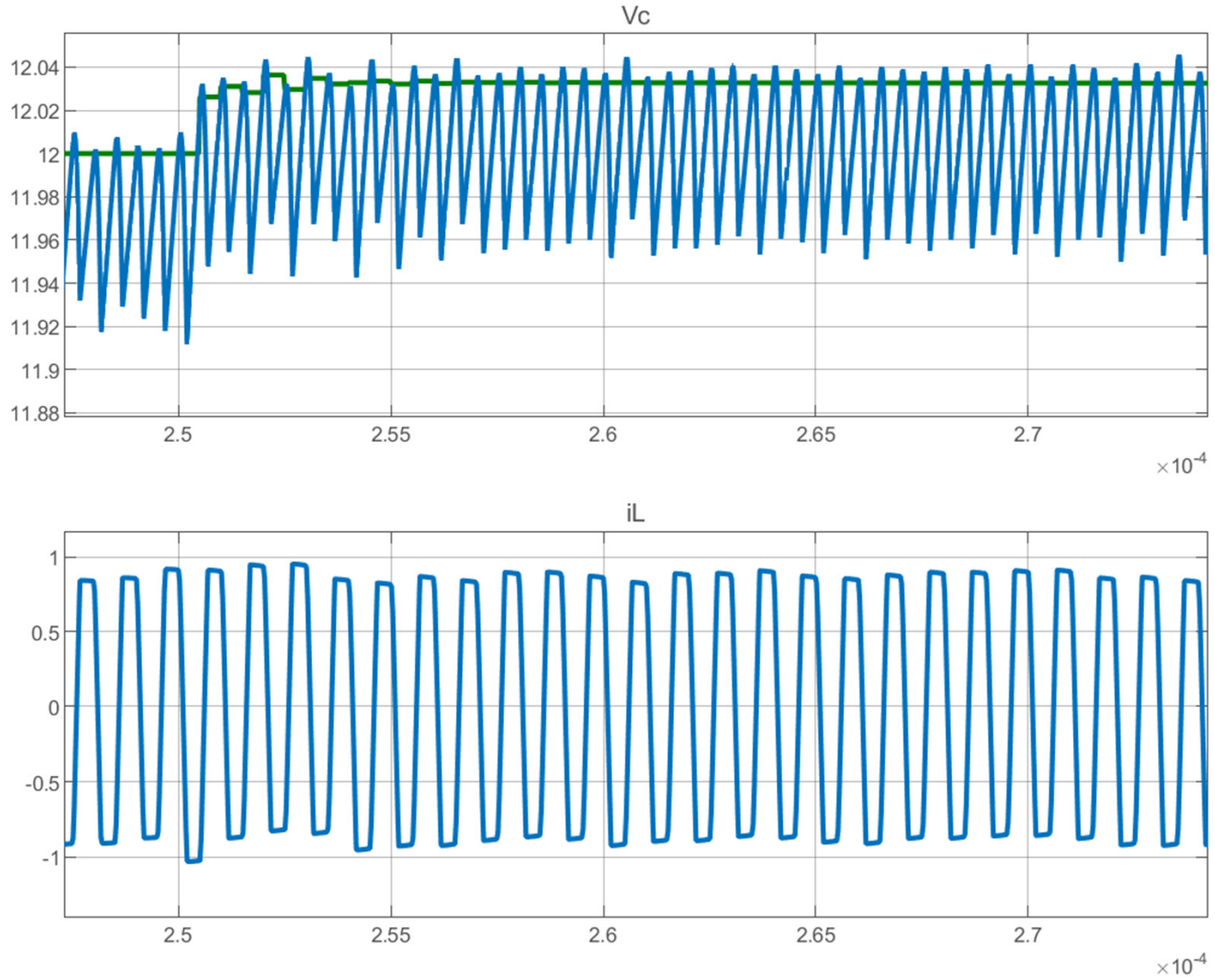


Simulation

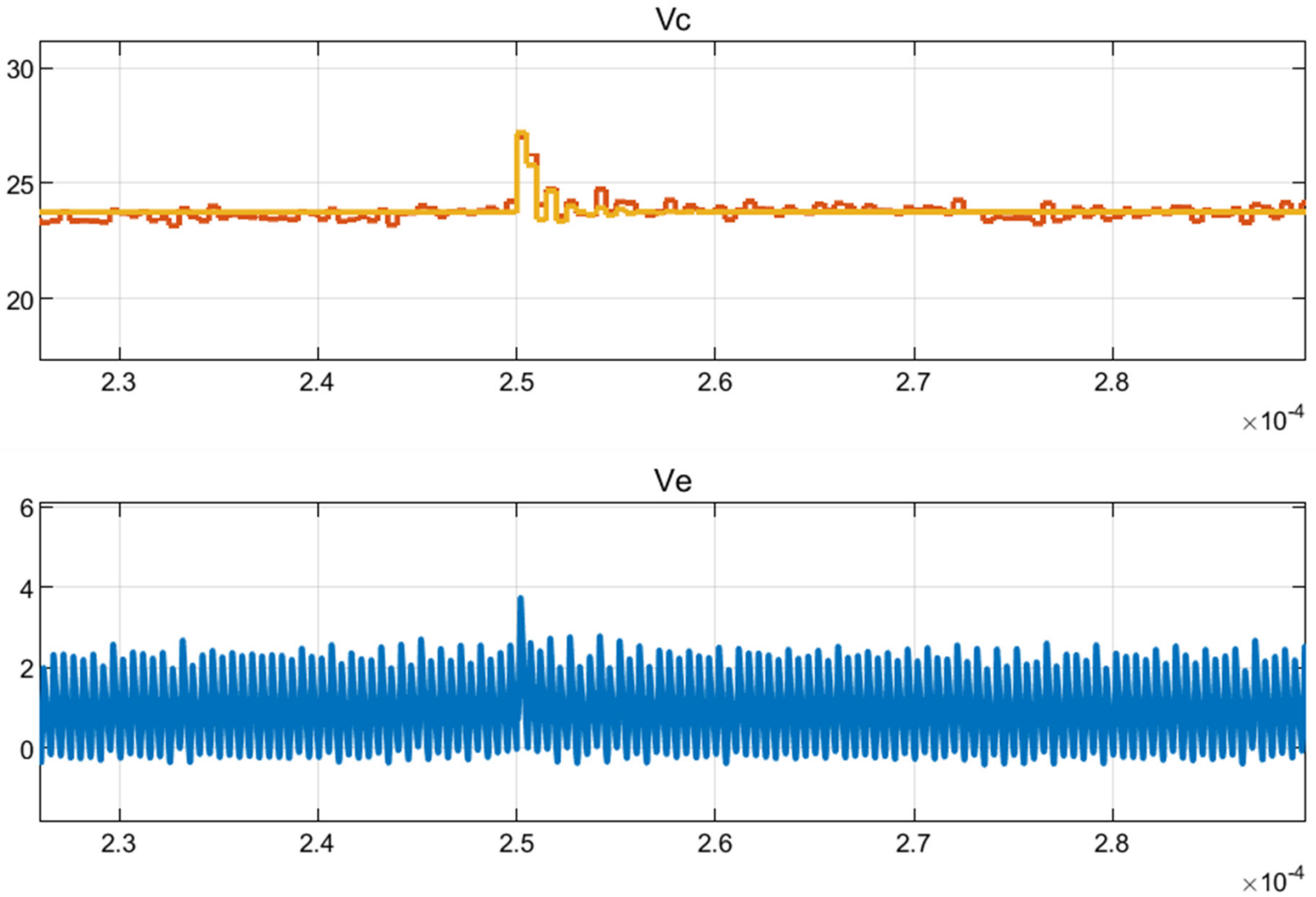

count
Nr
1
phi
2
dtp
3
dts
up
u
lo
y
NOT
1
g14
2
g23
3
g58
4
g67
Nr/2


g14
g23
g58
g67
PLECS Circuit
DAB
IL1
Vo1
Vs1
Vp1
iL
Vo
Vs
Vp
PSM
phi
dtp
dts
Vc
Ve
H
Kadc
Y(z)/U(z)
12*H*Kadc
ts(3)/Ts*Nr
ts(1)/Ts*Nr
ts(2)/Ts*Nr
Vo*
12
RefStep
KDpwm

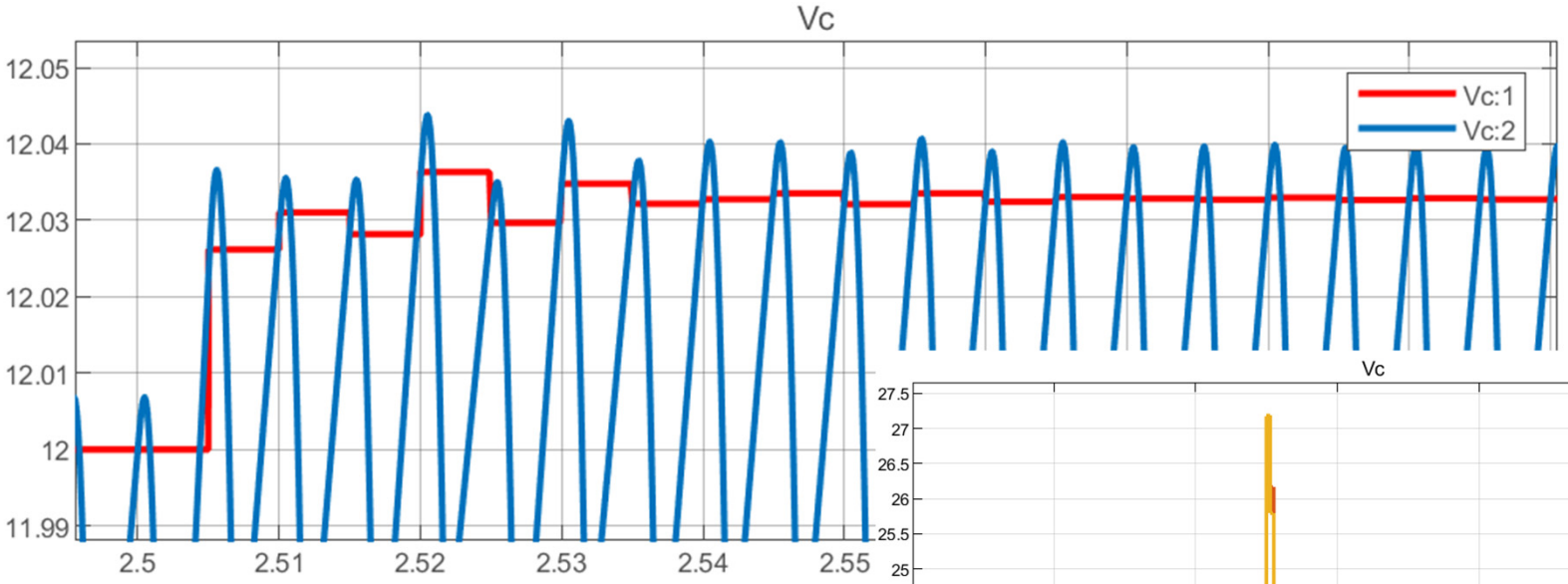
Simulation Results

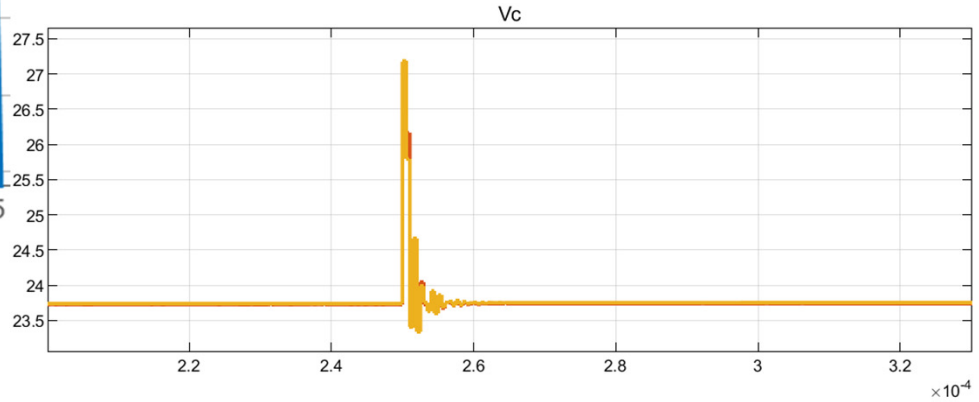


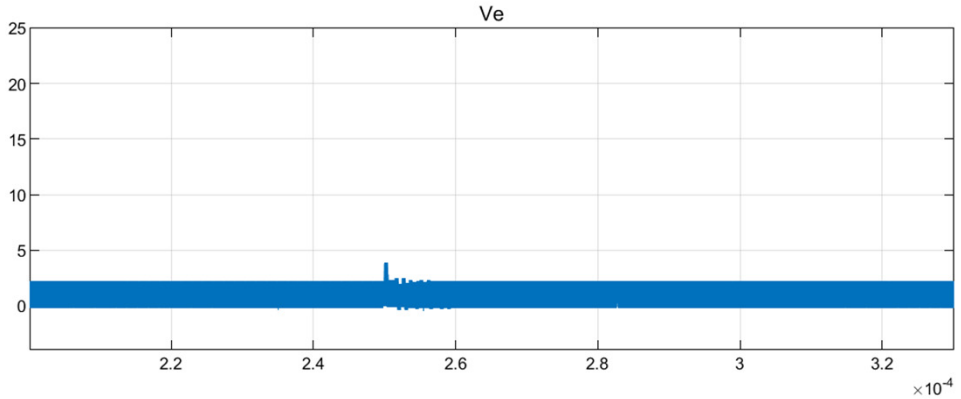
Simulation Results (cont)



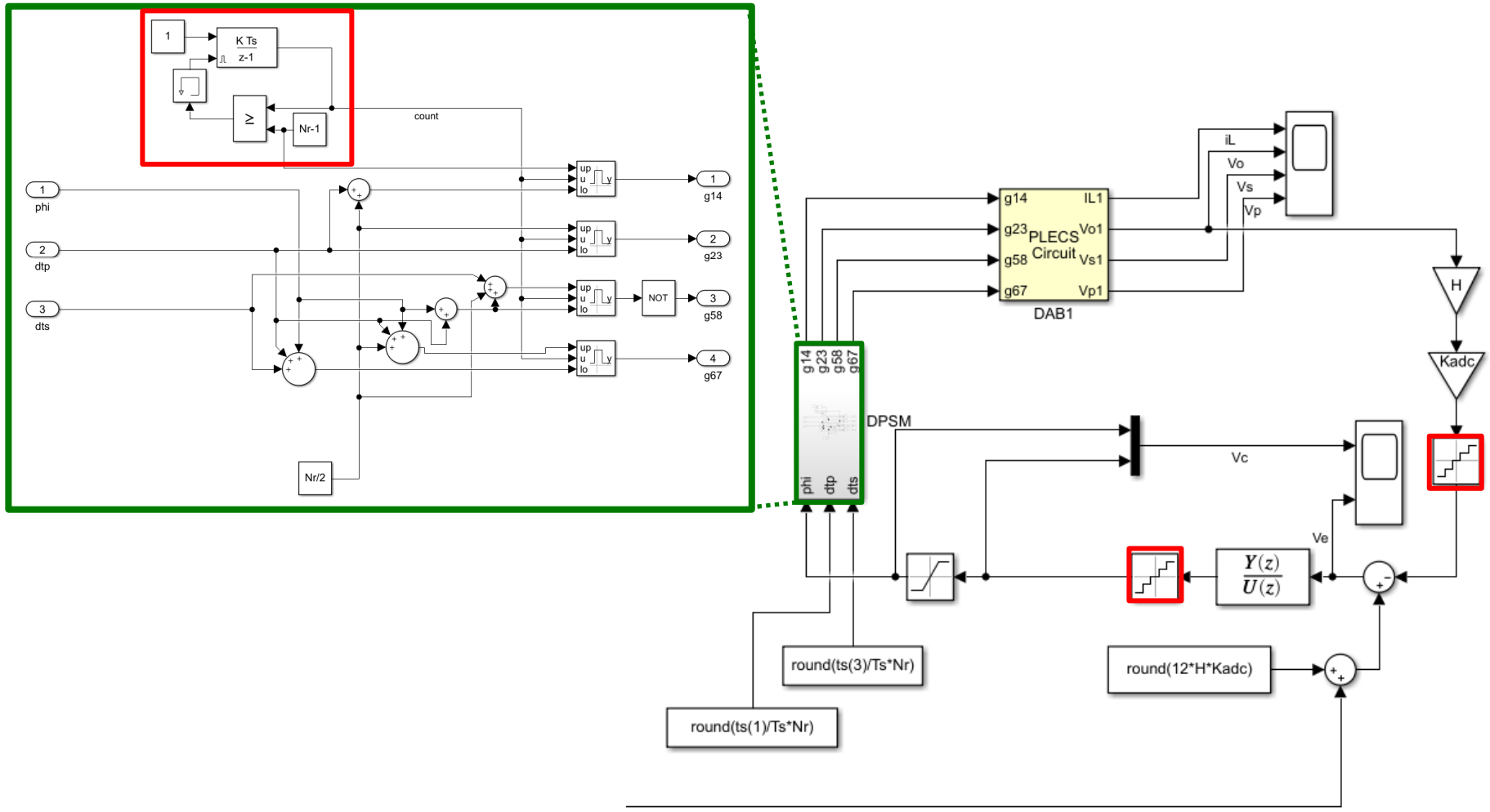
Simulation Results (max step 10ps)



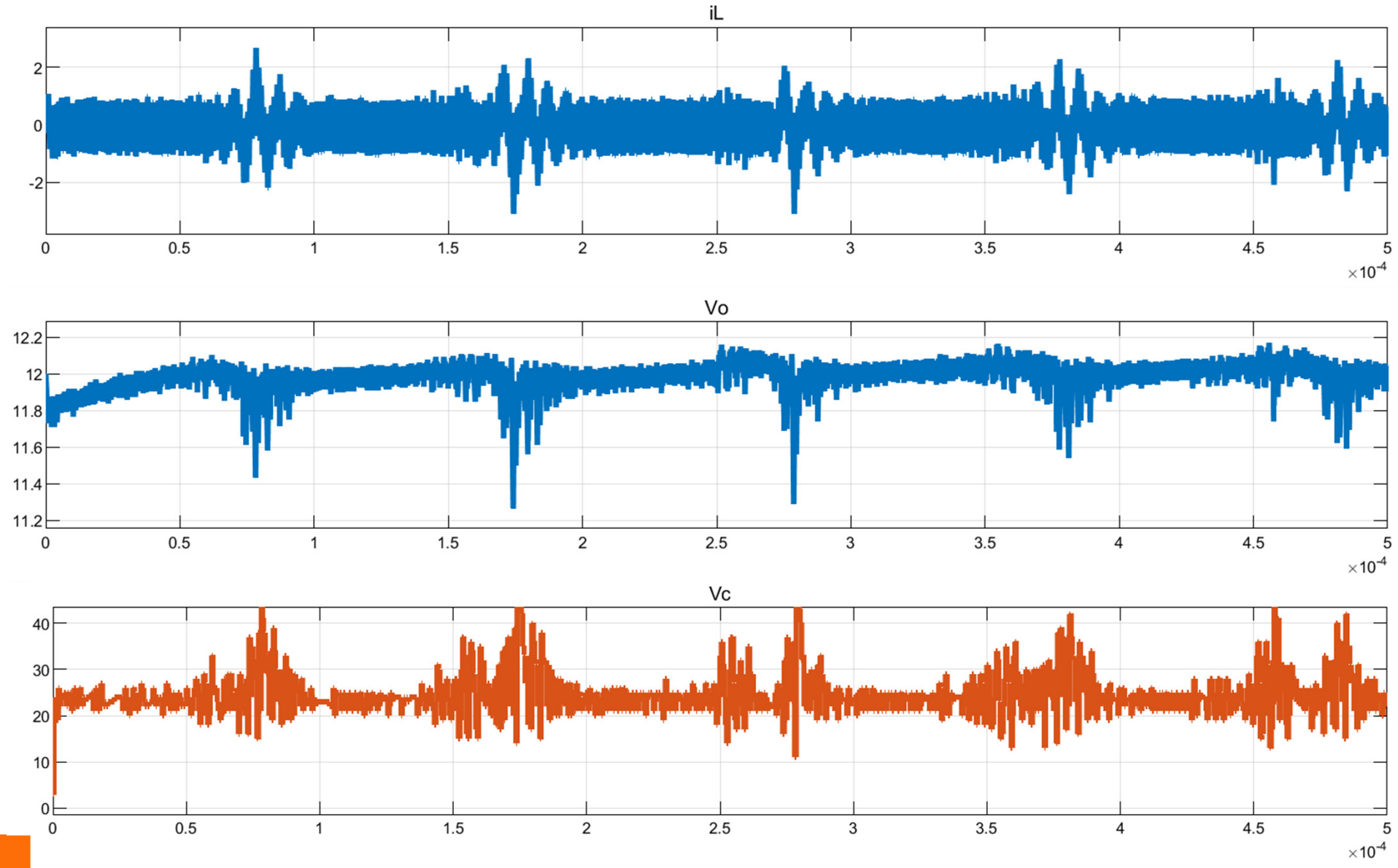




Quantization



Simulation with Quantization



Quantization Impact