Compensator Realizations (PID compensators)

$$G_{PID}(z;\boldsymbol{K}) \triangleq K_p + \frac{K_i}{1-z^{-1}} + K_d(1-z^{-1}), \qquad \boldsymbol{K} \triangleq [K_p, K_i, K_d]^T. \tag{6.5}$$

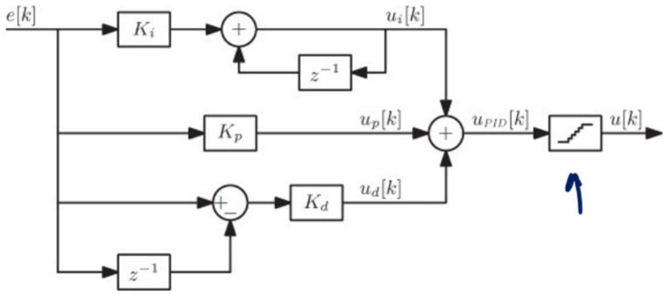


Figure 6.2 Parallel realization of a digital PID compensator.

$$G_{PID}(z;\boldsymbol{b}) \triangleq \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1-z^{-1}}, \qquad \boldsymbol{b} \triangleq [b_0, b_1, b_2]^T. \tag{6.6}$$

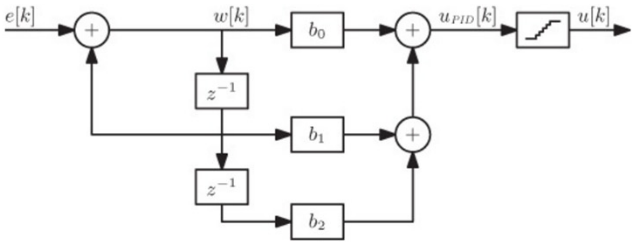


Figure 6.3 Direct realization of a digital PID compensator.

$$G_{PID}(z;\mathbf{c}) \triangleq \frac{K}{1-z^{-1}}\left(1+c_{z_1}z^{-1}\right)\left(1+c_{z_2}z^{-1}\right), \qquad \mathbf{c} \triangleq [K, c_{z_1}, c_{z_2}]^T, \tag{6.8}$$

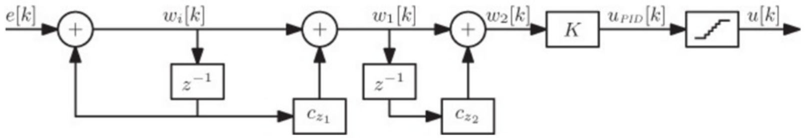


Figure 6.4 Cascade realization of a digital PID compensator.

Parallel Realization

$$u_p[k] = K_p e[k],$$

$$u_i[k] = u_i[k-1] + K_i e[k],$$

$$u_d[k] = K_d(e[k] - e[k-1]),$$

$$u[k] = u_p[k] + u_i[k] + u_d[k].$$ 4.10

The compensator coefficients K_p, K_i, and K_d are the proportional, integral, and derivative gains, respectively.

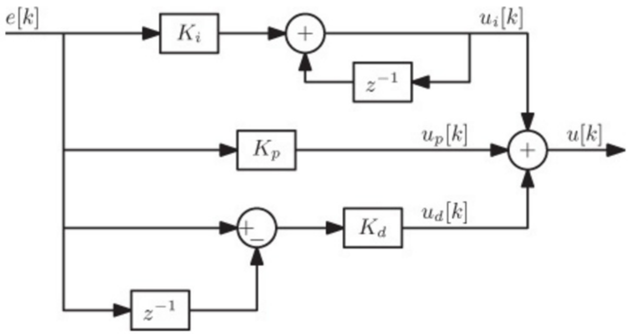
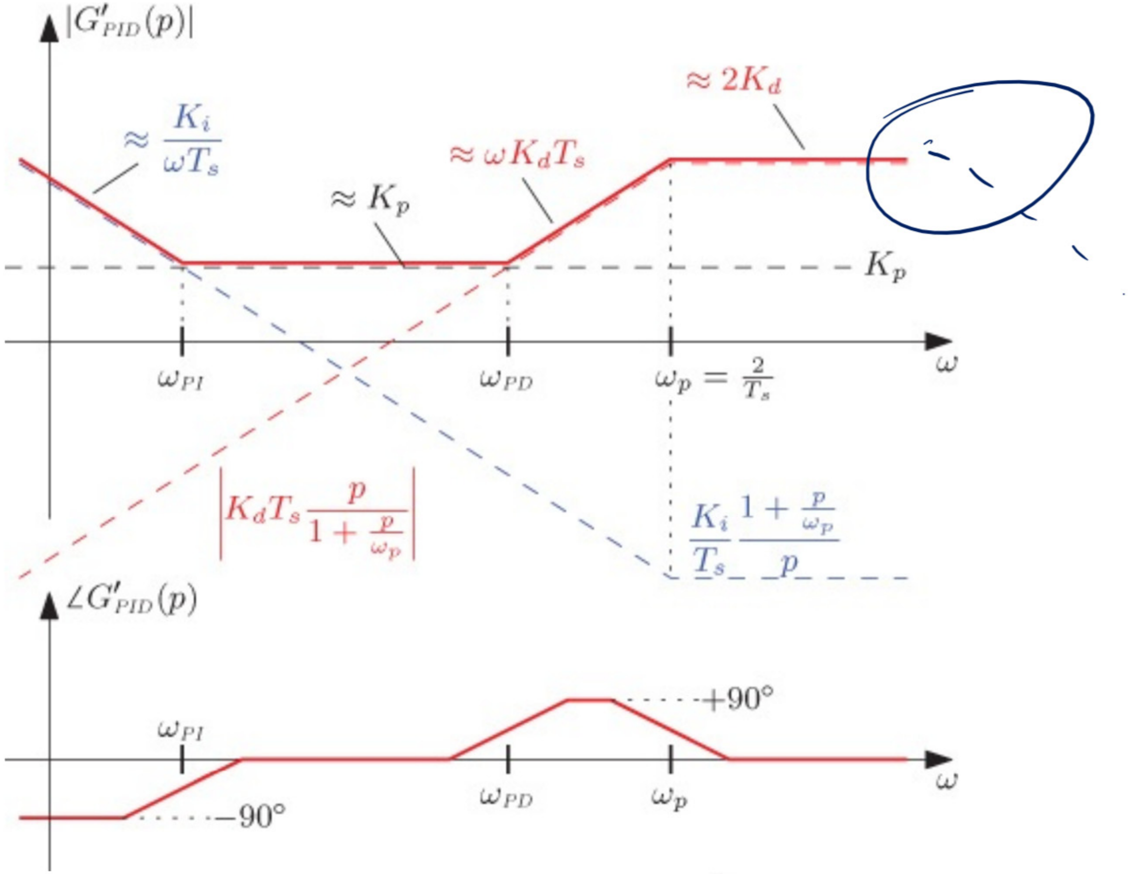


Figure 4.3 Block diagram of a digital PID compensator in the parallel form.

$$G_{PID}(z) = K_p + \frac{K_i}{1 - z^{-1}} + K_d(1 - z^{-1}).$$

$$G'_{PID}(p) = \underbrace{K_p}_{\text{Proportional term}} + \underbrace{\frac{K_i}{T_s}\frac{1 + \frac{p}{\omega_p}}{p}}_{\text{Integral term}} + \underbrace{K_d T_s \frac{p}{1 + \frac{p}{\omega_p}}}_{\text{Derivative term}},$$



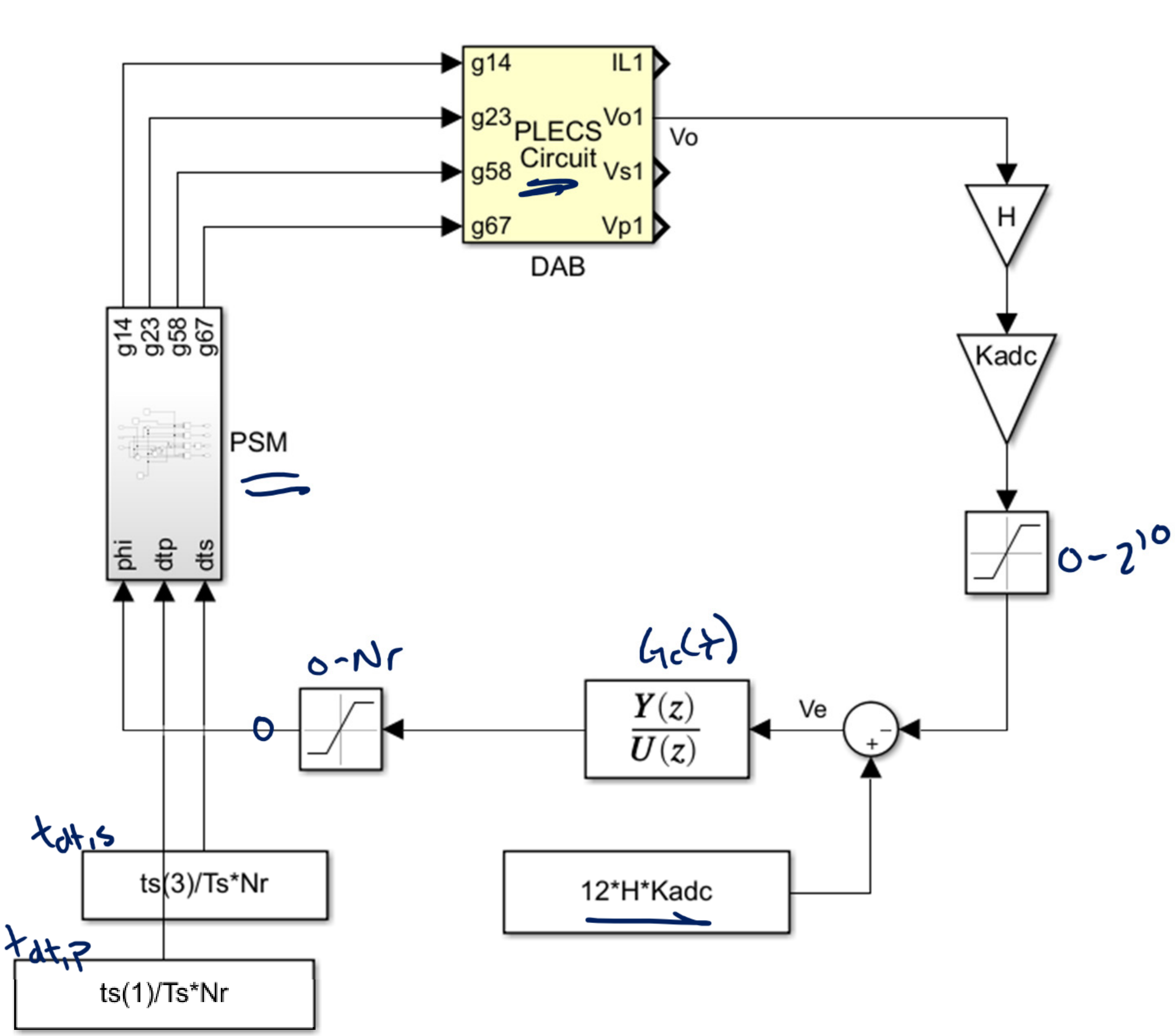
$$G'_{PID}(p) = \underbrace{G'_{PI\infty}\left(1 + \frac{\omega_{PI}}{p}\right)}_{PI}\underbrace{G'_{PD0}\frac{1 + \frac{p}{\omega_{PD}}}{1 + \frac{p}{\omega_p}}}_{PD},$$

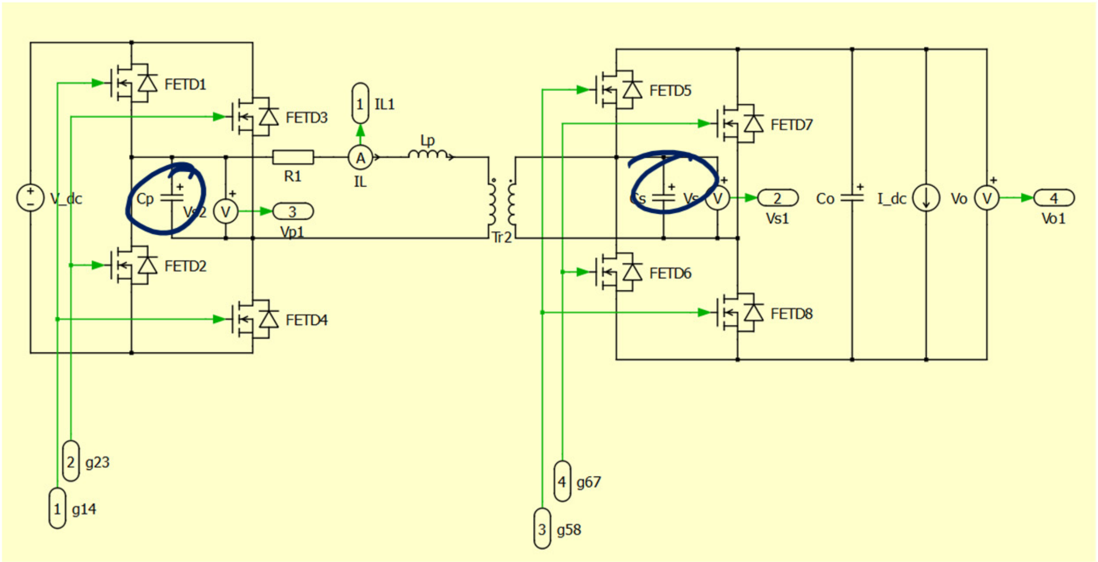
$$K_p = G'_{PI\infty}G'_{PD0}\left(1 + \frac{\omega_{PI}}{\omega_{PD}} - \frac{2\omega_{PI}}{\omega_p}\right),$$

$$K_i = 2G'_{PI\infty}G'_{PD0}\frac{\omega_{PI}}{\omega_p},$$

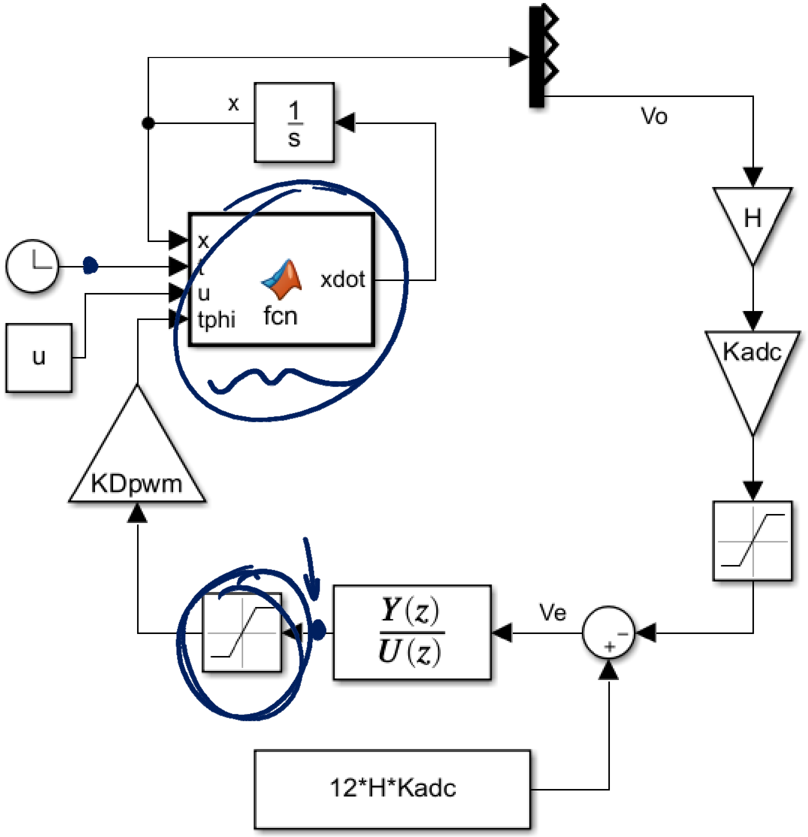
$$K_d = \frac{G'_{PI\infty}G'_{PD0}}{2}\left(1 - \frac{\omega_{PI}}{\omega_p}\right)\left(\frac{\omega_p}{\omega_{PD}} - 1\right).$$

Simulation (Large Signal)



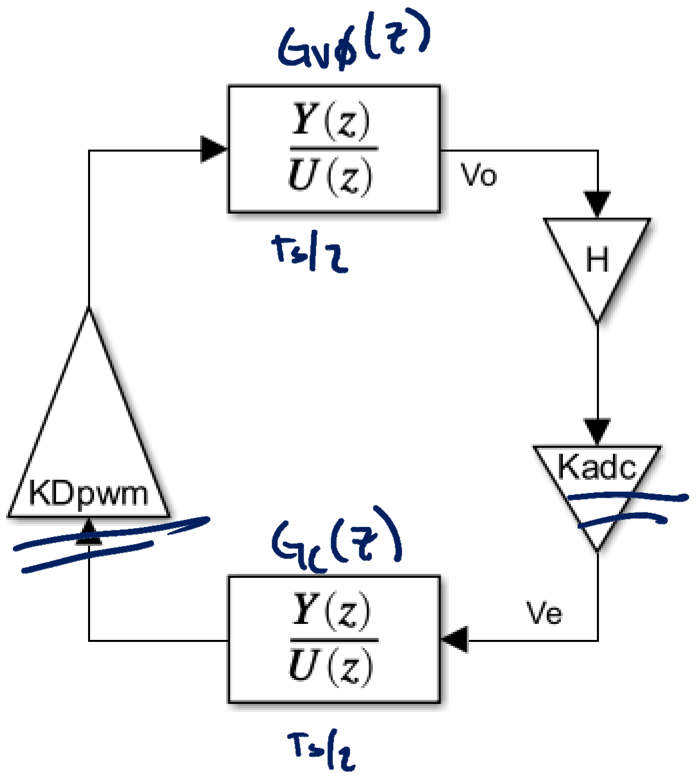


Alternative Simulation (Large Signal)

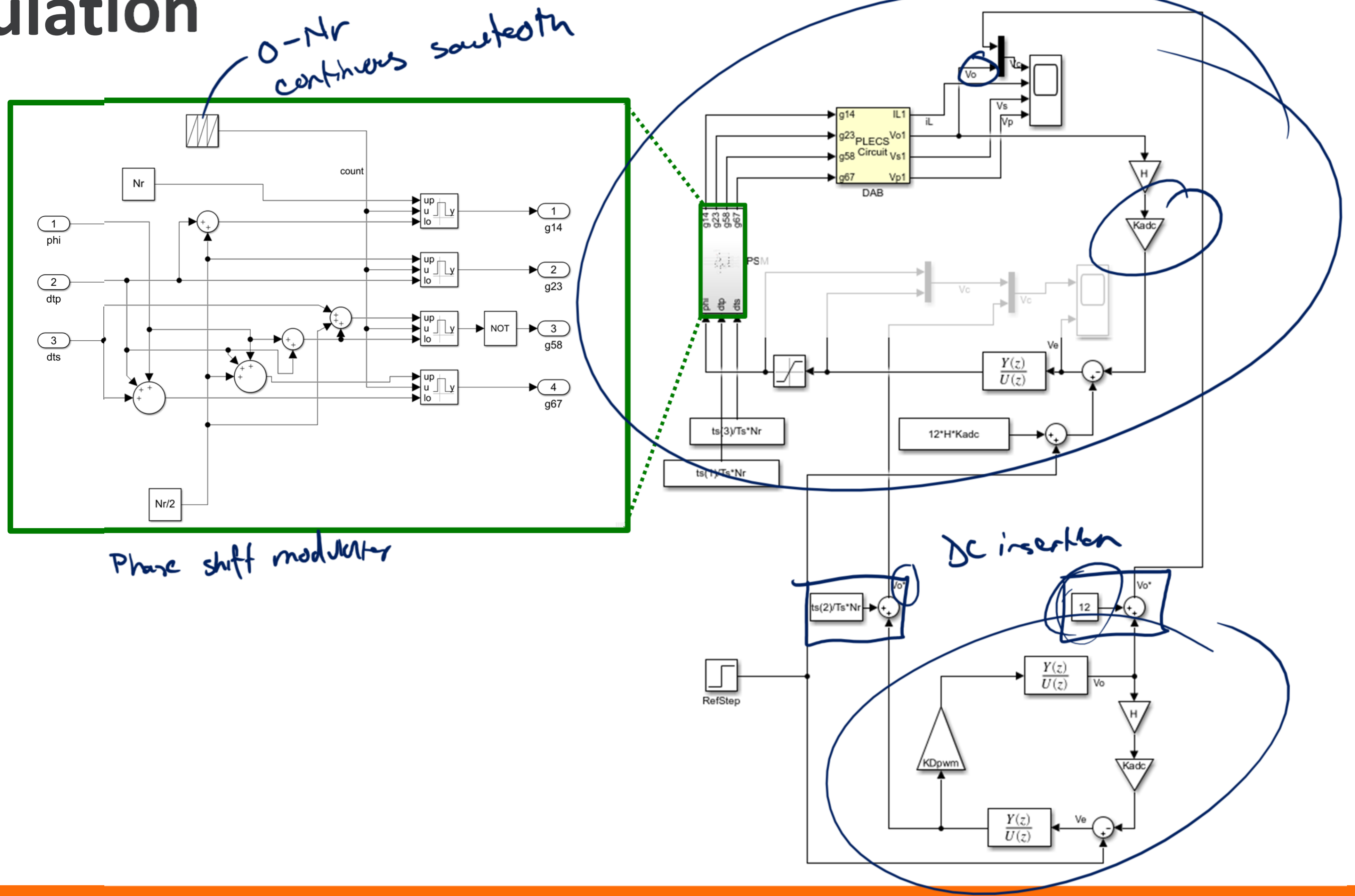



```
function xdot = fcn(x, t,
    u,tphi, A1, A2, B1, B2, Ts)

tp = mod(t,Ts);

if(tp<tphi)
    xdot = A1*x + B1*u;
else
    xdot = A2*x+B2*u;
end
```

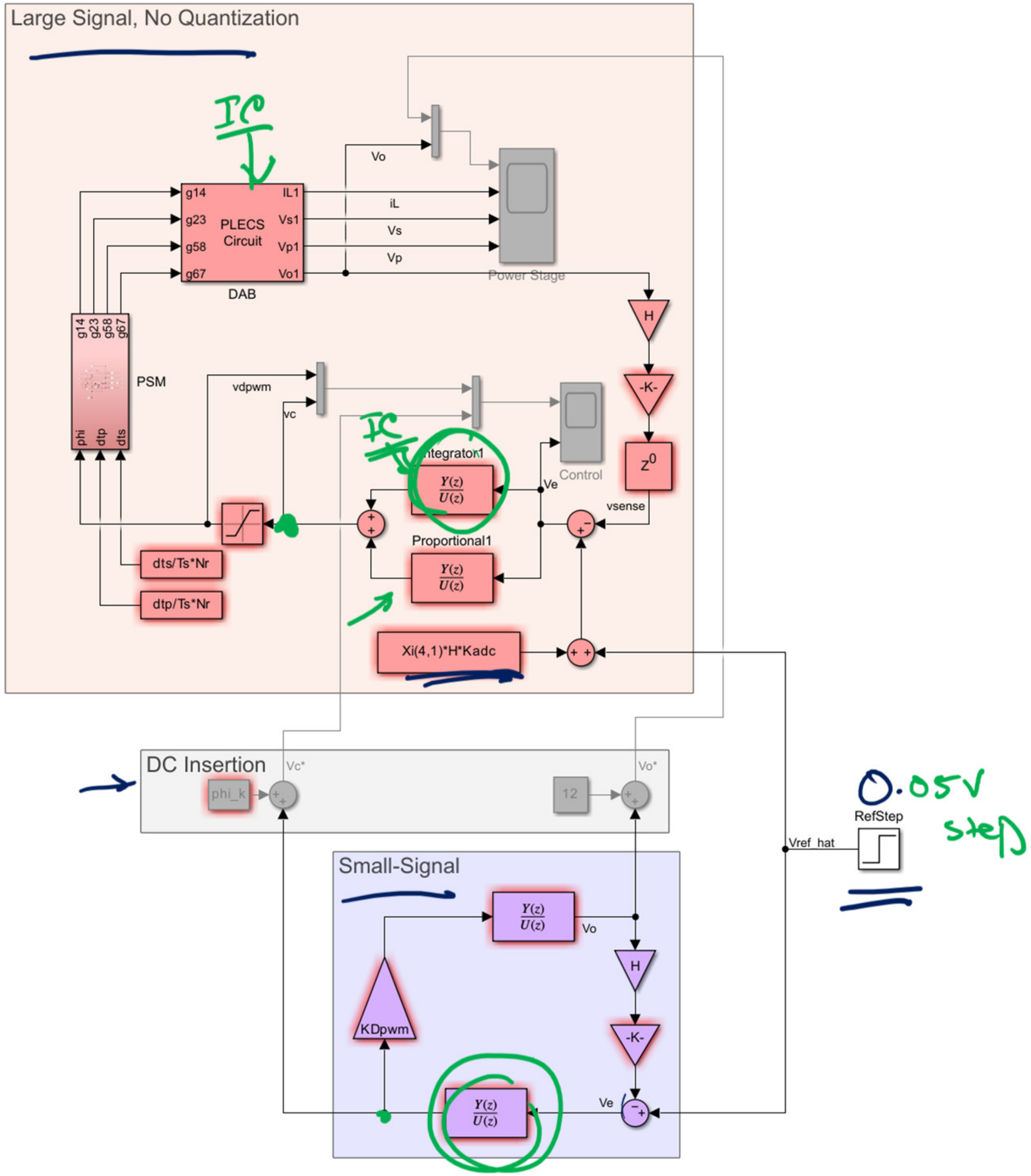
Simulation (Small Signal)



Simulation

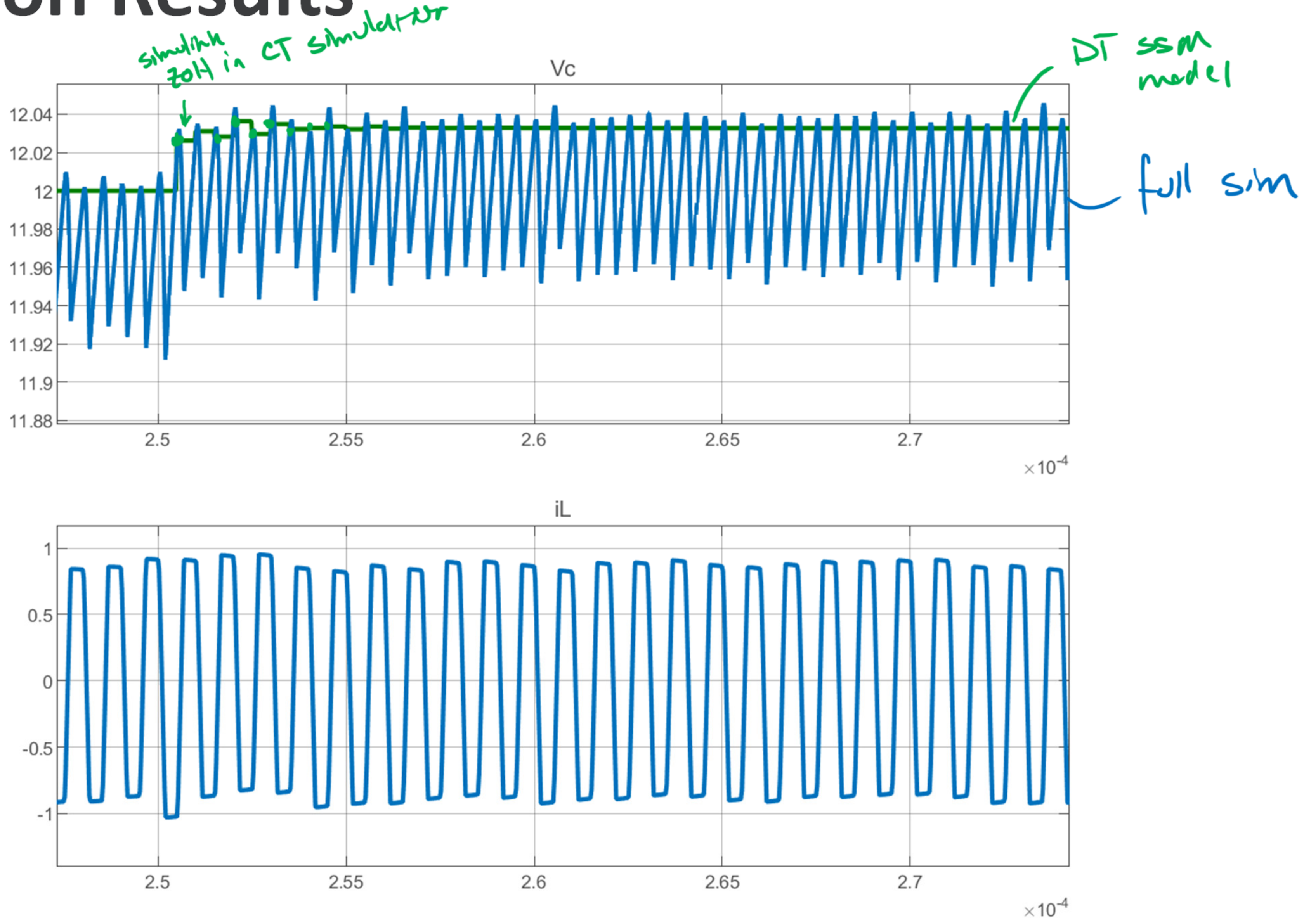


0-Nr continuous sawtooth
count
Nr
1 phi
2 dtp
3 dts
up u lo y
1 g14
2 g23
NOT
3 g58
4 g67
Nr/2
Phase shift modulator
g14 g23 g58 g67
PLECS Circuit
IL1 Vo1 Vs1 Vp1
DAB
iL
Vo
Vs
Vp
H
Kadc
PSM
phi dtp dts
Ve
Y(z)/U(z)
ts(3)/Ts*Nr
ts(1)/Ts*Nr
12*H*Kadc
DC insertion
ts(2)/Ts*Nr
Vo*
12
RefStep
KDpwm



Large Signal, No Quantization
IC
PLECS Circuit
DAB
g14
g23
g58
g67
IL1
Vs1
Vp1
Vo1
Vo
iL
Vs
Vp
Power Stage
H
-K-
PSM
phi
dtp
dts
vdpwm
vc
Integrator1
Control
Ve
vsense
Proportional1
dts/Ts*Nr
dtp/Ts*Nr
Xi(4,1)*H*Kadc
DC Insertion
Vc*
Vo*
phi_k
12
Small-Signal
KDpwm
Vref_hat
RefStep
0.05V step

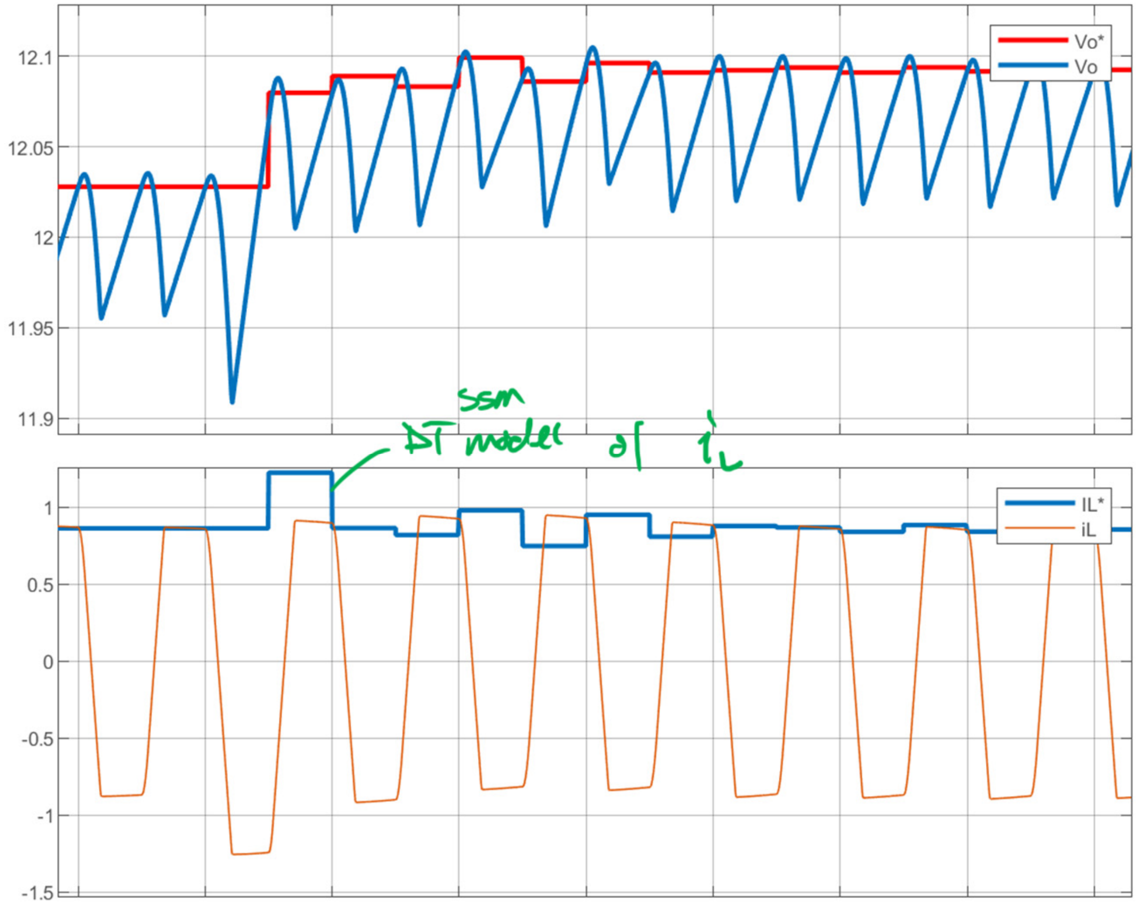
Simulation Results



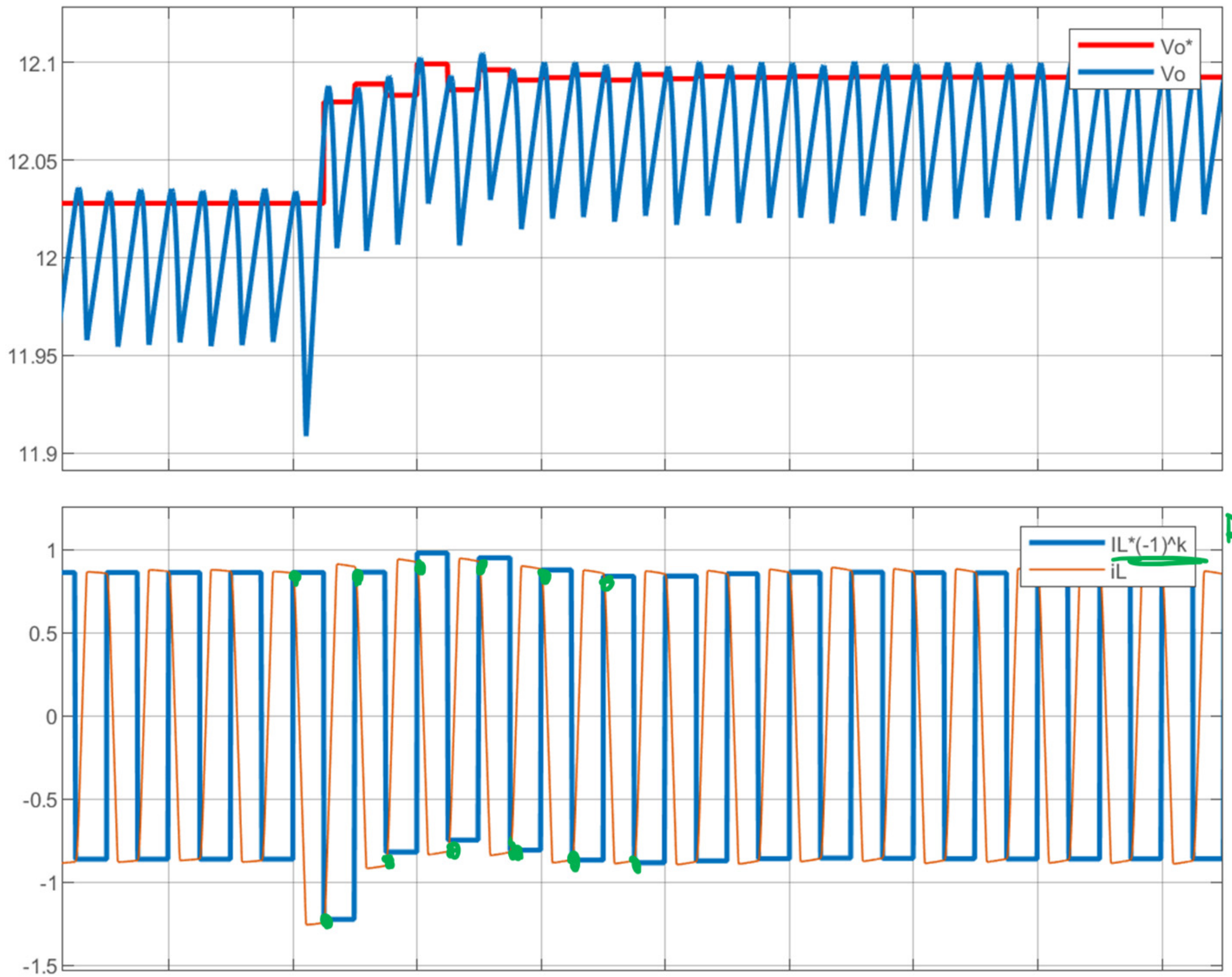
ac Waveform Comparison

Half-cycle symmetric DAB model

SSM DT model of i_L

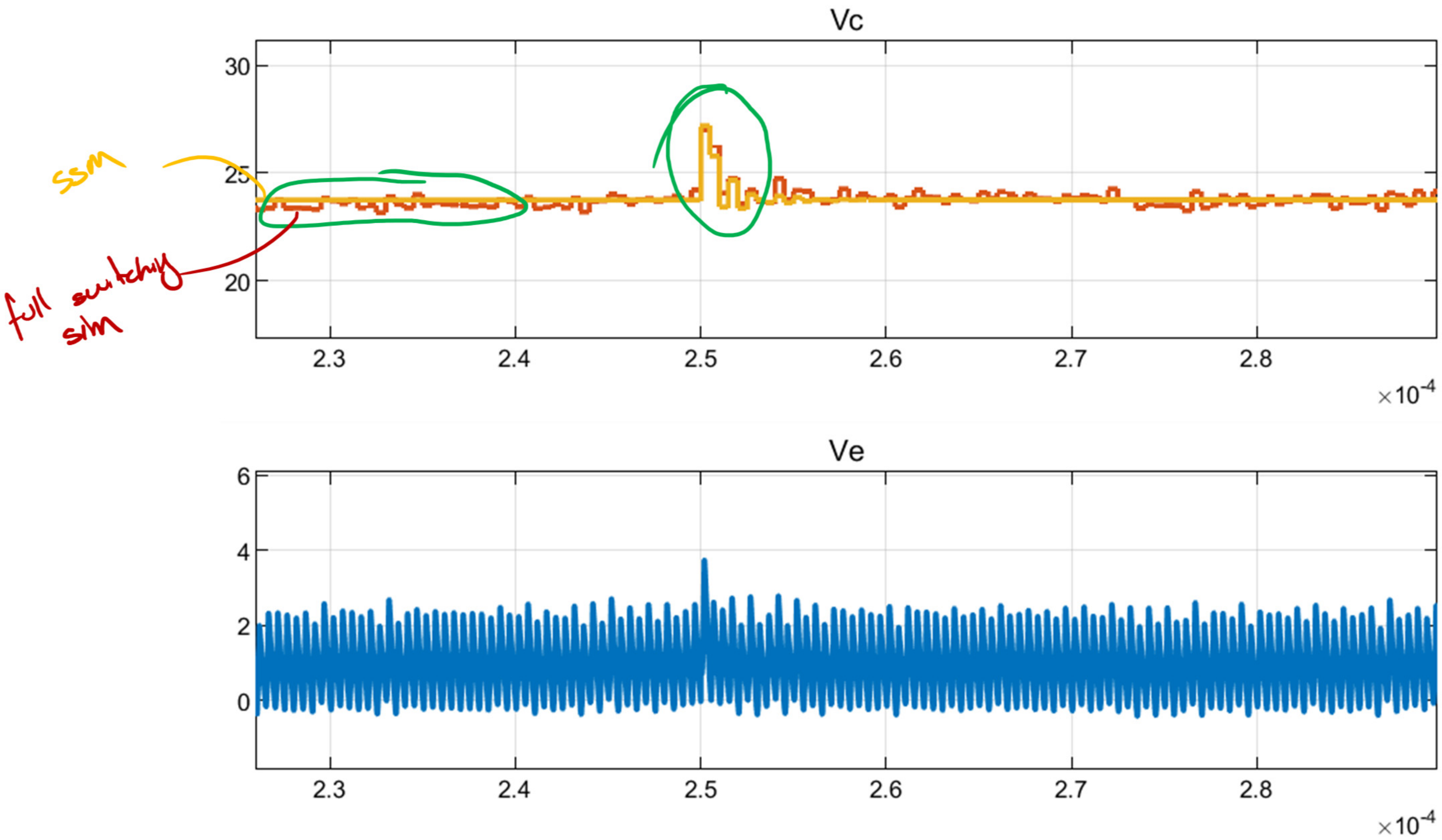


Inverting ac waveform

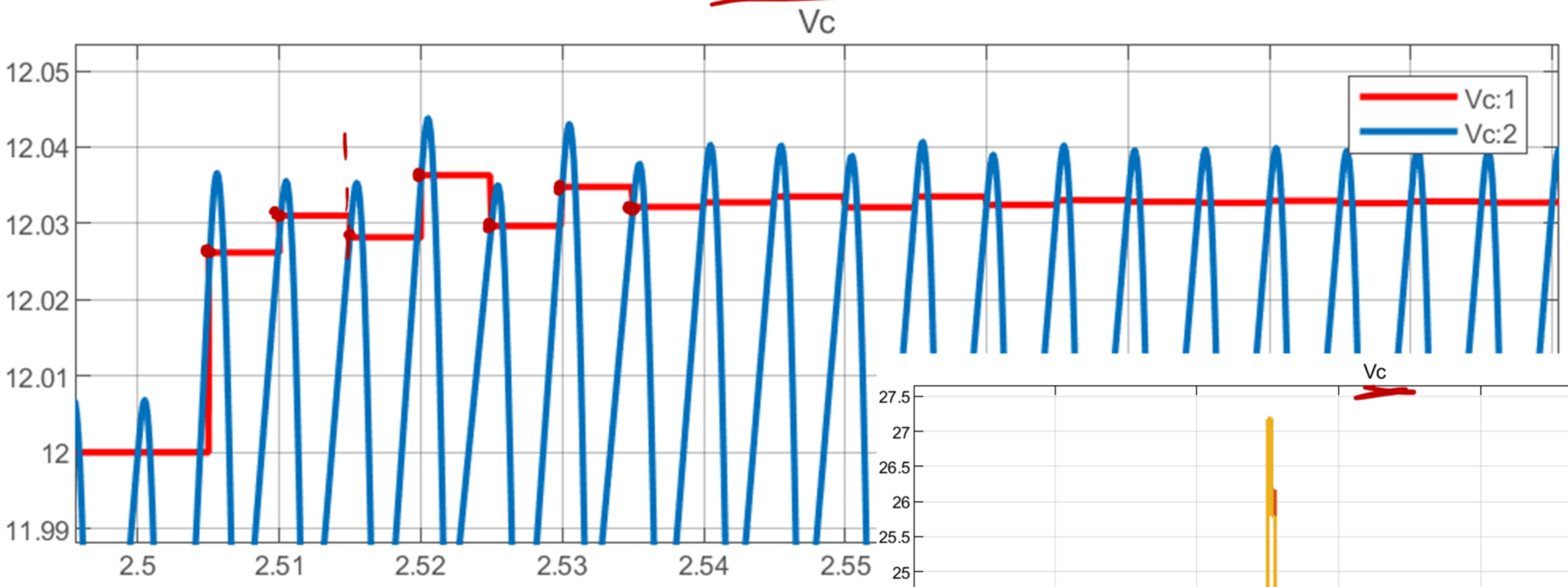


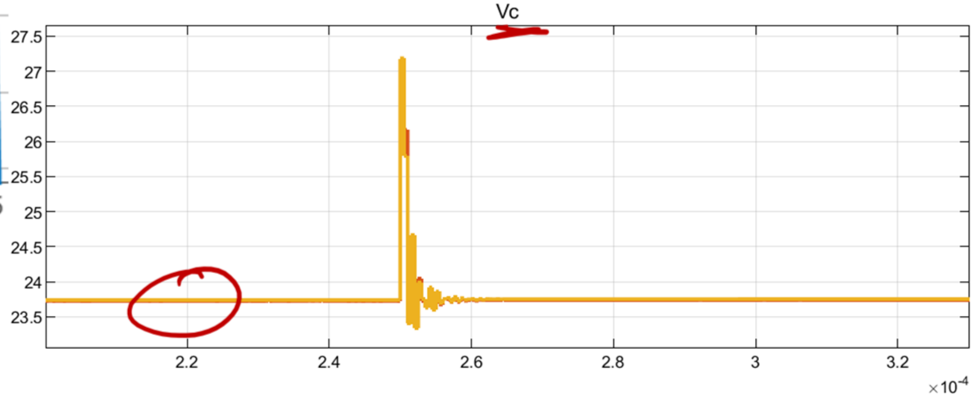
DT ssm model

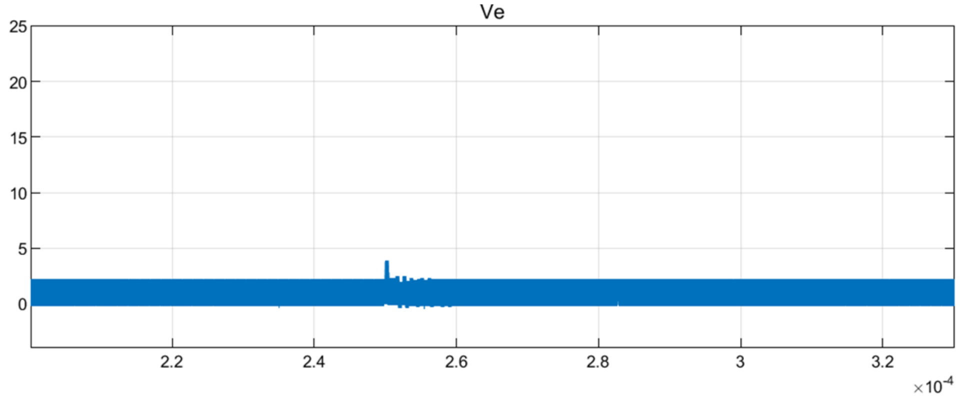
Simulation Results (cont)



Simulation Results (max step 10ps)

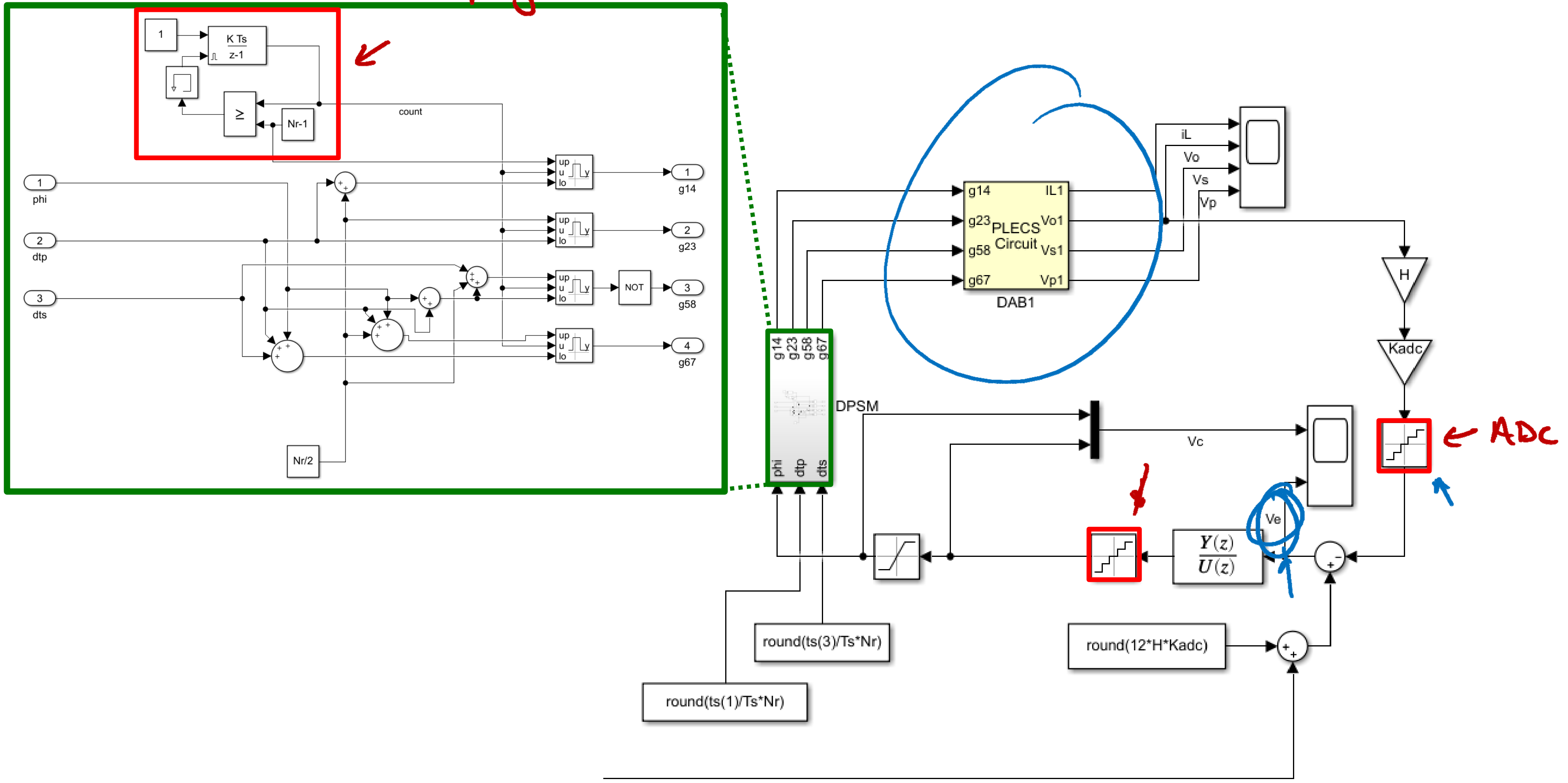


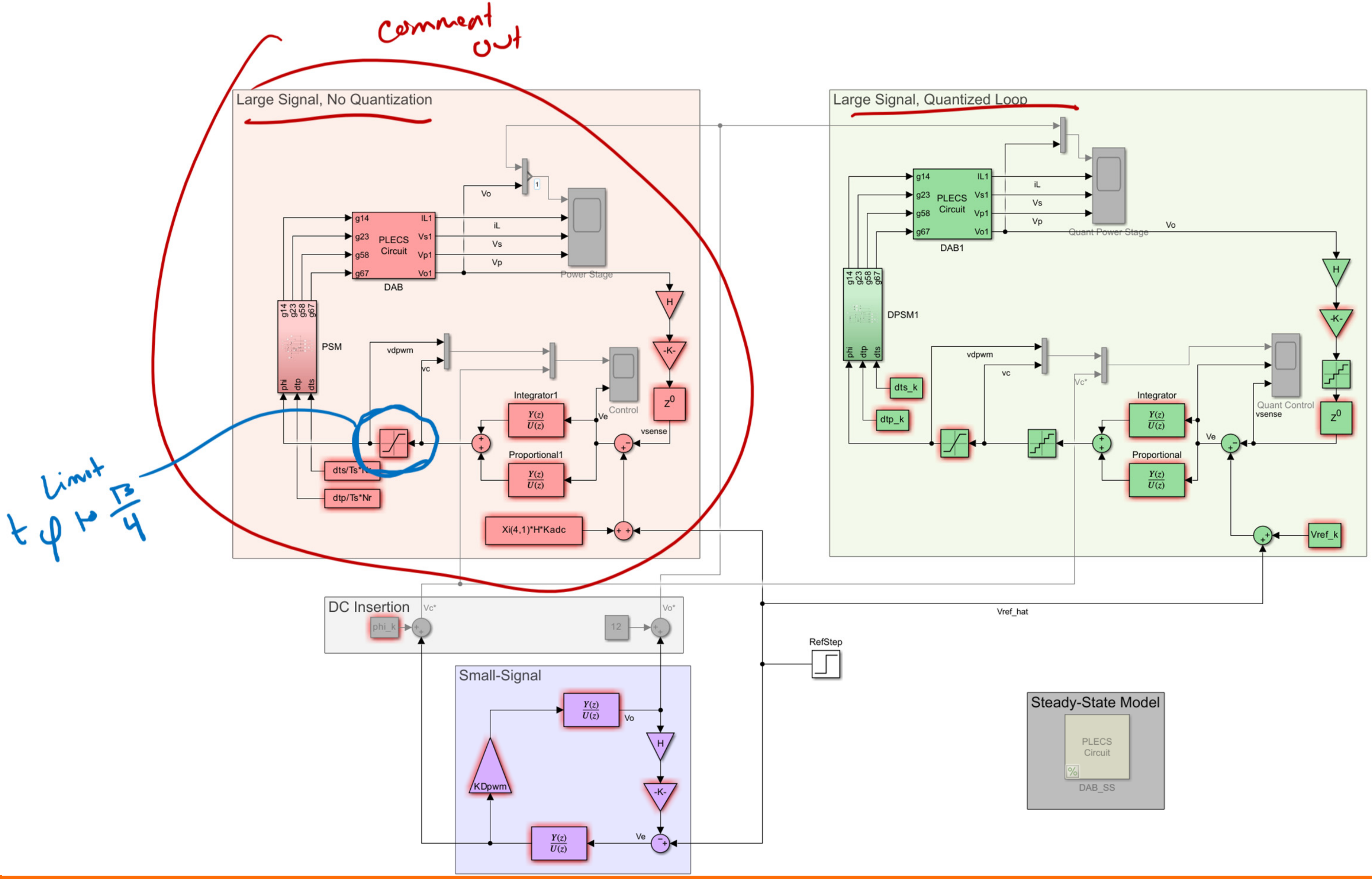




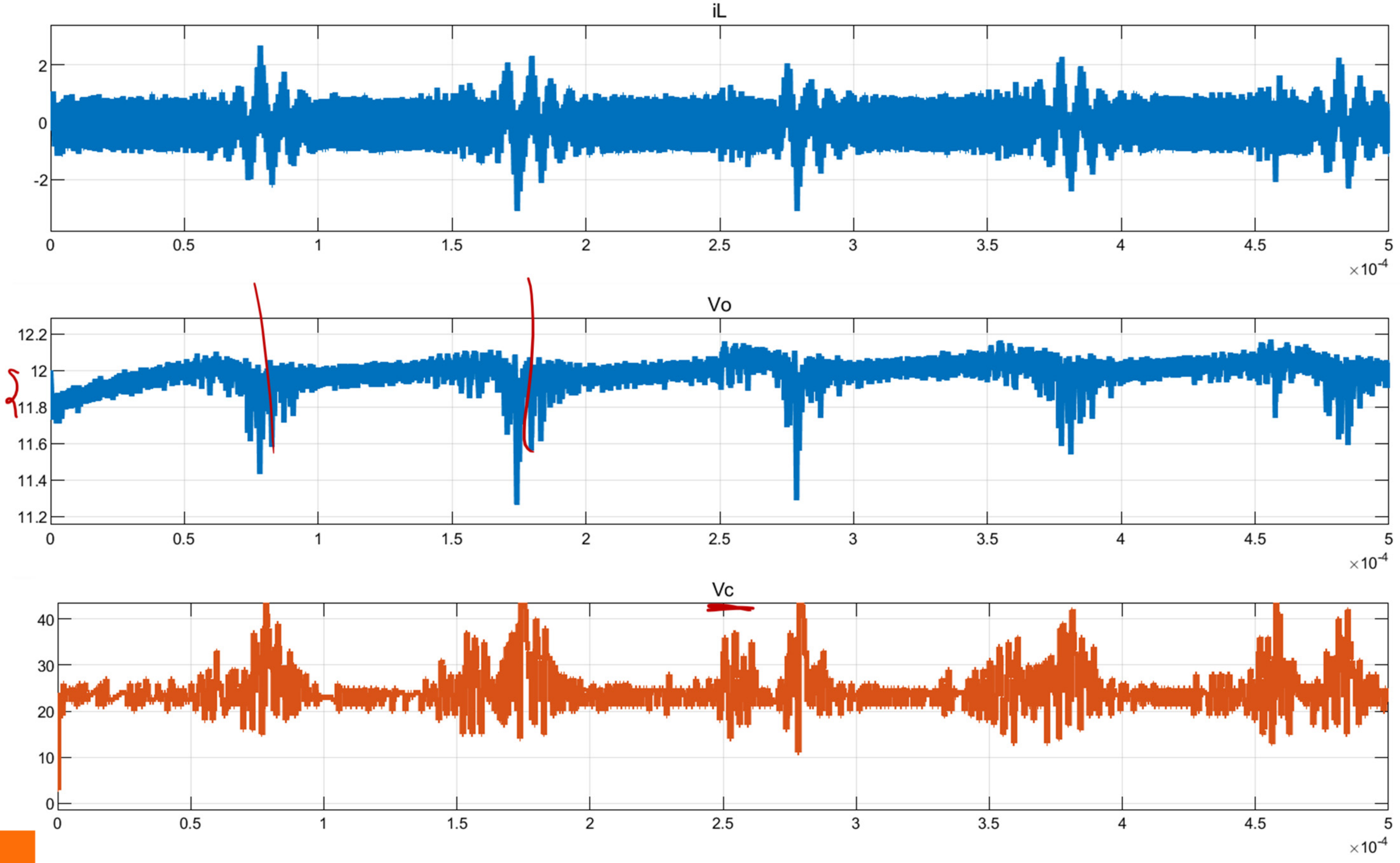
Quantization

0-Nr integer counter




Comment out
Limit φ to Ts/4
Large Signal, No Quantization
PLECS Circuit
DAB
Power Stage
PSM
vdpwm
vc
Integrator1
Proportional1
Control
Ve
vsense
dts/Ts*Nr
dtp/Ts*Nr
Xi(4,1)*H*Kadc
Large Signal, Quantized Loop
DAB1
DPSM1
Quant Power Stage
Quant Control
Integrator
Proportional
dts_k
dtp_k
Vref_k
Vc*
Vref_hat
DC Insertion
phi_k
12
Vo*
RefStep
Small-Signal
KDpwm
Steady-State Model
DAB_SS

Simulation with Quantization



Quantization Impact

Caused Limit cycling

$$q_{v_o}^{ADC} = \frac{1}{K_{ADC}} \frac{1}{H} = \frac{V_{FS}}{2^{n_{A/D}}} \cdot 10 = \boxed{32mV}$$ w/ 10-bit A/D

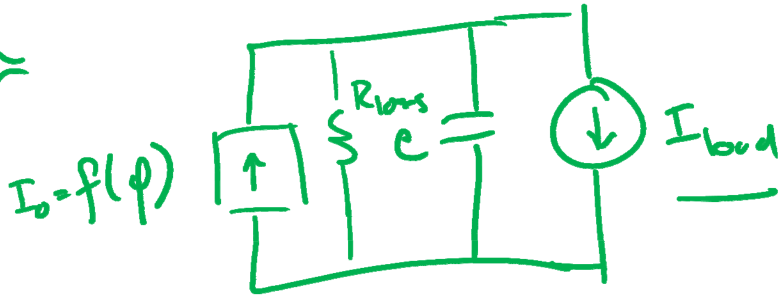
$$q_{v_o}^{DPWM} = \frac{1}{N_r}\left(\frac{\partial m(\varphi)}{\partial \varphi}\Big|_{\varphi_0}\right)\cdot V_g = \boxed{3.07\,V\,!}$$

@ $N_r = 200$

$$\boxed{q_{v_o}^{DPWM} \gg q_{v_o}^{ADC}} \sim 100x$$

limit cycling will occur

Note: DAB ≈



Try to remove Limit cycling:

DPWM: Add 6-bits to resolution (e.g. by a hybrid DPWM)

$$N_r = 200 \cdot 2^6 = 200 \cdot 64 = 12800$$

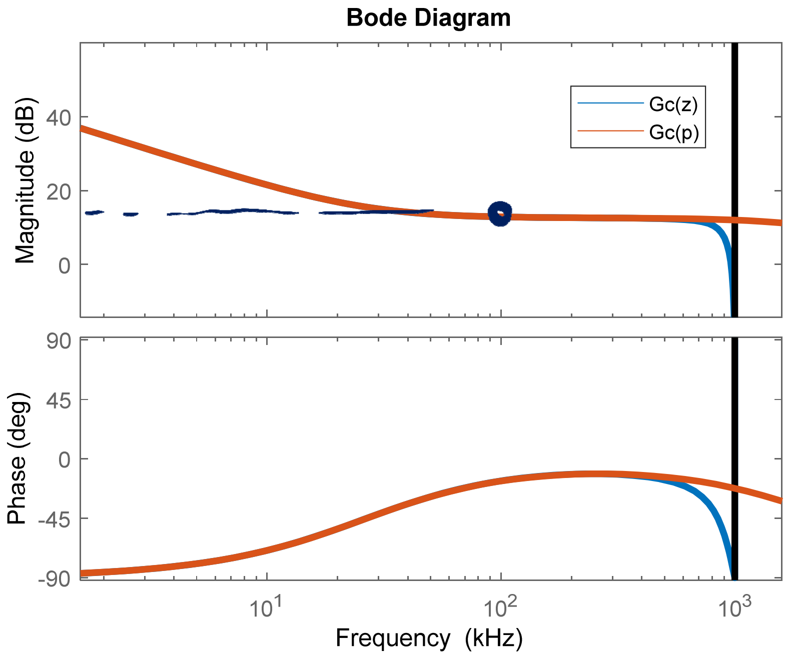
ADC: Drop ADC resolution to 9 bits

$$q_{v_o}^{ADC} = 64mV$$

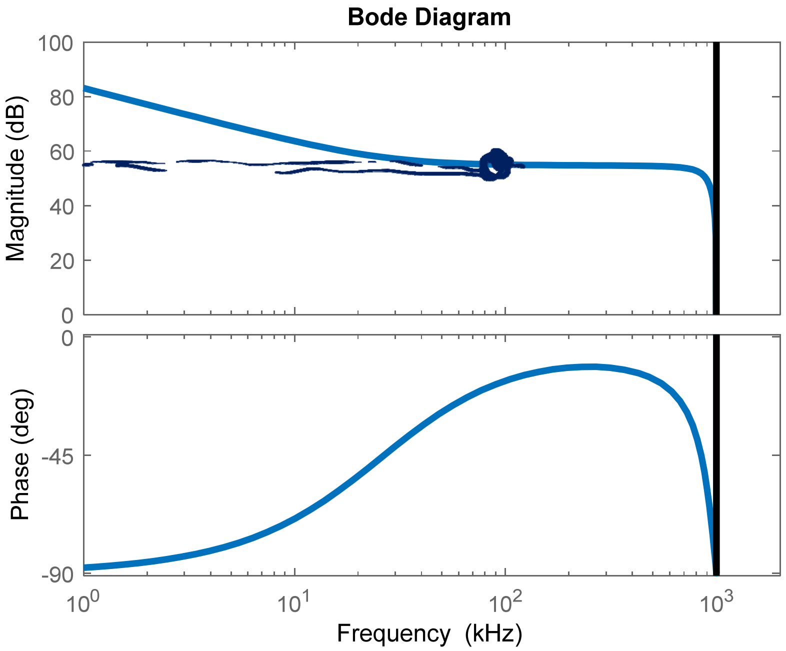
} 128x change in quantization comparison

New Compensator

OLD



New



128x

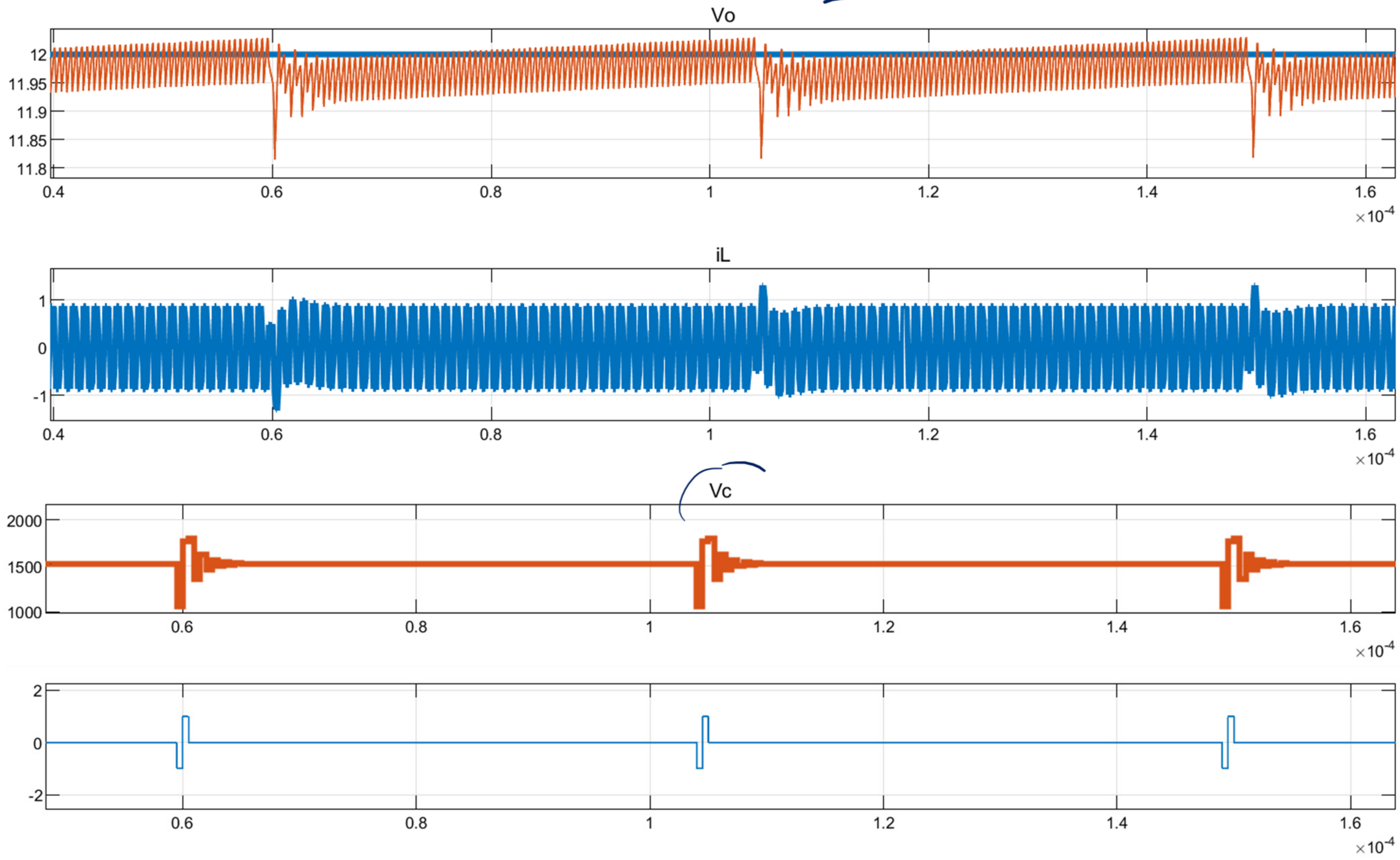
$$\left\{ \begin{array}{l} k_i' = k_i \cdot 128 \\ k_p' = k_p \cdot 128 \end{array} \right\}$$

T(z) remains unchanged

k_p' → new; k_p → old

High Res Modulator

Still Limit Cycling !



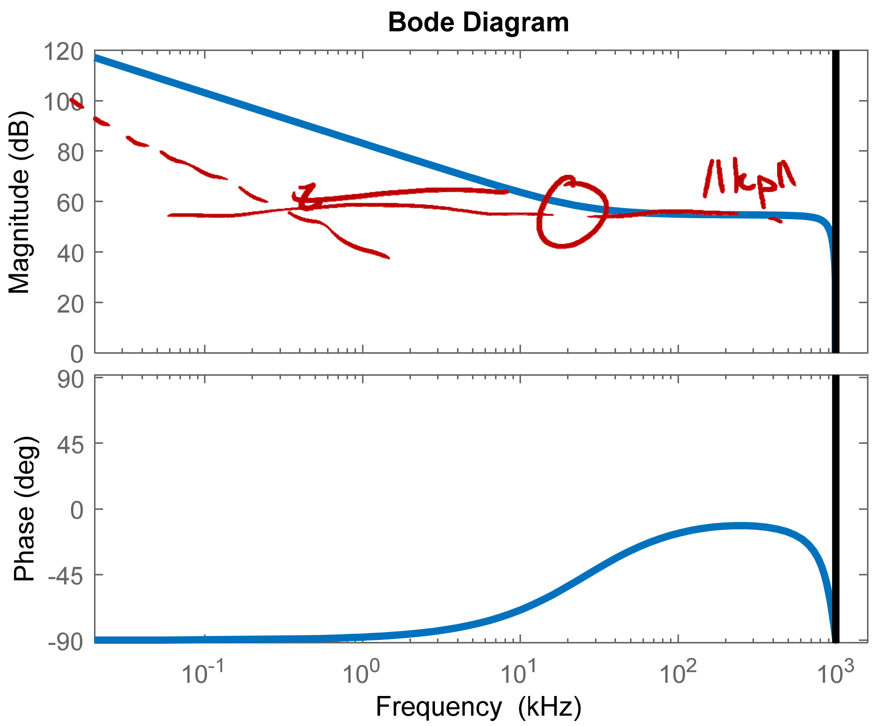
Integral Gain

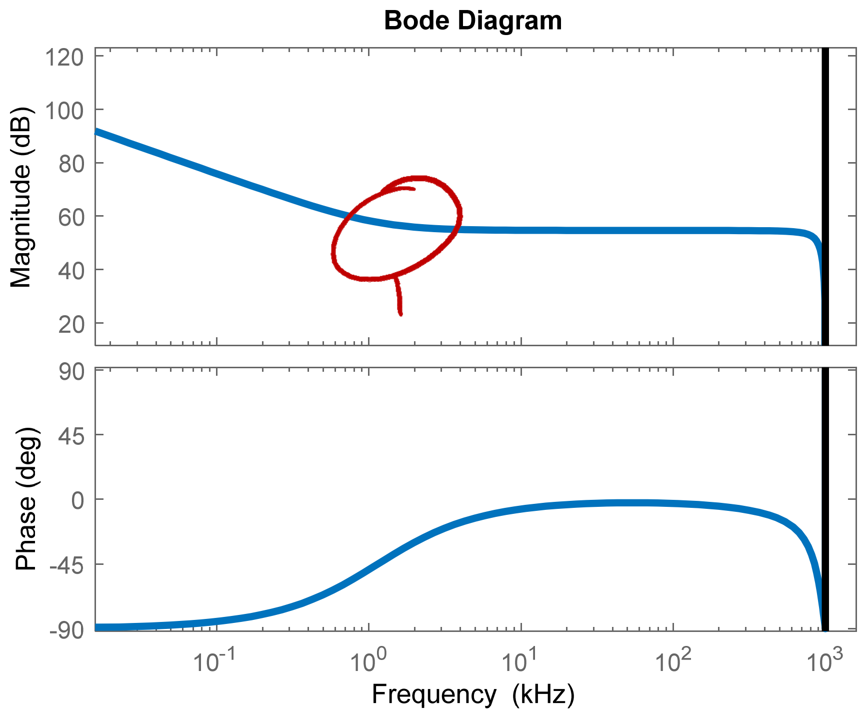
$k_i' = 22$ $\qquad$ $t_p' = 435.5$

because $k_i' > 1$, we can only get steady state $\tilde{\varphi}$ values of $\underline{n \cdot 22}$

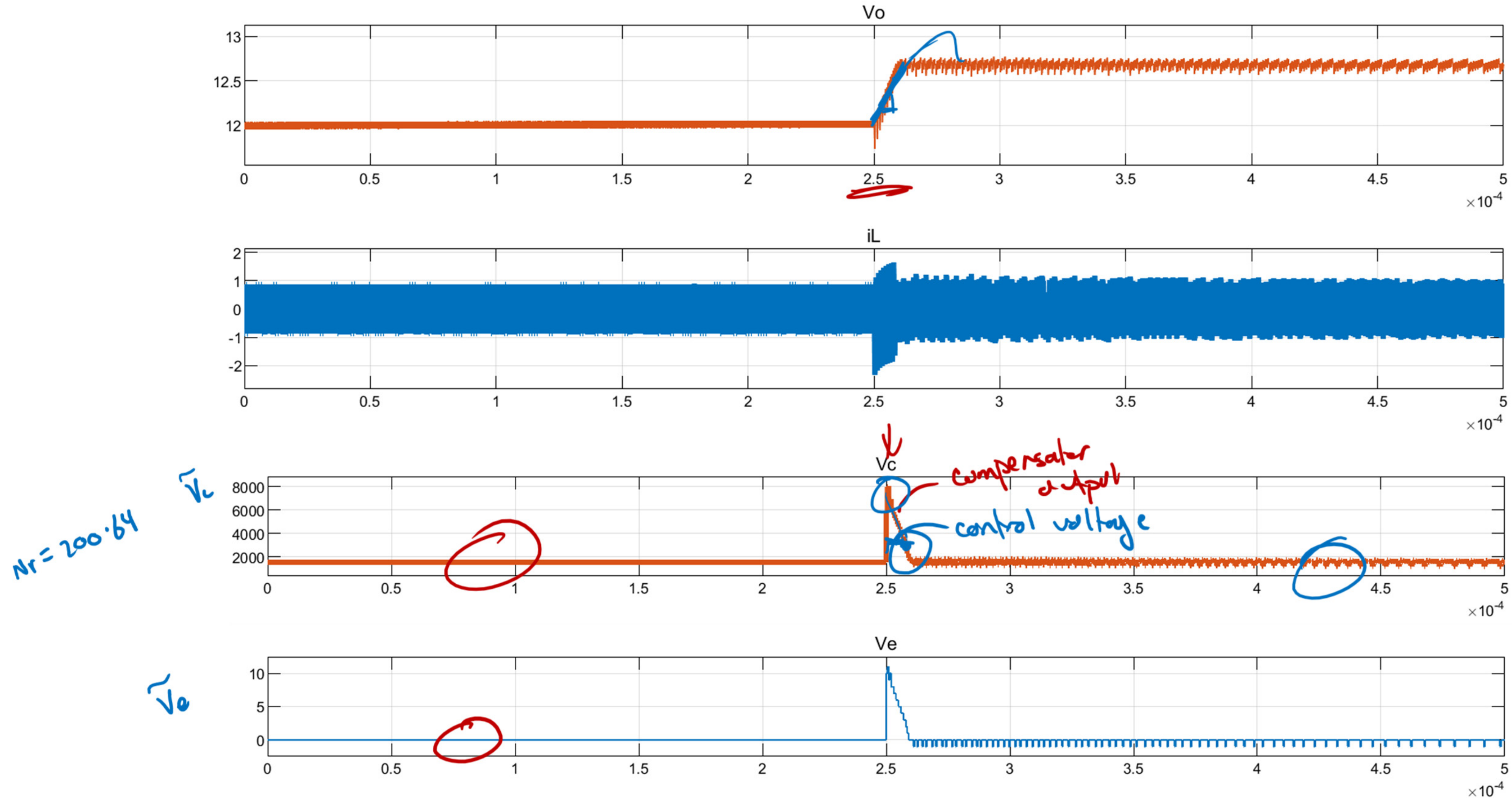
Can drop k_i to 1

New Compensator

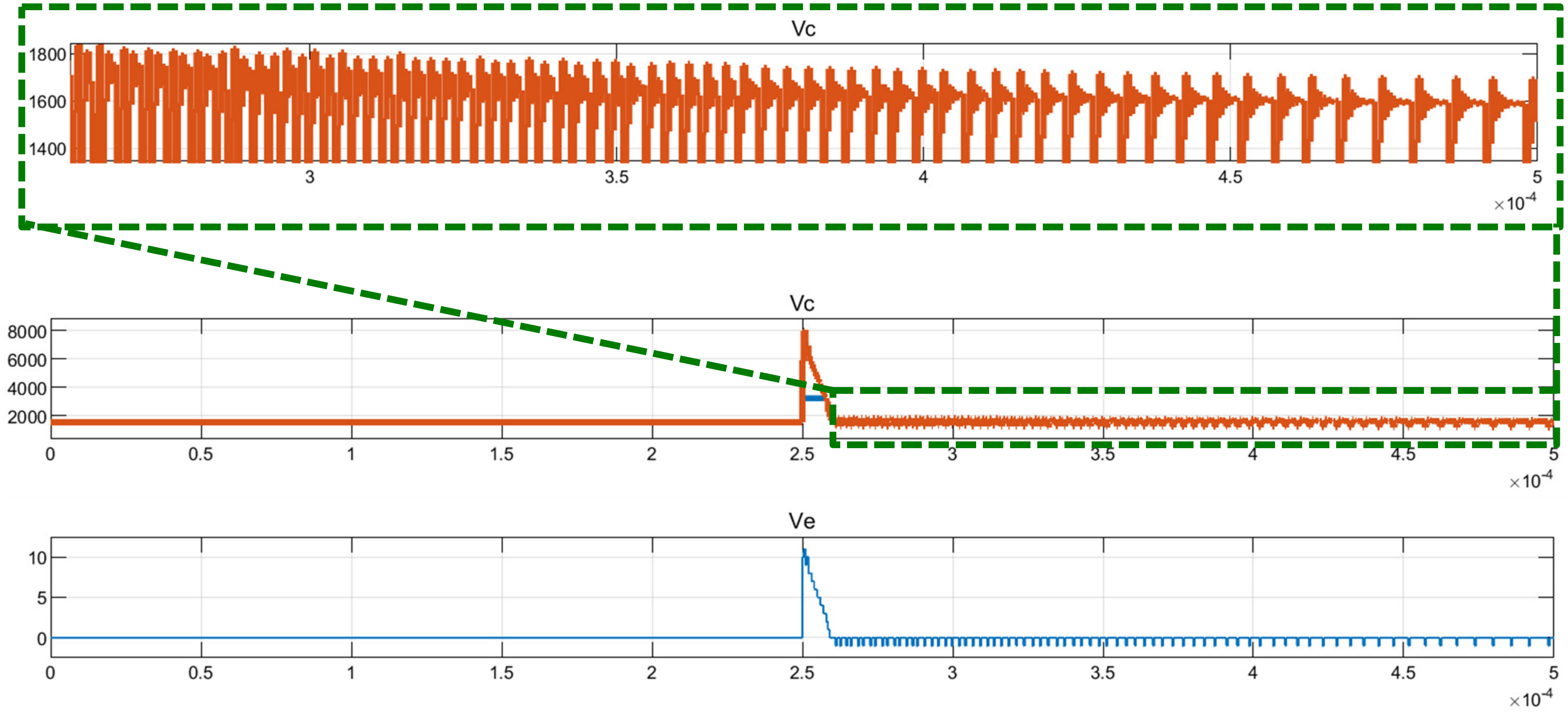




Low Ki


Vo
13
12.5
12
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
$\times 10^{-4}$
iL
2
1
0
-1
-2
$\times 10^{-4}$
Vc
8000
6000
4000
2000
$\times 10^{-4}$
Ve
10
5
0
$\times 10^{-4}$
compensator output
control voltage
Nr = 200·64
$\tilde{V}_c$
$\tilde{V}_e$

Low Ki



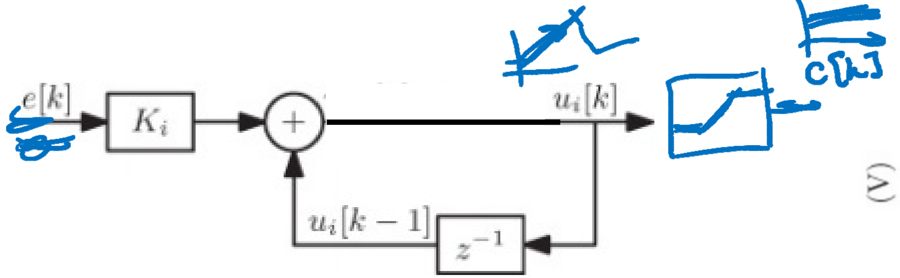
Vc
1800
1600
1400
3
3.5
4
4.5
5
×10⁻⁴
Vc
8000
6000
4000
2000
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
×10⁻⁴
Ve
10
5
0
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
×10⁻⁴

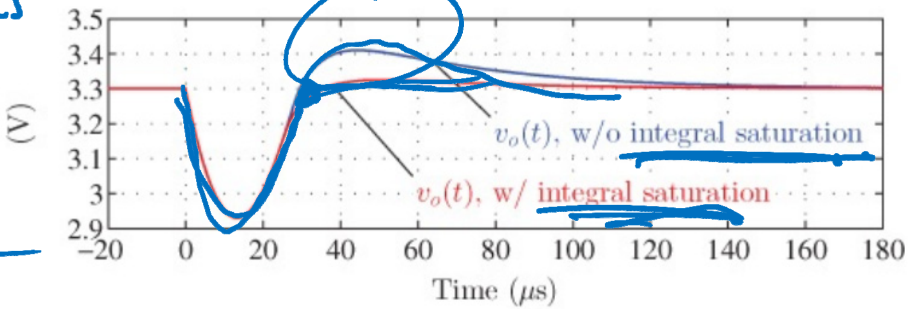
Anti-Windup

Not a problem in previous simulation

2nd transient to decrease integral term.

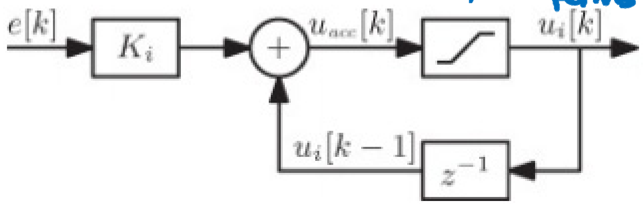
Integral compensator

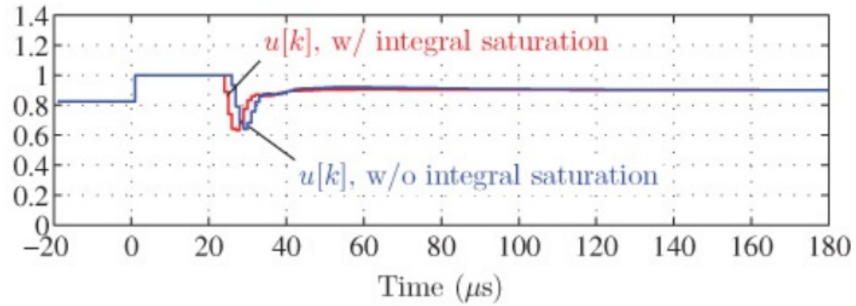




1st solution

only integral terms bounded





2nd solution (Better)