

# Final Project: Additional Comments

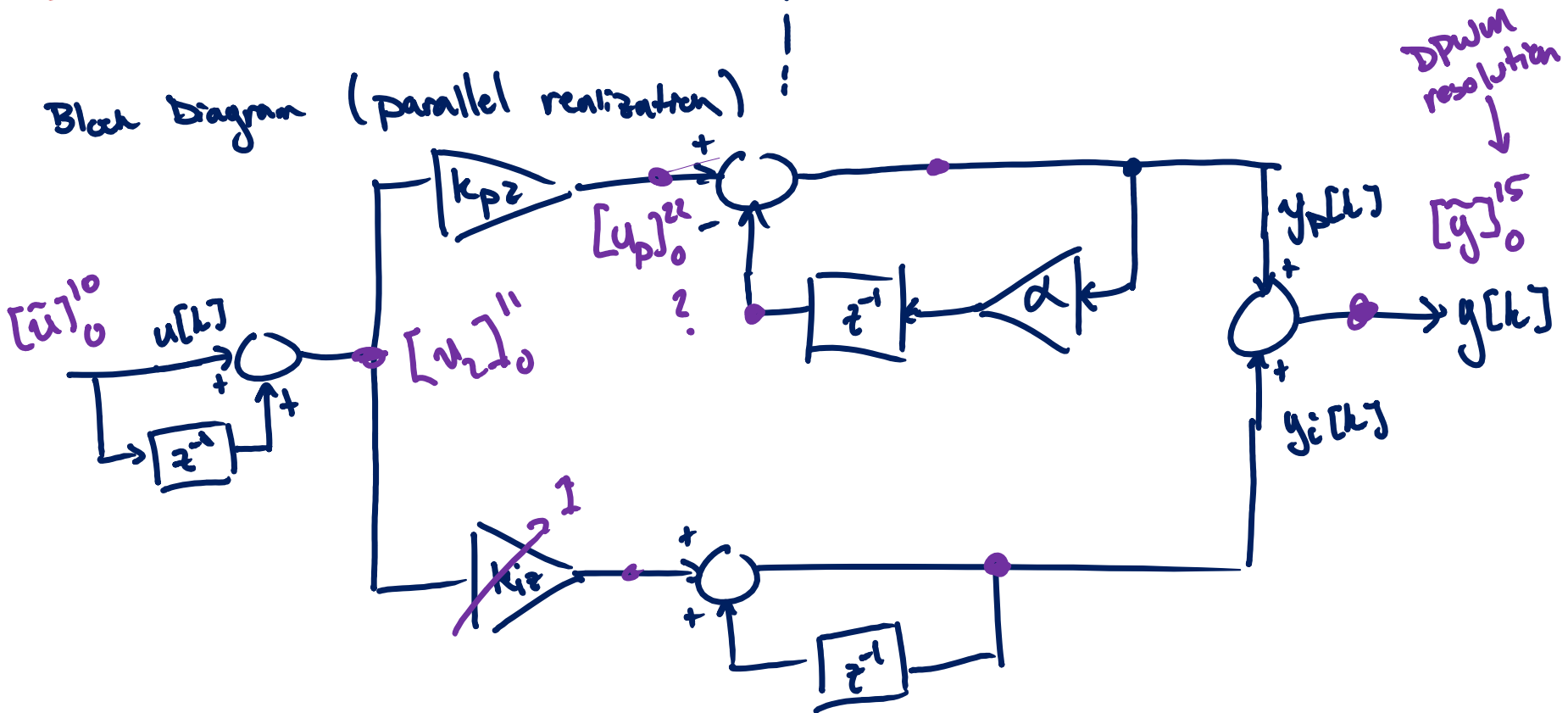
- Report should
  - Use theory from course (in non-trivial manner)
    - DT SSM, ADC and computation delay, quantization, synchronization, limit cycling, generalized state space
  - Detail analysis beyond/distinct from posted homework solutions
- Validation requires detailed, direct, quantitative comparison and discussion
  - Just running a simulation doesn't complete verification
- Be clear on what you did using ECE692 theory

# Compensator Implementation

$$G_c(z) = \frac{Y(z)}{U(z)} = \underbrace{k_{pz} \frac{1+z^{-1}}{1+\alpha z^{-1}}}_{G_{pz}(z)} + \underbrace{k_{iz} \frac{1+z^{-1}}{1-z^{-1}}}_{G_{iz}(z)}$$

$$g_p[k] = k_{pz}(u[k] + u[k-1]) - \alpha y_p[k-1] \quad g_i[k] = k_{iz}(u[k] + u[k-1]) + g_i[k-1]$$

Block Diagram (parallel realization)



# Software vs. Hardware Coding

Generally, floating point hardware too expensive/slow for  $f_s$ -rate control loops

- fixed point calculations preferred

Software: DSP/ $\mu$ C, embedded processor & defined word length

Hardware: FPGA/PLD/ASIC, variable bit-length

6.2-6.3  
AW & SW

{ Coefficient Scaling  $\rightarrow$  Incorporating  $K_{APC}$  &  $K_{DPM}$   
Coefficient Quantization  $\rightarrow$  Need small bit-length versions of constants

6.4-6.6  
- focused on  
AW imp.

- Fixed-point implementation  $\rightarrow$  determine bit-lengths of all signals & resolution

# Coefficient Scaling and Quantization

$$k_{i2} = 1$$

$$\alpha = 0.6111$$

$$k_{p2} = 435.4278$$

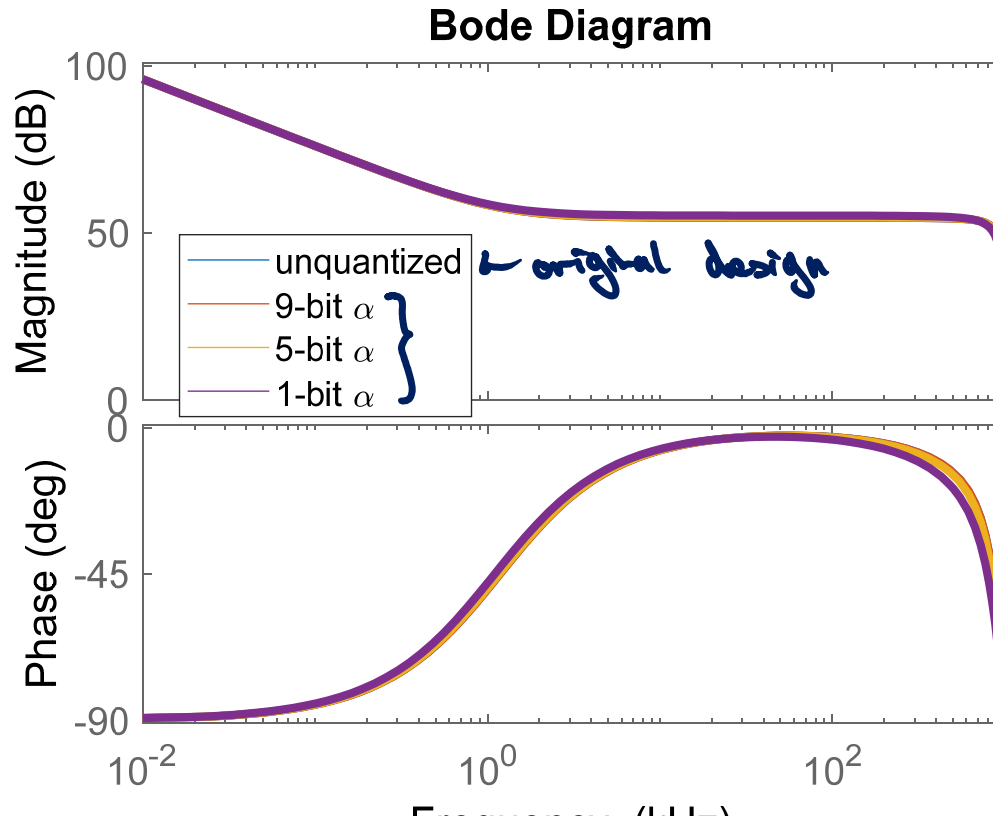
$k_{p2}$  &  $\alpha$  need a binary digital representation bit length

$$k_{p2} \approx \tilde{k}_{p2} = 435 = 110110011_2 \rightarrow [\tilde{k}_{p2}]_0^{10=a+1} \leftarrow \text{resolution}$$

$$\alpha \approx \tilde{\alpha} = \left( \frac{1}{2} + \frac{1}{2^4} + \frac{1}{2^5} + \frac{1}{2^6} + \frac{1}{2^a} \right) = 0.6113$$
$$= (100111001_2) \frac{1}{2^a} \rightarrow [\tilde{\alpha}]_{-q}^{10=q+1}$$

# Fixed-Point Storage

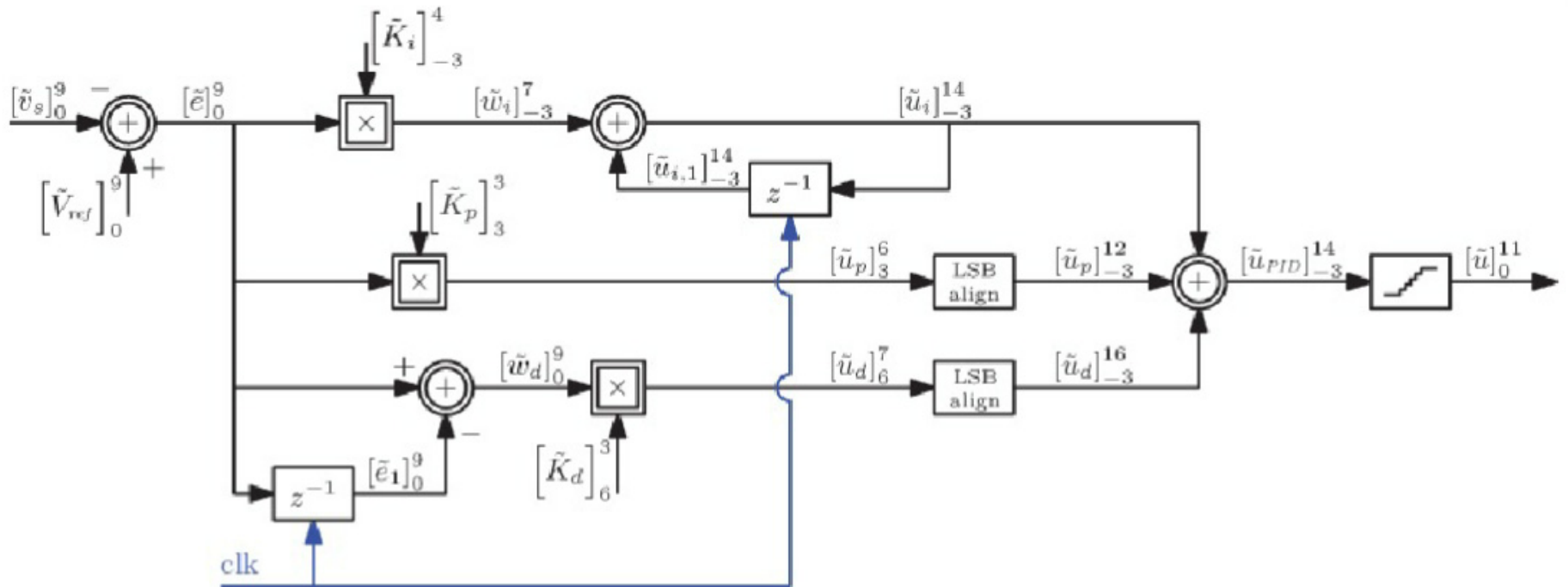
# Quantized $G_c(z)$



original  
 $\varphi_m = 71^\circ @ 250 \text{ kHz}$

1-bit  $\alpha$   
 $\varphi_m = 68^\circ @ 268 \text{ kHz}$

# Example Implementation



# MATLAB Tools

## Fixed Point Arithmetic

Block Parameters: Sum1

Sum

Add or subtract inputs. Specify one of the following:  
a) character vector containing + or - for each input port, | for spacer between ports (e.g. ++|-|+++)  
b) scalar, >= 1, specifies the number of input ports to be summed.  
When there is only one input port, add or subtract elements over all dimensions or one specified dimension

Main Signal Attributes

Require all inputs to have the same data type

Accumulator data type: `fixdt(0,13,2)` >>

Output minimum: `[]` Output maximum: `[]`

Output data type: `fixdt(0,16,5)` <<

Data Type Assistant

Mode: `Fixed point` Signedness: `Unsigned` Word length: `16`  
Scaling: `Binary point` Fraction length: `5`  
Data type override: `Inherit` [Calculate Best-Precision Scaling](#)

[Fixed-point details](#)

Representable maximum: `2047.96875`  
Output maximum: `[]`  
Output minimum: `[]`  
Representable minimum: `0`

Precision: `0.03125` [Refresh Details](#)

Lock data type settings against changes by the fixed-point tools

Integer rounding mode: `Floor`

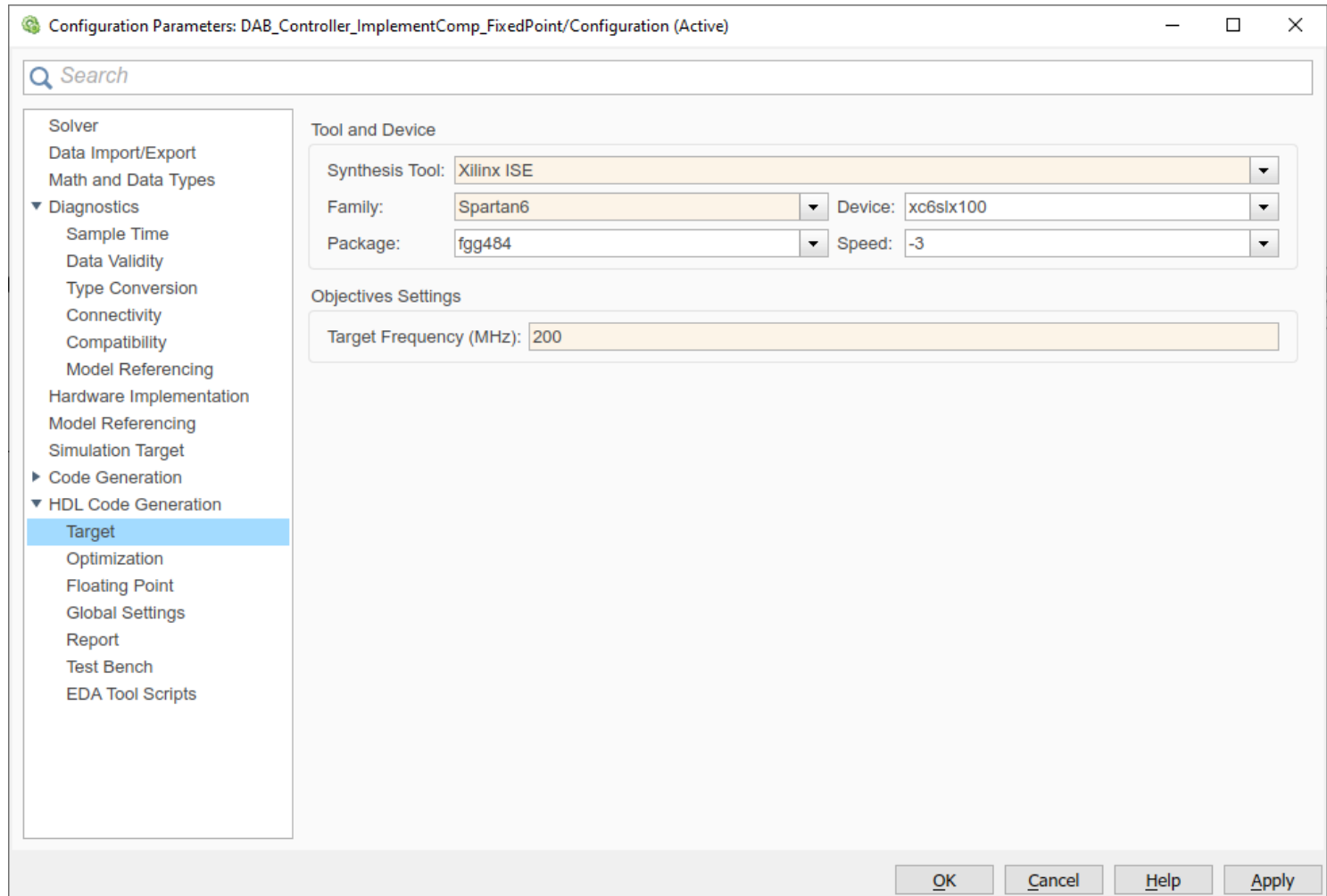
Saturate on integer overflow

[?](#) [OK](#) [Cancel](#) [Help](#) [Apply](#)



# MATLAB Tools

## VHDL Coder



# MATLAB Tools

## Fixed Point Tool

Fixed-Point Tool - Converting "CompSynthesis/Compensator"

FIXED-POINT TOOL EXPLORE

System Under Design: CompSynthesis/Com...

Simulation Ranges: Derived Ranges

Prepare Collect Ranges

Settings Signal Tolerances MATLAB Functions Propose Data Types Apply Data Types Simulate with Embedded Types Compare Results

PREPARE SYSTEM COLLECT RANGES CONVERT DATA TYPES VERIFY

MODEL HIERARCHY

- Simulink Root
  - Data Objects
  - CompSynthesis
    - Compensator

RUN BROWSER

- Ranges(Double)
- Run 1

Conversion Preparation

Results

Name	Run	CompiledDT	SpecifiedDT	SimMin	SimMax
Gain	Run 1	fixdt(1,12,0)	Inherit: Same as i...	0	0
Gain1	Run 1	fixdt(1,21,0)	fixdt(1,21,0)	0	0
Gain2	Run 1	fixdt(1,21,0)	fixdt(1,21,0)	0	0
Saturation2	Run 1	fixdt(0,14,0)	Inherit: Inherit via ...	1519	1519
Sum : Accumulator	Run 1	fixdt(1,12,0)	fixdt(1,12,0)	0	0
Sum : Output	Run 1	fixdt(1,12,0)	Inherit: Same as a...	0	0
Sum1 : Accumulator	Run 1	fixdt(1,13,0)	fixdt(1,13,0)	0	1519
Sum1 : Output	Run 1	fixdt(1,13,0)	Inherit: Same as a...	1519	1519
Sum2 : Accumulator	Run 1	fixdt(1,32,0)	Inherit: Inherit via ...	0	1519
Sum2 : Output	Run 1	fixdt(1,32,0)	Inherit: Inherit via ...	1519	1519
Sum3 : Accumulator	Run 1	fixdt(1,21,0)	fixdt(1,21,0)	0	0
Sum3 : Output	Run 1	fixdt(1,22,0)	fixdt(1,22,0)	0	0

Visualization of Simulation Data

Histograms of all results in the model

RESULT DETAILS

Select a result to view details.

PREPARATION DETAILS