Experiment 0
Half Bridge Layout
ECE 482

The objectives of this experiment are:

- To understand layout parasitic and their mitigation in power electronics
- To design and fabricate a PCB for use in future experiments
- To become familiar with Altium software using a simplified circuit topology

I. Introduction

In this experiment, you will design a printed circuit board (PCB) for a half bridge + gate driver, that will later be used to implement a Boost converter. In experiment 3, you will design this boost converter. For the moment, it is sufficient to know that the inductor current may be as high as 15A, and the dc bus voltage may be as high as 50V. The schematic and all component footprints are given in the supplied starter files.

PCBs will be fabricated using OSH Park 2-Layer Super Swift Service,

https://docs.oshpark.com/services/super-swift/

You will receive the required minimum 3 copies of your design. Your PCB should not exceed 4 in^2.

II. Half Bridge PCB Layout

A starter project in Altium is provided with this procedure. You should not need to edit the schematic, and may not alter part footprints or remove any components. The goal of this experiment is to complete the PCB layout of this schematic within the limitations on total PCB area.

Watch the recorded lectures posted to the course website along with this experiment. These videos cover topics related to power converter layout and practical implementation. After watching the lectures, complete the PCB layout of the half bridge power stage prioritizing (in order)

1. Power loop
2. Gate drive loops
3. All other connections

III. Deliverables

You will not complete a lab report for this experiment. Follow instructions on the course website or OSH Park support page to generate a zip file of Gerber and NC-drill files to submit to OSH Park. The layout must successfully pass the OSH Park automatic file verification (run automatically when uploading the design files to the main page) before submitting to canvas.

Teams must submit, through canvas, one .zip archive of the completed PCB layout. The zip archive should contain the following file types from the Altium project:

1. PrjPcb
2. SchDoc
3. SchLib
4. PcbLib
5. PcbDoc

You do not need to submit gerber files in your assignment submission in Canvas as long as the files listed above correspond exactly to those used to generate the manufacturing files that you submitted to OSH Park. The instructor will review the Altium design and provide feedback with an opportunity to revise before purchasing the PCB.

In your submission, include your username and password (make sure to change your password to something not used for any other personal account) to the OSH Park webpage. Prior to submission, place only the design for this class into your cart under your account.