An example of diode referenced self-biasing is shown below.
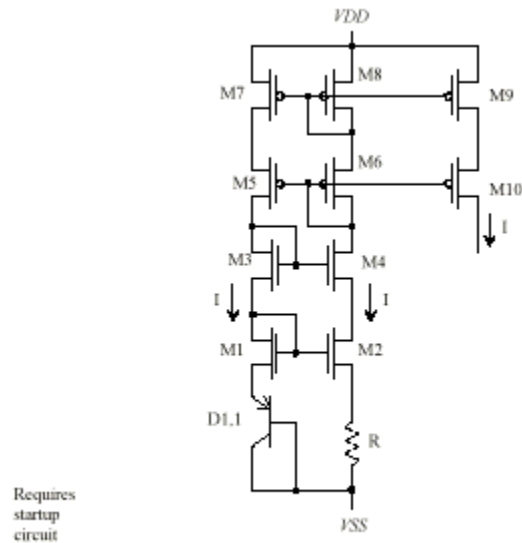

Figure 21.11 Diode referenced self-biasing circuit.

Since this circuit provides

$$I = \frac{V_d}{R} = I_s e^{V_d / n \cdot V_T} \,,$$

then *R* can be selected for a desired current level:

$$R = \frac{n \cdot V_T}{I} \ln \frac{I}{I_s}$$

This technique provides better matching on the same die, chip-to-chip, or wafer-to-wafer, compared to threshold voltage self-biasing. Again, however, a largely negative temperature coefficient is obtained. Note that TCV_d is approximately –2mV/°C (–3,300ppm/°C) for a 0.6V forward bias.

Connecting the parasitic *pnp* transistors as diodes help reduce the effective series resistance and substrate leakage.

The text provides diode-modeling information for simulating circuit like this one, including recommendations on how to estimate I_s.

An example of **thermal voltage referenced self-biasing** is shown below. As with the previous self-biasing techniques, a pMOS current mirror is used to force equal currents through each leg (i.e., VDD to VSS current path) of the circuit. Then, since the two diode connected parasitic pnp transistors have unequal emitter areas ($A_{E,D2} = K \cdot A_{E,D1}$, where K is an integer), the voltage across R is

$$IR = V_{d1} - V_{d2}$$

$$IR = \left(nV_T \cdot \ln \frac{I}{I_s} \right) - \left(nV_T \cdot \ln \frac{I}{K \cdot I_s} \right) = nV_T \cdot \ln \left(\frac{I/I_s}{I/(K \cdot I_s)} \right) = nV_T \cdot \ln K$$

Then

$$R = \frac{nV_T \cdot \ln K}{I} = \frac{nk \cdot \ln K}{qI} \cdot T \qquad \text{or} \qquad I = \frac{nk \cdot \ln K}{qR} \cdot T$$

RESULT $\Rightarrow$ A PTAT current! (PTAT $\equiv$ proportional to absolute temperature)

Recall that the previously discussed techniques provide currents with negative temperature coefficients.
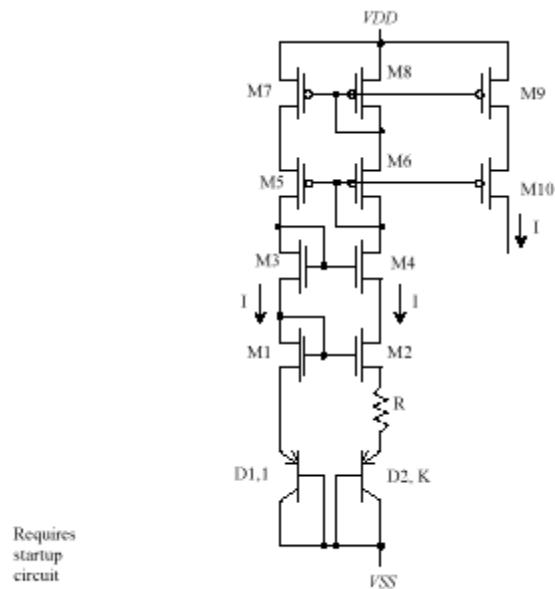

Figure 21.12 Thermal voltage referenced self-biasing circuit.

PTAT biasing is important in analog design. Here is one simple example why. Consider the temperature dependence of the BJT's transconductance:

$$g_m = \frac{I_C}{V_T} = \frac{qI_C}{kT}$$

If I_C is increasing linearly with temperature (a PTAT circuit could provide this), then g_m will remain constant over temperature.

In the design of the PTAT, matching between M1 and M2 is critical. If for example $n = 1$ and $K = 8$, then the voltage drop across R is only about 50mV. This could be comparable to $|V_{GS1} - V_{GS2}|$ if M1 and M2 are not well matched. Another potential problem is external (outside the reference circuit) noise coupling across R. The susceptibility of R to external noise will depend on how R is implemented.

Also note the absolute accuracy of I could vary 20% wafer-to-wafer, dependent upon the absolute accuracy of R. A precise I would require trimming. For example, some manufacturers might laser trim R.

The forte of this circuit is its temperature performance.

$$TC_I = \frac{1}{I} \cdot \frac{dI}{dT} = \frac{1}{V_T} \cdot \frac{\partial V_T}{\partial T} - \frac{1}{R} \cdot \frac{\partial R}{\partial T} = TC_{V_T} - TCR$$

The thermal voltage's temperature coefficient is given by

$$TC_{V_T} = \frac{1}{V_T} \cdot \frac{\partial V_T}{\partial T} = \frac{q}{kT} \cdot \frac{k}{q} = \frac{q}{kT} \cdot \left(0.085\text{mV/}^\circ\text{C}\right) \cong +3{,}300 \text{ ppm/}^\circ\text{C [or ppm/}^\circ\text{K]}$$

If TCR is approximately 2,000ppm/°C, then TC_I will be around +1,000ppm/°C (near room temperature). TC_I, just as with any previously discussed TC analysis, is temperature dependent.

Example 21.3 in the textbook provides helpful tips for simulating reference circuits.

Bandgap voltage references

Bandgap voltage references, if properly designed, can achieve extremely low temperature coefficients. A low *TC* is achieved by summing the negative *TC* of a diode's forward voltage (E_g of Si decreases with temperature — see chapter 9) with the thermal voltage's positive *TC*.

An example of **bandgap reference biasing** is shown below. The circuit's output, V_{ref}, is determined by the voltage across a series-connected resistor-diode combination which is biased by a thermal voltage referenced current. In the schematic, *L* signifies that the rightmost resistor is *L* times larger than the leftmost resistor. Diodes D2 and D3 are equal in size. The bandgap voltage reference's output is given by

$$V_{ref} = I \cdot L \cdot R + V_{d3} = L \cdot (IR) + V_{d3} = L \cdot (nV_T \cdot \ln K) + V_{d3} \qquad \text{[w.r.t. } VSS]$$
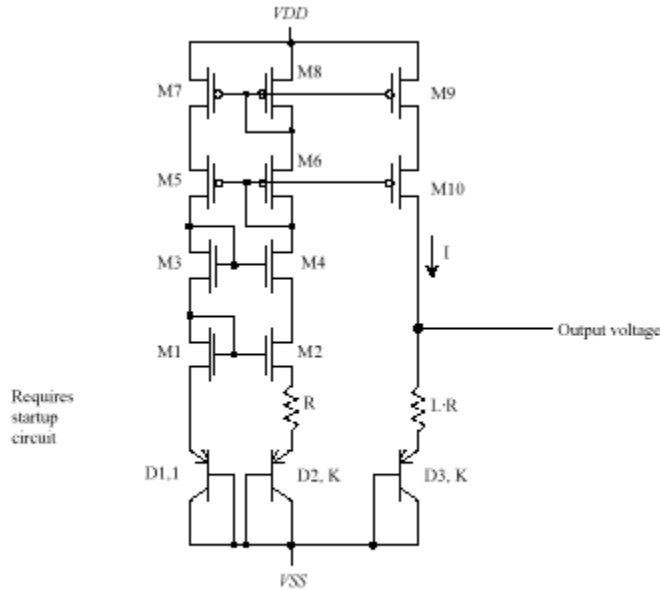

Figure 21.14 A bandgap voltage reference.

From the above expression, *TC* for V_{ref} is readily obtained.

$$TC_{V_{ref}} = \frac{1}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial T} = \frac{1}{V_{ref}} \cdot \left[L \cdot n \cdot \ln K \cdot \frac{\partial V_T}{\partial T} + \frac{\partial V_{d3}}{\partial T} \right] = \frac{1}{V_{ref}} \cdot \left[L \cdot n \cdot \ln K \cdot (0.085 \text{mV/}^\circ\text{C}) + (-2\text{mV/}^\circ\text{C}) \right]$$

Then, for V_{ref} to have a temperature coefficient of zero,

$$L \cdot n \cdot (\ln K) = \frac{2}{0.085} = 23.5$$

An alternate expression for V_{ref}, for a given current, is provided by

$$V_{ref} = (Ln \ln K) \cdot V_T + nV_T \cdot \ln \frac{I}{K \cdot I_s} = n \cdot \left(\frac{kT}{q}\right) \cdot \left(L \ln K + \ln \frac{I}{K \cdot I_s}\right)$$

At room temperature, a V_{ref} value of 1.25V is obtained for $I = 10\mu A$, $n = 1$, $I_s = 10^{-15}A$, $K = 8$, and $L = 12$. Note, however, that accurate predictions of V_{ref} across temperature and process corners require thorough characterization of the parasitic *pnp* transistors (to obtain accurate values for n and I_s).

The result of a simulation example of the bandgap voltage reference is shown below. Note the small variation in V_{ref} over a wide temperature range.
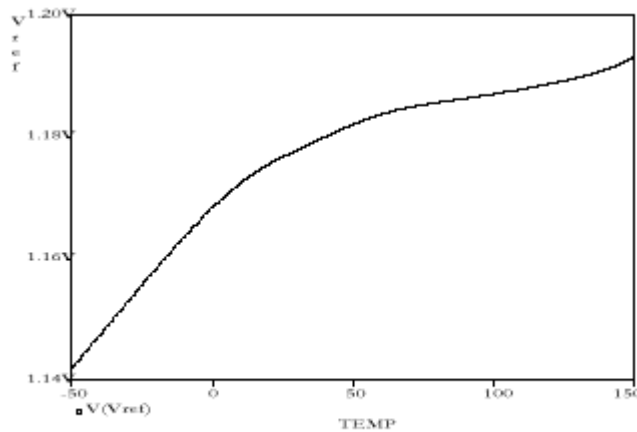

Figure 21.15 PSPICE simulation results of a bandgap voltage reference.

Beta Multiplier Referenced Self-Biasing

The **beta multiplier current reference** circuit provides an alternate scheme for (possibly) obtaining a PTAT-like current without using bipolar transistors. The basic form of the beta multiplier current reference is shown in the schematic below (excluding startup circuit). Note that the overall width of M2 is K times larger than M1 and $L_1 = L_2$ to provide $\beta_2 = K \cdot \beta_1$.
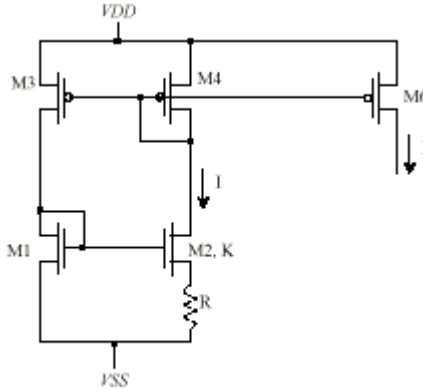

Figure 21.16 β multiplier referenced self-biasing (β₂ = K·β₁).

Neglecting mismatch and λ effects, the current mirror M3, M4 provides $I_{D1} = I_{D2}$. Applying KVL, we obtain

$$V_{GS1} = V_{GS2} + IR$$

After substituting for V_{GS} and neglecting body effect, channel-length modulation and mobility modulation,

$$\left(\sqrt{\frac{2I}{\beta_1}} + V_{THN} \right) = \left(\sqrt{\frac{2I}{\beta_2}} + V_{THN} \right) + IR$$

$$\left(\sqrt{\frac{2I}{\beta_1}} + V_{THN} \right) = \left(\sqrt{\frac{2I}{K \cdot \beta_1}} + V_{THN} \right) + IR$$

Solving for I provides the design equation for the beta multiplier current reference:

$$I = \frac{2}{R^2 \beta_1} \cdot \left(1 - \sqrt{\frac{1}{K}} \right)^2 \qquad \text{[SI sat.]}$$

Note the design variables that determine $I \Rightarrow$ ratioed gate widths (K) and the value of a single passive component (R).

The temperature coefficient for this reference's output current is described by

$$TC_I = \frac{1}{I} \cdot \frac{\partial I}{\partial T} = -2 \cdot \frac{1}{R} \frac{\partial R}{\partial T} - \frac{1}{KP(T)} \frac{\partial KP(T)}{\partial T} = -2 \cdot TCR + \frac{1.5}{T}$$

Obviously the resistor temperature coefficient (TCR) has significant impact on TC_I. In fact, TCR will determine if this reference achieves PTAT performance.

A practical example of a beta multiplier current reference is provided in example 21.4. The schematic for this example is included below. This circuit achieves a TC_I of 1,000ppm/°C at room temperature using a resistor with $TCR = 2000$ppm/°C. Note also the use of cascode MOSFETs to minimize the influence of finite MOSFET r_o.
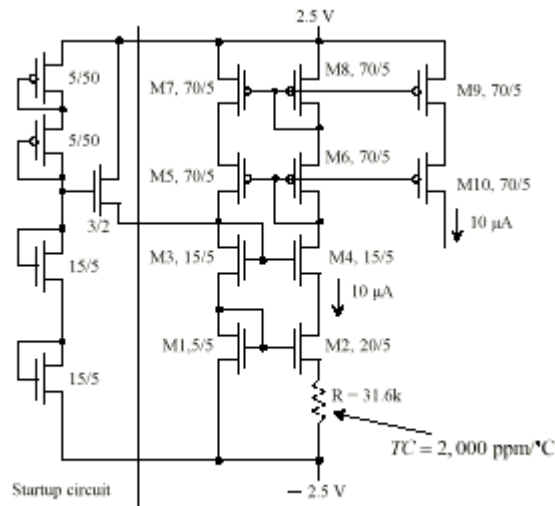

Figure 21.17 A 10 μA reference using a transconductance multiplier self-biased reference.

Recognize that the absolute accuracy of R dramatically effects the absolute accuracy of I. Additional sources of error for this circuit include device mismatch and body effect. Again, however, this technique does not require bipolar transistors that would need thorough characterization.

The same circuit can also used as a **beta multiplier voltage reference**. In this case, $V_{ref} = V_{GS1}$. In terms of current, we have

$$V_{ref} = V_{GS1} = \frac{2}{R\beta_1}\left(1 - \frac{1}{\sqrt{K}}\right) + V_{THN} \qquad \text{[SI sat.]}$$

Using this result, the change in V_{ref} with temperature can be predicted.

$$\frac{dV_{ref}}{dT} = \frac{dV_{THN}}{dT} - \frac{2}{R\beta_1}\left(1 - \frac{1}{\sqrt{K}}\right)\left[\frac{1}{R}\cdot\frac{\partial R}{\partial T} + \frac{1}{KP(T)}\cdot\frac{\partial KP(T)}{\partial T}\right]$$

And at room temperature, assuming TCR is 2,000ppm/°C, we obtain

$$\frac{dV_{ref}}{dT} = -2.4\frac{mV}{°C} + \frac{2}{R\beta_1}\left(1 - \frac{1}{\sqrt{K}}\right)\left[-2,000\frac{ppm}{°C} + \frac{1.5}{T}\right]$$

Selecting $K = 4$, a value for R can be determined that provides a temperature coefficient of zero for V_{ref}:

$$R = \frac{1}{0.8\cdot\beta_1}$$

The value of V_{ref} associated with this R is

$$V_{ref} = 0.8 + V_{THN} = 1.63\text{V}$$

in CN20 technology. Sources of error include variations in V_{THN}, R, are β and the change in T. Note that V_{THN} also depends on body effect. Often times, however, body effect is ignored since V_{THN} can sometimes vary up to 20%.

Its susceptibility to process variations make the beta multiplier voltage reference difficult to use as a precision voltage reference. The bandgap voltage reference circuit is better suited for use as a precision voltage reference.

Low-power CMOS reference design can utilize MOSFETs operating in the **subthreshold region**. Circuits using subthreshold (weak inversion) MOSFETs can consume less than 100nA. At such low current levels, obviously the basic current mirror and resistor biasing scheme should not be used due to the excessively large value of resistance required.

Recall that the saturated weak inversion MOSFET's drain current is given by

$$I_{Dn} = I_{DO} \frac{W}{L} \left(e^{(V_{GS} - V_{THN})/n \cdot V_T} \right)$$

Operating the beta multiplier reference circuit in weak inversion provides

$$V_{GS1} = V_{GS2} + IR$$

$$nV_T \cdot \ln\left[\frac{I \cdot L}{I_{DO} \cdot W} \right] + V_{THN} = nV_T \cdot \ln\left[\frac{I \cdot L}{I_{DO} \cdot K \cdot W} \right] + V_{THN} + IR$$

Then, solving for *I*, we obtain

$$I = \frac{n \cdot V_T}{R} \cdot \ln K$$

This result is identical to that of the thermal voltage referenced self-biasing technique! But without using BJTs and, most likely, less power.

Example 21.6 demonstrates using the beta multiplier in weak inversion. See the output current characteristic in Figure 21.19 of the text. The factor of two error in output current is due to body effect. Unless *p*MOS devices in the their own wells are used, the weak inversion beta multiplier will be very sensitive to body effect. Variations in *R* will also significantly effect the current.

Weak inversion operation of the beta multplier current reference also minimized its output voltage requirements.

Note also that in subthreshold operation the beta multiplier circuit can be used as a bandgap-like voltage reference.