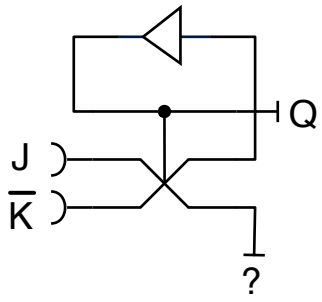

Figure II.27: Implementation of J-$\bar{\text{K}}$ flip-flop (adapted from Fredkin & Toffoli (1982)).

E Exercises

Exercise II.1 Show that the Fredkin gate is reversible.

Exercise II.2 Show that the Fredkin gate implementations of the NOT, OR, and FAN-OUT gates (Fig. II.16) are correct.

Exercise II.3 Use the Fredkin gate to implement XOR. Minimize the number of Fredkin gates you use.

Exercise II.4 Show for the eight possible inputs that Fig. II.17 is a correct implementation of a 1-line to 4-line demultiplexer. That is, show in each of the four cases $A_1A_0 = 00, 01, 10, 11$ the bit $X = 0$ or 1 gets routed to Y_0, Y_1, Y_2, Y_3, respectively. You can use a Boolean algebra proof, if you prefer.

Exercise II.5 Show that implementation of a J-$\bar{\text{K}}$ flip-flop with Fredkin gates in Fig. II.27 is correct. A J-$\bar{\text{K}}$ flip-flop has the following behavior:

J	$\bar{\text{K}}$	behavior
0	0	reset, Q $\rightarrow$ 0
0	1	hold, Q doesn't change
1	0	toggle, Q $\rightarrow \bar{\text{Q}}$
1	1	set, Q $\rightarrow$ 1

Exercise II.6 Show that the inverse of the interaction gate works correctly. Hint: It only needs to work correctly for outputs that actually occur. Therefore, to invert a *pq* output, balls must be shot into outputs A and D simultaneously.

Exercise II.7 Show that the realization of the Fredkin gate in terms of interaction gates (Fig. II.26) is correct, by labeling the inputs and outputs of the interaction gates with Boolean expressions of a, b, and c.