ECE-255 Project #1

Design of a 4-bit Adder Using FPGA with Schematic Capture and VHDL

Objectives
1. Design a circuit diagram for a full 1-bit adder using the schematic editor and generate a graphical symbol.

2. Design a 4-bit carry lookahead adder using four 1-bit adders and schematic capture.

3. Implement your adder using the Diligent Basys FPGA boards. Use the switches and board LEDs as the inputs and outputs respectively.

4. Implement your adder using VHDL code.

Procedure

1. Develop (a) equations for a generic s_i, each c_i, and the arithmetic overflow, and then (b) a circuit diagram and VHDL code for your adder.
2. Use schematic capture to lay out your circuit and then program the FPGA.

Specifications

Assume that only positive numbers are inputted. Therefore, the maximum value of each input is 15 and the maximum value of the output is 15. Your output should be 4 sum bits plus a bit that indicates whether or not arithmetic overflow has occurred. Your adder should not produce a carryout bit.

Results
1. Have the course instructor or TA verify that your design works; he will try various combinations of inputs to see if the output is correct.
2. Your report should contain the following:
   a. Equations, schematic, VHDL code
   b. Simulation results.
   c. Check off by TA or instructor.