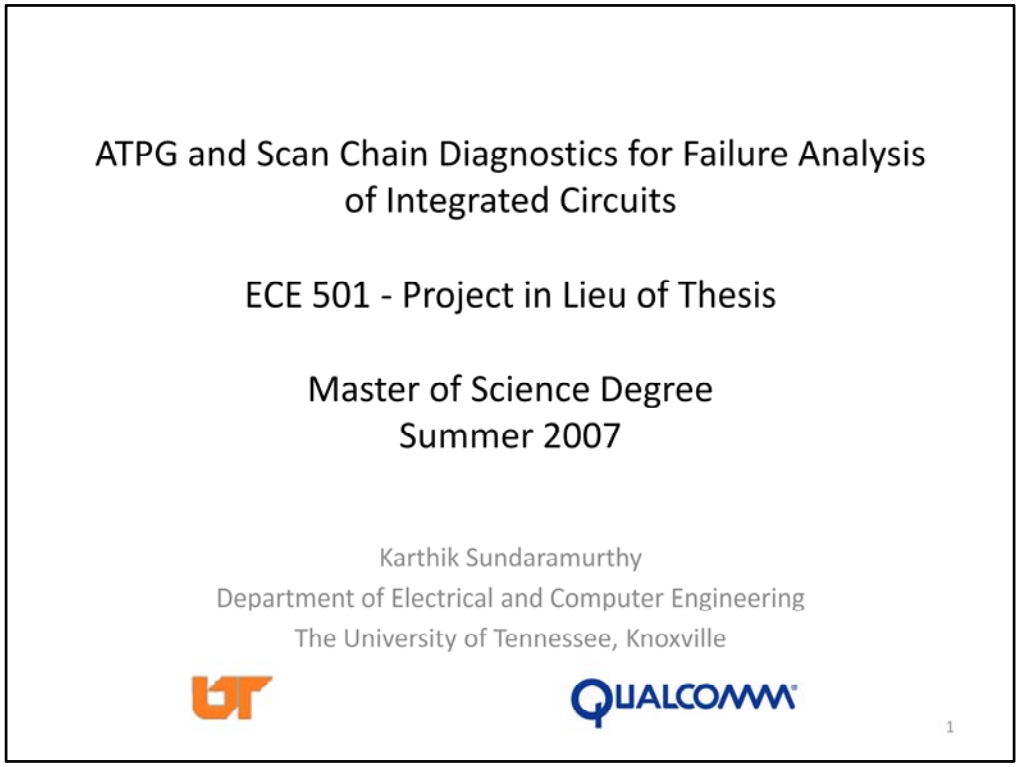
ATPG and Scan Chain Diagnostics for Failure Analysis of Integrated Circuits
ECE 501 - Project in Lieu of Thesis
Master of Science Degree
Summer 2007
Karthik Sundaramurthy
Department of Electrical and Computer Engineering
The University of Tennessee, Knoxville
QUALCOMM
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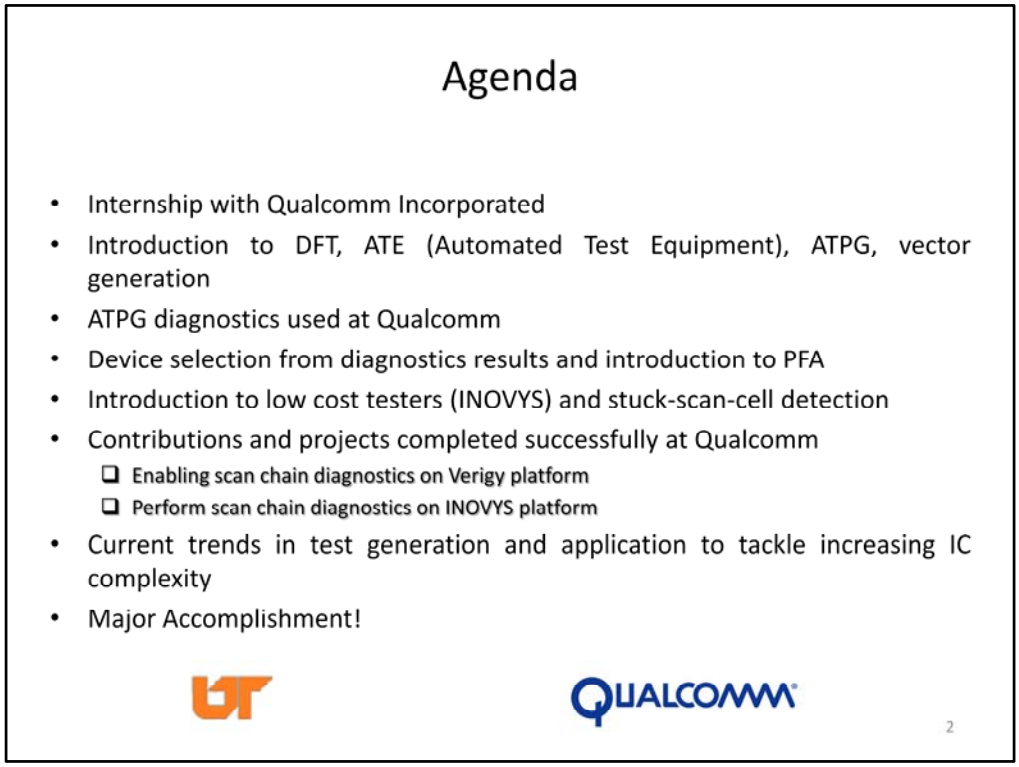
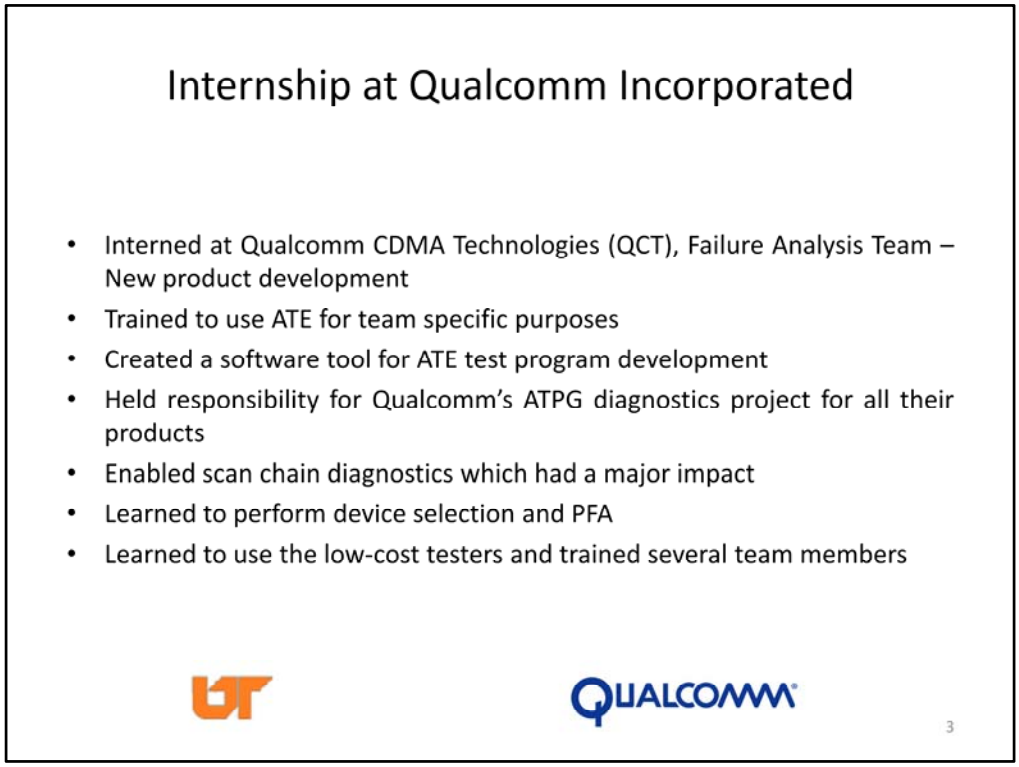
Title slide.



Agenda for the project presentation is as follows. I will be discussing about my internship with Qualcomm Incorporated, San Diego, CA. I was responsible for part of a huge project called ATPG Diagnostics. I will be discussing about the project flow, equipment used and my contributions to this project. The post processing steps such as candidate selection from diagnostic results and PFA will also be discussed. I will go over another successful project called scan chain diagnostics, which I enabled on the Verigy as well as the INOVYS platform. I'll also be going over the current trends in testing in the semiconductor industry as it is a crucial investment for a company. Finally, one of my major accomplishments will be presented.



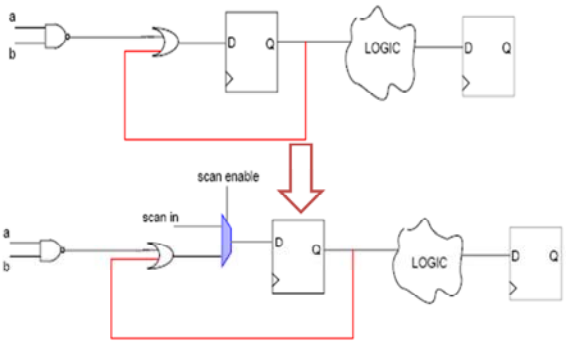
I had an excellent opportunity to pursue an internship with Qualcomm Incorporated. I was with the Failure Analysis Team and was involved in new product development. The main purpose for our team was to find new ways to find the causes for defects and failures in our products. Several FA tools and equipment are used for this purpose. Several home grown innovative projects were also being used, one of which was ATPG diagnostics. I started off creating several software tools for team-specific purposes and got trained on the automated test equipment.

In the summer term I was getting trained on the software tool created for ATPG diagnostics, its usage and all the post processing steps. I was also introduced to task of performing device selection from the diagnostics results and PFA. Out of personal interest I also created several software tools using Perl to automate several processes. Later on in the Fall term I was responsible for the whole project for all the Qualcomm products. With this project we initially were not able to account for scan chain failures. Our test flow would just bin those devices which failed the scan chain integrity test and would not collect the failing pin and failing cycle information and process them. So, I developed a C++ test method to automate this process of testing scan chain failing dice and collecting the fail information. This test method could be run on the ATE with a custom test program built specifically for that. This project had a huge impact because the results were so crucial for our team as well as Qualcomm.

I also got a chance to work on the low-cost INOVYS testers and performed scan chain diagnostics on the INVOYS platform. My research yielded interesting results which were really important for us.

What is DFT?

- Methodology to increase testability
- Testability is an extent up to which a design can be tested
- Difficult to purely test with functional vectors
  - ❑ Functional test objective is conformation to design specs
- Controllability and observability are the key issues



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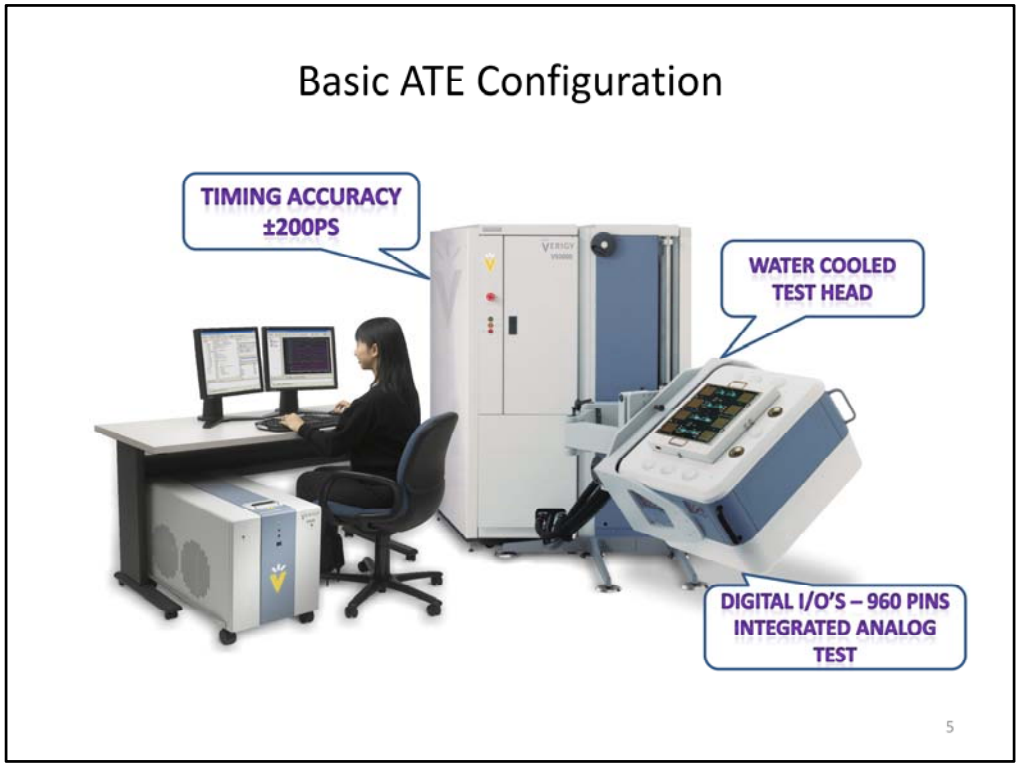
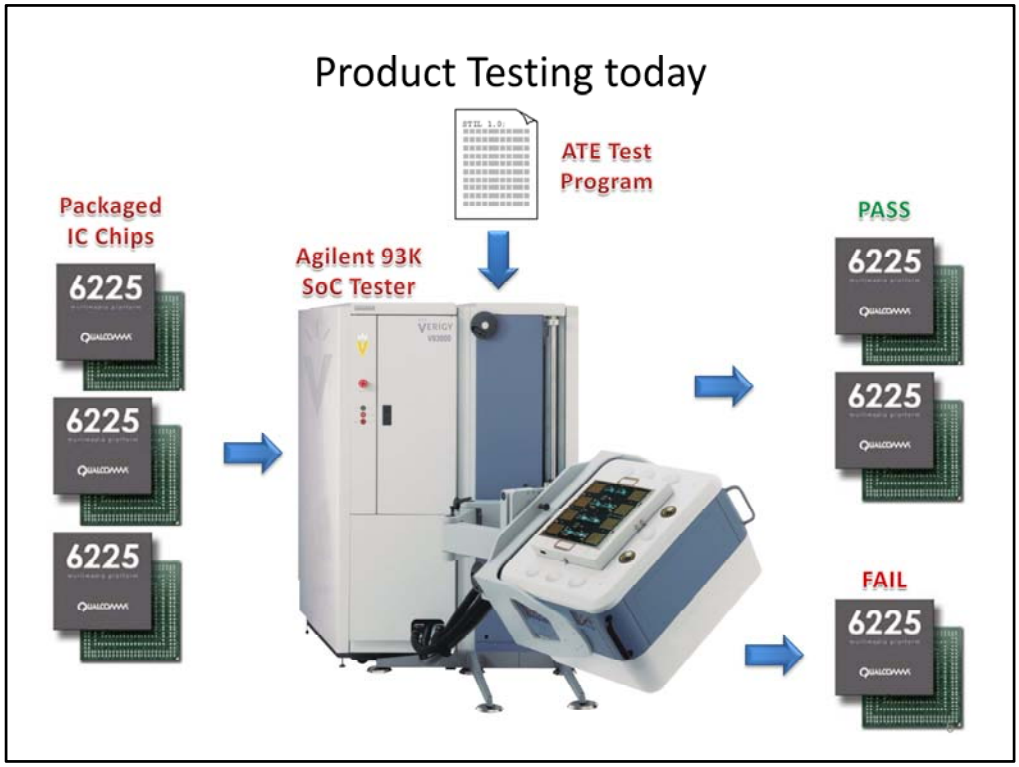
The following slides give a very basic introduction to DFT, ATE and their basic usage as these details will be required as a starting point for the slides to follow. These slides will help anyone to get some insight into how testing is done in the industry today and also to follow the slides that explain the project. DFT or design for test is a methodology to increase testability. It is the extra design effort invested in making an IC testable. Testability enhances controllability and observability in the design. For example, in the schematic shown above, by including the additional multiplexer in the front of the flop or scan cell, the ability to control the inputs and outputs increases due to the additional pin which has been inserted. This makes the normal flip-flop into a multiplexed flip-flop or a scan type flip-flop.



This slide explains the basic ATE's configuration and illustrates state-of-the-art SoC test equipment. The ATE industry has been developing high cost equipment with several capabilities to meet the growing SoC testing requirements. The test system hardware is controlled by a computer which executes a set of instructions (test program). The tester must present the correct voltages (levels file), currents, timings (timing file) and vectors to the DUT (device under test) and monitor the response for each test. The ATE operates at a very high frequency, has a high pin count of ~960 pins and is integrated with analog test capabilities to test the analog blocks in a SoC. The test head is water cooled and houses the pin electronics card which enables the PIs (primary inputs) to be driven and POs (primary outputs) to be observed. Inside the ATE there are programmable clock generators that synchronize the DUT to the ATE during the test program. In general all the clocks fed into the DUT are of the same frequency but the phase may differ. The cost of these high end production ATEs are around 1 – 1.5 million dollars.



This slide gives a very basic introduction to how product testing is performed today in the semi-conductor industry. Product testing is still a PASS/FAIL proposition. The main equipment required for testing packaged ICs is the ATE (automated test equipment) whose capabilities are discussed in the next slide. A custom built test program (a lengthy series of tests for potential defects) must first be built to screen the devices and bin them appropriately based on the FAIL category. If a unit fails, it is discarded and sent to the Failure Analysis lab for analyzing the reasons for failure. Units which pass all the tests are shipped to the customers.

The Test Program

- Controls the test hardware such that the DUT meets its design specs
- It is segmented into various parts such as DC tests, functional tests, AC tests and structural tests
- Controls the test system hardware such that each test gives a PASS/FAIL result
- Separates devices into categories based on their performance – binning
- Test methods (structural tests) are used in addition to pre-defined routines depending on the H/W and S/W capabilities of the ATE
- Several constraints have to be considered while building a test program like
  - ❑ Hardware limitations – Test H/W should meet the timing requirements, operating frequency, external hardware
  - ❑ Throughput
  - ❑ Loadboard tests
  - ❑ Power and ground, voltage and current requirements for the DUT
  - ❑ DUT pins to tester pin mapping

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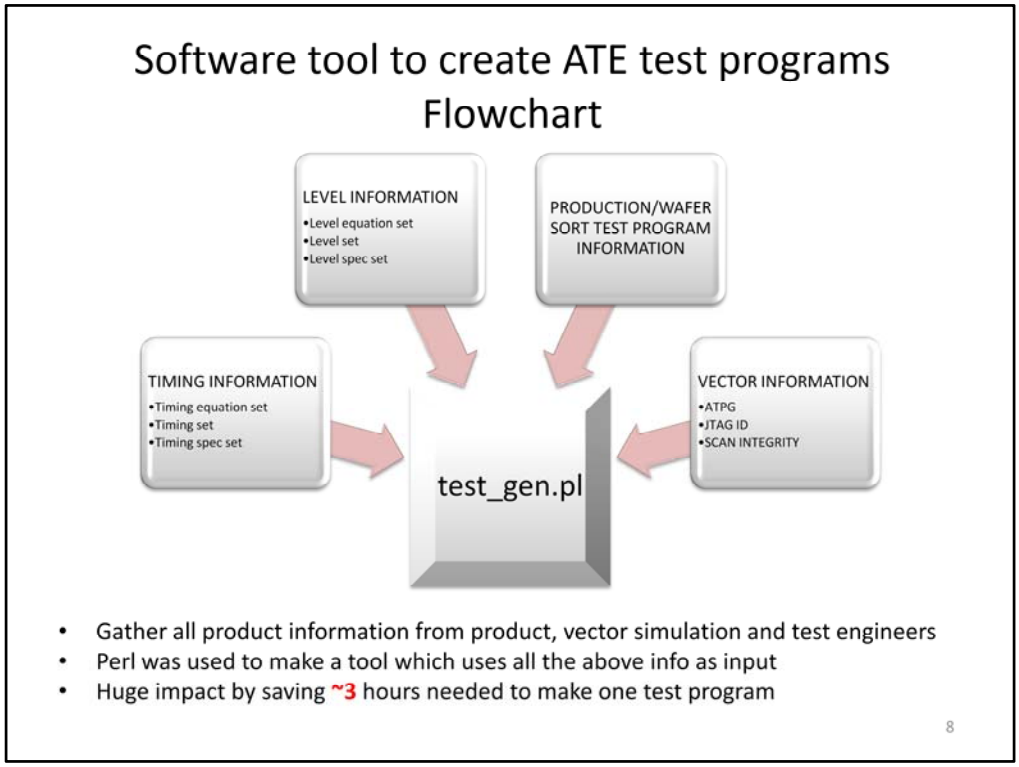
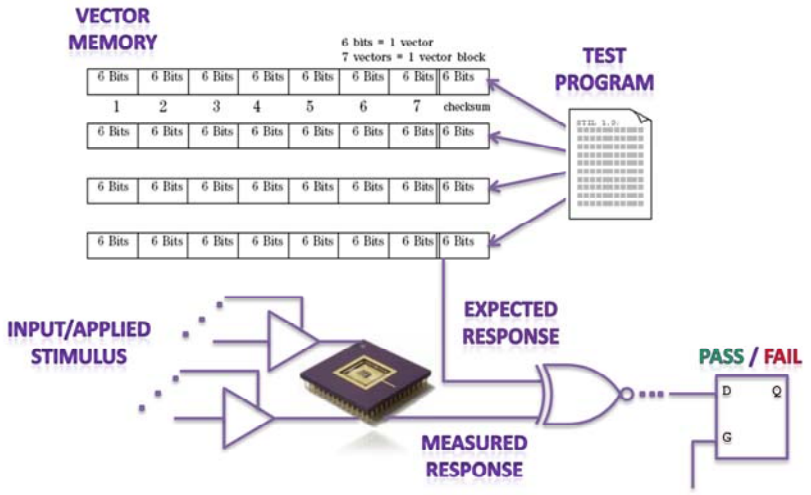
The test program details are explained in this slide.



This flow chart shows the inputs that the software tool required. All the timing and levels information for the test suites used in our flow had to be collected from the test engineers. A test program used for product testing and wafer sort testing is also required by the tool. Most importantly, all the vectors that each of the test suite requires will also be required as they are the main requirement for the test program to run. Once all the desired information is obtained, the tool can be executed which will complete in a few minutes and create a complete test program for a specific device which is ready to be used on the ATE.

Fault Detection by Pattern Execution using ATE



If the measured response doesn't match the expected response a FAILURE is detected

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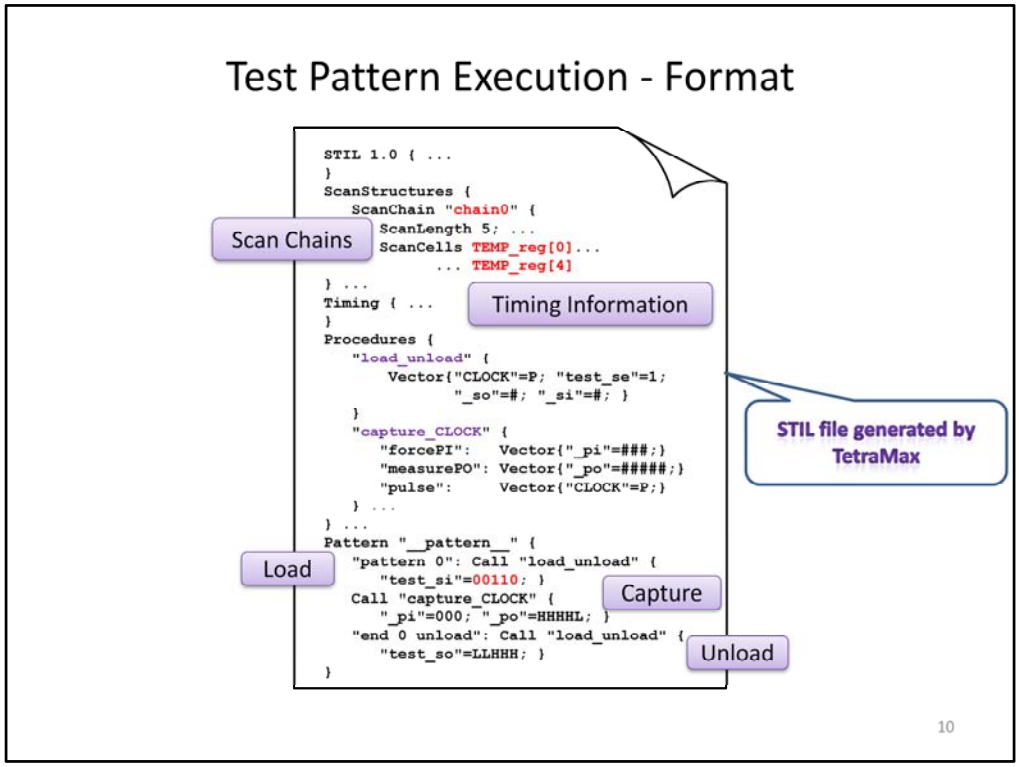
This slide explains how a fault detection is implemented by the ATE hardware. The basic criterion is that a fault is detected by an applied input if the measured output doesn't match the expected response. This is a conceptual diagram using differential comparators to detect the differences between the responses, if any.

The flow of events begins when the current test pattern is read out of pattern memory (it is loaded into the pattern/vector memory by the test program). Each pattern is read out of pattern memory and parsed into stimulus and response. Thus, the ATE derives the input stimuli from the pattern and applies it to the PIs of the DUT. The steady state output response is measured at the POs after a given amount of settling time. Both the measured and expected responses are compared by the comparator.

As already mentioned before, a fault is detected if the measured response from the DUT differs from the expected response. The PASS/FAIL result is strobed into the local pin memory and the FAIL data is logged into a file (with failing pin and failing cycle information).

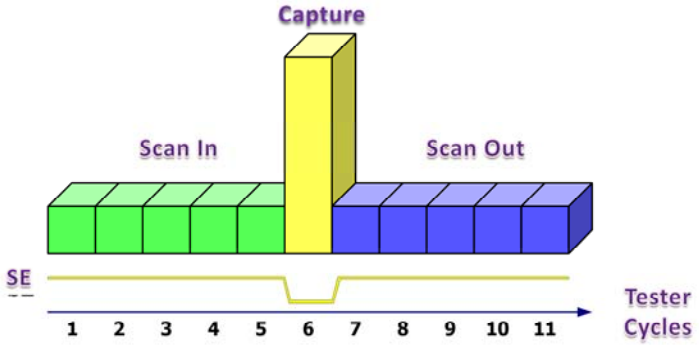


This slide explains how TetraMax creates the patterns and dumps them (writes out) into a STIL file. This is an example of an executable STIL file generated by TetraMax. STIL stands for standard test interface language and it is an industry standard. It encompasses a tester description of test patterns, pin timing protocol and scan paths. This example STIL files show how user procedures are created to concisely describe repetitive actions. Let us consider an example of a 5-bit scan chain chain_0.

Procedures load_unload asserts SE and shifts serial stimulus data into the scan chain, chain_0. Once the chain is loaded (after the load_unload procedure is complete) the scan chain TEMP_reg[4:0] will contain the scan data 00110. Here, pattern 0 targets a stuck-at-1 fault, that, if present, would cause the last bit (MSB) to freeze at '1'. The expected data captured into the scan chain and later scanned out is LLHHH as against LLHHL. If the ATE's measured response is H, instead of L in the last bit (MSB), then a stuck-at-1 fault is present. As explained above, a pattern is executed in three phases, LOAD, CAPTURE CLOCK and UNLOAD.

Thus a STIL file describes every detail needed for the ATE to execute a test pattern. The timing section also includes the pin timing definition which has been illustrated here.

Test Pattern Execution -Basic Waveform



- There are three phases involved while the ATE executes a pattern
  - ❑ Load all the scan chains (length varies for each pin)
  - ❑ Capture – one clock cycle
  - ❑ Unload all the scan chains

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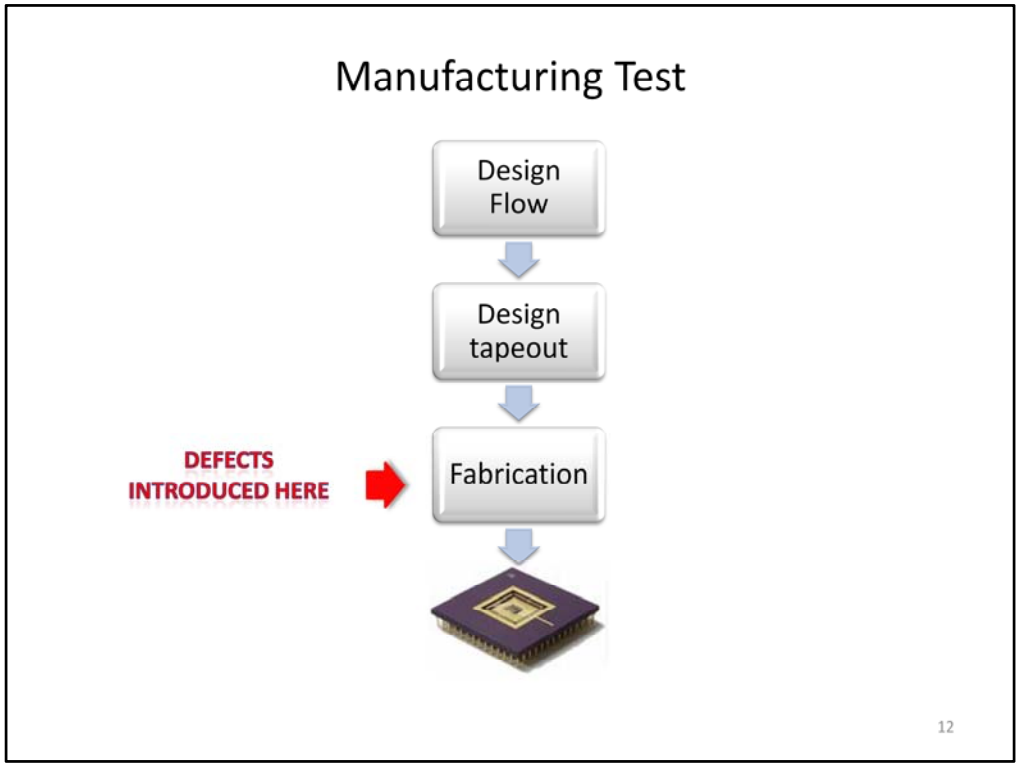
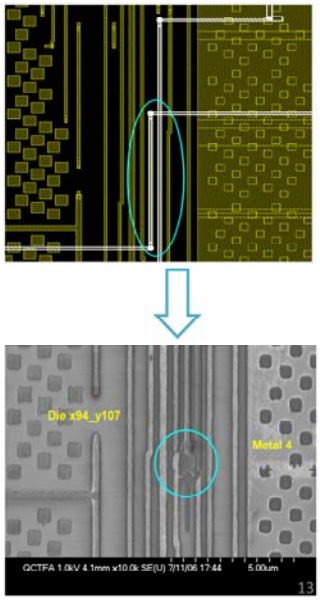
This slide is a graphical representation of the various stages that are required by a tester to execute a pattern. In the previous example, a 5-bit scan chain was considered, so it takes 5 tester cycles to load and unload each pattern. It takes one tester cycle for the ATE to perform the capture procedure, (force the PIs and observe the POs). A detailed explanation is included in the previous slide.



Details of how defects are introduced in a chip are explained here. Defects are generally introduced during the fabrication step. It is during fabrication that several processes and steps are followed and the chances of defects are really high. No fabrication process or plant can be 100% perfect. Given the number of steps that have to be carried out before producing a final product, a defect can be introduced anywhere. Therefore, high quality test programs are required to check for defects during manufacturing. Manufactured chips have to be tested regardless of the design flow. So testing checks for manufacturing defects in ICs.

Types of Defects

- Physical defects
  - ❑ Open circuit
  - ❑ Short circuit
  - ❑ Threshold voltage changes
- Fabrication defects
  - ❑ Silicon defects
  - ❑ Mask contamination
  - ❑ Defective oxide
  - ❑ Process variations
  - ❑ Photolithography defects
- Other defects
  - ❑ Material, time-dependent, packaging, etc.

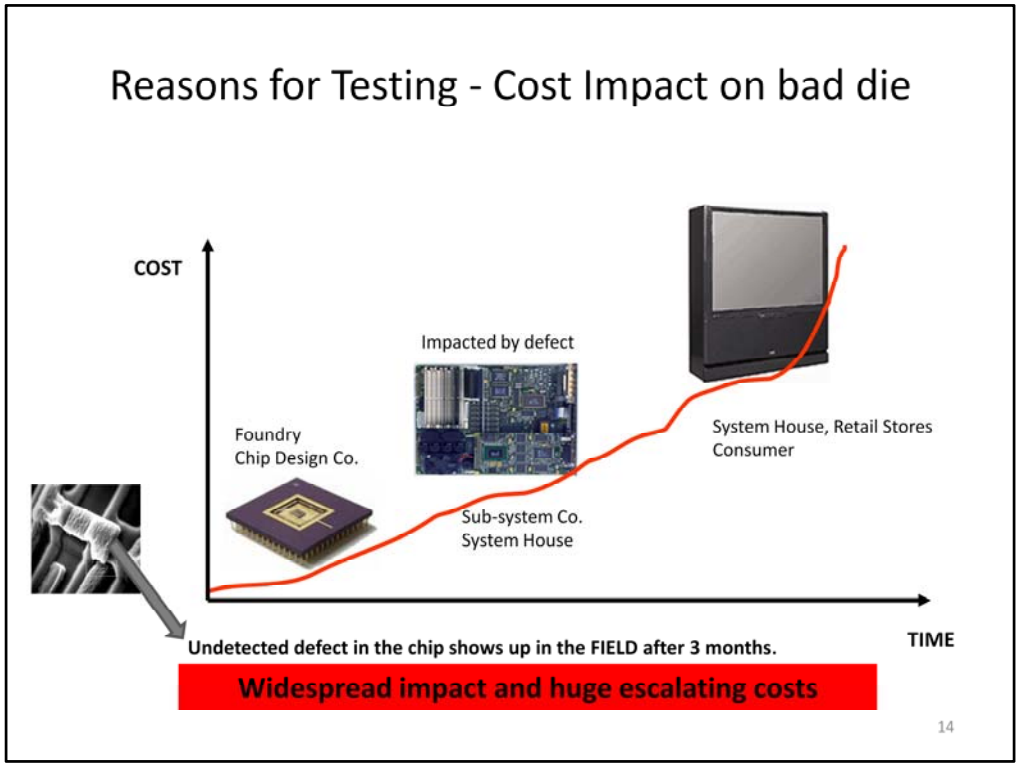


There are several defects that could be introduced in chips. A few of the most prominent defects are mentioned in this slide.

Physical defects are introduced mostly during packaging of an individual die or ASIC that causes the whole chip to malfunction. Physical defects could manifest themselves in several ways such as an open circuit, short circuit, etc. Physical defects can be easily found by probing every pin using a curve tracer to determine if it is shorted to ground or a neighboring pin or open. Once the exact pin is determined, the cause for the defect can easily be found using other FA techniques explained later.

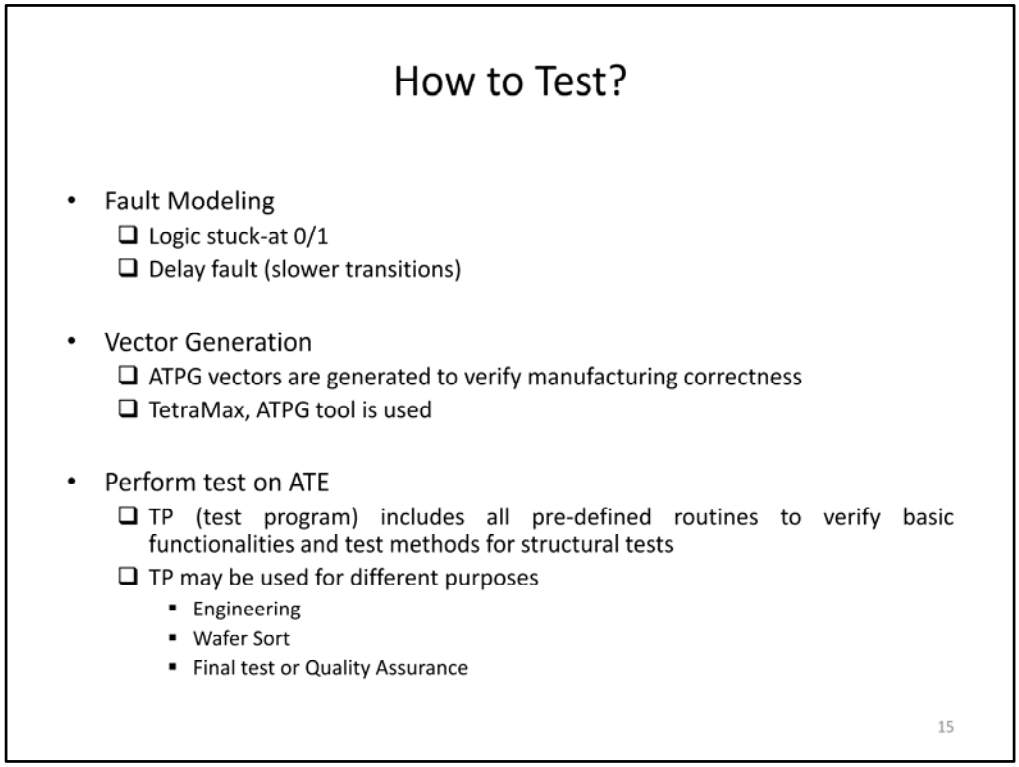
Fabrication defects are mostly introduced during several processes during fabrication. Some of the are mentioned in this slide. One of the most common fabrication defect is a bridging fault shown in the figure above. A bridging fault is caused by some sort of contamination or dust that is left between two adjacent metal lines of the same cell or different cells. Excess unetched metal can cause bridging or excess shorts to power or ground.

Other kinds of defects include material defects (cracks, crystal imperfection, surface impurities – ion migration or conductive holes on through insulating oxides) and time dependent defects (dielectric breakdown or electromigration).



This slide explains the most important reason (time to market) why testing and verification are very important. If a defect is determined early on in the cycle, the cost of correcting it is very low. As it passes on to successive levels, the cost increases exponentially. If a defect is determined once the product is shipped to the customers, the amount of loss a company would incur will be tremendous as all the products will have to be recalled and corrected chips have to be shipped. Thus time to market of a product is very crucial in the semi-conductor industry.

So it is extremely important for companies to have well defined verification and testing procedures.



This slide explains the basic requirements to perform testing. Most of the defects explained in the previous slides manifest themselves as stuck-at faults or even delay faults. So, the initial requirement is to come up with a specific fault model. An ATPG tool (usually TetraMax) is used to generate vectors to verify manufacturing correctness for the above mentioned fault models. Once the vectors are generated they are verified on the Automated Test Equipment (ATE) using a custom test program.

Then a final test program is built which uses the vectors and separates the devices by binning. ATEs have pre-defined routines to verify the basic functionalities like continuity of pins, etc, and test methods to perform certain structural tests like IDDQ, etc (but the vectors have to be generated for each device by vector simulation engineers). Several other custom test methods will also be used for performing other structural tests like ATPG and scan chain integrity which is explained in detail in the following slides.

Test programs are used for several different purposes staring from the wafer level. A wafer sort test program runs the tests at the wafer level and bins them as PASS and FAIL. The failing wafers will be sent for further analysis to the PFA laboratory depending on the type of failures. The yield of wafers is usually determined at this point.

Once the dice are separated from the wafers, an engineering test program is created that screens the devices with accurate FAIL details. For example, if a device fails a continuity test, the failing pin, current and voltage values and short or open can be determined from the log.

The final test program is used at the last level to just screen the devices. Those devices which PASS all the tests will be shipped to customers and the rest will be discarded.

Defect vs. Yield

- Manufacturing defect
  - ❑ can cause the chip to function incorrectly
  - ❑ is caused by errors during fabrication
  - ❑ could be stuck-at, short, open, resistive opens, resistive shorts, etc.
- In general there are around ~1500 dice per wafer
- Yield is expressed as a percentage of good dice produced to the total number of dice in a wafer
  - ❑ Good chips have no manufacturing defect
  - ❑ Bad chips have manufacturing defect
- Yield of a wafer or a product is never close to 100% of the manufactured dice

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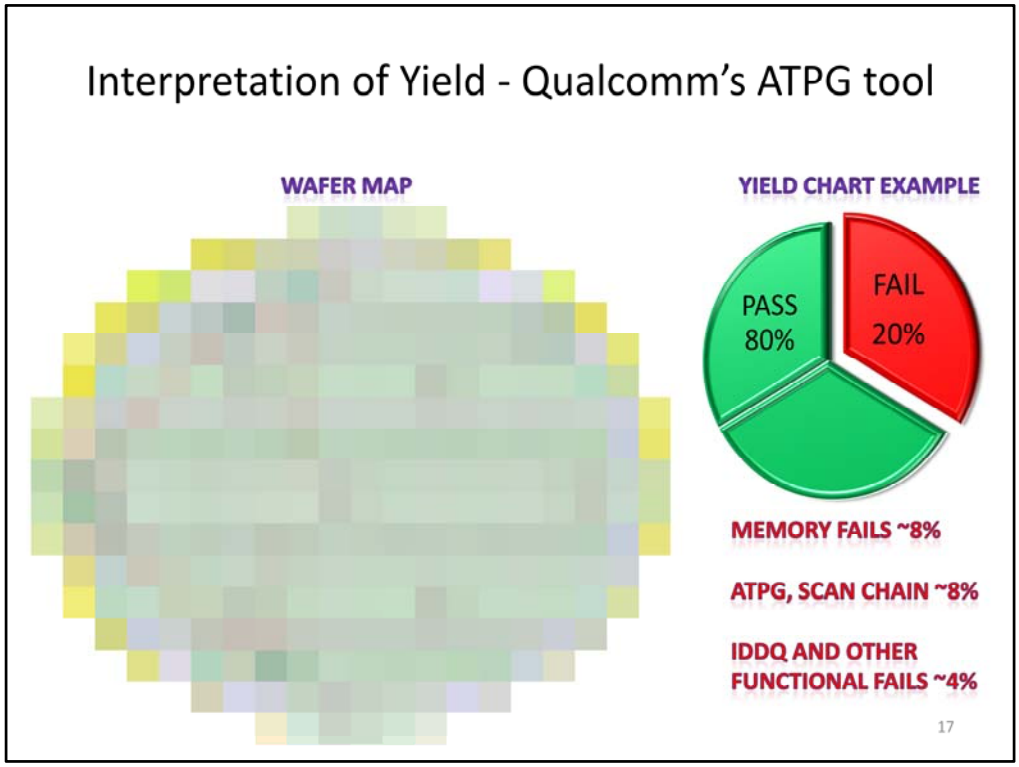
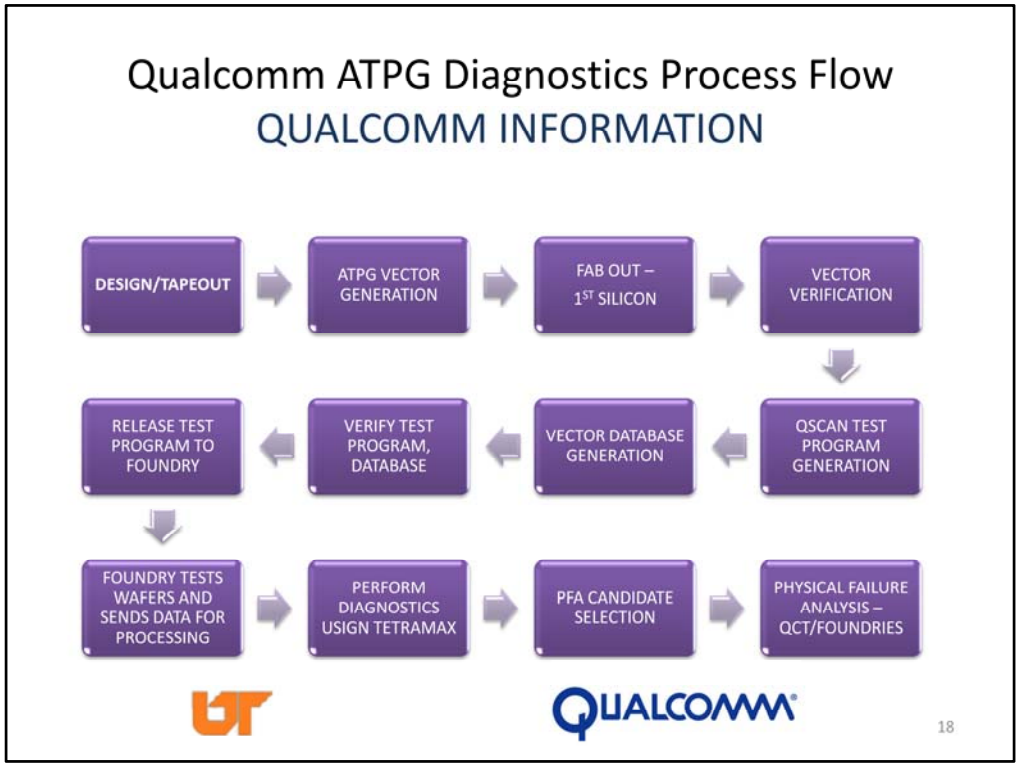
This slides basically explains how defects contribute to reduction in yield of wafers. The lesser the yield, the greater are the chances of more defects in the die. The more the defects, the greater are the problems with process variations.



An example of a wafer map is shown in the figure above. The dice marked in blue FAIL some tests. Most of the FAILS are usually related to Memory fails, ATPG and scan chain integrity fails or some other kind of functional failures. The yield of an initial wafer is around 80% which is reasonable. Several automated tools exist for handling each of the failure modes shown and I was involved with ATPG and scan chain integrity fails.

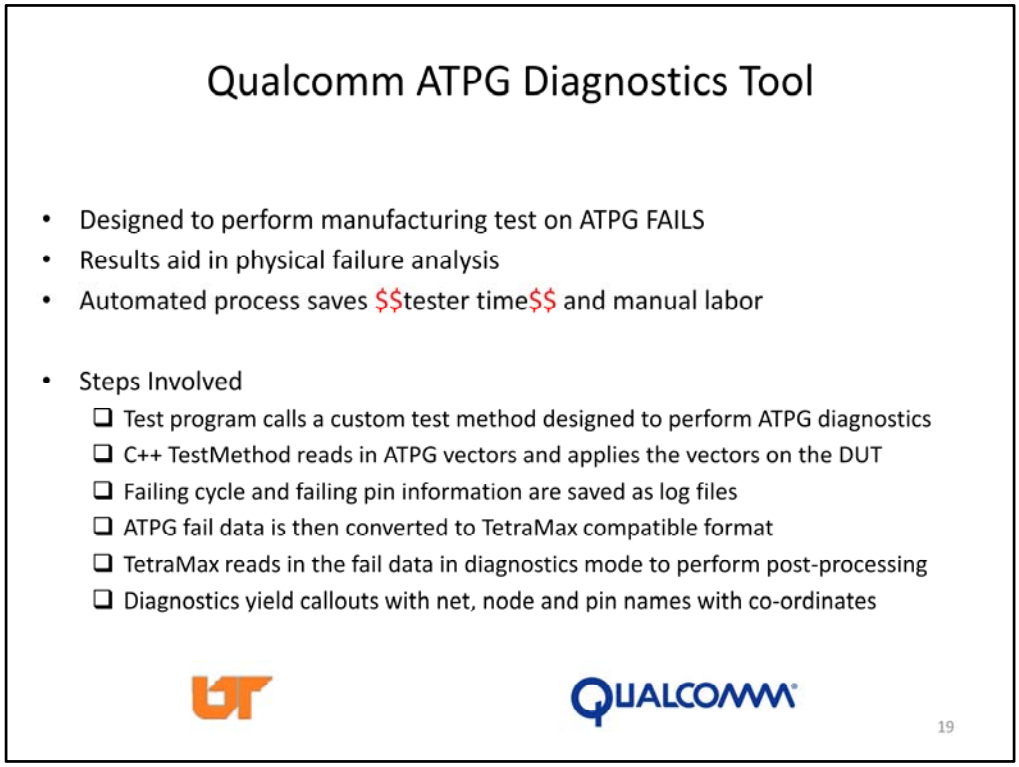


The details included in this slide and the following slides describe the procedure used by Qualcomm. This slide shows a sequence of steps that leads to ATPG diagnostics and the post processing steps that follow.

Once the design is verified and taped out to the foundry, ATPG vectors are generated using a ATPG tool (usually TetraMax) with several design constraints that are given by the designers.
Once the first set of wafers are ready (1st silicon), the vectors are verified using these dice with a custom test program. Once the vectors are verified, the same program is used to bin these devices and a custom ATPG diagnostic test program is created. The vec sim engineers create a diagnostic database. The test program is verified in-house by running it on known ATPG FAIL units and collecting the FAIL data (failing pin and failing cycle info). This data is then processed using the ATPG tool to perform diagnostics. If the database matches the vectors used for testing, then accurate callouts will be written out by the ATPG tool or else a mismatch warning would occur.

After thorough verification, the test program is released to the foundries, so that they can run it on the wafers using a wafer prober. The foundries run these tests successfully on all the fabricated wafers and send the FAIL data to us for further processing.

As explained above, the data is then processed using the vectors database to perform diagnostics. The ATPG tool gives all the callouts based on the FAIL data with exact net names, co-ordinates, type of failure mode and the match %. Based on these callouts, a expert analysis is performed to determine excellent candidates that could be the source for defects. Once the candidates are chosen, PFA (physical failure analysis) is performed using several FA tools and techniques to determine the cause of failure. Each FAIL determined using this flow is very valuable as it is used to find if ther are any process anomalies and improve yield. The final two steps, device selection and PFA are explained in the following slides.



This slide explains the advantages of the Qualcomm ATPG diagnostics tool and how it is performed. The basic steps involved are also explained in detail.

A test program is built specifically to account for ATPG fails. This test program uses a custom C++ test method which is the heart of this project. This is an automated C++ software tool which reads in the ATPG vectors into the pattern memory (explained previously), applies the input stimulus on the DUT. For ever failing pattern, the tester cycle and the failing pin information are stored in a log file. This data is later converted to TetraMax compatible format.

The FAIL data is then processed as explained above to perform diagnostics.

Qualcomm ATPG Diagnostics Tool – contd.

- Perform automated test on the ATPG fails
- Find the reasons for failure – defects introduced during fabrication
- Improve the yield of manufactured dice
- Assists FA engineers with valuable callouts pertaining to the fail data
- FA engineers look for those nodes, nets or scan cells in the die
- Cause of defects can be determined
- Defects give valuable information about process anomalies

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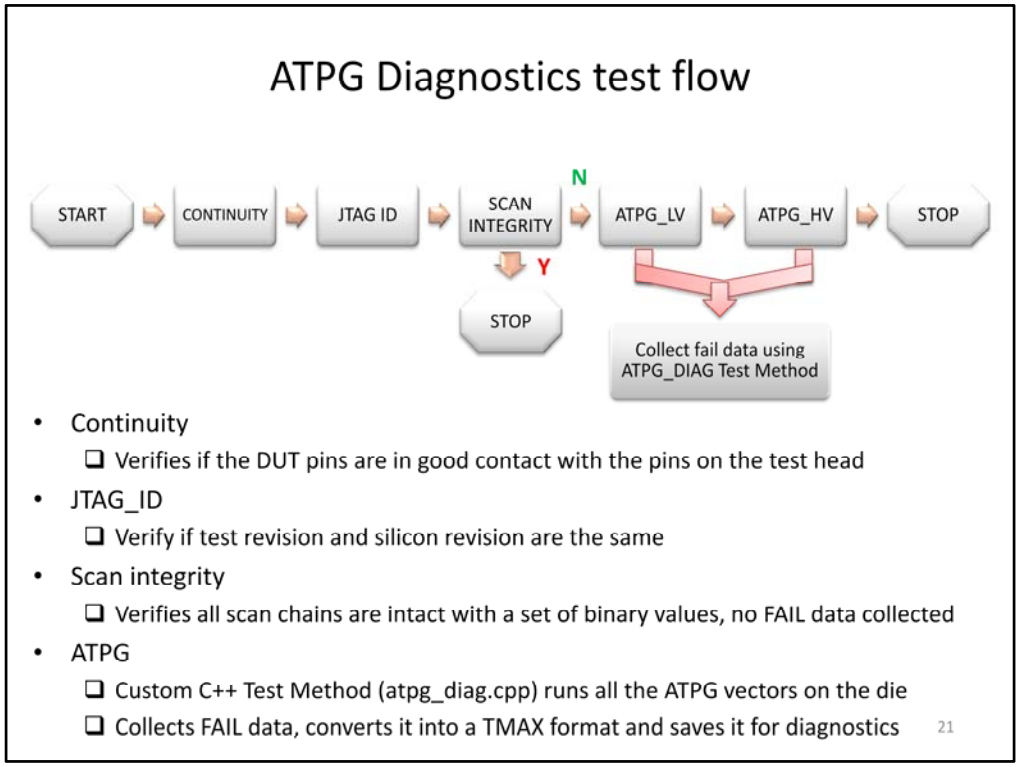
The major advantages of Qualcomm ATPG diagnostics tool are discussed in this slide.



The test flow used to perform ATPG diagnostics and collect FAIL information is explained in this slide. The test flow consists of test suites to perform the following functions.

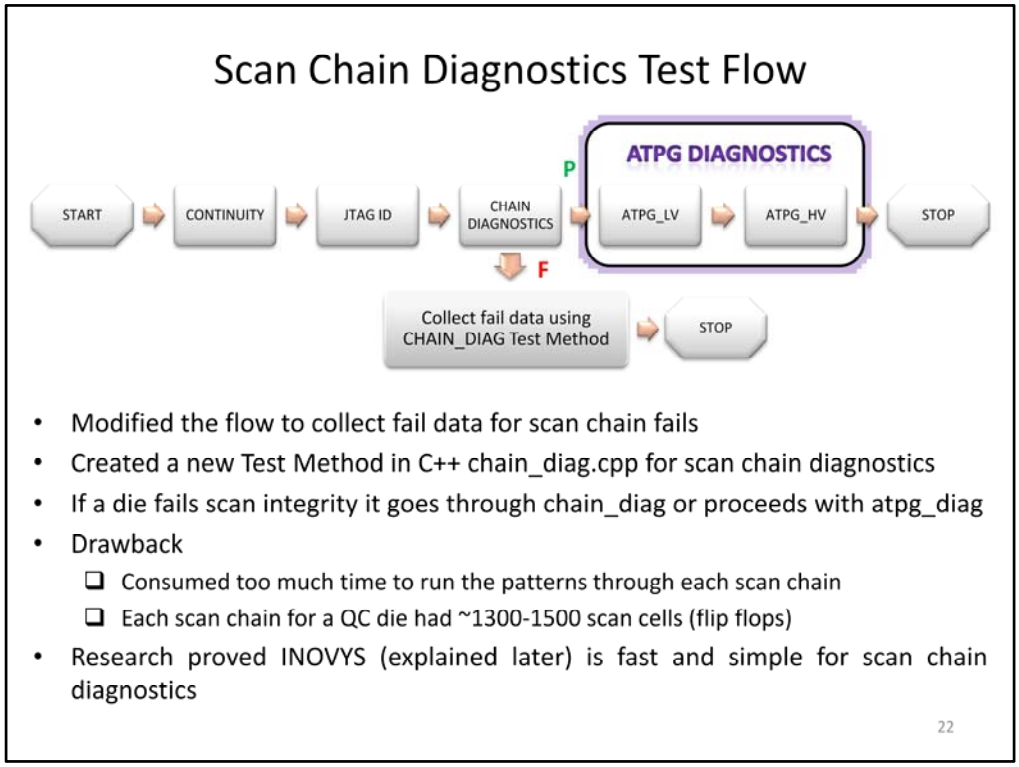
The continuity test suite tests if the DUT pins are in proper contact with the test head and also make sure the EOS diodes for each pin functions properly (not shorted or grounded).

JTAG_ID test suite is used to verify if the test revision and the silicon revision are the same.

JTAG_ID and continuity test suite make use of a routine which is pre-defined within the ATE. Functional vectors have to be generated to verify the JTAG_ID.

The scan chain integrity test suite makes sure all the scan chains in the design are intact by just scanning through a set of values. Separate vectors are generated for the same. The ATPG_DIAG test method was so created that FAIL data is collected only if the device fails ATPG. If the device fails any other test, then the ATE would stop testing at that failing test suite. ATPG test is performed at both low as well as high voltages to account for voltage dependent fails.

As already explained for each device that fails ATPG for a specific pattern, the failing tester cycle and failing pin information are collected. This data is later converted to a tool specific format and is processed using TetraMax to perform diagnostics.



This slide explains how I created a tool to capture FAIL data for scan chain integrity fails. This test method called CHAIN_DIAG.cpp used a similar flow, but it was modified to treat the scan chain integrity fails differently. The basic idea behind this test method is as follows.

If a device fails scan chain integrity, the chain_diag test method will be activated by the test suite. This will read in the scan integrity vectors, apply the stimulus on the pins and collect the failing pin and failing tester cycle information. The ATE would stop testing after collecting scan chain fails because such a device would drastically fail ATPG for all the pins for almost every tester cycle and pattern.

If the device passes scan integrity, it would be run through the ATPG test suites, which has been explained in the previous slide.

This was a important breakthrough for our team because it was never performed before. Interesting results were obtained which were really important for research purposes. Based on the results obtained from this experiment, we decided to invest in low cost structural testers (explained later) which were much faster and effective that ATEs for scan chain diagnostics.

Processing ATPG Fail data – TetraMax in Diagnostic Mode

- Create a diagnostic database with the ATPG vectors used for testing
- Read the database (read image) into TetraMax
- Set the patterns to external (set pat ext)
- Run diagnostics for each file
- TetraMax generates callouts (nets, pins or nodes) with co-ordinates of the nets
- Candidate selection performed from the callouts
- Most suitable candidates considered for PFA

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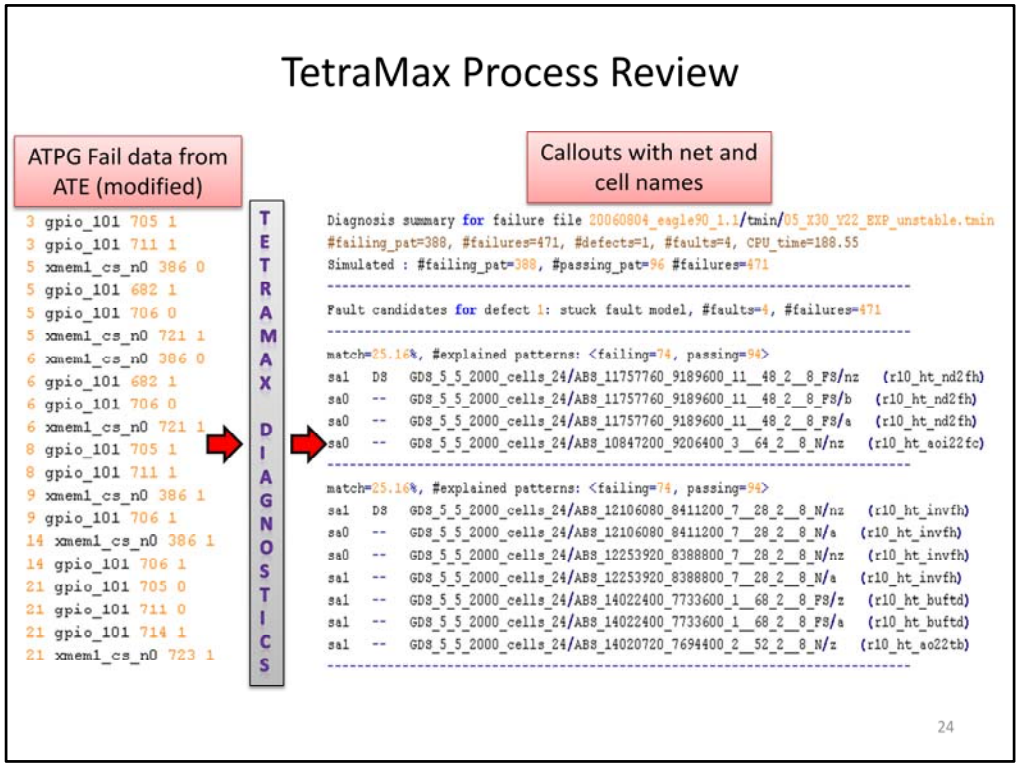
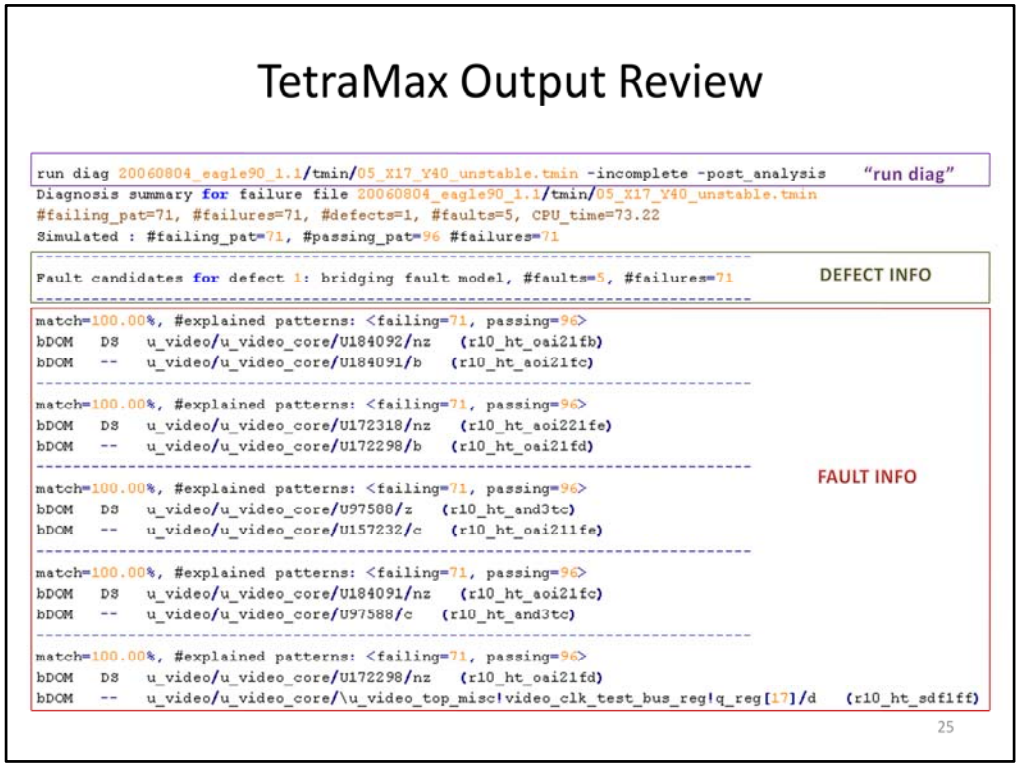
This slide explains the commands that are used to run the ATPG tool in diagnostics mode to process the ATPG fail data.



This slide shows an example of the fail data collected from the ATE. The actual ATE fail data (failing pin and failing cycle) is converted to a format shown on the left so that it is tool compatible. The ATPG tool, processes the fail data using a diagnostics vectors database and provides the following callouts as illustrated above. The callouts have precise information about the failing cell and the nets. The basic criteria for selecting candidates for physical failure analysis is explained later. The net names shown above is hierarchical, starting from the topmost layers. Going to such lower layers to find the cause for defects is very challenging.



This slide is a more detailed description of the diagnostic results from the ATPG tool.

The fault information contains the match score, the number of unexplained patterns, the hierarchical net name and the failing cell.

The defect information just gives the type of fault model (bridging, sa1, sa0, etc) and the number of faults that were determined for the given fail data log file.

Candidate Selection for PFA

- Callouts are analyzed based on the following criteria to determine which failing devices are the best candidates for PFA
- Candidate Selection Criteria
  - Stuck-at-0/1 Fault
    - Short nets with fewer metal layers
    - Fewer (or single) callouts that explain a high percentage of failing patterns
  - Bridging Faults (Adjacent nets)
    - Two unique nets of different (or same) cells running parallel to each other
    - Higher the level of metal layer in the hierarchy, greater are the chances of finding a defect
  - Bridging Faults (Crossing nets)
    - Two unique nets crossing each other
- Bridging faults on adjacent nets are the most determined defects

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The callouts generated by the ATPG tool have to be analyzed to determine which failing devices are the best candidates are the best for physical failure analysis. The basic criteria that need to be followed are explained in this slide.

A stuck-at-0/1 fault will usually manifest itself as short nets with fewer metal layers. Most importantly, fewer or single callouts that explain a high percentage of the failing patterns and have a match scores of 90% or higher would be the most appropriate candidates.

If two nets (unique) of different cells or same cells run parallel to each other then they would be ideal candidates for PFA, as results have sown higher success rates. If the nets are from higher level cells, more are the chances of finding it easily.

Bridging faults on adjacent nets are the most prominent defects. Results illustrating the bridging defects will be shown in the next few slides.

Physical Failure Analysis – PFA
what?? how??

- Diagnostic process for determining the "root cause" of a failure
- Defects provide valuable information about the process anomalies
- Results support process improvements impacting product yield, quality and reliability
- Excellent technical expertise and skills are required!!

- General PFA flow involves
  - Continuity test using a curve tracer (verify shorts, open, resistive shorts and opens)
  - Visual inspection using X-ray imaging
  - Decapping to expose the bare die (from the package)
  - Continuous analysis using optical microscopes and SEM
  - Hypervision (defect isolation), reactive ion etcher(removing oxide layers)
  - P-lapping to de-process the metal layers to go down to the desired layer

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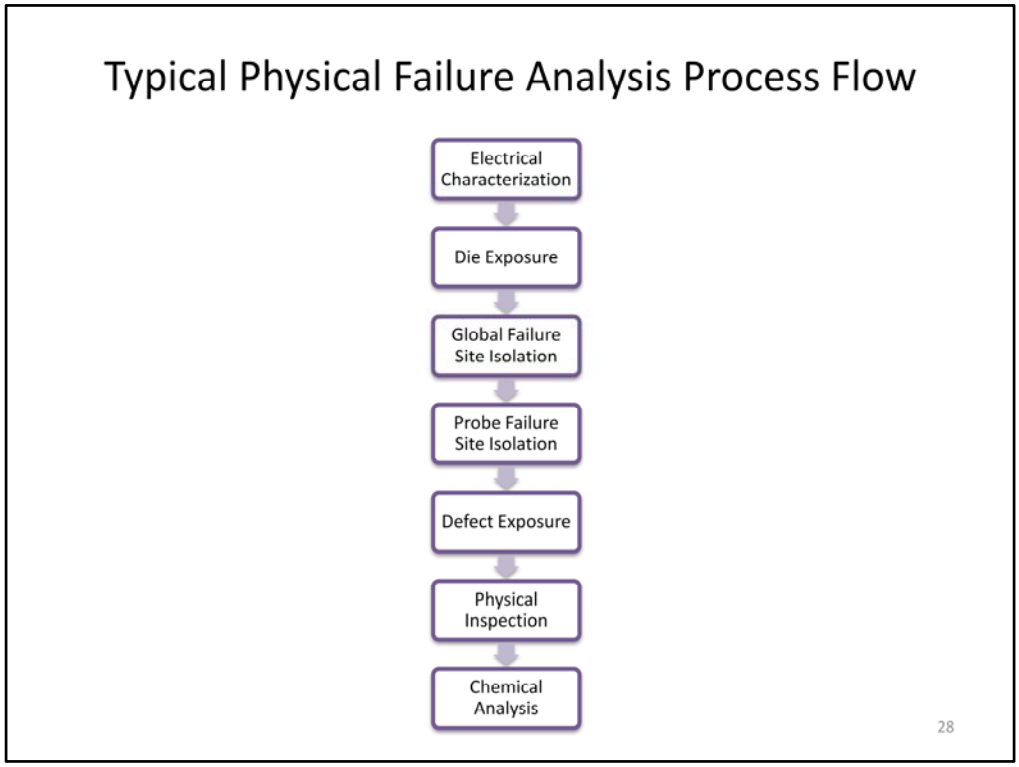
Failure Analysis is defined as a diagnostic process for determining the root cause of failure. The results are so valuable that they support process improvements that are crucial in improving the product yield, quality and reliability. There are several tools and techniques used to perform physical failure analysis. A general PFA flow with examples for each step is explained in this slide and the actual flow is shown later. A detailed explanation for the flow can be seen in the next slide.



This slide explains each step followed in a typical failure analysis flow.

The initial electrical verification process provides a general understanding of how the device is failing electrically. For example, continuity tests are performed using a curve tracer (I-V characterization), shmoo plots (characterization as a function of temperature, power supply voltage or frequency) and other techniques can be used. The major requirement is that the failing device must be placed into the failing electrical condition.

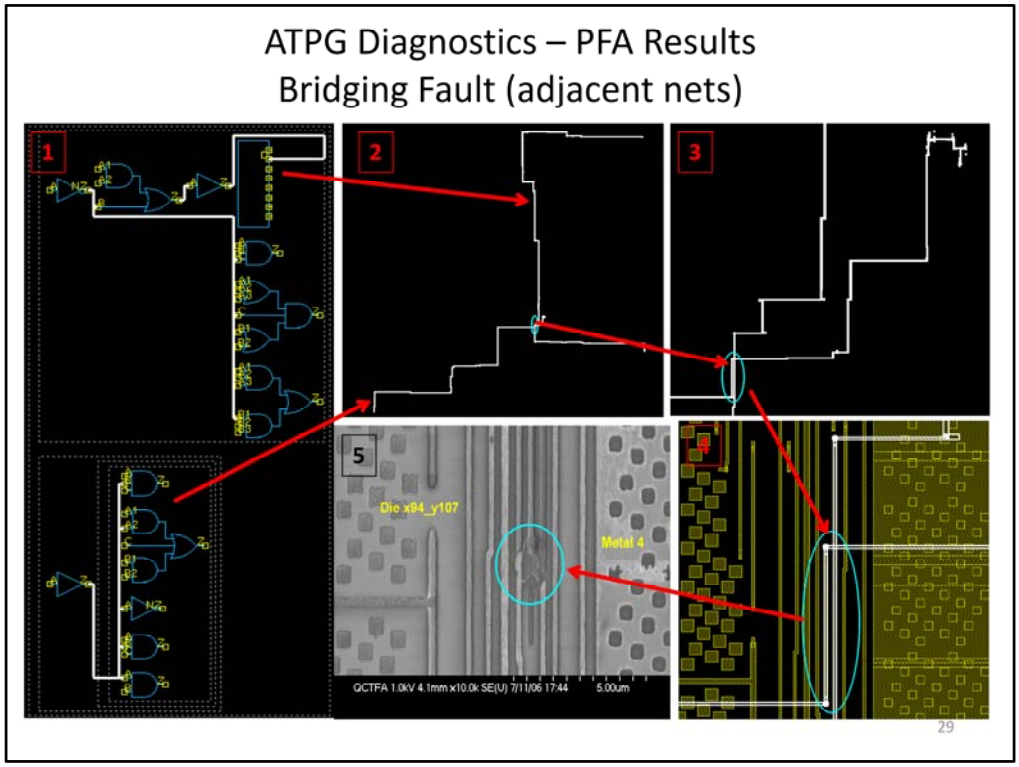
Die exposure is performed to get direct access to the device(by removing it from the package) for failure site isolation. The major requirement is that the electrical integrity of the device is unaltered so that the device continues to fail electrically in the same manner.

Several techniques are followed to isolate the failure. Certain techniques that I got trained and used are thermal detection technique (attempts to identify the heat generated at a failure site) and photon emission microscopy (identifies anomalous light emissions from failure sites due to electron-hole recombination).

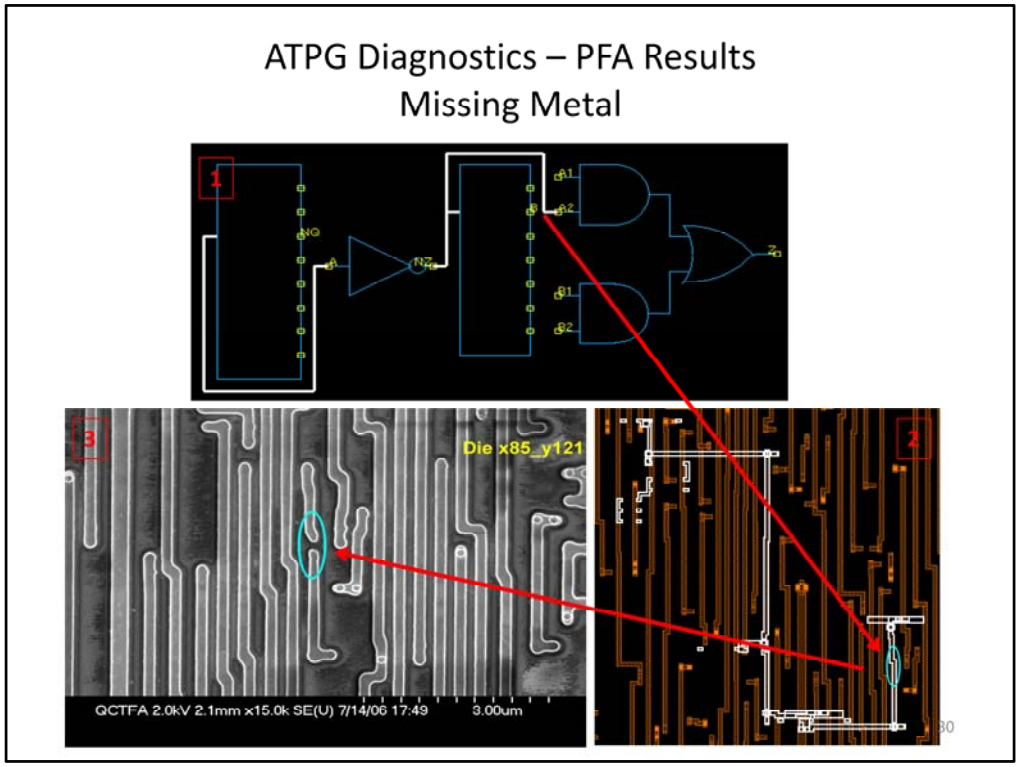
Package analysis is sometimes performed to determine any opens, shorts or leakages without destructing the package by certain techniques like X-ray and SAM (Scanning Acoustic Microscope).

Physical and chemical analysis techniques are a set of steps performed after failure site isolation to identify the physical cause of the failure. General techniques include deprocessing, parallel polishing and cross sectioning. During each of these steps the device has to be visually inspected using optical microscopes and SEM's (Scanning Electron Microscope).

I worked on almost all of these devices and learned most of the techniques to perform PFA.

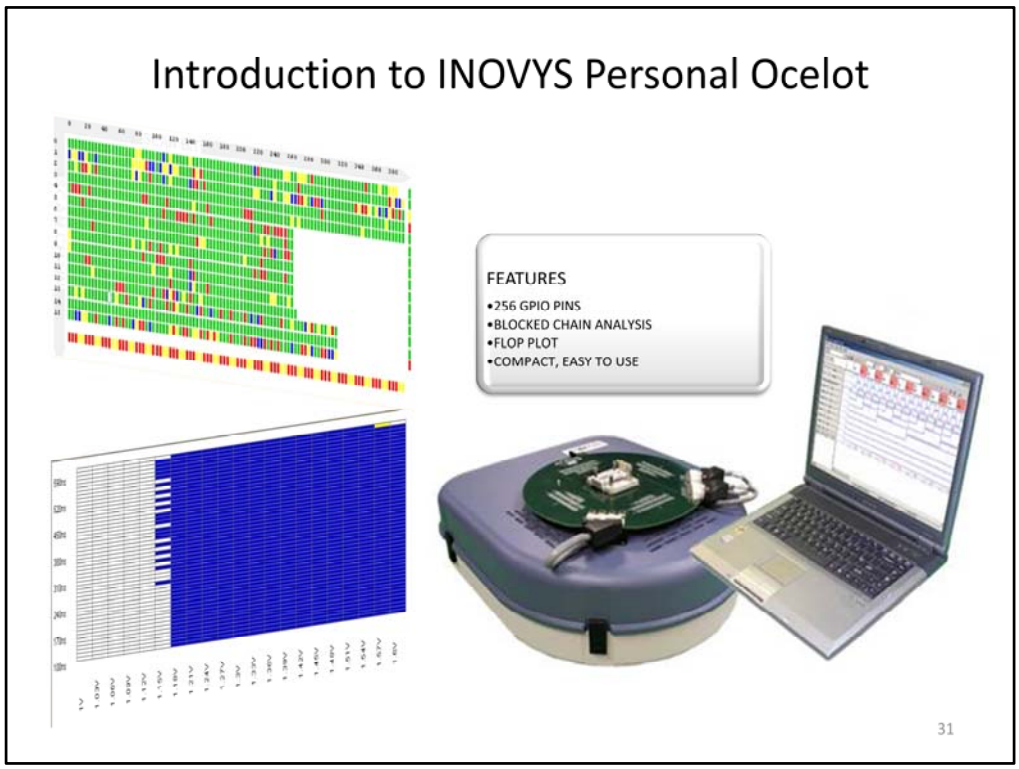


The next two slides shows the final results obtained from ATPG diagnostics after PFA. Figure 1, shows the schematic of the net that was suspected to be a defect location based on candidate selection explained previously. The two nets (same meta layers) run parallel to each other as shown in figure 4 and after following the PFA flow the defect was determined and it was found that a speck of impurity was present which caused a bridging defect between the two adjacent nets. Steps 1 – 4 are usually followed while selecting candidates for PFA and the physical layout on the die is compared with the actual layout at all times to make sure the correct location is being looked for. This bridging defect would have manifested itself as a short circuit during electrical characterization. The callouts from the ATPG tool would have explicitly indicated these set of nets as a bridging fault.

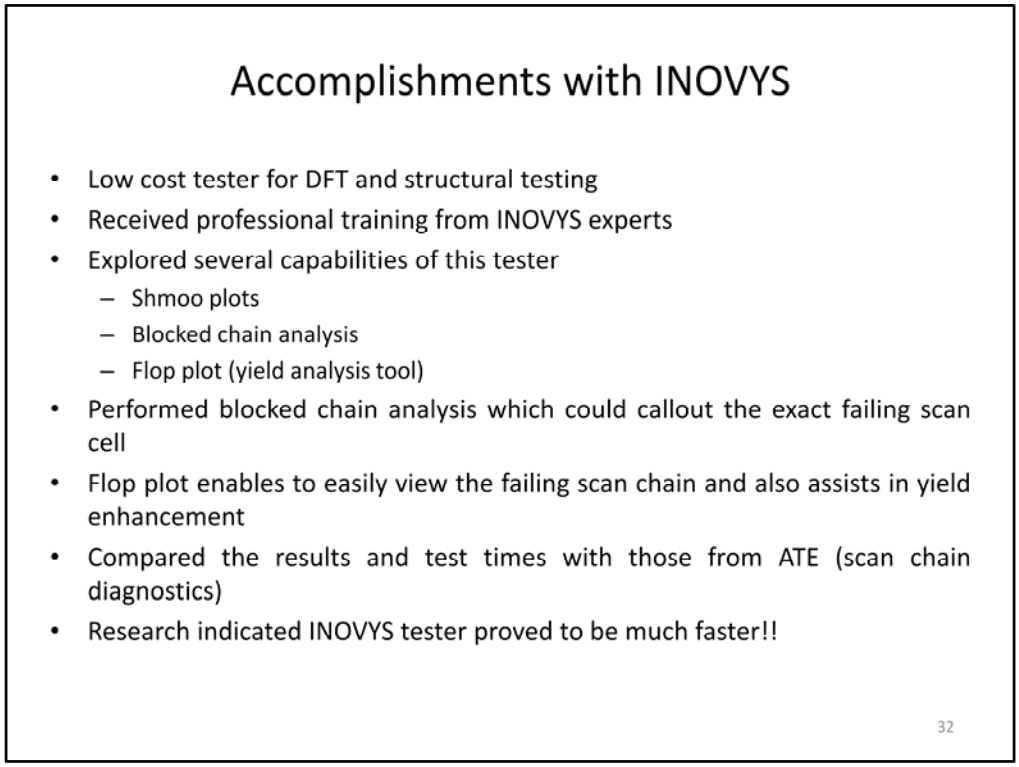


Another example is shown here where a metal line has a small piece of metal missing. This could be due to a small impurity that could have been introduced during the fabrication process exactly at this step.

The results obtained provide such valuable information about the process anomalies and contribute a great deal in the improvement of yield to foundries. The defects shown above and the previous slides were present in most of the wafers (1st silicon).



INOVYS personal ocelot, a low cost DFT tester currently being used in the industry is introduced here. This tester has several built-in features which makes it really excellent to perform certain operations very easily. A few of the capabilities of this tester like the flop-plot, shmoo plots and the logic analyzer are shown above. It has several nice feature like blocked chain analysis tool and flop plot which are mainly used to determine the failing scan cell and also assists in yield analysis. It is portable and very easy to use.



I had an excellent opportunity to work on a few projects with INOVYS. I was trained by INOVYS experts about the equipment. I explored several capabilities of this tester like blocked chain analysis which could callout the exact failing scan cells in the design. My research with this specific tool yielded very good results as I could perform scan chain diagnostics on this in a relatively smaller amount of time and easier way compared to the ATE. The results were so crucial to our team that we decided to go in for these low cost structural testers to analyze scan chain fails.

The major drawback with these testers are low pin count (~256 pins) and the blocked chain analysis can be used only if the logic for a specific pin is stuck-at-0/1. Timing and voltage related fails cannot be analyzed using BCA.

Future Trends in Testing and Test Application

- Companies are exploring several possibilities to cut down cost of manufacturing testing
- Test Generation
  - Extending basic fault models like stuck-at, delay and IDDQ
    - Multiple stuck-at faults are being considered
    - Delay faults refined to detect minor timing deviations which may not cause errors
    - Newer fault models considered for analog and memory devices
  - Augmenting the test set
    - Hand pick test vectors to detect specific faults
- Test Application
  - High speed tester required to cope with increasing speed of IC's
  - At-speed vectors considered to detect faults at device operating speeds
  - Structural testers with embedded DFT circuits provide high accuracy and speed

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This slide discusses the current and future trends in the industry. The extremely high cost of manufacturing testing has prompted companies to consider several other options like low-cost testers. In general strategies for test generation and test application are the major areas of change. The basic fault models used for generating test vectors are being modified to cope up with the increasing complexity of ICs. One of the newer techniques has been to generate vectors to target specific defects to achieve more success in finding the source of failure.

With regard to testers, at-speed testing has become the most popular testing strategy and will continue so, because more failures can be determined because of testing at the device operating speeds. Most importantly, low cost testers with embedded DFT circuits have been preferred because of its high accuracy and speed.

Conclusion

- ATPG tool successfully created for all Qualcomm products
- Yield increased by ~10% with excellent diagnostic and PFA results
- Qualcomm saved around "1 million dollars" with our diagnostic software
- All steps were automated which saved lot of engineering time
- Scan chain diagnostics proved to perform better on INOVYS test platform

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My contributions are summarized here.

Acknowledgement

- Dr. Bouldin, for all the help and support to pursue this Internship
- Qualcomm Incorporated to have given me this excellent opportunity
- Dr. Islam and Dr. Peterson, to be part of the committee
- My Family, who gave excellent support during the tough long 7 months

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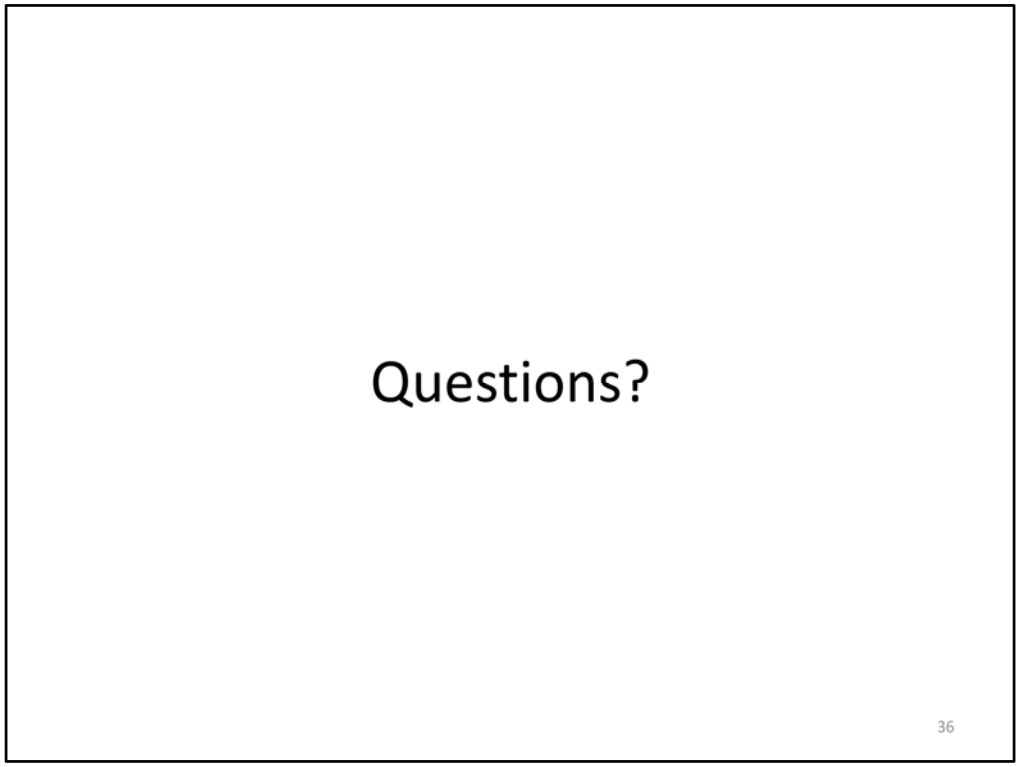
Thanks.



Questions?