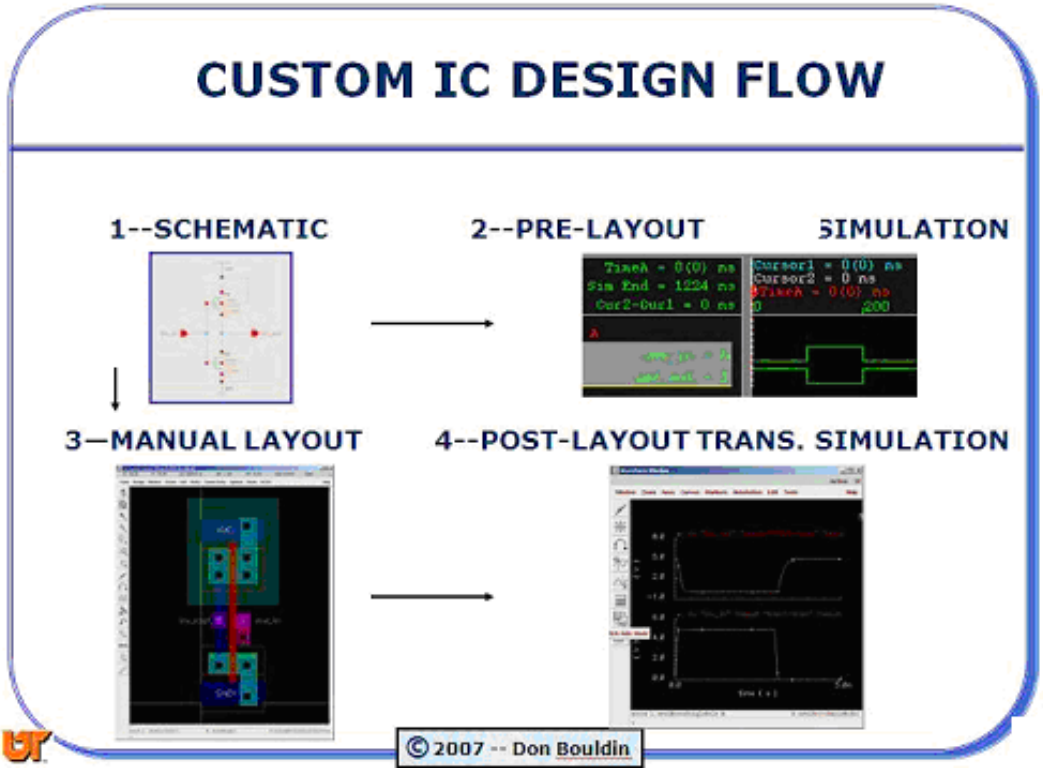
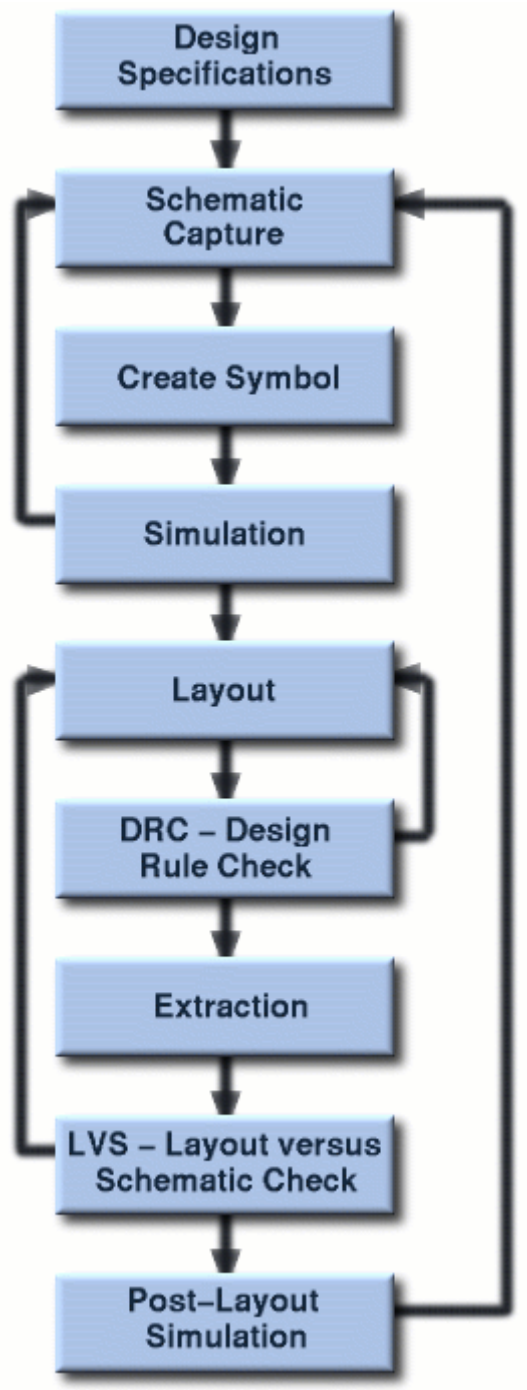
CUSTOM CELL DESIGN

Prof. Don Bouldin



Custom Cell Design Flow

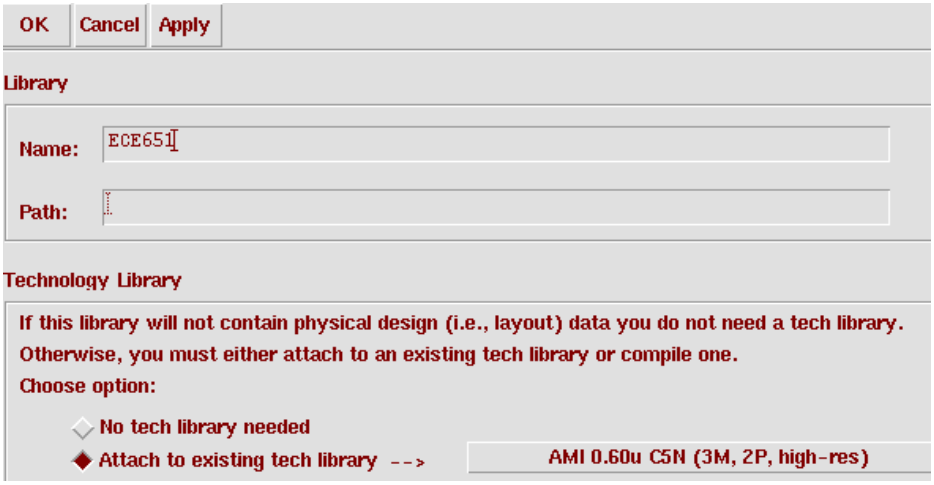


1. **mkdir cadence**
2. **cd cadence**
3. **cp /usr/local/ncsu/ncsu-cdk-1.5.1/cdssetup/cdsinit .cdsinit**
4. **cp /usr/local/ncsu/ncsu-cdk-1.5.1/cdssetup/cdsenv .cdsenv**
5. **cp /usr/local/ncsu/ncsu-cdk-1.5.1/cdssetup/cds.lib cds.lib**
6. **Edit "cds.lib" to point to the OSU_AMI06 library:**

   DEFINE OSU_AMI06 /usr/local/osu/lib/ami05/OSU_stdcells_ami05
7. **cp /usr/local/ncsu/ncsu-cdk-1.5.1/bin/startcad startcad**
8. **source startcad**
9. **Now, create a new schematic using Composer:**

File→New→Library

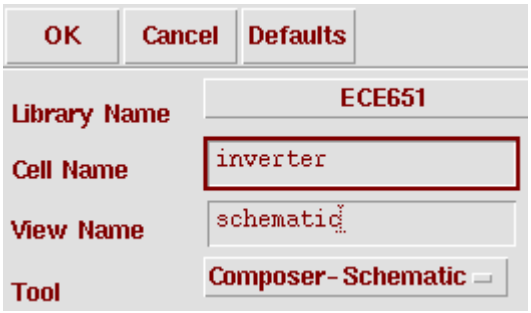
10. **Fill in the name "ECE651" and attach the AMI 0.60u C5N technology**



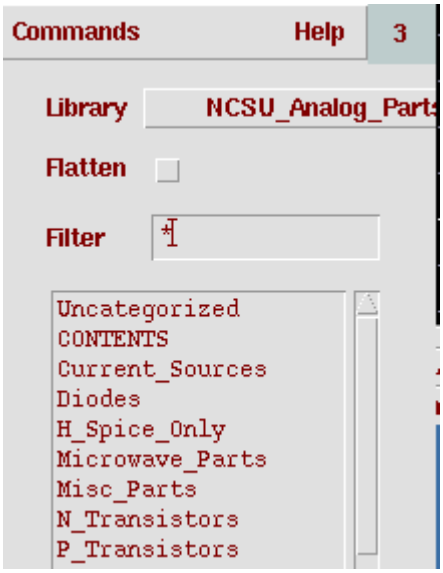
11. Click OK, then select ECE651.

12. Then, select File → New → Library

13. Then, select File→New→Cell View and fill in "inverter" & "schematic"



14. Select Add→Instances and then "NCSU Analog Parts" and then N transistors and then "nmos" and set W = 3u



15. **Add→Instances “NCSU Analog Parts” → P transistors → pmos and set W = 6u**

16. **Add→Instances “NCSU Analog Parts” → Supply Nets → vdd**

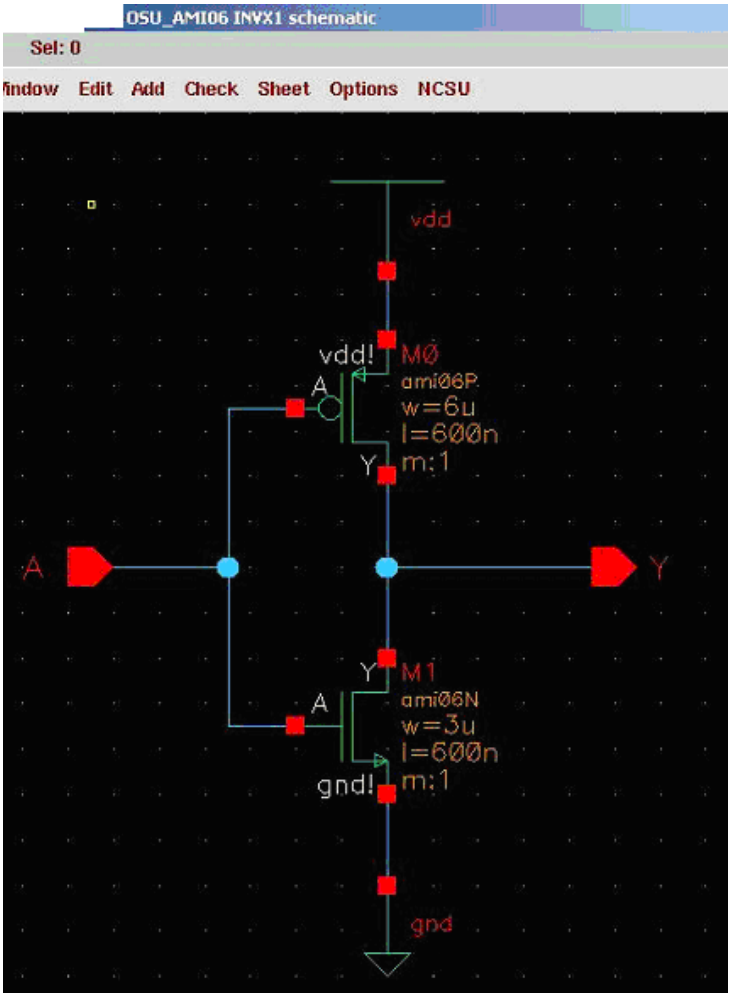
17. **Add→Instances “NCSU Analog Parts” → Supply Nets → gnd**

18. **Add→wire (narrow) Connect the parts**

19. **Add→pin select input → IN (or A)**

20. **Add→pin select output → OUT (or Y)**

The completed schematic should match the OSU schematic:



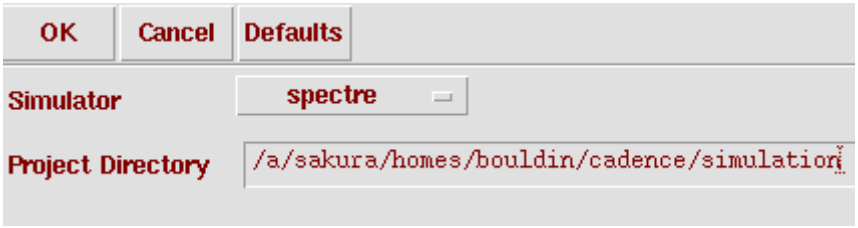
21. Design→Check and save

Optional: Create a symbol.

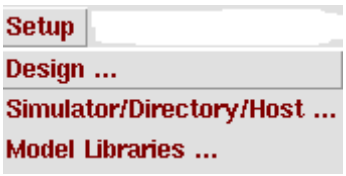
22. Tools→Analog Environment

23. Setup→Simulator

24. Select "spectre" and click OK

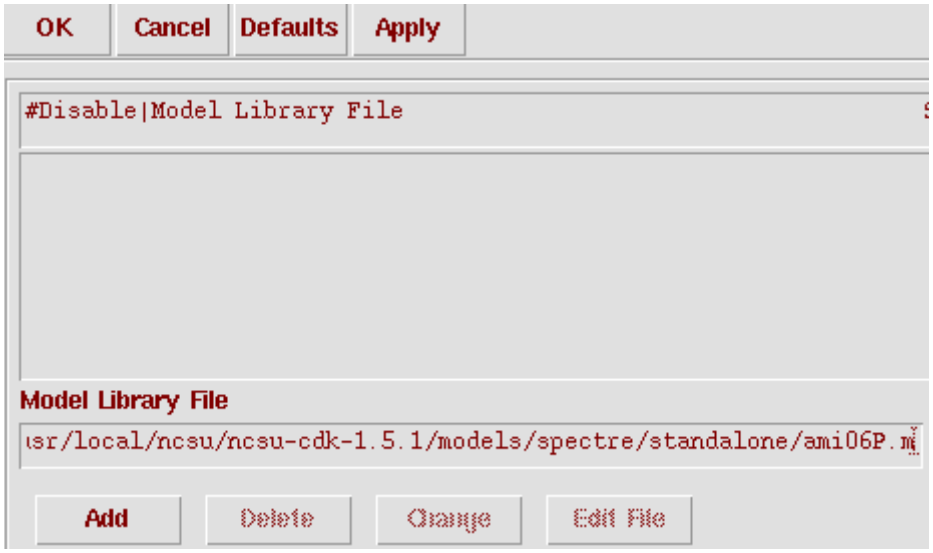


25. Setup→Model Libraries



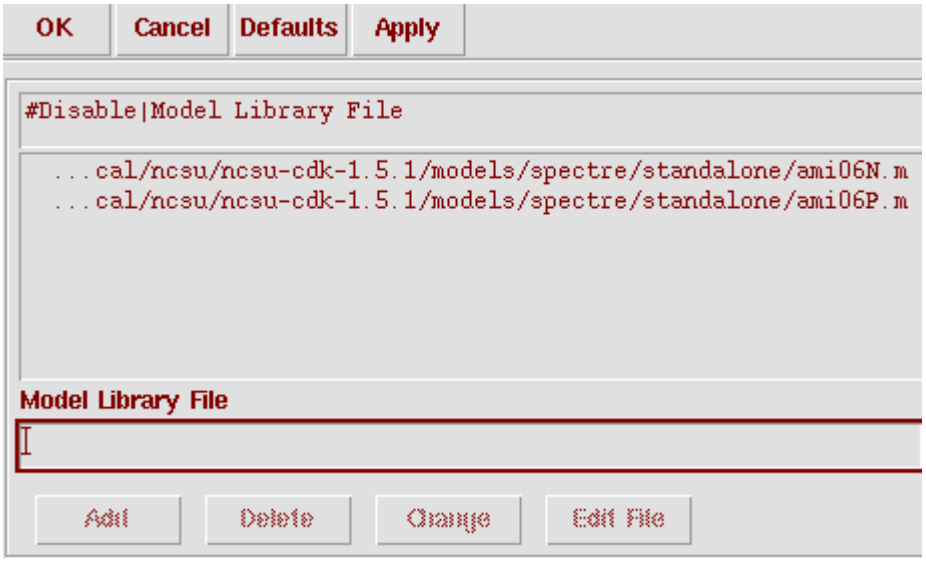
26. Fill in the path to “ami06P.m” and click ADD

/usr/local/ncsu/ncsu-cdk-1.5.1/models/spectre/standalone/ami06P.m



27. Repeat for “ami06N.m” and click ADD and OK

/usr/local/ncsu/ncsu-cdk-1.5.1/models/spectre/standalone/ami06N.m



28. Simulation→Netlist→Create

29. Edit the file:

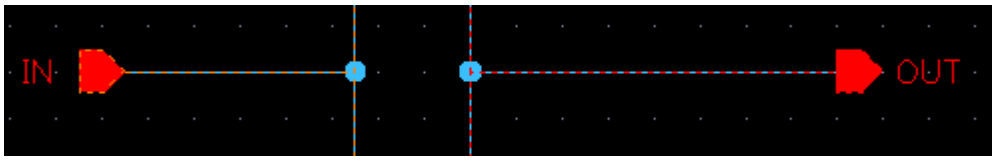
~username/cadence/simulation/inverter/spectre/schematic/netlist/netlist

30. Add the following statements and be sure you have the matching labels

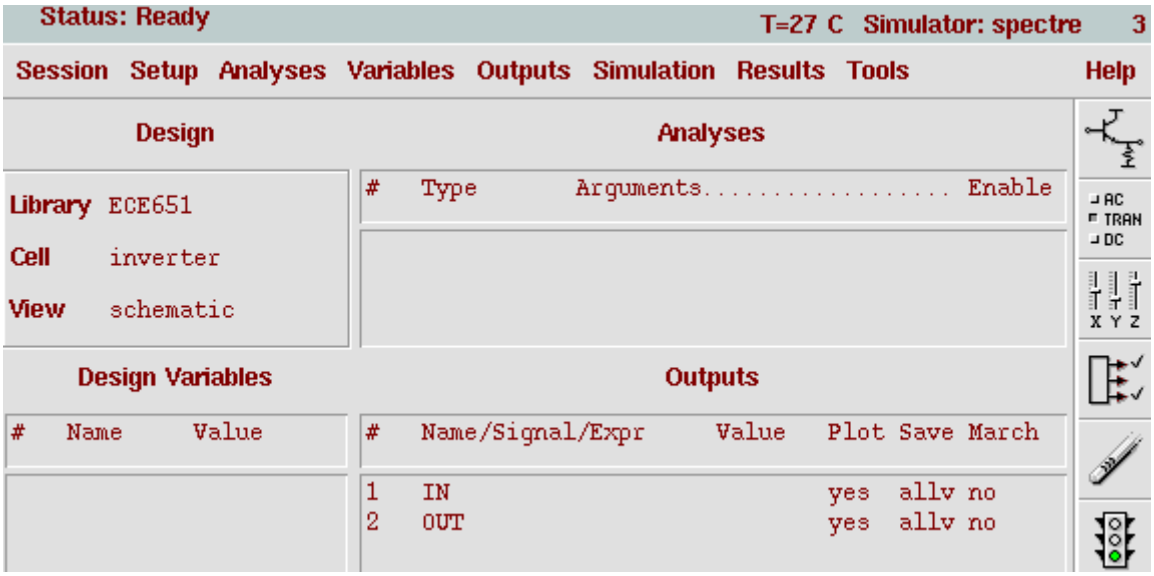
```
//include "/usr/local/ncsu/ncsu-cdk-1.5.1/models/spectre/standalone/ami06P.m"
//include "/usr/local/ncsu/ncsu-cdk-1.5.1/models/spectre/standalone/ami06N.m"
// Add output capacitor
Cout (inv_out 0) capacitor c=0.01pf
// Spectre Source Statements
Vdd (vdd! 0) vsource dc=5
Gnd (gnd! 0) vsource dc=0
Vin (inv_in 0) vsource type=pwl wave=[0n 0 1n 0 1.5n 5 3n 5 3.5n 0 6n 0]
// Transient Analyses
tran1 tran start=0 stop=6n step=0.1n errpreset=moderate
```

31. Outputs→To be Plotted→On schematic

32. Click on IN and OUT to highlight them:

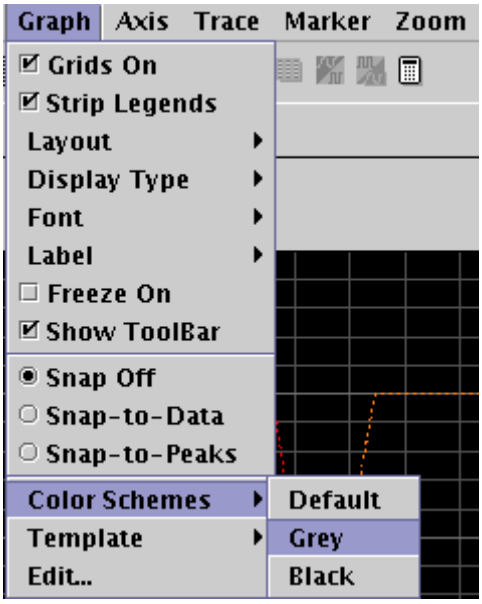


Note these outputs will be listed in the Simulation window:



33. Simulation→Run

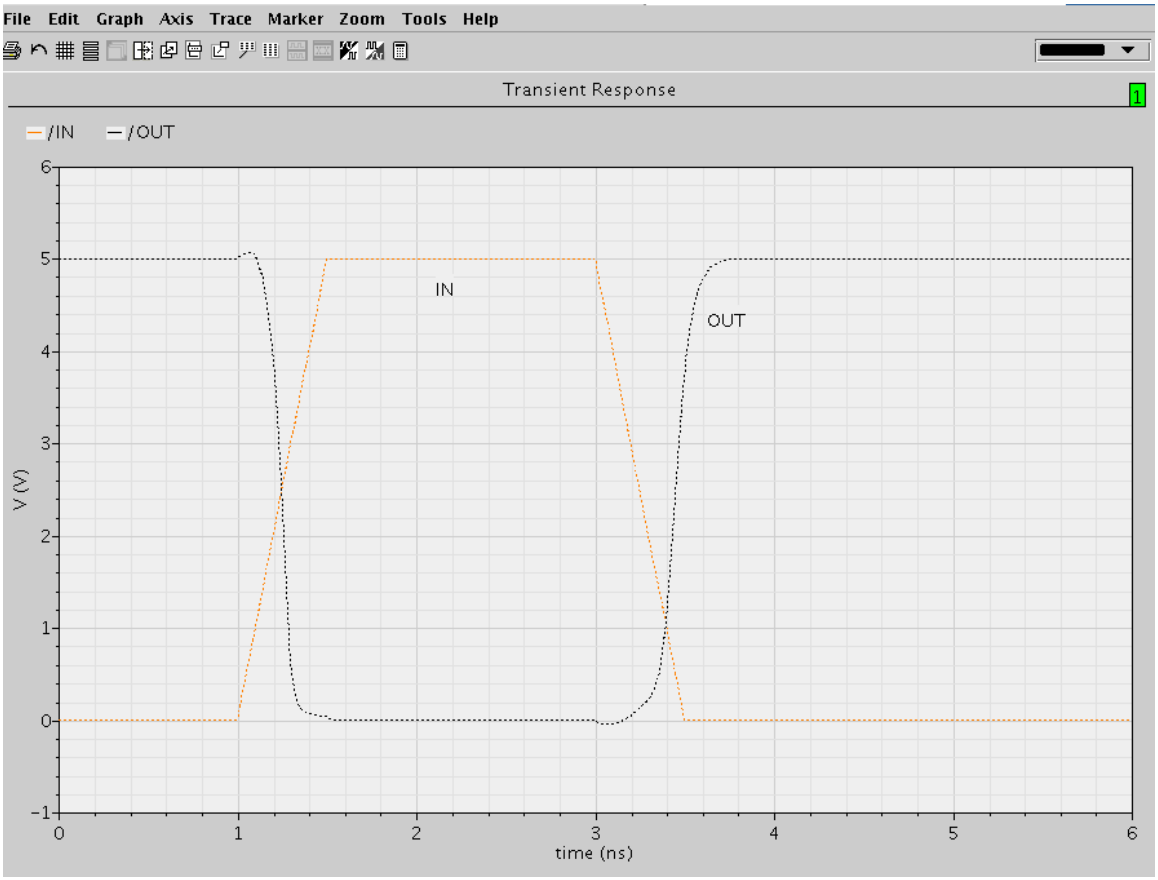
34. Change the color scheme to “grey”:



35. Add labels as desired:

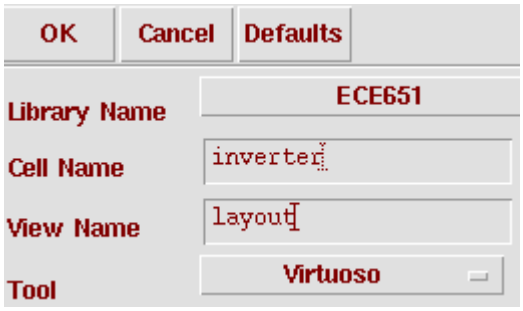
36. Select the OUT trace and then select a new color (black)

37. Capture the plot and put it on your protected website:

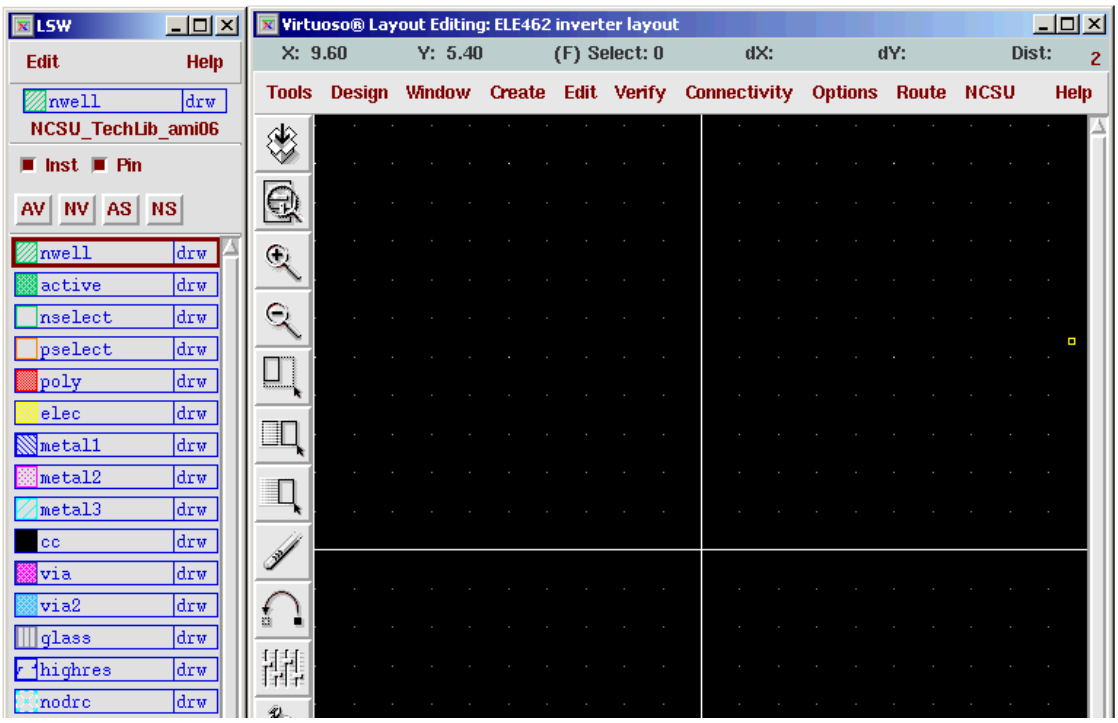


38. In the Library Manager Window, select File → New → CellView

39. Select "Virtuoso" and "layout":



40. The LSW and Virtuoso windows should appear:



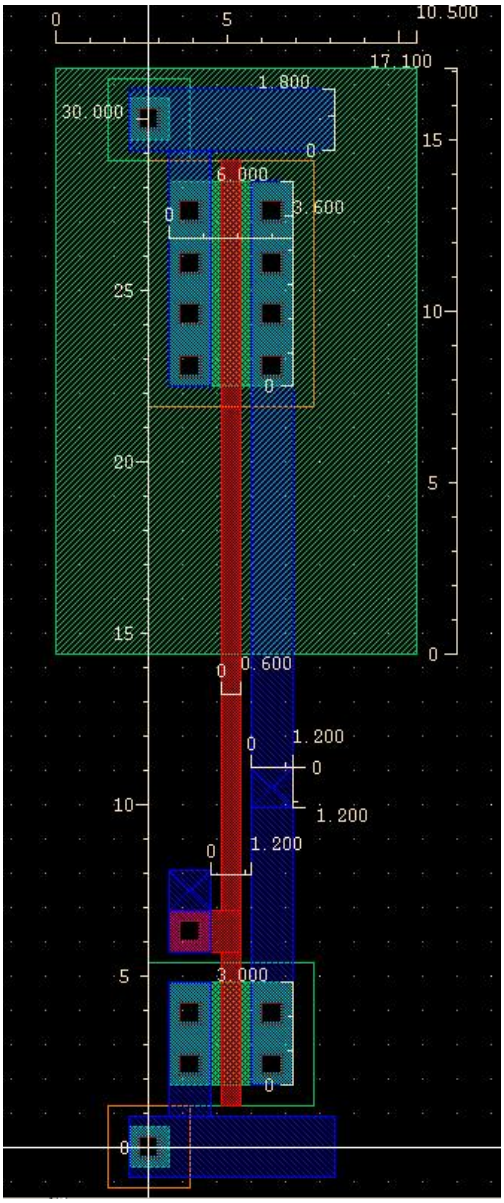
41. Follow the procedures described in

http://analog.ece.utk.edu/Cadence/virtuoso.htm

or

http://www.ece.utk.edu/~bouldin/protected/utah-ch05.pdf

to produce a standard-height cell with the exact measurements as shown below:



- **Hot keys**

  ***i*: Add instances**
  ***q*: Edit properties**
  ***r*: Add rectangles**
  ***p*: Add path**
  ***P*: Add Polygon**
  ***ctrl+p*: Add a pin**
  ***l*: Label a wire**
  ***z*: Zoom in**
  ***Z*: Zoom out by 2X**
  ***ctrl+z*: Zoom in by 2X**
  ***f*: fit the layout in your layout window**
  ***right mouse button*: repeat last command**

You can always cancel the current operation in schematic or layout editors by pressing the ESC key.

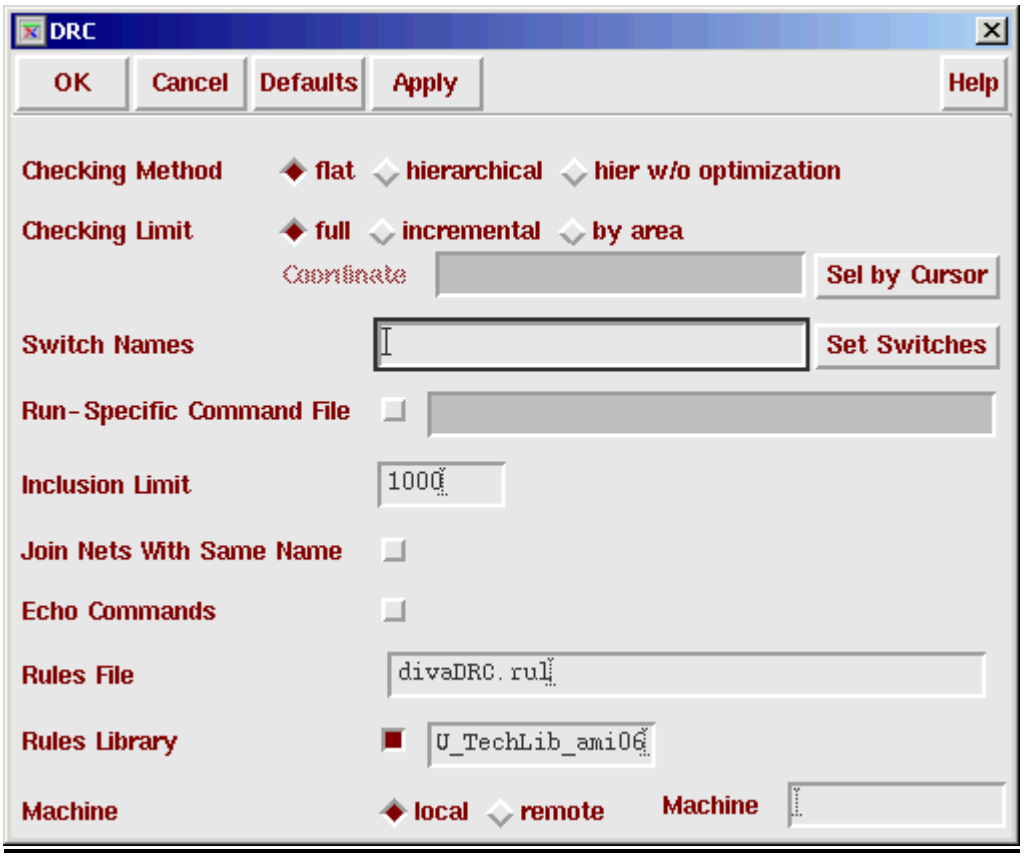
Perform DRC, LVS, Extraction and repeat the Spectre simulation for the layout.

http://analog.ece.utk.edu/Cadence/LVS.htm

or

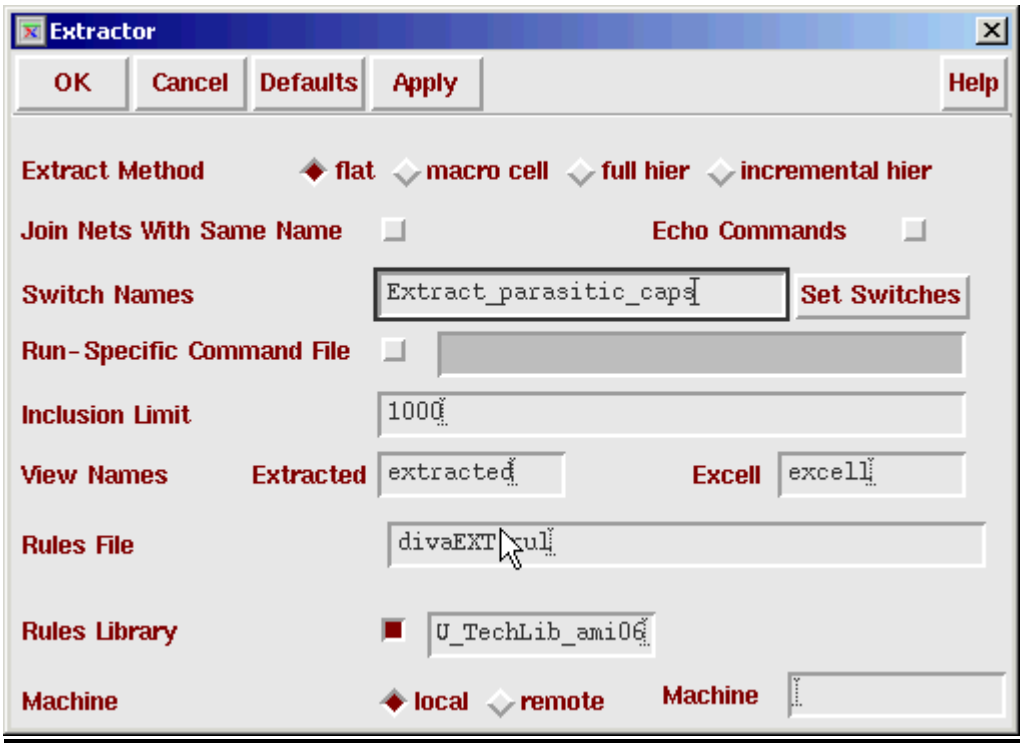
http://www.ece.utk.edu/~bouldin/protected/utah-ch06.pdf

42.Verify → DRC



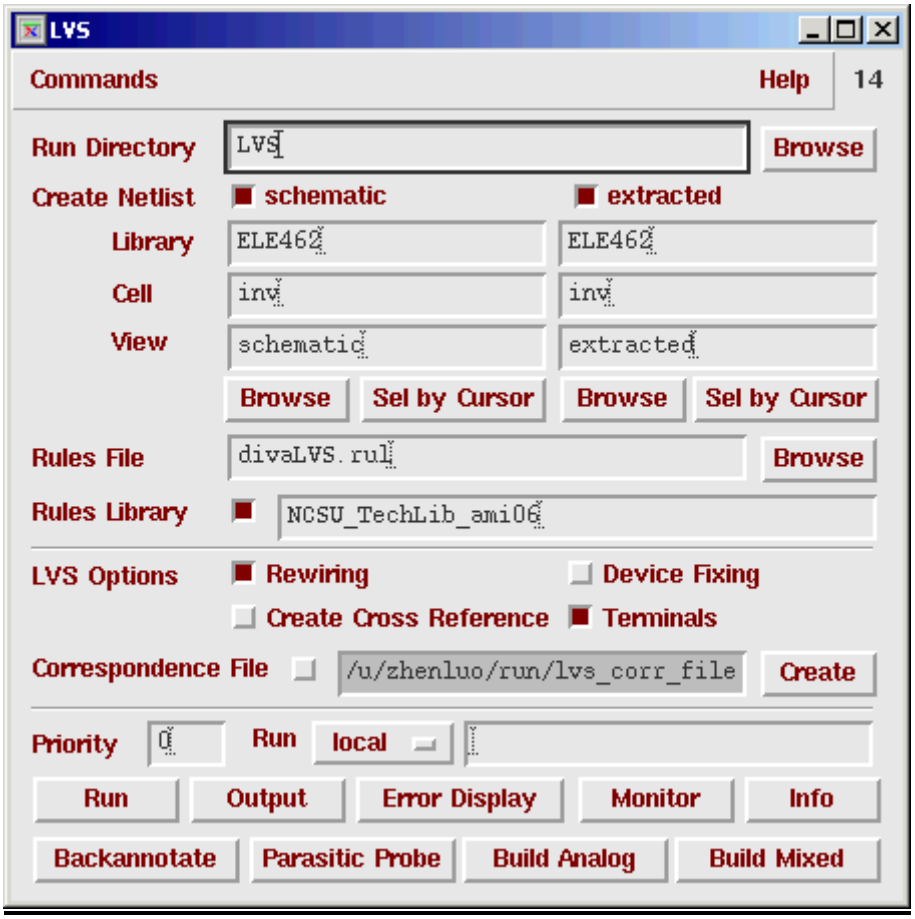

```
cell:     inv
view:     layout
Rules come from library NCSU_TechLib_ami06.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running drclayout analysis
Flat mode
Full checking.
DRC started.......Sun Apr  1 21:18:53 2001
    completed ....Sun Apr  1 21:18:53 2001
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violation for cell "inv layout"
   Total errors found: 0
```

43.Verify → Extract



If the process is not successful, you can click on "Info" in the LVS window or you can check the log file.

44. Verify → LVS



If there is an error, then in the LVS window, click on "Error Display".