THE UNIVERSITY OF TENNESSEE



# **CUSTOM CELL DESIGN**

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## **Custom Cell Design Flow**



- 1. mkdir cadence
- 2. cd cadence
- 3. cp /usr/local/ncsu/ncsu-cdk-1.5.1/cdssetup/cdsinit .cdsinit
- 4. cp /usr/local/ncsu/ncsu-cdk-1.5.1/cdssetup/cdsenv .cdsenv
- 5. cp /usr/local/ncsu/ncsu-cdk-1.5.1/cdssetup/cds.lib cds.lib
- 6. Edit "cds.lib" to point to the OSU\_AMI06 library:

DEFINE OSU\_AMI06 /usr/local/osu/lib/ami05/OSU\_stdcells\_ami05

- 7. cp /usr/local/ncsu/ncsu-cdk-1.5.1/bin/startcad startcad
- 8. source startcad
- 9. Now, create a new schematic using Composer:

File→New→Library

File	
New	Library.

10. Fill in the name "ECE651" and attach the AMI 0.60u C5N technology

ок	Cancel	Apply		
Library				
Name	ECE	651 <u>[</u>		
Path:	Ĭ.			
Techno	logy Lib	rary		
If this Other Choos	s library wise, yo se optior	will not : ou must 1:	contain physical design either attach to an exis	(i.e., layout) data you do not need a tech library. ting tech library or compile one.
	⇔No te	ech librar	y needed	
	🔶 Attac	h to exi:	sting tech library>	AMI 0.60u C5N (3M, 2P, high-res)

- 11. Click OK, then select ECE651.
- 12. Then, select File  $\rightarrow$  New  $\rightarrow$  Library

<u>File</u>		
New	⊳	Library
Open	^0	Cell View

13. Then, select File→New→Cell View and fill in "inverter" & "schematic"

OK Cano	el Defaults					
Library Name	ECE651					
Cell Name	inverter					
View Name	schematic					
Tool	Composer-Schematic 🖃					

14. Select Add $\rightarrow$ Instances and then "NCSU Analog Parts" and then N transistors and then "nmos" and set W = 3u

Commands		Help	3
Library	NCSU_	Analog	_Parts
Flatten			
Filter	4		
Uncateg CONTEN Current Diodes H_Spice Microwa Misc_Pa N_Trans P_Trans	gorized FS t_Sources e_Only ave_Parts arts sistors sistors		

- 15. Add→Instances "NCSU Analog Parts" → P transistors → pmos and set W = 6u
- 16. Add→Instances "NCSU Analog Parts" → Supply Nets → vdd
- 17. Add→Instances "NCSU Analog Parts" → Supply Nets → gnd
- **18.** Add→wire (narrow) Connect the parts
- **19.** Add $\rightarrow$ pin select input  $\rightarrow$  IN (or A)
- **20.** Add  $\rightarrow$  pin select output  $\rightarrow$  OUT (or Y)

The completed schematic should match the OSU schematic:



### 21. Design $\rightarrow$ Check and save

Design Check and Save f8

**Optional:** Create a symbol.

#### 22. Tools→Analog Environment

Tools AMS Opts. Analog Environment

### 23. Setup→Simulator

Setup
Design
Simulator/Directory/Host

### 24. Select "spectre" and click OK

ОК	Cancel	Defaults
Simulator		spectre 🖃
Project D	irectory	/a/sakura/homes/bouldin/cadence/simulation

#### 25. Setup→Model Libraries

Setup	l
Design	
Simulator/Directory/Host	
Model Libraries	

### 26. Fill in the path to "ami06P.m" and click ADD

/usr/local/ncsu/ncsu-cdk-1.5.1/models/spectre/standalone/ami06P.m

ОК	Cancel	Defaults	Apply		
#Disab	le Model	Library F	'ile		
Model L	ibrary File				
usr/loc	al/nesu/	nosu-odk-i	1.5.1/mode	ls/spectre/st	andalone/ami06P.mǧ
				[ [	1
Ad	ld	Delete	Oranifie	Edit File	

### 27. Repeat for "ami06N.m" and click ADD and OK

/usr/local/ncsu/ncsu-cdk-1.5.1/models/spectre/standalone/ami06N.m

ОК	Cancel	Defaults	Apply	
#Disab	leiModel	Librarv 1	File	
	al/ncsu/r	ncsu-cdk-	1.5.1/mo	els/spectre/standalone/ami06N m
c	al/ncsu/r	nosu-odk-	1.5.1/mo	lels/spectre/standalone/ami06P.m
Model L	ibrary File			
Ι				
Ad		Delete	Cian	je Edit File

#### 28. Simulation→Netlist→Create

Simulation	
Netlist and Run	
Run	
Stop	
Device Checking	
Options	$\sim$
Netlist	Create

#### 29. Edit the file:

~username/cadence/simulation/inverter/spectre/schematic/netlist/netlist

30. Add the following statements and be sure you have the matching labels

//include ''/usr/local/ncsu/ncsu-cdk-1.5.1/models/spectre/standalone/ami06P.m''
//include ''/usr/local/ncsu/ncsu-cdk-1.5.1/models/spectre/standalone/ami06N.m''
// Add output capacitor
Cout (inv\_out 0) capacitor c=0.01pf
// Spectre Source Statements
Vdd (vdd! 0) vsource dc=5
Gnd (gnd! 0) vsource dc=0
Vin (inv\_in 0) vsource type=pwl wave=[0n 0 1n 0 1.5n 5 3n 5 3.5n 0 6n 0]
// Transient Analyses
tran1 tran start=0 stop=6n step=0.1n errpreset=moderate

#### 31. Outputs→To be Plotted→On schematic



### 32. Click on IN and OUT to highlight them:

١Þ		·		 		· 1	÷				-		
					·								

Status: Ready T=27 C Simulator: spectre 3 Session Setup Analyses Variables Outputs Simulation Results Tools Help Design Analyses # Type Arguments..... Enable ⊐ AC ¤ TRAN ⊐ DC Library ECE651 Cell inverter III III XYZ View schematic **]** Design Variables Outputs # # Value Name/Signal/Expr Value Plot Save March Name yes allv no 1 IN 2 OUT yes allv no 8

Note these outputs will be listed in the Simulation window:

#### 33. Simulation→Run



**34.** Change the color scheme to "grey":



#### 35. Add labels as desired:



**36.** Select the OUT trace and then select a new color (black)

## **37.** Capture the plot and put it on your protected website:



## 38. In the Library Manager Window, select File $\rightarrow$ New $\rightarrow$ CellView

## 39. Select "Virtuoso" and "layout":

ок	Cance	el Defaults			
Library Name		ECE651			
Cell Name		inverter			
View Name		layout			
Tool		Virtuoso 😑			

## 40. The LSW and Virtuoso windows should appear:

<b>ISW</b>	- U ×	💌 Virtu	ioso® Lay	out Editing	g: ELE462	invert	er layout				- I I X
Edit	Help	X: 9	.60	Y: 5.40	1	(F) S	elect: O	dX:	dY:	Dis	t: 2
nwell	drw	Tools	Design	Window	Create	Edit	Verify	Connectivity	Options Route	NCSU	Help
NCSU_TechLit	o_ami06	ഷം					· .				• A
🔳 Inst 🔳 Pin		<u> </u>									
AV NV AS	NS	Q									
mwell	drw 🛆	Ę									
nselect	drw	Q									
pselect poly	drw drw										
elec	drw										
metall metal2	drw										
metal3	drw drw										
via	drw	<i>»</i>									
via2 IIIglass	drw drw										
r highres	drw										
nodrc	drw	42									

### 41. Follow the procedures described in

http://analog.ece.utk.edu/Cadence/virtuoso.htm

#### or

http://www.ece.utk.edu/~bouldin/protected/utah-ch05.pdf

to produce a standard-height cell with the exact measurements as shown below:



• Hot keys

i: Add instances q: Edit properties r: Add rectangles p: Add path P: Add Polygon ctrl+p: Add a pin l: Label a wire z: Zoom in Z: Zoom out by 2X ctrl+z: Zoom in by 2X f: fit the layout in your layout window right mouse button: repeat last command

You can always cancel the current operation in schematic or layout editors by pressing the ESC key.

Perform DRC, LVS, Extraction and repeat the Spectre simulation for the layout.

http://analog.ece.utk.edu/Cadence/LVS.htm

or

http://www.ece.utk.edu/~bouldin/protected/utah-ch06.pdf

42.Verify  $\rightarrow$  DRC

<b>DRC</b>				×
ОК	Cancel	Defaults	Apply	Help
Checking	Method	🔶 flat	♦ hierarchical ♦ hier w/o optimization	
спескіпд	LIMIT	Tuli Caprain	vate Sel by Qur	sor
Switch N	ames		I Set Switc	hes
Run-Spe	cific Comr	nand File		
Inclusion	Limit		1000	
Join Nets	With Sam	ne Name		
Echo Con	nmands			
Rules File	)		divaDRC.rul	
Rules Lib	rary		U_TechLib_ami06	
Machine			🔶 local 🔷 remote 🛛 Machine 📗	

cell: inv view: layout Rules come from library NCSU\_TechLib\_ami06. Rules path is divaDRC.rul. Inclusion limit is set to 1000. Running drclayout analysis Flat mode Full checking. DRC started.....Sun Apr 1 21:18:53 2001 completed ....Sun Apr 1 21:18:53 2001 CPU TIME = 00:00:00 TOTAL TIME = 00:00:00 \*\*\*\*\*\*\*\*\*\* Summary of rule violation for cell "inv layout" Total errors found: 0

## 43.Verify $\rightarrow$ Extract

Extractor		×
OK Cancel Defaults	Apply	Help
Extract Method 🔶 fla	t $ \diamondsuit$ macro cell $ \diamondsuit$ full hier $ \diamondsuit$ incremental hier	
Join Nets With Same Name	Echo Commands	
Switch Names	Extract_parasitic_caps Set Switch	es
Run-Specific Command File	<b>□</b>	
Inclusion Limit	1000	
View Names Extracted	extracted Excell excell	
Rules File	divaEXT	
Rules Library	U_TechLib_ami06	
Machine	🔶 local 🔷 remote 🛛 Machine 📋	

If the process is not successful, you can click on "Info" in the LVS window or you can check the log file.

## 44. Verify $\rightarrow$ LVS

X LVS						
Commands			Help 14			
Run Directory	r∧aĮ		Browse			
Create Netlist	📕 schematic	🔳 extracted				
Library	ELE462	ELE462				
Cell	inv	inv				
View	schematič	extracted				
	Browse Sel by Cursor	Browse Sel	by Cursor			
Rules File	divaLVS.rulį̇́		Browse			
Rules Library	NCSU_TechLib_ami06					
LVS Options	E Rewiring	🔲 Device Fixin	g			
🔟 Create Cross Reference 🔎 Terminals						
Correspondence File 🔟 /u/zhenluo/run/lvs_corr_file Create						
Priority 🗓 Run local 🖃						
Run	Output Error Display	Monitor	Info			
Backannotate	Parasitic Probe Build	Analog Bui	ld Mixed			

If there is an error, then in the LVS window, click on "Error Display".