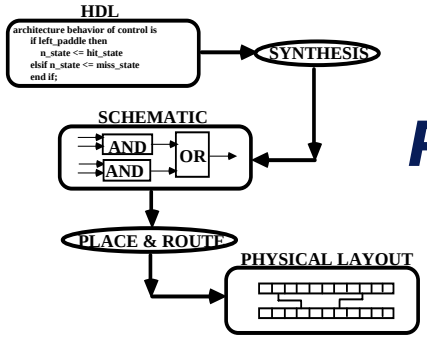
DESIGNING ASICS

ECE 651 Overview



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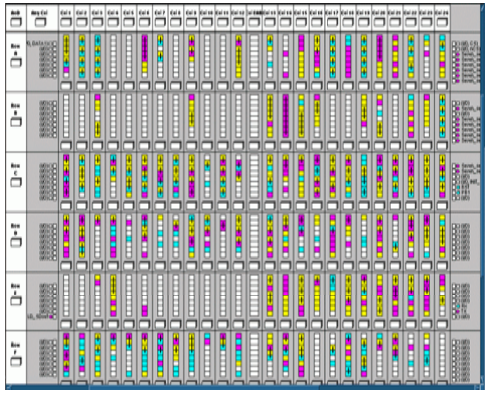
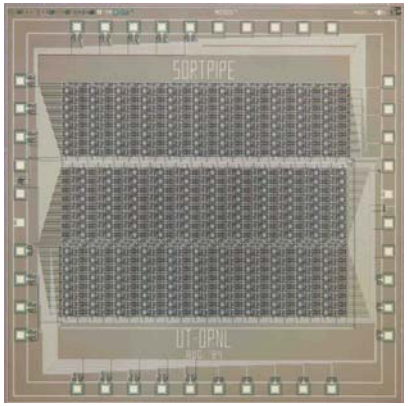
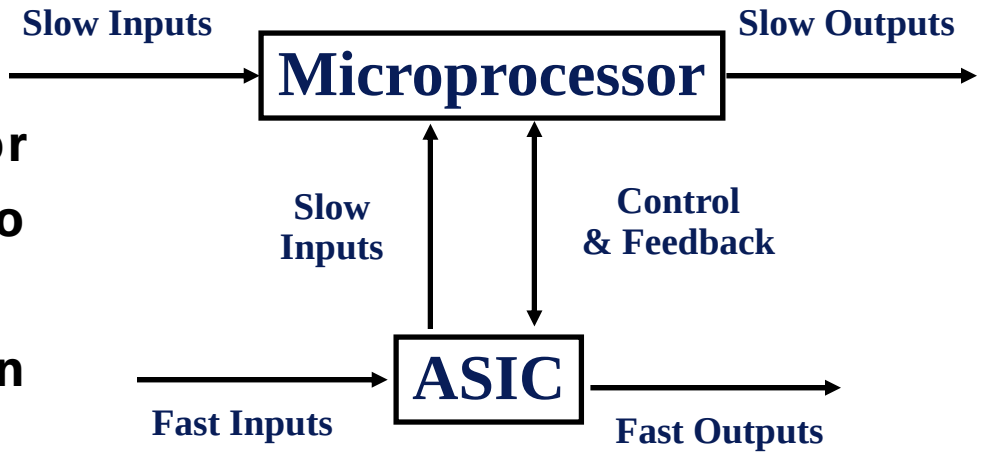


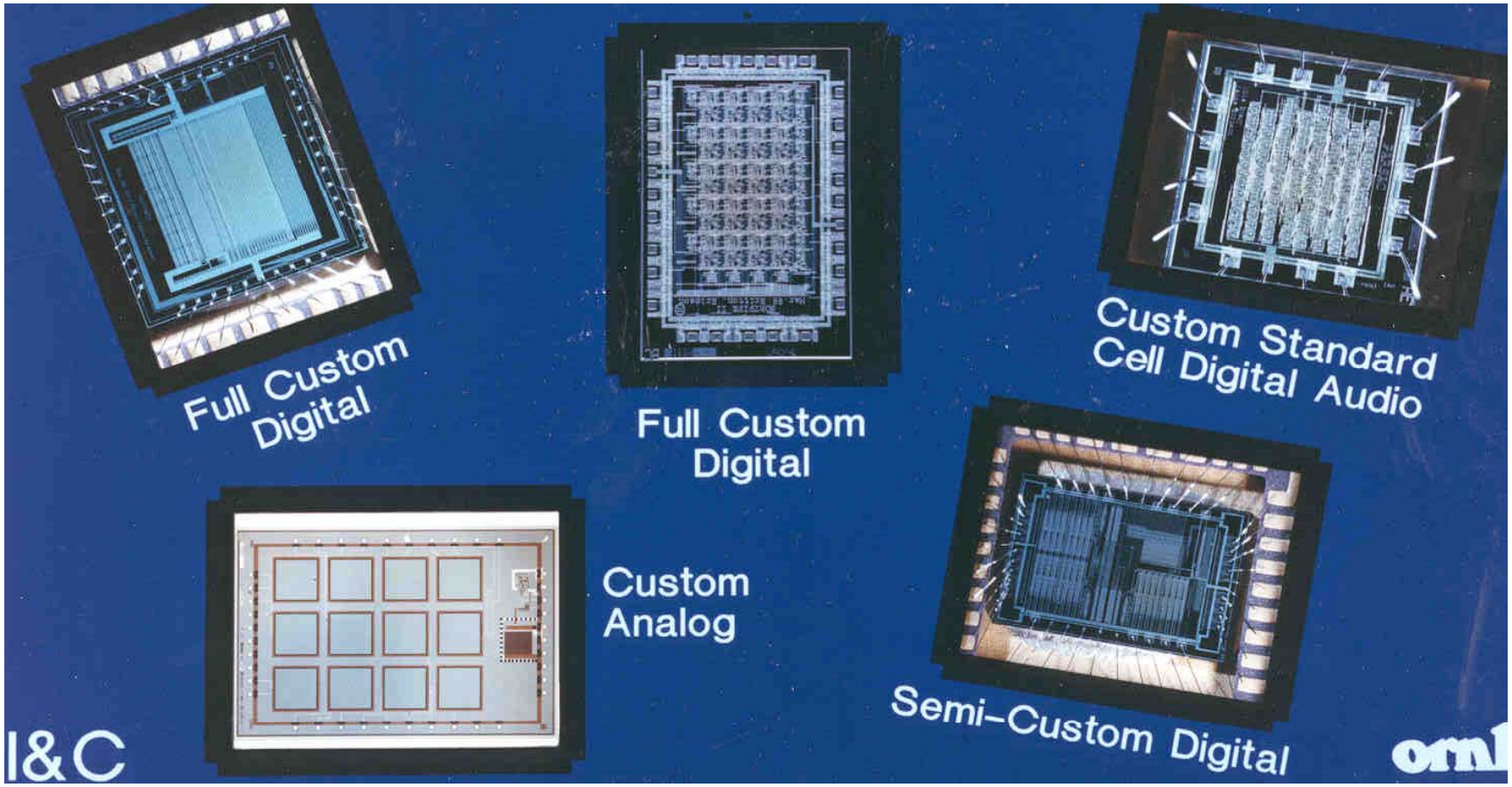


SYSTEM FUNCTIONS ARE OFTEN SPLIT BETWEEN THE CPU AND AN ASIC

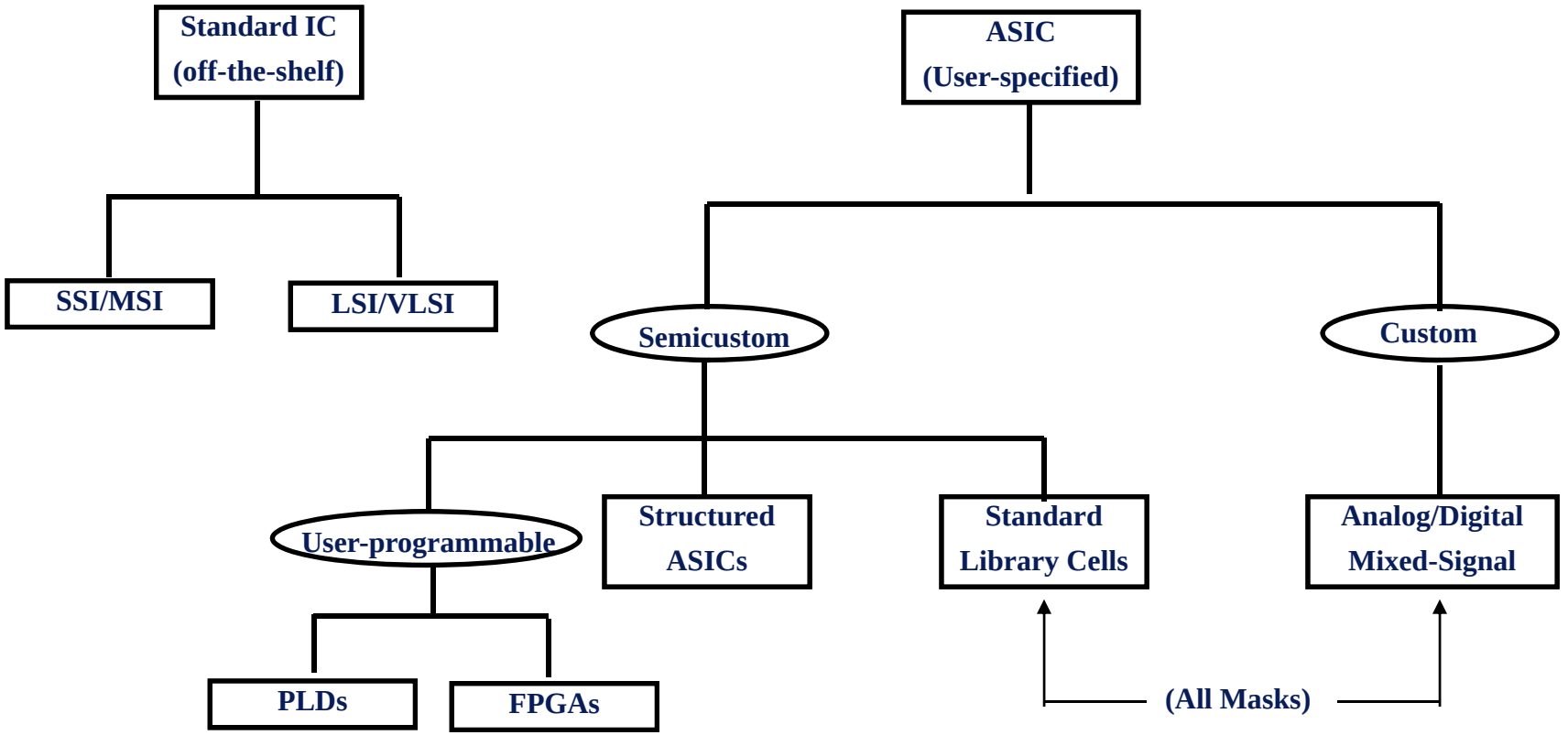
- The most economical means of implementing logic functions is to use a microprocessor.
- When the microprocessor is too slow or too busy to handle some fast inputs and outputs, an ASIC can be used to implement high-speed concurrent operations.



A VARIETY OF ICS ARE POSSIBLE

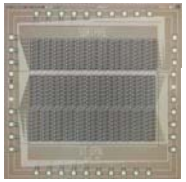


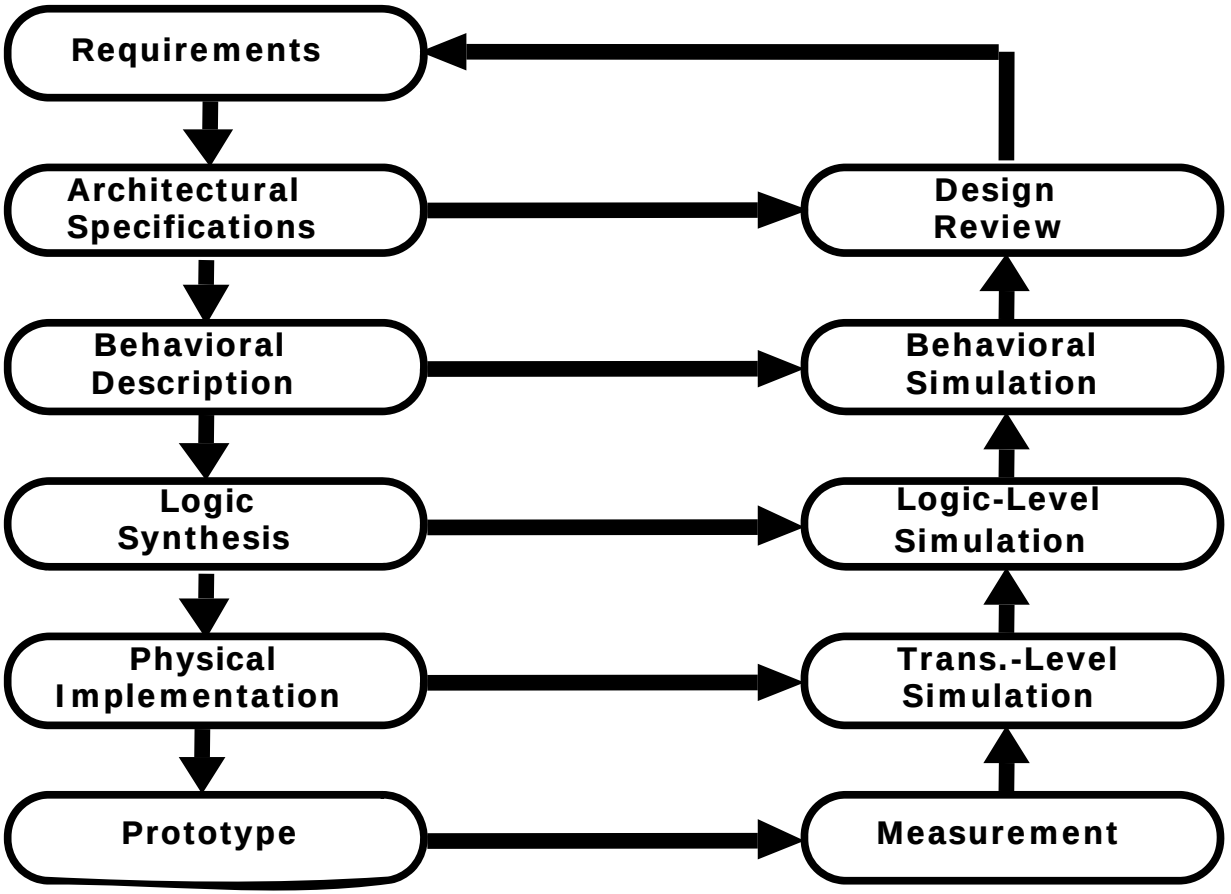
APPLICATIONS MAY USE STANDARD ICs or FPGAs/ASICs



MICROELECTRONIC SYSTEM DESIGN CONSISTS OF ITERATIVE REFINEMENTS OF SYNTHESIS AND VERIFICATION

TRENDS





ECE 551 & ECE 651

- ECE 551 (logic level; b/w):
  - Pairs create project using VHDL
  - Simulate pre-synthesis and post-layout
  - Demonstrate using 200K-gate Xilinx FPGA on Spartan3 Board with I/O
  - Implement on screen only using Altera FPGA

- ECE 651 (physical level; color):
  - Perform custom IC design (but not submit for fab)
  - Compare manual design vs. automated tools
  - Study nanometer design issues (cross-talk, power)

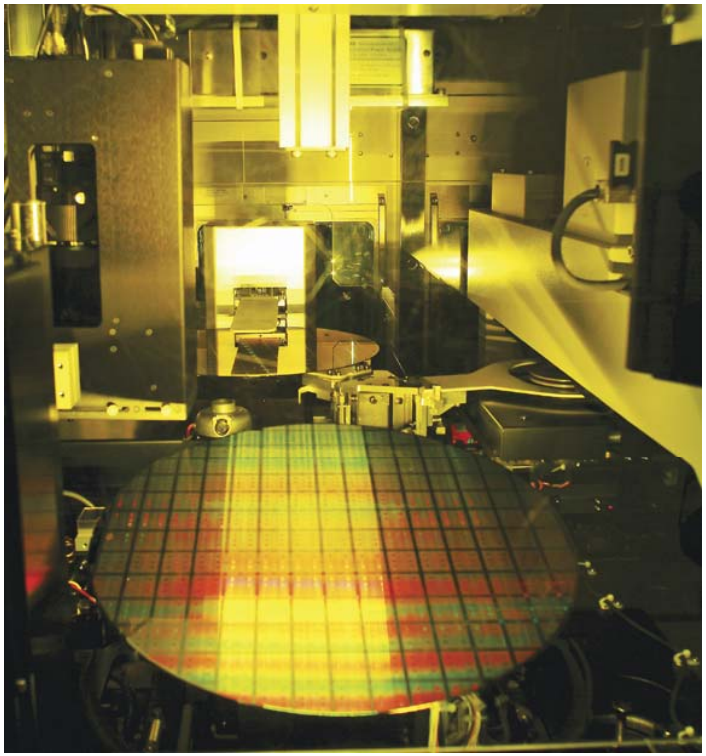
FAB FOUNDRIES COST BILLIONS

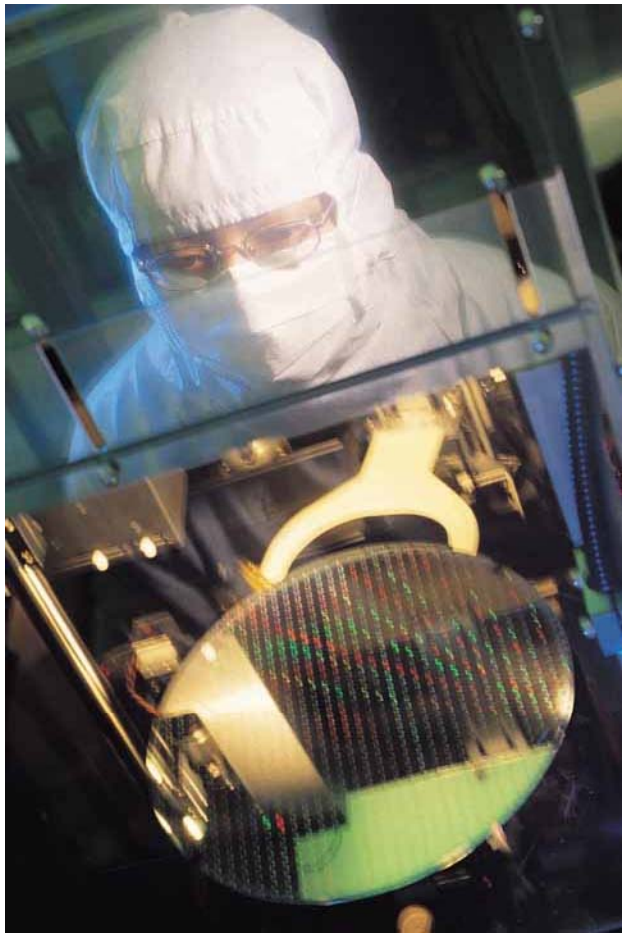
- Intel spent $3 billion to construct and equip its integrated circuit fabrication facility in Chandler, Arizona.
- The foundry produces 300-mm wafers using feature sizes of 45 nanometers.

http://www.intel.com/

MASK CHARGES COST MILLIONS

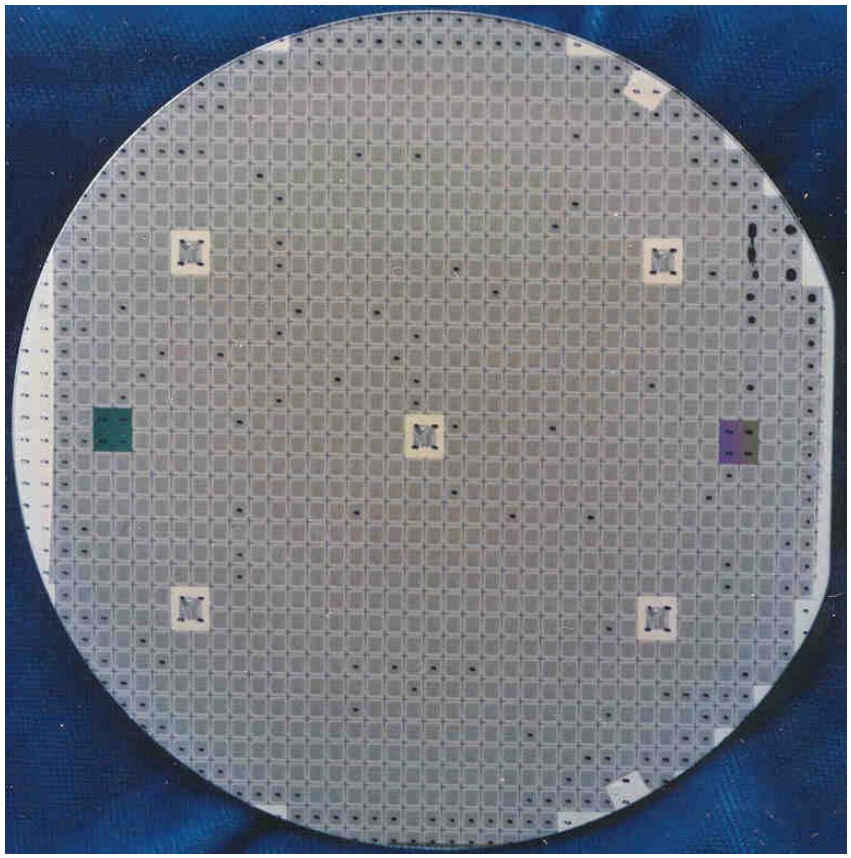
- **According to SemaTech, a mask set for 65-nm costs $3 million.**



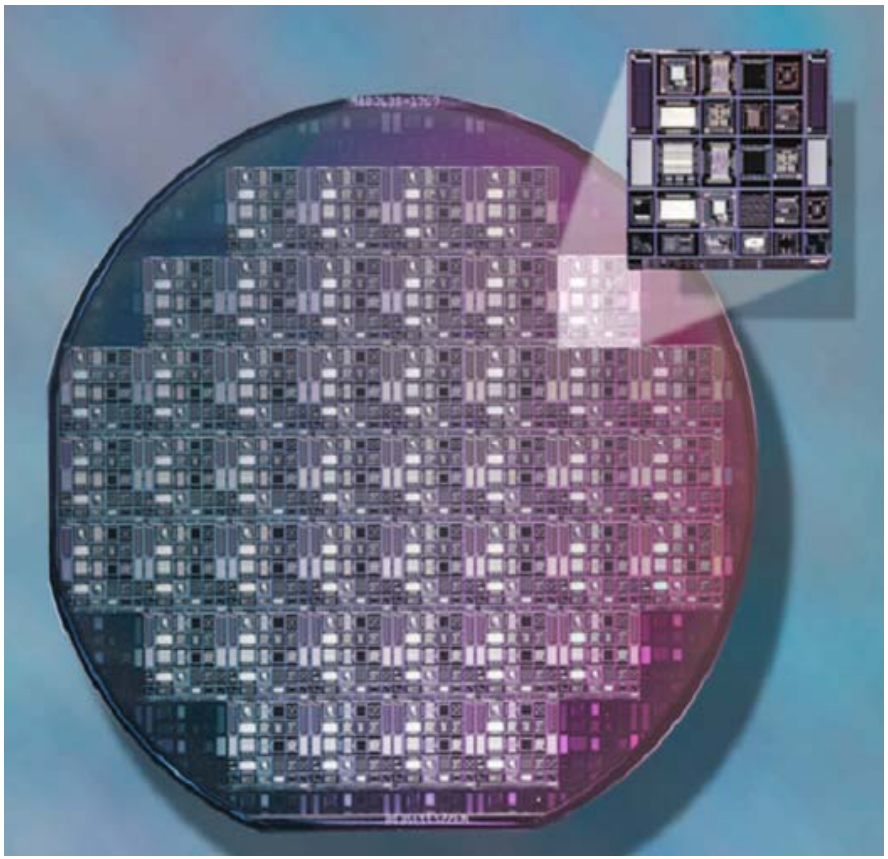


http://www.tsmc.com/

SHARING MASK / WAFER COSTS



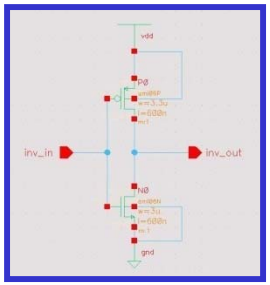
http://www.ssec.honeywell.com/



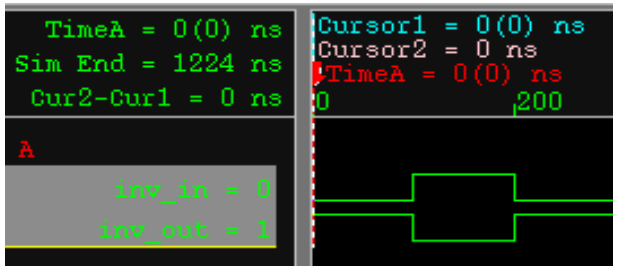
http://www.mosis.org/

CUSTOM IC DESIGN FLOW

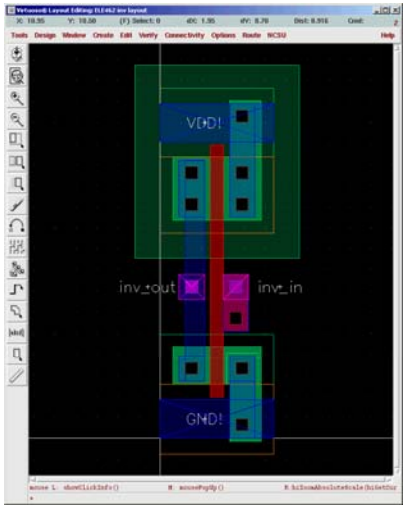
1--SCHEMATIC



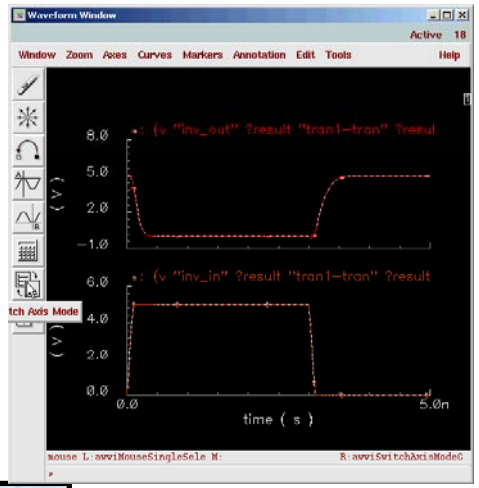
2--PRE-LAYOUT LOGIC SIMULATION



3—MANUAL LAYOUT

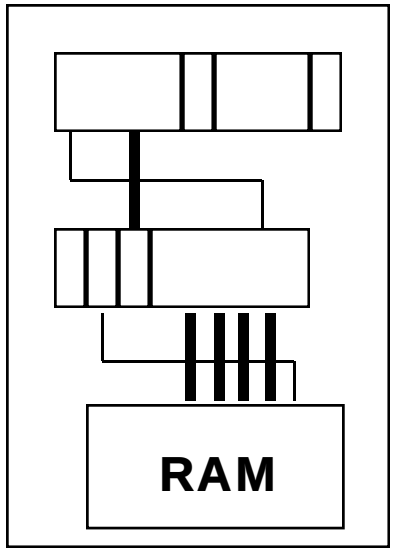


4--POST-LAYOUT TRANS. SIMULATION



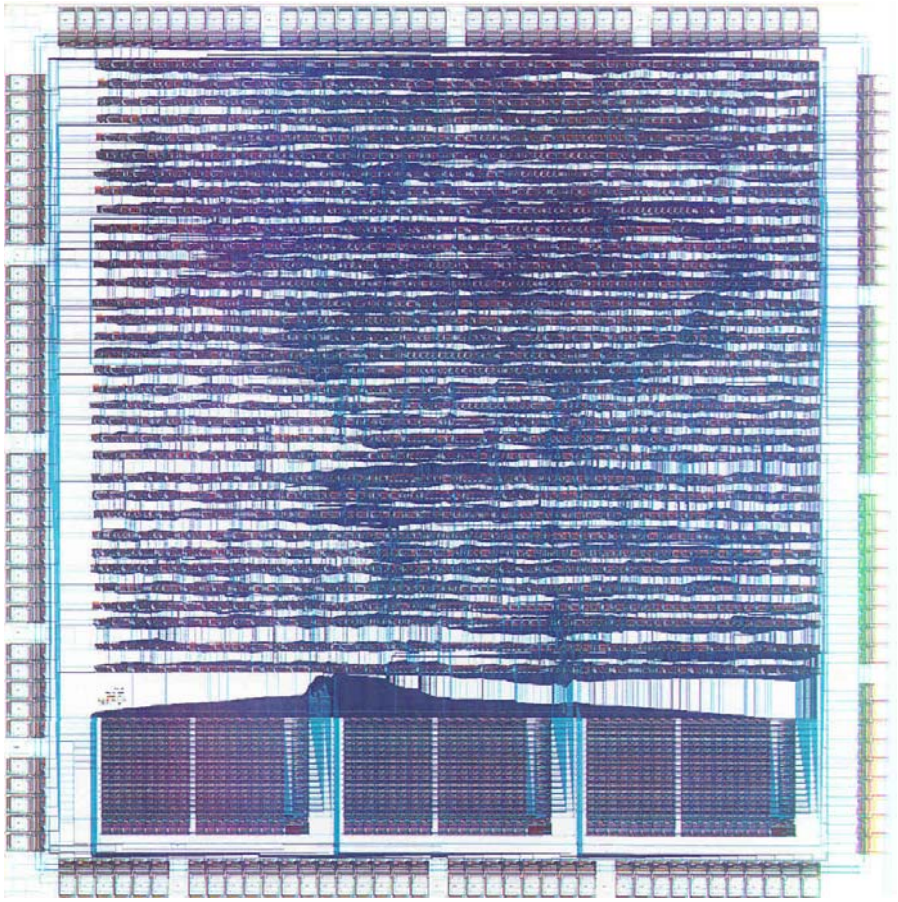
STANDARD-CELLS ARE BEST FOR HIGH-QUANTITY APPLICATIONS WITH RAM

Standard-Height Library Cells

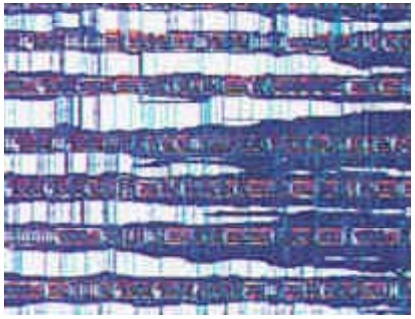


- Vendor develops library disk files of logic functions (and internal RAM or cache).
- User selects cells and specifies *two* layers of interconnections
- After place & route, masks are made for *all* layers
- Replaces 20,000 to 2,000,000 gates (or more)
- Workstation-based development system costs more than $ 200K
- Turnaround time for prototypes is 8 weeks

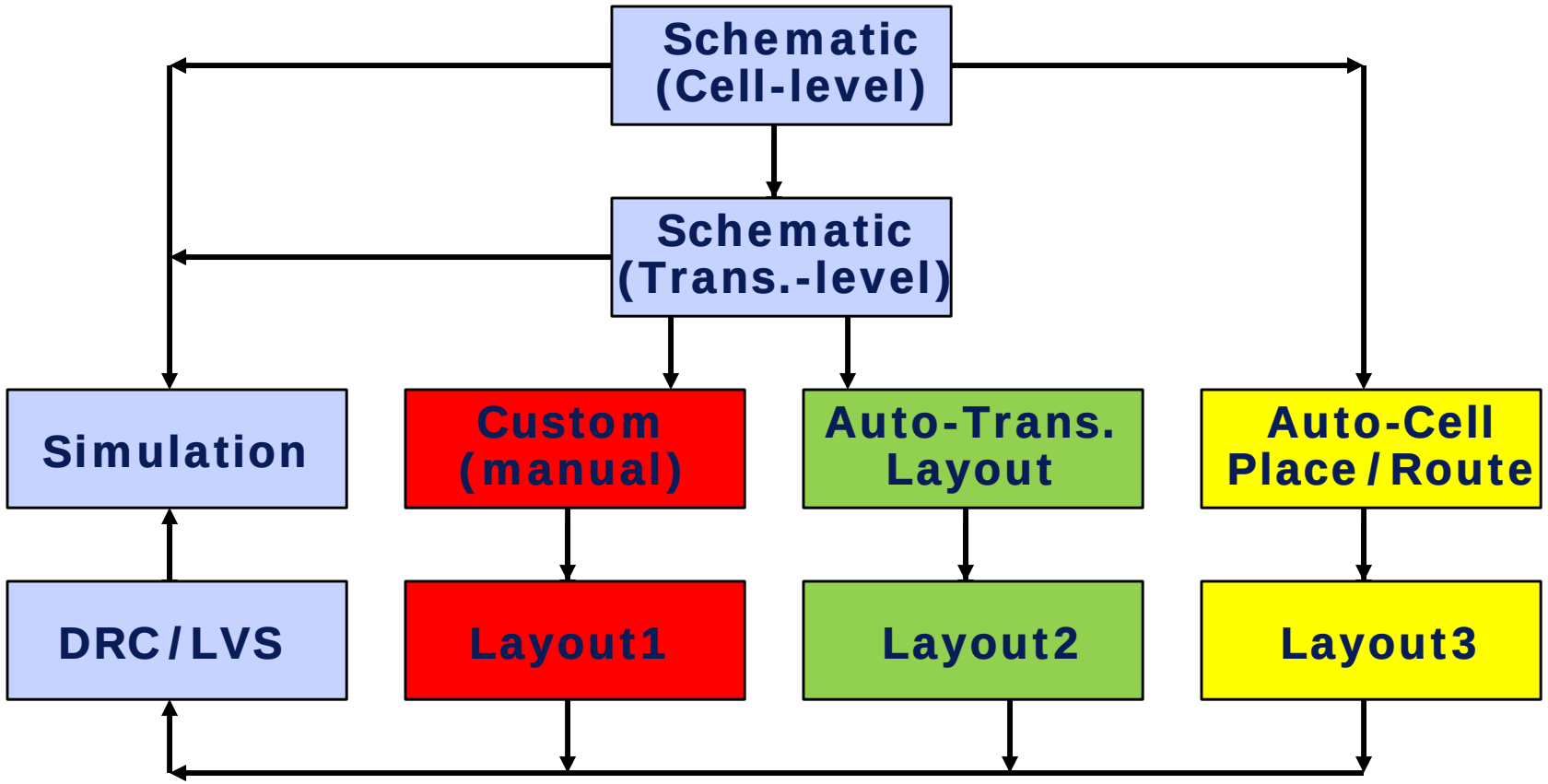
STANDARD-HEIGHT CELL CHIPS CAN ALSO USE EMBEDDED RAM



Space between rows for wiring can be varied as needed.

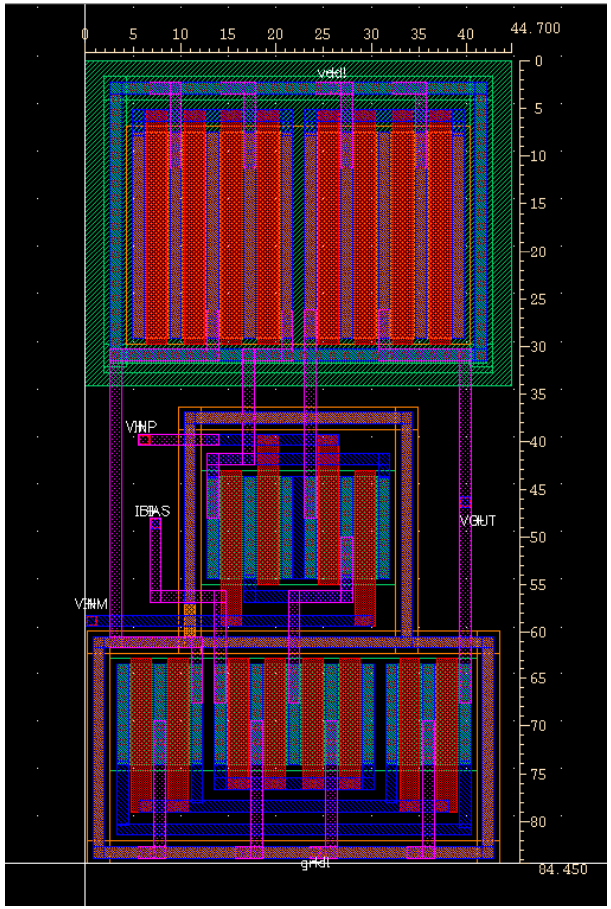


LAYOUT COMPARISONS



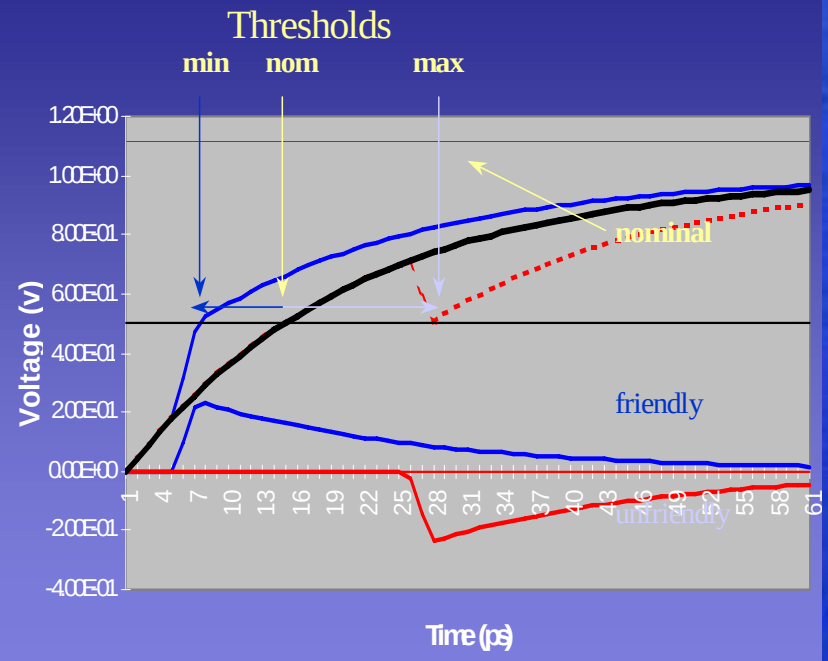
SPECIAL TECHNIQUES ARE USED FOR LAYOUT OF ANALOG CIRCUITS

- Layouts use multi-gate fingers and common-centroid symmetry to improve matching of devices.
- Poly2-Poly1 capacitors save space.
- Switched-capacitor circuits replace large resistors.
- Guard rings reduce noise.



SIGNAL INTEGRITY AND POWER ISSUES ARE ESCALATING

Effects of Crosstalk: Delay Uncertainty



http://vlsicad.ucsd.edu/ http://www.tomshardware.com/

COURSE GOALS

This design-oriented course involves:

(1) comparison of layout methods (manual vs. two automatic ones)

(2) nanometer design issues (cross-talk, power, yield)

(3) with local/remote access to LINUX workstations

(4) grade depending on homework and final exam

(5) all presentation slides will be posted on the web:

http://web.eecs.utk.edu/~bouldin/courses/651/overview.html