0.5 Micron CMOS Standard Cell Data Book AMI5HS 5.0 Volt

AMERICAN MICROSYSTEMS, INC.

AMERICAN MICROSYSTEMS, INC.

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ON-LINE UPDATES TO THIS INFORMATION

The information contained herein was the most current and accurate available at the time of printing. AMI's on-line data books at http://www.amis.com/databooks is kept current with all the latest updates. Updates to sales office information can also be found at http://www.amis.com/sales. In order to assist in the design of ASIC's, AMI has written several application notes on a wide range of design topics that can be accessed online at http://www.amis.com/app_notes. We suggest that you visit AMI's web site to ensure that you have the latest information and assistance prior to beginning the design of your ASIC.

GENERAL INTRODUCTION

American Microsystems, Inc. - Providing customers the best total ASIC solution for more than 30 years.

American Microsystems, Inc. (AMI) pioneered the development of the world's first custom MOS ICs in 1966. With more experience than any other ASIC vendor, you can be assured that when you bring your ASIC development project to AMI, you are working with a dependable team that has the depth of experience to provide you with an optimum solution, on time and on budget.

The vision shared by all employees at AMI is expressed in our mission statement:

> *We will provide customers the best total solution employing our digital and mixed signal capabilities coupled with extraordinary service.*

AMI strives to realize this vision by offering a range of products and services aimed at improving cycle time, reducing overall design cost, achieving world-class reliability, and designing to customer need. AMI provides a full range of digital and mixed-signal ASICs, ASIC design software and services, including FPGA-to-ASIC translations, and modular foundry services. AMI's standard product offerings, including Waveplex™ wireless products, aimed at the communication industry, and timing generator products.

AMI is a corporation whose headquarters and ASIC design and manufacturing operations are located in a 492,000 square foot facility in Pocatello, Idaho. AMI has a software R&D facility in Twain Harte, California, and owns a subsidiary, AMI (Philippines), Inc., located in a 64,000 square foot facility in Manila, Philippines, for electrical testing of AMI's products.

Markets

- Communications
- Industrial
- Automotive
- EDP
- Medical
- Military

Sales and Distribution

- Eight full-service sales and technical support offices located in key markets throughout North America.
- Six technical service centers located in San Jose, Los Angeles, Boston, Portland, Dresden, and Tokyo, which offer customers a full range of digital ASIC design resources and services.
- 41 sales representative offices throughout North America, with more than 110 outside salespeople.
- AMI's standard product and ASIC offerings are available through 151 distributor's offices in the United States and Canada.
- In Europe, AMI is represented by distributors or sales representatives in the United Kingdom, Germany, France, Italy, Spain, Netherlands, Switzerland, Belgium, Israel, Finland, Norway, Sweden, and Denmark. AMI maintains a technical service center in Dresden, Germany.
- In addition to a sales office in Tokyo, Japan, AMI is represented by distributor/sales representatives in that country and in Singapore, Taiwan, Australia, Hong Kong, and India.

General Introduction

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Products

ASICs

- Digital and mixed-signal, standard cell, and gate array ASICs. AMI's ASIC products are supported with a library of more than 500 digital cells, memories, and megacells, designed in the company's 0.35, 0.5, 0.6 and 0.8 micron CMOS process technologies. These libraries support industry standard core and I/O voltages. They are also compatible with all popular industry-standard CAE environments.

ASIC Design Software

- ACCESS Design Tools™ software offers customers the ability to design, optimize and verify their ASIC circuits through post-layout sign-off simulation with a suite of software tools that efficiently support the ASIC design engineering function.
- AMI's ACCESS product line includes NETRANS™ FPGA-to-ASIC and ASIC second-sourcing conversion software for a cost-effective migration path to an AMI gate array or standard cell development.

Services

PLD/FPGA/ASIC Conversions

- 12 years conversion experience with NETRANS.
- Over 1000 designs converted
- Low-cost replacements
- Pin-for-pin socket replacements
- Multiple-to-one conversions
- Vectorless migration option
- Significant power reductions
- Improved performance

ASIC Design

- Design Checker™, Gate Gobbler™, and Clock-Tree Synthesis software for optimizing ASIC designs.
- Equation Based Delay Calculator, Pattern Checker, 5-Corner Logic Simulator™, Verilog and VHDL sign-off simulators for accurate design verification.
- Tempest™ cell-compiler software swiftly customizes logic functions for specific customer applications.

ASIC Design for Test Solutions

- NETSCAN™—AMI's proprietary scan-chain insertion software and automated test-pattern generator software for increasing fault coverage.
- NETTAG™—AMI's JTAG insertion software for boundary scan testing.

Foundry Services

- Advanced CMOS technology brings low power consumption, high noise immunity, and high circuit densities to digital and mixed-signal ASICs.
- Feature sizes as small as 0.5 micron (drawn), and as large as 5 micron (drawn).
- Process modularity enables automated fabrication steps to be variously combined in ways tailored to meet the specific manufacturing requirements of analog, digital, and mixed-signal devices.
- "Flexible factory" provides a diversity of fabrication processes and schedule options to meet customer requirements.
- Long term support of mature processes.

Corporate Headquarters

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SELECTION GUIDE

Simple Gates

Complex Gates

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Pull Pieces

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Overview

AMI5HS 0.5 micron CMOS Standard Cell

Description

The “AMI5HS” standard cell family combines compact, building block standard cells and megacells with high speed memory and datapath functions. Using a 0.5µm, high performance, CMOS process, the AMI5HS family offers a lower cost alternative to gate arrays for high volume applications.

Features

- **Minimum drawn length: 0.6µ**
- **Excellent performance:**
  – 590 MHz maximum toggle rate on clocked flip-flops (T_J = 135°C)
  – 218 ps delay (FO=2; L=2mm) for a 2-input NAND gate
  – 103 ps delay (FO=2; L=0mm) for a 2-input NAND gate
  – 6 ns clock to out performance (CL = 35 pF)
- **Unparalleled temperature ranges:**
  Operating temperatures range from -55 to 125°C.
- **Clock Tree Synthesis:**
  Clock drivers are placed to minimize clock skew and latency effects on circuit performance. Parameterized clock buffers model the clock trees before layout. AMI matches the simulation parameters of the prelayout models with a physical clock tree during layout.
- **Cost driven architecture:**
  A choice of 2 or 3 level metal interconnect provides the lowest device cost for the number of gates and pads required.
- **Extensive library for quick design:**
  – Complete primary cell and I/O library
  – Synchronous ROM compiler from 64x1 to 16Kx32 bits
  – Megacells include processors, peripherals, and datapath synthesizers
  – 100% compatible with AMI’s proven ASIC Library
- **Extensive RAM support:**
  – Asynchronous, synchronous, single, dual, and n-port
  – Build from any configuration of 16x1 and 256x8, 512x4, 1024x2, and 2048x1 blocks up to the maximium gate count of the array
- **Extensive I/O cell options:**
  – User-configurable pad cells with predefined components
  – 1 to 24 mA per single I/O cell
  – Custom configurations for I/O drive up to 96 mA
  – Standard and slew rate limited available
  – PCI 33 MHz compliant
  – CMOS, TTL, LVCMOS, LVTTL, PCI (33MHz) levels
- **Mixed voltage operation:**
  – Split power supply bussing between core and pads
  – 3.0 or 5.0V core operation
  – Mixed 3.3V and 5.0V I/O pads
  – 5V input tolerance on 3.3V pads
  – 5V output drive with 5.0V power pads
- **Extensive packaging capabilities:**
  – QFPs, CQFPs, TQFPs, PLCCs, LCCs, JLCCs, PBGA, BGAs, PGAs, CPGAs, SOICs, TSOPs, PDIPs, PQZs, M-QUADs, individual die
  – Burn-in capability as required
- **Automatic Test Program Generation:**
  Scan macros (NETSCAN™) for high fault coverage
- **JTAG Boundary Scan macro support**
- **Full operating voltage range from 2.7V to 5.5V**
- **ESD protection > 2kV; latchup > 100 mA**
- **Power dissipation:**
  1.58µW/MHz/gate (FO=1; V_{DD}=5.0V)

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AMI5HS 0.5 micron CMOS Standard Cell

Architectural Overview

Some important elements of the AMI5HS standard cell family include: (see figure 1: Standard Cell Architecture)

- Selectable 2 or 3 level metal interconnect allows the lowest device costs.
- Individually compacted cells have each cell function tightly compacted to a fixed bus height. Cells are placed in rows, and V_{DD} and V_{SS} supplies feed through the cells. Cell widths and heights increase to accommodate functions with more gates. Transistor sizes and routing are optimized for each function, giving a much tighter cell design than with gate arrays or fixed pad, ring embedded, array products.
- Routing channel width varies with local cell routing requirements. Rows of cells can be placed adjacently if little routing is required between them, or greatly separated to allow routing a large data bus. Tracks of unused channels are not lost as in gate array or embedded array products. For 3 level metal, this feature can combine with routing over cells to give a very “area efficient” design.
- Power pads are placed as required among I/O cells and can be placed in corners. Each individual I/O can be powered to 3.3V or 5.0V. Core operating voltage range is 2.7V to 5.5V.
- Megacells and datapath functions are soft cells built from AMI’s ASIC Library. They are placed as if part of the customer defined logic. Full netlists are provided to allow customization of the cells.
- Compiled memory blocks are individually compacted to customer defined width and depth. Table 2, “AMI5HS Standard Cell Memories,” on page 2-6 lists the available memory compilers.

Figure 1: Standard Cell Architecture

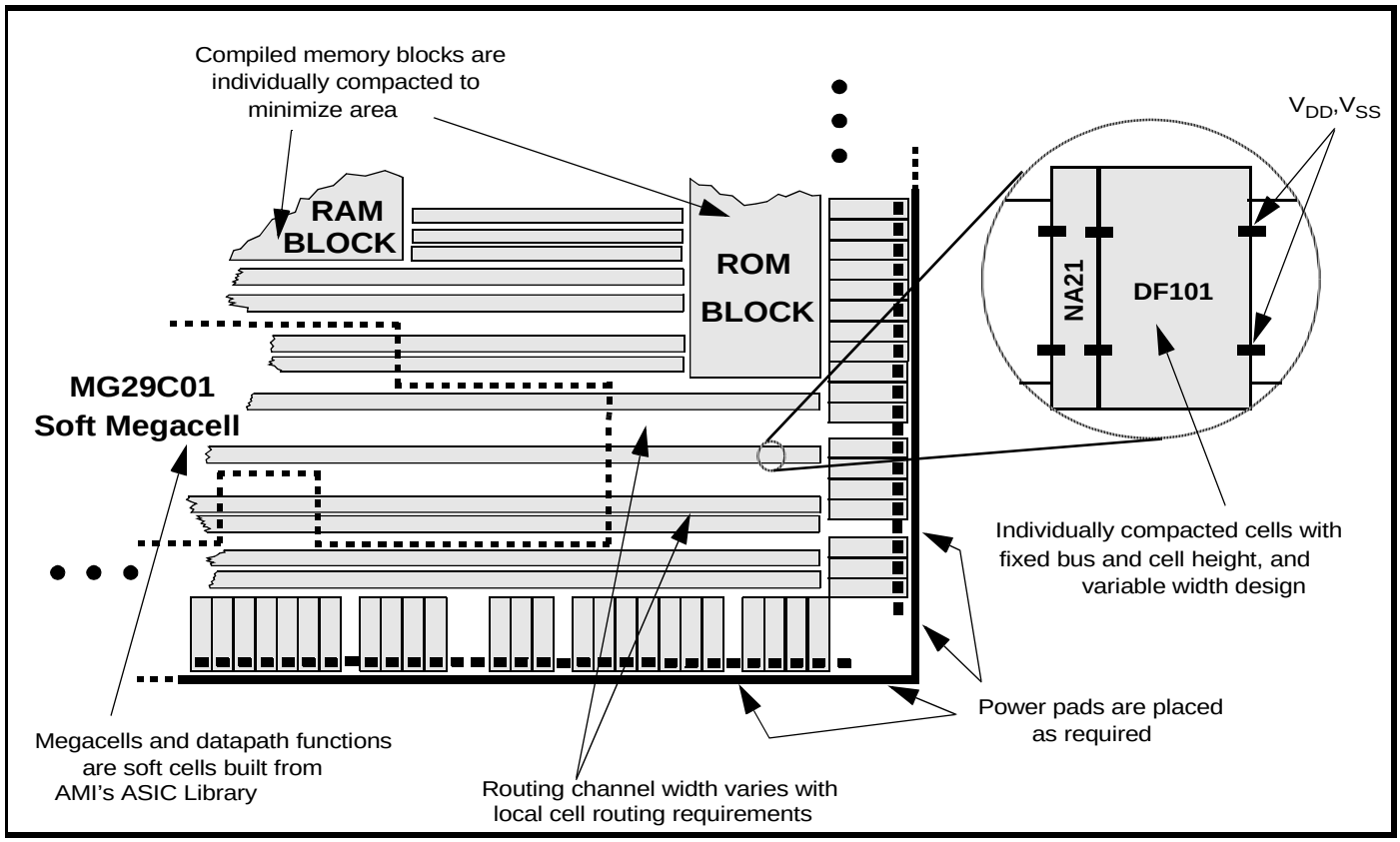

Table 1: AMI5HS Standard Cell Family

Feature		Description	Comment
Complexity		Up to 1,980,000 gates[1] Up to 1,600,000 gates	50% memory, 50% megacell and user defined logic 100% user defined logic
I/O Count		Up to 512 pins Up to 836 pins	Test equipment limit; signal pins only Die size limit; includes power supply pins
Delay Time	Internal Gate	82 ps (Fanout=1, L=0mm) 103 ps (Fanout=2, L=2mm)	2 input NAND gate, T=25°C, V_{DD}=5.0V
	Input Buffer	589 ps (Fanout=2, L=2mm)	CMOS Input buffer, T=25°C, V_{DD}=5.0V
	Output Buffer	1019 ps (C_L=15pf)	CMOS Output buffer,T=25°C, V_{DD}=5.0V

1. Compact memory arrays greatly increase gate count on an equivalent gate basis.

MIXED VOLTAGE I/O MACROS FOR 5 VOLT TOLERANT AND 5 VOLT COMPATIBILITY

- Technology continues to drive down the maximum core and I/O operating voltages of ASICs. Since board level compatibility with the older interface standards continues to exist, ASICs must be able to provide a mixed voltage I/O solution on the same design. The two industry terms that describe these interface requirements are 5 volt tolerant and 5 volt capable. In the following explanations of mixed voltage I/O the two voltages used are 5V and 3.3V, however, the same explanations apply to any mixed voltage I/O application (i.e. 3.3V and 2.5V).
- **5 VOLT TOLERANT:** When operating at 3.3V, special output pad cells are required to drive 3.3V levels and withstand 5V during input or tri-state mode. When receiving signals above 3.3V, these I/O cells must be used to prevent damage to the circuit or disruption of normal circuit operation. The TTL input portion of the I/O cell are programmed to achieve proper switching levels for either 5V or 3.3V inputs but not both. Maximum drive of these cells is less than non 5 volt tolerant macros in the library since many of the output devices in the pad are used to construct the 5 volt tolerant circuitry.
- **5 VOLT CAPABLE:** 5 volt capable I/O requires the cell both accept and drive 5V signals. Separate power pins are required for each of the core and I/O voltages. One or more power pins are used for core and low voltage pad macros and additional power pins are used for high voltage pad macros. All core macros and low voltage pad macros are tied to the 3.3V supply. 5 volt capable pad macros must be used when receiving/driving signals above 3.3V. Each I/O cell has voltage level shifters to allow either 5V or 3.3V external signals to interface to the 3.3V core logic.

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Product Applications

The AMI5HS standard cells are targeted at high volume digital ASIC products. The low device cost accommodates designs requiring significant on-board memory, data path logic, or megacells.

PLD OR FPGA CONVERSION: For high volume products, AMI's NETRANS® converts netlists from PLDs and FPGAs to more cost and performance effective AMI5HS designs.

2ND SOURCE FOR EXISTING PRODUCTS: AMI's netlist conversion capabilities allow AMI5HS to be a cost-effective, alternate supply for existing high volume products.

PROCESS UPGRADE: AMI ASICs designed in 1.25µm, 1.0µm, 0.8µm, and 0.6µm processes can be easily upgraded to the AMI5HS family. The AMI ASIC Library provides a common netlist design base.

ADDING CUSTOM BLOCKS: AMI specializes in adding custom logic and simple analog functions to ASIC designs.

ASIC Design Tools and Methodology

AMI ASICs are supported on many third party software platforms:

- Cadence®
- Mentor Graphics™
- Synopsys®
- Viewlogic®
- Veribest®
- Motive™
- Exemplar Leonardo™
- SDF back-annotation
- VHDL Vital simulation™ (sign-off pending)
- Verilog® simulation (sign-off)
- IKOS® Classic and Voyager simulation accelerator (sign-off)

AMI's proprietary expert-system software, ACCESS Design Tools™, is an integrated suite of software tools for digital ASIC verification, FPGA migration, and ASIC second sourcing. ACCESS allows greatly shortened development spans, lower NRE, and increased first silicon success. AMI's software support methodology ensures a tight, well-coupled design to the fabrication process. AMI's dedicated, experienced engineering staff can assist at any step in the design process.

ASIC Design Flow

(See Figure 2: "ASIC Design Flow" on page 2-5) To help customers design their ASICs, AMI supplies a design kit with a cell library containing symbols, simulation models, and software for design verification, timing calculation, and netlist generation. Prelayout timing simulations use capacitance and resistance values derived from statistical averages of known layouts. After the actual layout is completed by AMI, a post-layout interconnect capacitance and resistance table is supplied for final validation of device timing.

Working with an AMI design center, customers capture and verify their designs using AMI's ASIC Library. They also create test vectors for the logical part of their manufacturing test. AMI provides automatic test program generation software, megacells, and netlist rule checkers to greatly speed up the design. A fault coverage check of the test vector set is an optional service.

A "Design Start Package" is completed by the customer and submitted to AMI engineers for review. The Start Package contains the device specification, netlist, pin list, critical timing paths, and test vectors. The design is pre-screened using AMI's ACCESS Design Tools and then resimulated on IKOS Classic and Voyager, VHDL, and Verilog (AMI's sign-off simulators). The results are compared to the customer's simulation results.

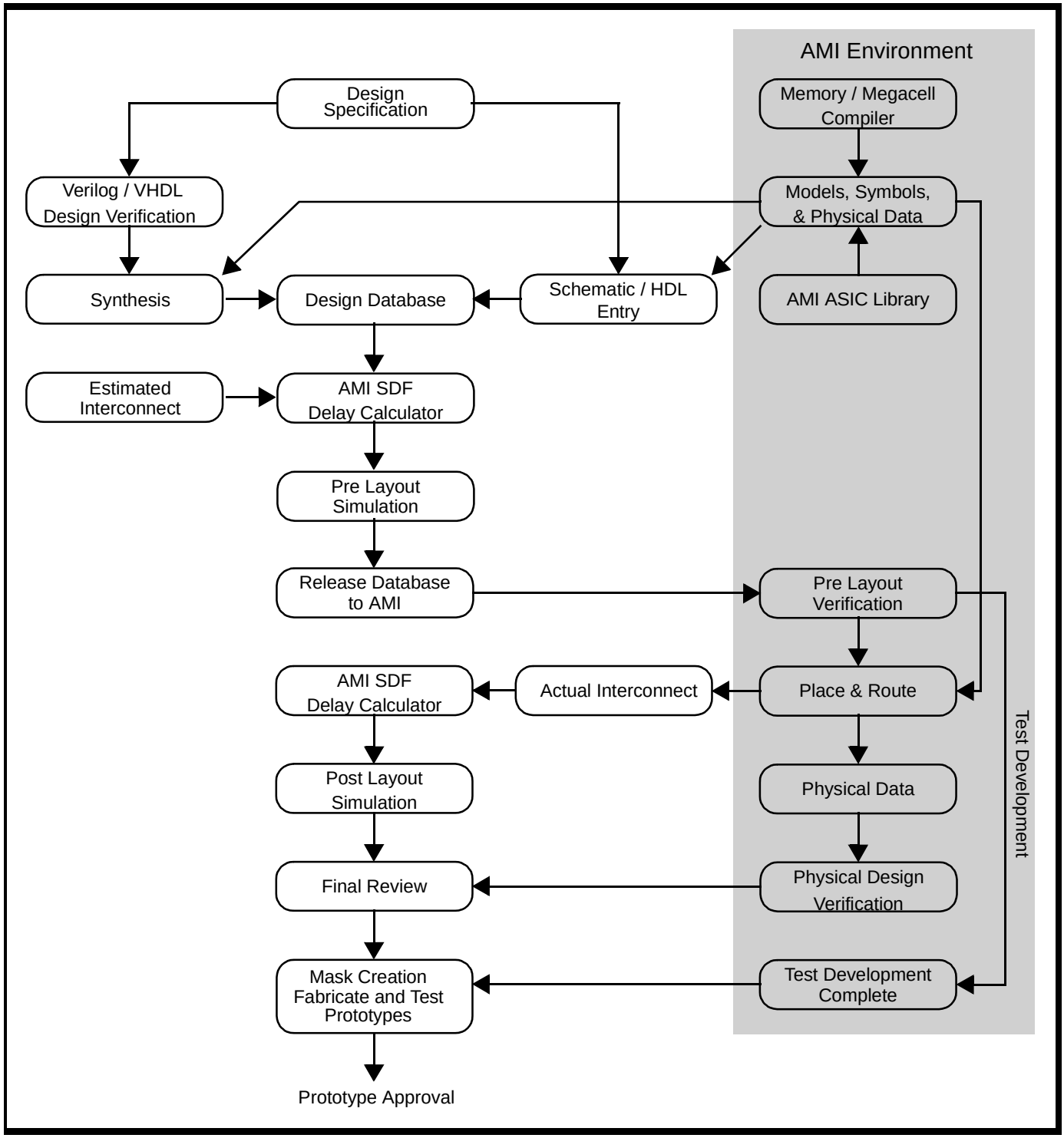
Once the design has passed the initial screening, it is ready for layout. The layout begins by placing memory and megacells, assigning priority to critical paths, and designing the distribution and buffering of clocks. Layout is completed with automatic place-and-route on the balance of the circuit.

After layout is complete, the interconnect data is extracted from the physical layout and fed back to the sign-off simulator for final circuit verification. The post layout interconnect data is sent to the customer for final validation on their simulator. When the post-layout simulation is complete and approved by the customer, the design is released for mask and wafer fabrication.

The test program is developed in parallel with the design using automatic test program generation software. This allows prototypes to be tested before they are shipped.

AMI uses Verilog/VHDL to speed ports between various software products.

Figure 2: ASIC Design Flow



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The Design Library

AMI's design library provides a robust collection of building blocks for the AMI5HS family. A broad range of primary cells is complemented with memory cell compilers and useful megafunctions. Custom cells are quickly designed by AMI's extensive, US-based design team.

The AMI ASIC Library

The AMI ASIC Library contains a rich set of core cells and configurable pad cells. The library is portable across all of AMI's gate array and standard cell families.

AMI's Innovative Pad-Piece Methodology

AMI's ASIC Library provides an innovative approach to I/O pad cell design. Thousands of different I/O cell configurations are possible by choosing from an array of input, output, and pullup/pulldown pad piece cells and making the appropriate schematic or HDL connections. In addition, AMI conversion libraries can easily migrate netlist designs from older technologies that use ASIC Standard pad cells. AMI's ACCESS Design Tools software maps pad cells to their functional (fundamental), pad-piece blocks. Custom configurations are made by combining the pieces. Pad-piece design benefits AMI customers by drastically reducing the need for workstation simulation models of I/O pad cells that do not yet exist. For detailed information of pad-piece usage, see the AMI applications note *Pad Pieces* (4401035).

Memories

AMI's 5HS family includes the memories shown in Table 2. Each of the thousands of possible memory blocks is optimized precisely to the customers' parameters rather than built from a presized leaf cell that covers a range of sizes. This optimizes device size and performance for each memory. All memories are available with Built-In Self Test (BIST) which uses the SMarch test algorithm to maximize fault coverage and simplify testing at a minimal cost in silicon area.

Customers supply cell specifications to AMI, and then eceive simulation timing specifications overnight, and full simulation models for any AMI supported software within five working days. See AMI's web page (www.amis.com) for more information.

Table 2: AMI5HS Standard Cell Memories

Memory	Max. Bits
SRAM (single-port, synchronous, self-timed)	144 KBits
SRAM (dual-port, synchronous)	144 KBits
ROM (single-port, synchronous)	2 MBits
SRAM (single-port, asynchronous)	144 KBits

Megacells

The AMI gate array and standard cell families offer megacells for many popular functions, including: Core Processors, Peripherals, FIFOs, and Datapath (see Tables 3, 4, 5, and Table 6, "Peripherals," on page 2-7). AMI core processors and peripherals duplicate the function of industry standard parts. Data path and FIFO megacells are developed using parameterized logic synthesizers. Most of AMI's megacells are "soft" or "firm" cores that are technology independent and can be customized for specific applications. Detailed functional information can be found in AMI's standard device data sheets.

Table 3: Core Processors

Name	Core Processor Function
MG29C01	4-bit microprocessor slice
MG29C10	Microprogram controller/sequencer
MG65C02	8-bit microprocessor
M8042	8-bit slave microcontroller
M8048	8-bit microcontroller
MGMC32	Core processor, 8051 compatible
MGMC32FB	Core processor, 8051FB compatible
MGMC32SD	Reduced function MGMC32
M320C25	16-bit fixed point DSP
M320C50	16-bit fixed point DSP

Table 4: Datapath

Name	Datapath Function[1]
MGAxxyyDv	Adder
MGAxxyyEv	Adder-subtractor
MGBxxyyAv	Barrel/arithmetic shifter
MGBxxBv	Barrel shifter
MGBxxyyCv	Arithmetic shifter
MGCxxAv	2-function binary comparator
MGCxxBv	6-function binary comparator
MGDxxAv	Decrementer
MGIxxAv	Incrementer
MGIxxBv	Incrementer/decrementer
MGMxxyyDv	Signed/unsigned multiplier
MGMxxyyEv	Multiplier-accumulator
MGSxxyyAv	Signed/unsigned subtractor

1. Datapath logic functions are optimized for either a minimum or specified delay, or a minimum gate count.

Table 5: FIFOs

FIFO Name	FIFO Function[1]
MGFxxyyC1	Fall-through FIFO
MGFxxxxyyD	Synchronous FIFO
MGFxxxxyyE	Asynchronous FIFO

1. AMI supports both latched-based and dual-port RAM-based FIFOs. The latch-based FIFO has a fall-through architecture and is appropriate when the FIFO size is limited. The RAM-based FIFO is appropriate for large-size FIFOs.

Table 6: Peripherals

Name	Peripheral Function
MG1468C18	Real-time clock
M16C450	UART
M16C550	UART
M6402	UART
M6845	CRT controller
M765A	Floppy disk controller
M8251A	Communication interface USART
M8253	Programmable interval timer
M82530	Serial communications controller
MG82C37A	Programmable DMA controller
MG82C50A	Asynchronous comm. element
MG82C54	Programmable interval timer
MG82C55A	Programmable peripheral interface
MG82C59A	Programmable interrupt controller
M8490	SCSI controller
M85C30	Serial communications controller
M8868A	UART
M91C36	Digital data separator
M91C360	Digital data separator
MFDC	Floppy disk controller
MGI2CSL	I^2C Serial bus slave transceiver
MI2C	I^2C Bus Interface

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DC Specifications

Table 7: Operating Specifications

Parameter		Minimum	Maximum	Units
V_{DD} Supply Voltage		2.7	5.5	Volts
Ambient Temperature	- Military	-55	125	°C
	- Commercial	0	70	°C
Junction Temperature	- Military	-55	135	°C
	- Commercial	0	85	°C
CMOS Input Specifications (4.5V<VDD<5.5V; 0°C<T<70°C)				
Vil	Low Level Input Voltage		$0.3*V_{DD}$	Volts
Vih	High Level Input Voltage	$0.7*V_{DD}$		Volts
Iil	Low Level Input Current		-1.0	µA
Iih	High Level Input Current		1.0	µA
Iil	Input Pull-Up Current	-30	-110	µA
Iih	Input Pull-Down Current	30	135	µA
Vt-	Schmitt Negative Threshold	$0.2*V_{DD}$		Volts
Vt+	Schmitt Positive Threshold		$0.8*V_{DD}$	Volts
Vh	Schmitt Hysteresis	1.0		Volts
TTL Input Specifications (4.5V<VDD<5.5V; 0°C<T<70°C)				
Vil	Low Level Input Voltage		0.8	Volts
Vih	High Level Input Voltage	2.0		Volts
Iil	Low Level Input Current		-1.0	µA
Iih	High Level Input Current		1.0	µA
Iil	Input Pull-Up Current	-30	-110	µA
Iih	Input Pull-Down Current	30	135	µA
Vt-	Schmitt Negative Threshold	0.7		Volts
Vt+	Schmitt Positive Threshold		2.1	Volts
Vh	Schmitt Hysteresis	0.4		Volts

Table 8: Output Operating Specifications (4.5V<VDD<5.5V; 0°C<T<70°C)

Driver[1]	Vol Maximum	Voh Minimum	Iol Maximum	Ioh Maximum
1 mA Driver	0.4	2.4	1.0	-1.0
2 mA Driver	0.4	2.4	2.0	-2.0
4 mA Driver	0.4	2.4	4.0	-4.0
8 mA Driver	0.4	2.4	8.0	-8.0
16 mA Driver	0.4	2.4	16.0	-16.0
24 mA Driver	0.4	2.4	24.0	-24.0

1. See “DC Characteristics” on page 2-10 for specific output requirements.

Vol = Low Level Output Voltage given in Volts

Voh = High Level Output Voltage given in Volts

Iol = Low Level Output Current given in mA

Ioh = High Level Output Current given in mA

Table 9: Absolute Maximum Ratings

Parameter		Minimum	Maximum	Units
V_{DD}, Supply voltage		-0.3	6.0	Volts
Input pin voltage		-0.3	V_{DD}+0.3	Volts
Input pin current		-10.0	10.0	mA
Storage temperature	- Plastic packages	-55	125	°C
	- Ceramic packages	-65	150	°C
Lead temperature			300	°C for 10 sec.

Note: The specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect the long term reliability of the device.

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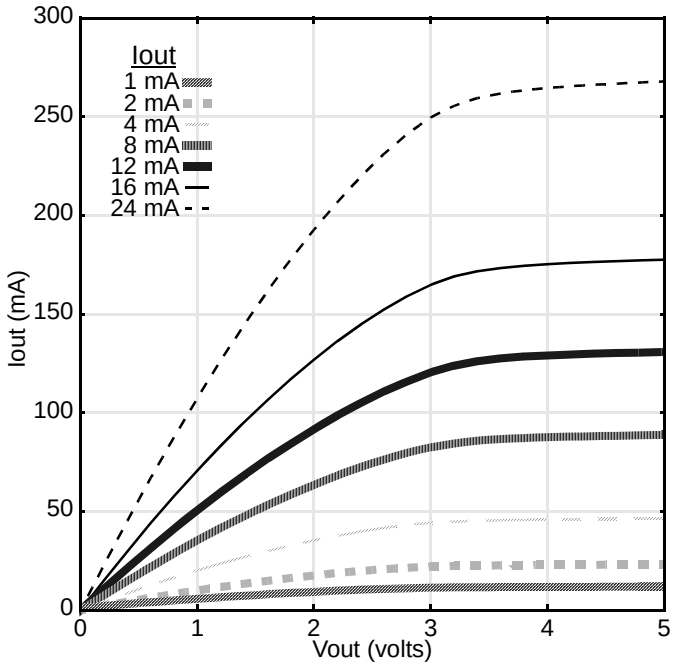
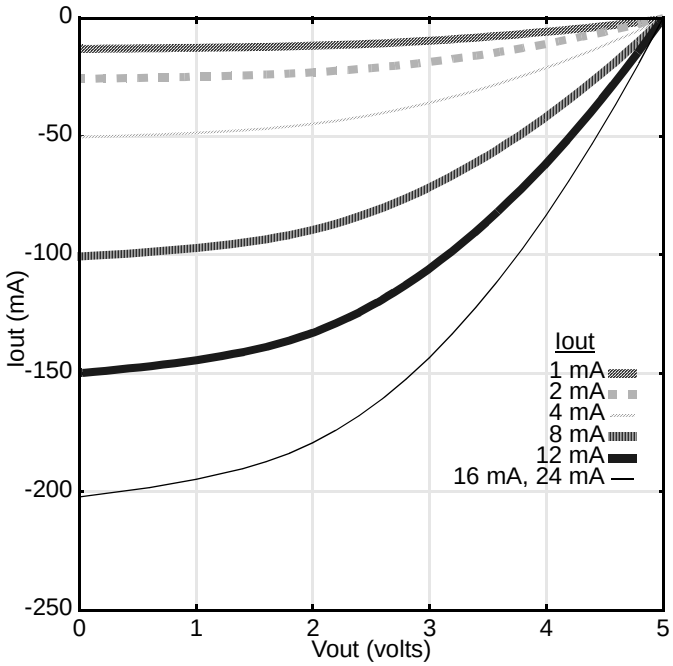
DC Characteristics

(V_{DD} = 5.0V, T = 25°C, Typical Process)

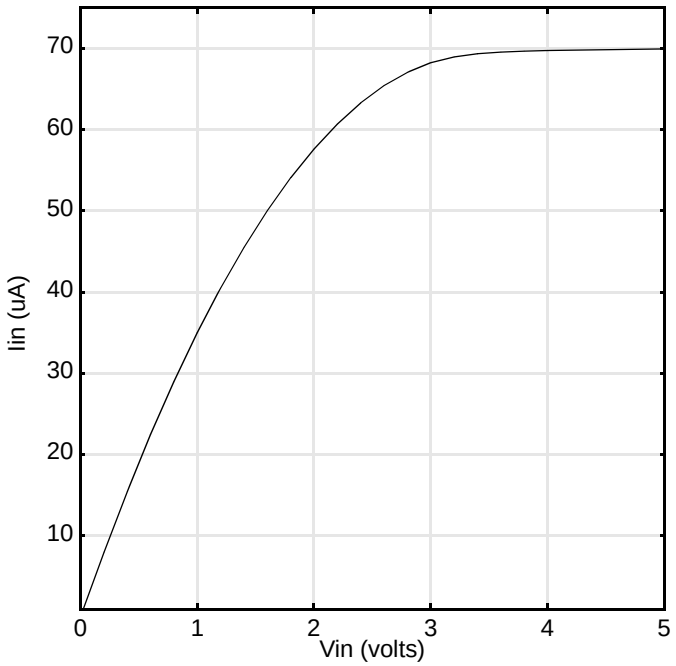
N-Channel Output Driver



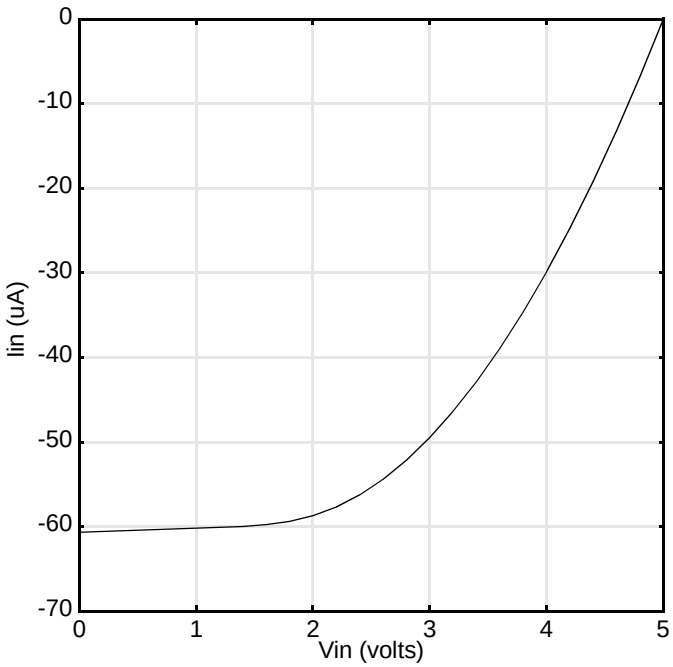
P-Channel Output Driver



N-Channel Pull-Down Device



P-Channel Pull-Up Device



DC Derating Information

The DC Characteristics shown on page 2-10 can be derated to obtain values at other operating conditions using the formula:

$$I_{DC} = (I_{DC}(typ) \cdot K_{PDC} \cdot K_{VDC} \cdot K_{TDC})$$

where: I_{DC}(typ) is a value from the DC characteristic current curves on page 2-10; K_{PDC} is the DC process derating coefficient determined at the processing limits; K_{VDC} is the DC voltage derating coefficient; and K_{TDC} is the DC temperature derating coefficient. The N-channel driver has a different set of coefficients for K_{PDC} and K_{TDC} due to the ESD protection structures.

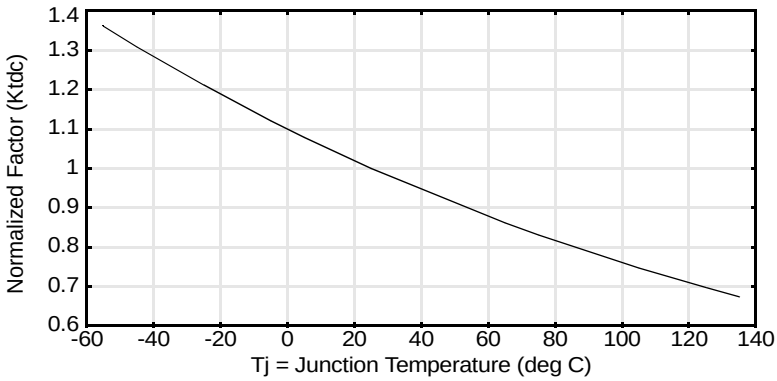
Table 10: DC Variations with Process (KPDC)

	N-Channel Output Driver (Vol = 0.4V)			N-Channel Pull-Down Device (Vol = 0.4V)			All P-Channel (Voh = 2.4V)		
Process	WCS	TYP	WCP	WCS	TYP	WCP	WCS	TYP	WCP
K_{PDC}	0.62	1.00	1.18	0.63	1.00	1.19	0.74	1.00	1.27

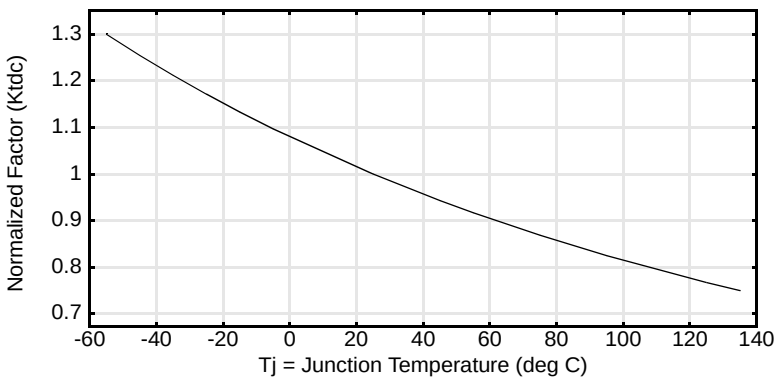
Table 11: DC Variations with Voltage (K_{VDC})

	All N-Channel (Vol = 0.4V)			All P-Channel (Voh = 2.4V)		
V_{DD}	4.5	5.0	5.5	4.5	5.0	5.5
K_{VDC}	0.98	1.00	1.01	0.80	1.00	1.21

DC Variations with Temperature for the N-Channel Output Driver (K_{TDC})



DC Variations with Temperature for all other N-Channel and P-Channel Devices



Delay Derating Information

The propagation delays listed in the data sheets are for typical temperature (25°C), typical supply voltage (5.0V), and typical processing conditions. To calculate the delay at other conditions, use the following equation:

$$T_{pdx} = T_{pdx}(\text{typ}) \cdot K_P \cdot K_V \cdot K_T$$

where T_{pdx}(typ) is given in the data sheets; K_P is the process derating coefficient (determined at the processing limits); K_T is the temperature derating coefficient; and K_V is the supply voltage derating coefficient.

Delay Variations with Temperature (K_T)

Delay varies linearly with temperature. K_T, the temperature derating coefficient, is determined by the following formula and table of common operating point values:

Temp	K_T
-55°C	0.79
-25°C	0.86
0°C	0.96
25°C	1.00
70°C	1.13
100°C	1.22
125°C	1.29

Temp. Range	K_T Formula
-55°C to 140°C	$K_T = 1.0 + (T_J\text{-}25)(2.756E\text{-}3)$

Where T_J is the temperature (in °C) at the silicon junction.

Delay Variations with Process (K_P)

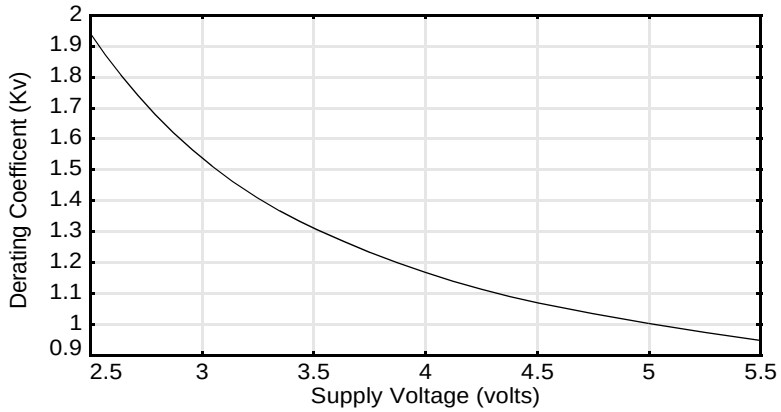
Delay variations with process are fixed constants determined at the limits of acceptable processing. Values for K_P, the process derating coefficient, are shown below:

Derating Coefficient (K_P)	Process Variation Point
1.30	Delay increase due to “Worst Case Speed” (WCS) processing
1.00	Typical delay; Processing target
0.70	Delay reduction due to “Worst Case Power” (WCP) processing

Delay Variations with Voltage (K_V)

Delay varies nonlinearly with voltage. Values of K_V for common operating points are shown below, and a characteristic curve is shown at right.

V_{DD}	K_V
2.7V	1.75
3.0V	1.54
3.3V	1.39
4.5V	1.07
5.0V	1.00
5.5V	0.95



Description of Data Sheet Features

CELL NAME: AMI's cell name.

LIBRARY TYPE: Designates the minimum transistor gate length and library type, such as standard cell or gate array.

DESCRIPTION: Describes the function of the cell.

LOGIC SYMBOL: Shows a picture of the symbol as it appears in the workstation design kits.

TRUTH TABLE: A boolean table showing the output logic levels as a function of the input logic levels.

Types of logic levels found in the logic tables are as follows:

- H = High level steady state,
- L = Low level steady state,
- ↑ = Transition from low level to high level,
- ↓ = Transition from high level to low level,
- X = Any level including transitions,
- NC = No change in output level for a given set of input levels,
- IL = The output level is unknown for this set of illegal input levels,
- Z = High impedance level,
- UN = Un-driven node or input,
- Q(n) = The level of Q before an active transition on the affecting node, and
- QN(n) = The level of QN before an active transition on the affecting node.

EQUIVALENT GATES: The cell area normalized to the area of the NA21, 2-input NAND gate.

HDL SYNTAX: Verilog and VHDL instantiation syntax.

EQUIVALENT LOAD: An equivalent load is defined as the capacitive pin load of an NA21 cell "A" pin. It is equal to 30.9 fF. In the propagation delay tables 13 fF of interconnect capacitance is added to each equivalent load. For a more accurate estimation of interconnect capacitance see Table 12, "Interconnect Load Estimation," on page 2-15**.**

PIN LOADING: A table of cell input loads in units of equivalent loads (the input load normalized to the input load of an NA21, 2-input NAND gate).

POWER CHARACTERISTICS: Power for the cell can be described in three parts, as shown by the three terms in the Power Equation for Core Cells and Input Buffers below. First, the power dissipated due to Static I_{DD} across the channels and through the formed diodes. Second, the power due to the switching voltage across loads on the internal nodes of the cell. Third, the power due to the switching voltage across a load that a cell is driving.

The power characteristics table provides Static I_{DD} for a junction temperature of 85°C, and the dissipative load for all the switching nodes in the cell in terms of equivalent loads.The load that a cell drives is calculated by adding up input loads, and then adding the estimated load from the Load Estimation table on page 2-15. Below are equations for calculating the power dissipation:

Core Cells and Input Buffers

$$\text{POWER} = (\text{Static } I_{DD})\ V_{DD} + (30.9\text{fF})EQL_{pd}V_{DD}^2 f + (30.9\text{fF})EQL_I V_{DD}^2 f$$

Output Buffers

$$\text{POWER} = (\text{Static } I_{DD})\ V_{DD} + (30.9\text{fF})EQL_{pd}V_{DD}^2 f + C_{ol}V_{DD}^2 f$$

where:

- Static I_{DD} = Static leakage current of the cell
- V_{DD} = Operating voltage
- EQL_{pd} = Load of the switching nodes in the cell
- f = Frequency of operation
- C_{ol} = Load in farads on the output buffer
- EQL_I = Load of the driven interconnect and driven input pins

Description of Data Sheet Features (continued):

The frequency term of the power equation dominates, making the static current term insignificant, except to give the standby current.

Three types of buffers (input, output, and bidirectional) may be assembled using pad piece cells. Calculating power characteristics for pad pieces is dependent on the buffer type. The power dissipated by a buffer is the cumulative power dissipated by its component pad pieces.

- *ID pieces* use the input buffer equation. (The input and output buffer equations are described on the previous page).
- *Output pieces* use the output buffer equation. C_{OL} does not include any PADM pin loading of ID or PL pad piece cells that may be connected to the OD piece.
- *PL pieces* use the output buffer equation. C_{OL} does not include any PADM pin loading of ID or OD pad piece cells that may be connected to the PL piece.

PROPAGATION DELAYS : The Propagation Delays table in a data sheet contains timing data for the various input to output paths in the cell. The path for the delay is identified by two pins. Delay values are given for each path's propagation delay or timing parameters corresponding to each of the five equivalent loads. The equivalent loads are given over the range of allowed loading for the cell, up to the maximum load the cell can drive. The output buffer loading is in picofarads. To find the delay for a cell, add up the loads of all the inputs that the cell is driving, then add the estimated interconnect load from the Load Estimation table on page 2-15. Finally, look up the value for the desired timing parameter corresponding to the load on the cell. Interpolate to find values in between load columns.

The Delay Characteristics table in a data sheet may contain the following propagation delays and timing parameters:

t_{PLH} = Input to output propagation delay for a rising edge on the output

t_{PHL} = Input to output propagation delay for a falling edge on the output

t_{ZH} = High impedance to high level delay

t_{ZL} = High impedance to low level delay

t_{HZ} = High level to high impedance delay

t_{LZ} = Low level to high impedance delay

t_{su} = Input setup time with respect to clock

t_h = Input hold time

t_w = Input pulse width

AMI models the effects of input slew, and output resistive and capacitive loading for a particular cell's path delay. The delay in the data sheets represents a typical load on the inputs of the cell. Due to differing capabilities of logic simulators, the delay modeling method varies and may still be a linear model. Loads beyond the maximum load are an extrapolation of the model, and their accuracy is not guaranteed. More accurate delays can be determined using an AMI workstation kit. Contact your sales representative or the factory about modeling for specific workstation kits and simulators.

Interconnect estimation

For pre layout simulation, AMI provides an estimated interconnect value based on statistical data. Table 12 provides data points from those non-linear equations to enable the designer to estimate timing based on data book information.

Table 12: Interconnect Load Estimation

Die Size	Fan Out (Equivalent Loads)							
	1	3	6	9	12	20	35	50
100	0.3	1.2	2.3	3.4	4.5	7.2	11.9	16.4
125	0.4	1.3	2.6	3.8	5.0	8.0	13.2	18.1
150	0.4	1.4	2.8	4.2	5.4	8.6	14.3	19.6
175	0.4	1.6	3.1	4.5	5.8	9.3	15.3	21.0
200	0.5	1.7	3.3	4.8	6.2	9.8	16.3	22.3
225	0.5	1.8	3.4	5.0	6.5	10.4	17.1	23.5
250	0.6	1.9	3.6	5.3	6.9	10.9	18.0	24.7
300	0.6	2.0	3.9	5.7	7.5	11.8	19.5	26.8
350	0.7	2.2	4.2	6.2	8.0	12.7	20.9	28.7
400	0.7	2.3	4.5	6.5	8.5	13.4	22.2	30.4
450	0.8	2.5	4.8	6.9	9.0	14.2	23.3	32.0
500	0.8	2.6	5.0	7.2	9.4	14.9	24.5	33.6
550	0.9	2.7	5.2	7.6	9.8	15.5	25.5	35.0
600	0.9	2.8	5.4	7.9	10.2	16.1	26.5	36.4
650	1.0	3.0	5.6	8.2	10.6	16.7	27.5	37.7

The equivalent loads that are provided in the propagation delay tables within the data sheets include 13 fF of interconnect capacitance for each equivalent load. Table 12 was created from a non-linear statistical model and provides a more accurate representation of estimated interconnect for the various die sizes, base arrays and fanout. To compute equivalent loads driven by a given cell use the following formula:

$$\text{total\_eq\_loads} = \Sigma \text{ fanout loads (from pin loading tables)} + \text{estimated interconnect value (table 12)}$$

The equivalent loads in the propagation delay tables need to be scaled by multiplying each equivalent load by 1.42.

Packaging

A variety of popular packages is available for the AMI gate array and standard cell families.

For information on special packages or packaging requirements, contact an AMI sales representative.

Table 13: Package Offering

Package Type	Pin Count
Plastic Quad Flatpack, PQFP	44, 52, 64, 80, 100, 120, 128, 144, 160, 184, 208, 240, 256, 304
Thin Quad Flatpack, TQFP	32, 44, 48, 64, 80, 100, 120, 128, 144, 160, 176, 208
Metal Quad Flatpack, MQUAD®	128, 144, 208
Power Quad 2, PQ2	128, 144, 160, 208, 304
Ceramic Quad Flatpack, CQFP	40, 44, 52, 64, 84, 100, 132, 144, 172, 196, 256, 352
Plastic Leaded Chip Carrier, PLCC	20, 28, 32, 44, 52, 68, 84
Ceramic Leaded Chip Carrier, JLDCC	28, 44, 52, 68, 84
Ceramic Leadless Chip Carrier, CLCC	20, 24, 28, 32, 36, 40, 44, 48, 52, 68, 84
Ceramic Pin Grid Array, CPGA	65, 68, 69, 84, 85, 101, 109, 121, 132, 145, 155, 177, 181, 208, 225, 257, 299, 476
Ball Grid Array, BGA	(121), 169, 208, 225, 256, 313, 352, 388

( ) = Lead time required

ON-LINE APPLICATION NOTES

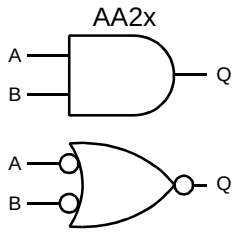
AMI provides a collection of application notes to aid the engineer in the design of gate array and standard cell Application Specific Integrated Circuits (ASICs). Each of the topics found on AMI's web site http://www.amis.com/app_notes provides supplemental information to those found in this book in addition to other very useful guidelines and helps. Some of the subjects currently available are Boundary Scan, internal scan, clocking schemes, crystal oscillators usage, guidelines for supplying test vector simulation, using megacells and memories, sequential device metastability, on-chip pull-up/pull-down resistors, using pad pieces, power estimation, Programmable Phase Locked Loop (PLL) , standard test philosophy, synchronous design, thermal resistance of packages, using nand tree circuits for Input parametric testing, and VHDL based design methodology. This site will be continually updated with useful information to assist the designer.

SECTION 3
CORE LOGIC

Description

AA2x is a family of 2-input gates which perform the logical AND function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

HDL Syntax

Verilog ..... AA2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: AA2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads			
	AA21	AA22	AA24	AA26
A	1.0	1.0	1.9	1.9
B	1.0	1.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AA21	1.2	TBD	2.7
AA22	1.5	TBD	3.9
AA24	2.8	TBD	7.6
AA26	3.5	TBD	10.5

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

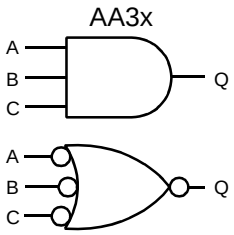
AA21	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.23 0.23	0.30 0.32	0.40 0.44	0.52 0.59	0.61 0.71
AA22	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.24 0.25	0.34 0.37	0.41 0.46	0.48 0.55	0.56 0.66
AA24	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.22 0.22	0.30 0.33	0.37 0.42	0.44 0.52	0.51 0.61
AA26	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.27 0.28	0.36 0.37	0.44 0.47	0.50 0.56	0.57 0.64

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AA3x is a family of 3-input gates which perform the logical AND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

HDL Syntax

Verilog ..... AA3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: AA3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads			
	AA31	AA32	AA34	AA36
A	1.0	1.0	2.0	2.9
B	1.0	1.0	1.9	2.9
C	1.0	1.0	1.9	2.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AA31	1.7	TBD	3.5
AA32	2.0	TBD	4.7
AA34	4.0	TBD	10.3
AA36	5.2	TBD	14.5

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

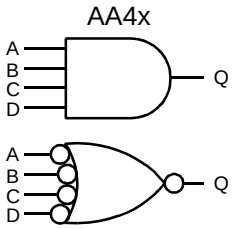
AA31	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.26 0.26	0.33 0.36	0.43 0.48	0.55 0.63	0.64 0.73
AA32	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.29 0.29	0.39 0.42	0.48 0.52	0.55 0.61	0.63 0.71
AA34	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.31 0.24	0.37 0.35	0.44 0.47	0.50 0.57	0.56 0.64
AA36	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.26 0.25	0.36 0.36	0.44 0.44	0.51 0.53	0.57 0.61

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AA4x is a family of 4-input gates which perform the logical AND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

HDL Syntax

Verilog ..... AA4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AA4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AA41	AA42	AA44	AA46
A	1.0	1.0	2.9	2.9
B	1.0	1.0	2.9	2.9
C	1.0	1.0	2.9	2.9
D	1.0	1.0	3.0	3.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQLpd (Eq-load)
AA41	2.0	TBD	3.9
AA42	2.2	TBD	5.1
AA44	5.2	TBD	13.5
AA46	5.7	TBD	16.4

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

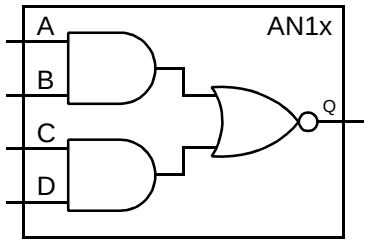
AA41	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.28 0.29	0.35 0.38	0.46 0.50	0.59 0.65	0.68 0.76
AA42	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.32 0.32	0.42 0.45	0.51 0.55	0.59 0.64	0.69 0.75
AA44	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.27 0.26	0.37 0.35	0.44 0.44	0.51 0.54	0.58 0.64
AA46	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.30 0.27	0.40 0.38	0.49 0.48	0.56 0.58	0.62 0.66

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN1x is a family of AND-NOR circuits consisting of two 2-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
H	H	X	X	L
X	X	H	H	L

HDL Syntax

Verilog ..... AN1x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AN1x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AN11	AN12	AN14	AN16
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	1.9
C	1.0	1.0	1.0	2.0
D	1.0	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN11	1.7	TBD	2.9
AN12	2.8	TBD	7.1
AN14	3.5	TBD	9.0
AN16	6.0	TBD	17.9

a. See page 2-13 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

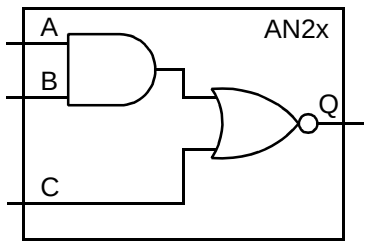
AN11	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.21 0.20	0.27 0.26	0.39 0.37	0.57 0.53	0.70 0.63
AN12	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.32 0.38	0.39 0.46	0.48 0.58	0.61 0.75	0.70 0.87
AN14	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.35 0.40	0.44 0.53	0.52 0.63	0.59 0.72	0.67 0.82
AN16	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.33 0.21	0.40 0.36	0.48 0.50	0.54 0.62	0.60 0.71

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN2x is a family of AND-NOR circuits consisting of one 2-input AND gate into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	Q
H	H	X	L
X	X	H	L
All other combinations			H

HDL Syntax

Verilog ..... AN2x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: AN2x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads			
	AN21	AN22	AN24	AN26
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	2.0
C	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN21	1.5	TBD	2.5
AN22	2.5	TBD	6.8
AN24	3.2	TBD	8.7
AN26	5.2	TBD	16.7

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

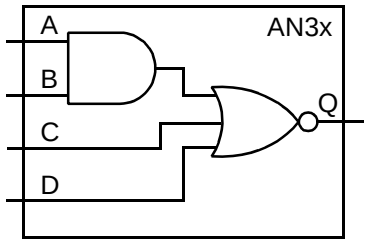
AN21	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.14 0.21	0.20 0.28	0.31 0.40	0.47 0.57	0.57 0.70
AN22	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.33 0.38	0.40 0.47	0.49 0.60	0.61 0.76	0.70 0.87
AN24	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.35 0.42	0.44 0.53	0.51 0.63	0.59 0.73	0.67 0.83
AN26	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.32 0.37	0.38 0.48	0.46 0.57	0.53 0.66	0.61 0.75

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN3x is a family of AND-NOR circuits consisting of one 2-input AND gate into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	L	H
X	L	L	L	H
H	H	X	X	L
X	X	H	X	L
X	X	X	H	L

HDL Syntax

Verilog ..... AN3x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AN3x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AN31	AN32	AN34	AN36
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	1.9
C	1.0	1.0	1.0	2.0
D	1.0	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN31	1.8	TBD	3.0
AN32	2.8	TBD	7.2
AN34	3.7	TBD	9.3
AN36	6.0	TBD	18.3

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

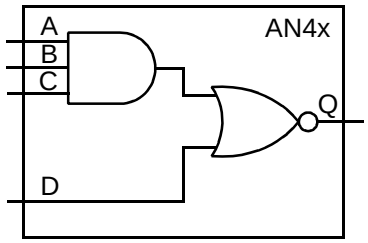
AN31	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.18 0.26	0.24 0.33	0.37 0.49	0.44 0.56	0.58 0.71
AN32	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.31 0.39	0.38 0.48	0.47 0.60	0.59 0.76	0.68 0.87
AN34	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.33 0.43	0.42 0.56	0.50 0.66	0.57 0.76	0.64 0.86
AN36	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.29 0.32	0.38 0.45	0.46 0.57	0.52 0.67	0.58 0.75

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN4x is a family of AND-NOR circuits consisting of one 3-input AND gate into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
H	H	H	X	L
X	X	X	H	L
All other combinations				H

HDL Syntax

Verilog ..... AN4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: AN4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	AN41	AN42	AN44	AN46
A	1.0	1.0	1.0	1.9
B	1.0	1.0	1.0	2.0
C	1.0	1.0	1.0	2.0
D	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN41	1.7	TBD	3.1
AN42	2.8	TBD	7.4
AN44	3.7	TBD	9.5
AN46	5.7	TBD	18.1

a. See page 2-13 for power equation.

Core Logic

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

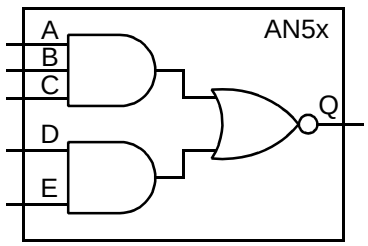
AN41	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.17 0.26	0.23 0.33	0.35 0.48	0.41 0.55	0.51 0.69
AN42	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.43	0.43 0.52	0.52 0.65	0.64 0.80	0.73 0.91
AN44	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.46	0.48 0.57	0.56 0.67	0.63 0.76	0.71 0.86
AN46	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.43	0.43 0.52	0.50 0.62	0.58 0.71	0.64 0.80

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN5x is a family of AND-NOR circuits consisting of one 3-input AND gate and one 2-input AND gate into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	H	X	X	L
X	X	X	H	H	L
All other combinations					H

HDL Syntax

Verilog ..... AN5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: AN5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	AN52	AN54	AN56
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.0	1.9
E	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN52	3.0	TBD	7.6
AN54	3.7	TBD	9.3
AN56	7.0	TBD	19.7

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

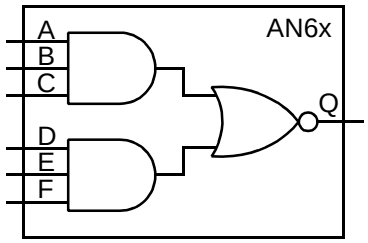
AN52	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.35 0.44	0.41 0.52	0.51 0.64	0.64 0.79	0.74 0.90
AN54	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.45	0.47 0.57	0.55 0.67	0.63 0.77	0.72 0.87
AN56	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.43	0.42 0.51	0.50 0.60	0.57 0.69	0.66 0.80

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN6x is a family of AND-NOR circuits consisting of two 3-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

HDL Syntax

Verilog ..... AN6x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: AN6x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	AN62	AN64	AN66
A	1.0	1.0	1.9
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN62	3.2	TBD	8.3
AN64	4.2	TBD	9.9
AN66	7.5	TBD	21.4

a. See page 2-13 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

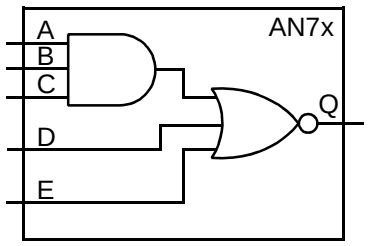
AN62	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.44	0.43 0.53	0.52 0.65	0.63 0.80	0.71 0.91
AN64	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.45	0.48 0.57	0.55 0.67	0.62 0.76	0.70 0.87
AN66	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.35 0.42	0.44 0.53	0.51 0.63	0.58 0.71	0.64 0.79

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN7x is a family of AND-NOR circuits consisting of one 3-input AND gate into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
All other combinations					H

HDL Syntax

Verilog ..... AN7x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: AN7x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	AN72	AN74	AN76
A	1.0	1.0	1.9
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN72	3.0	TBD	7.8
AN74	3.7	TBD	9.6
AN76	6.8	TBD	20.2

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

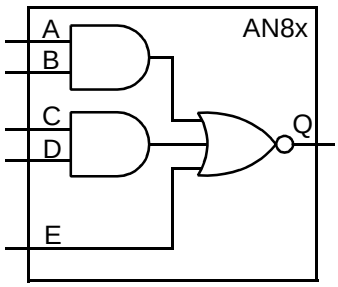
AN72	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.42	0.43 0.51	0.52 0.63	0.64 0.79	0.73 0.90
AN74	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.45	0.48 0.57	0.55 0.67	0.62 0.76	0.70 0.86
AN76	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.35 0.42	0.43 0.54	0.51 0.63	0.57 0.71	0.64 0.79

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN8x is a family of AND-NOR circuits consisting of two 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	X	X	X	L
X	X	H	H	X	L
X	X	X	X	H	L
All other combinations					H

HDL Syntax

Verilog ..... AN8x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: AN8x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	AN82	AN84	AN86
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN82	3.7	TBD	9.6
AN84	4.2	TBD	11.2
AN86	7.5	TBD	22.6

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

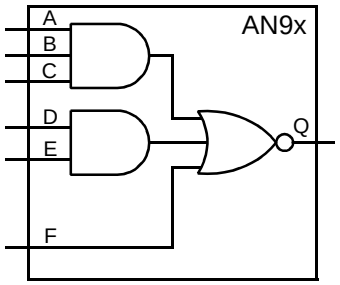
AN82	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.43	0.43 0.51	0.53 0.63	0.65 0.79	0.75 0.90
AN84	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.44	0.49 0.57	0.57 0.67	0.64 0.76	0.72 0.87
AN86	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.38 0.40	0.47 0.51	0.55 0.61	0.62 0.70	0.68 0.79

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AN9x is a family of AND-NOR circuits consisting of one 3-input AND gate and one 2-input AND gate into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	H	X	X	X	L
X	X	X	H	H	X	L
X	X	X	X	X	H	L
All other combinations						H

HDL Syntax

Verilog ..... AN9x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: AN9x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	AN92	AN94	AN96
A	1.0	1.0	1.9
B	1.0	1.0	2.0
C	1.0	1.0	1.9
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN92	4.0	TBD	10.2
AN94	4.5	TBD	11.6
AN96	8.5	TBD	24.2

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

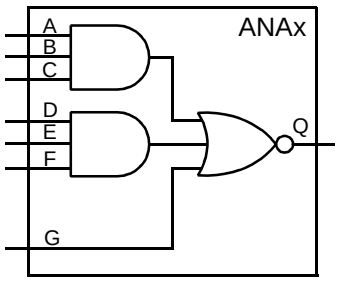
AN92	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.40 0.47	0.47 0.56	0.56 0.68	0.69 0.84	0.78 0.96
AN94	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.43 0.49	0.53 0.62	0.61 0.72	0.68 0.81	0.76 0.92
AN96	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.38 0.44	0.49 0.58	0.58 0.68	0.65 0.76	0.71 0.83

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANAx is a family of AND-NOR circuits consisting of two 3-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
H	H	H	X	X	X	X	L
X	X	X	H	H	H	X	L
X	X	X	X	X	X	H	L
All other combinations							H

HDL Syntax

Verilog ..... ANAx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ANAx port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads		
	ANA2	ANA4	ANA6
A	1.0	1.0	2.0
B	1.0	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0
G	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANA2	4.2	TBD	10.8
ANA4	4.7	TBD	11.9
ANA6	9.2	TBD	25.8

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

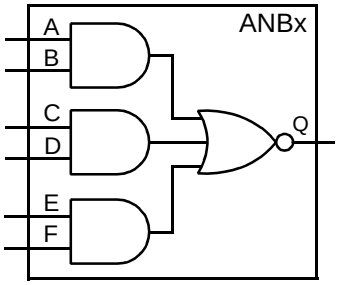
ANA2	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.40 0.46	0.47 0.55	0.57 0.68	0.69 0.84	0.78 0.96
ANA4	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.42 0.48	0.52 0.61	0.60 0.71	0.67 0.80	0.75 0.89
ANA6	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.40 0.45	0.51 0.56	0.60 0.67	0.66 0.76	0.71 0.84

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANBx is a family of AND-NOR circuits consisting of three 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	X	X	X	X	L
X	X	H	H	X	X	L
X	X	X	X	H	H	L
All other combinations						H

HDL Syntax

Verilog ..... ANBx *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ANBx port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	ANB2	ANB4	ANB6
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	1.9
F	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANB2	3.7	TBD	9.9
ANB4	4.7	TBD	11.7
ANB6	8.5	TBD	24.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

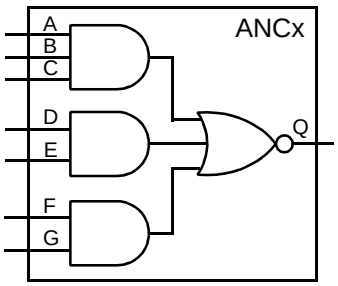
ANB2	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.41	0.43 0.50	0.52 0.63	0.65 0.79	0.74 0.91
ANB4	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.40 0.44	0.49 0.56	0.57 0.66	0.64 0.75	0.72 0.86
ANB6	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.41	0.47 0.53	0.55 0.63	0.62 0.71	0.68 0.78

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANCx is a family of AND-NOR circuits consisting of one 3-input AND gate and two 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
H	H	H	X	X	X	X	L
X	X	X	H	H	X	X	L
X	X	X	X	X	H	H	L
All other combinations							H

HDL Syntax

Verilog ..... ANCx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ANCx port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads		
	ANC2	ANC4	ANC6
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0
G	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANC2	4.0	TBD	10.5
ANC4	5.0	TBD	12.2
ANC6	9.2	TBD	25.6

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

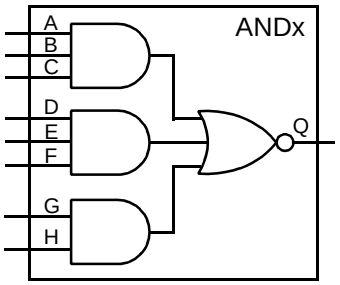
ANC2	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.40 0.46	0.46 0.55	0.56 0.68	0.68 0.84	0.77 0.95
ANC4	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.42 0.48	0.51 0.60	0.59 0.70	0.67 0.79	0.76 0.89
ANC6	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.46	0.50 0.56	0.57 0.66	0.64 0.75	0.70 0.84

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ANDx is a family of AND-NOR circuits consisting of two 3-input AND gates and one 2-input AND gate into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
H	H	H	X	X	X	X	X	L
X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	H	H	L
All other combinations								H

HDL Syntax

Verilog ..... ANDx *inst_name* (Q, A, B, C, D, E, F, G, H);

VHDL..... *inst_name*: ANDx port map (Q, A, B, C, D, E, F, G, H);

Pin Loading

Pin Name	Equivalent Loads		
	AND2	AND4	AND6
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.0	1.9
E	1.0	1.0	2.0
F	1.0	1.0	1.9
G	1.0	1.0	2.0
H	1.0	1.0	2.0

AMI5HS 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AND2	4.5	TBD	11.2
AND4	5.0	TBD	12.7
AND6	10.2	TBD	27.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

AND2	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.40 0.46	0.47 0.56	0.57 0.69	0.69 0.84	0.77 0.95
AND4	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.45 0.49	0.56 0.61	0.64 0.71	0.71 0.80	0.80 0.90
AND6	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.48	0.48 0.57	0.57 0.66	0.65 0.76	0.72 0.86

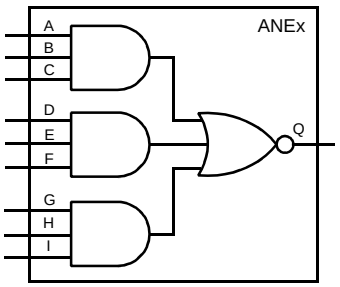
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI5HS 0.5 micron CMOS Standard Cell

Description

ANEx is a family of AND-NOR circuits consisting of three 3-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Q
H	H	H	X	X	X	X	X	X	L
X	X	X	H	H	H	X	X	X	L
X	X	X	X	X	X	H	H	H	L
All other combinations									H

HDL Syntax

Verilog ..... ANEx *inst_name* (Q, A, B, C, D, E, F, G, H, I);

VHDL..... *inst_name*: ANEx port map (Q, A, B, C, D, E, F, G, H, I);

Pin Loading

Pin Name	Equivalent Loads		
	ANE2	ANE4	ANE6
A	1.0	1.0	1.9
B	1.0	1.0	1.9
C	1.0	1.0	1.9
D	1.0	1.0	1.9
E	1.0	1.0	2.0
F	1.0	1.0	1.9
G	1.0	1.0	2.0
H	1.0	1.0	2.0
I	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANE2	4.7	TBD	11.9
ANE4	5.5	TBD	13.8
ANE6	11.0	TBD	29.2

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

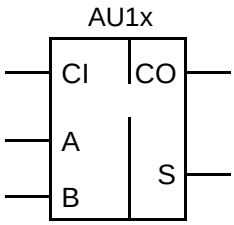
ANE2	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.47	0.46 0.56	0.56 0.68	0.68 0.83	0.78 0.94
ANE4	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.43 0.49	0.53 0.63	0.61 0.73	0.68 0.82	0.76 0.92
ANE6	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.34 0.45	0.46 0.57	0.58 0.67	0.65 0.76	0.70 0.85

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

AU1x is a family of combinational one-bit full adders.

Logic Symbol



Truth Table

CI	A	B	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

HDL Syntax

Verilog ..... AU1x *inst_name* (CO, S, A, B, CI);

VHDL..... *inst_name*: AU1x port map (CO, S, A, B, CI);

Pin Loading

Pin Name	Equivalent Loads	
	AU11	AU12
A	4.7	9.8
B	4.6	9.9
CI	3.6	7.5

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AU11	4.7	TBD	12.7
AU12	12.7	TBD	27.3

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

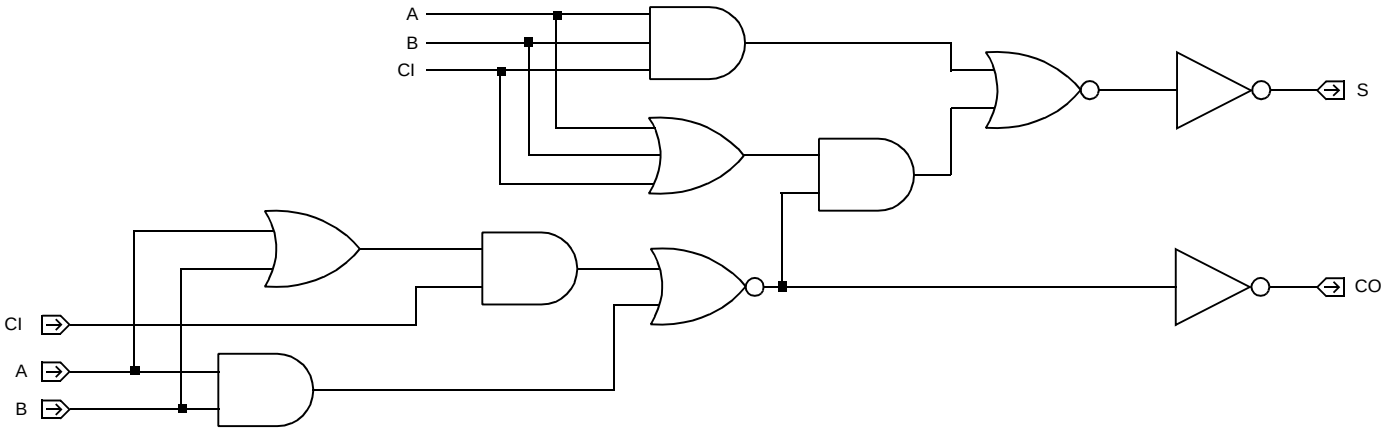
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
AU11	From: A To: S	t_{PLH} t_{PHL}	0.44 0.78	0.52 0.87	0.61 1.00	0.72 1.16	0.80 1.27
	From: B To: S	t_{PLH} t_{PHL}	0.39 0.87	0.46 0.97	0.55 1.11	0.67 1.26	0.75 1.37
	From: CI To: S	t_{PLH} t_{PHL}	0.36 0.87	0.44 0.98	0.54 1.11	0.66 1.26	0.74 1.36
	From: A To: CO	t_{PLH} t_{PHL}	0.38 0.49	0.46 0.60	0.57 0.75	0.70 0.92	0.79 1.04
	From: B To: CO	t_{PLH} t_{PHL}	0.39 0.51	0.48 0.62	0.58 0.76	0.71 0.93	0.80 1.04
	From: CI To: CO	t_{PLH} t_{PHL}	0.39 0.40	0.47 0.50	0.57 0.65	0.70 0.81	0.79 0.93
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
AU12	From: A To: S	t_{PLH} t_{PHL}	0.45 0.68	0.56 0.82	0.64 0.93	0.71 1.04	0.78 1.15
	From: B To: S	t_{PLH} t_{PHL}	0.39 0.74	0.49 0.89	0.57 1.01	0.64 1.11	0.73 1.22
	From: CI To: S	t_{PLH} t_{PHL}	0.35 0.75	0.45 0.89	0.54 1.00	0.62 1.10	0.70 1.21
	From: A To: CO	t_{PLH} t_{PHL}	0.28 0.42	0.37 0.58	0.46 0.70	0.54 0.81	0.64 0.93
	From: B To: CO	t_{PLH} t_{PHL}	0.29 0.42	0.38 0.57	0.47 0.70	0.54 0.81	0.63 0.93
	From: CI To: CO	t_{PLH} t_{PHL}	0.29 0.32	0.39 0.47	0.47 0.59	0.54 0.69	0.62 0.81

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



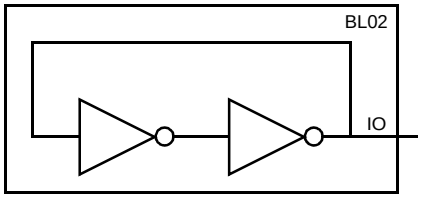
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

BL02 is a tristate bus latch that stores the final binary level on the bus when left undriven.

Logic Symbol



Truth Table

N/A

Pin Loading

	Equivalent Load
IO	3.4

Equivalent Gates 2.2

HDL Syntax

Verilog ..... BL02 *inst_name* (IO);

VHDL..... *inst_name*: BL02 port map (IO);

Size And Power Characteristics

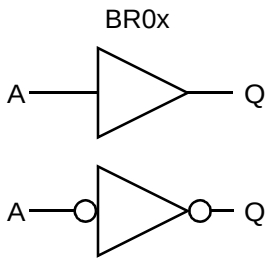
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	4.7	Eq-load

See page 2-13 for power equation.

Description

BR0x is a family of non-inverting bus receivers with a single output to be used as the output of tristate busses.

Logic Symbol



Truth Table

A	Q
L	L
H	H

HDL Syntax

Verilog ..... BR0x *inst_name* (Q, A);

VHDL..... *inst_name*: BR0x port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads		
	BR02	BR04	BR06
A	1.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
BR02	1.2	TBD	3.7
BR04	2.2	TBD	6.6
BR06	2.5	TBD	9.7

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

BR02	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.21 0.20	0.31 0.32	0.37 0.41	0.44 0.50	0.51 0.60
BR04	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.21 0.19	0.26 0.29	0.30 0.38	0.36 0.46	0.45 0.54
BR06	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.18 0.25	0.28 0.35	0.37 0.43	0.43 0.51	0.48 0.58

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

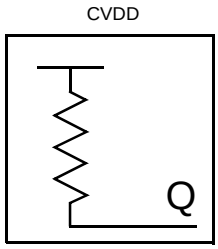
CVDD is the resistive tie-up to the core V_{DD} bus for all cell inputs.

Equivalent Gates 0.9

HDL Syntax

Verilog ..... CVDD *inst_name* (Q);

VHDL..... *inst_name*: CVDD port map (Q);



CVSS

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

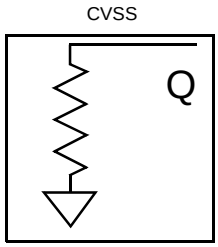
CVSS is the resistive tie-down to the core V_{SS} bus for all cell inputs.

Equivalent Gates 0.9

HDL Syntax

Verilog ..... CVSS *inst_name* (Q);

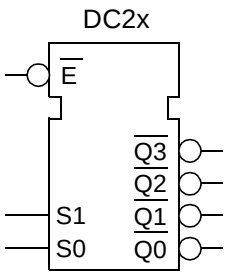
VHDL..... *inst_name*: CVSS port map (Q);



Description

DC2x is a family of two-to-four line decoder/demultiplexers with active low enable.

Logic Symbol



Truth Table

EN	S1	S0	Q0N	Q1N	Q2N	Q3N
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

HDL Syntax

Verilog ..... DC2x *inst_name* (Q0N, Q1N, Q2N, Q3N, EN, S0, S1);

VHDL..... *inst_name*: DC2x port map (Q0N, Q1N, Q2N, Q3N, EN, S0, S1);

Pin Loading

Pin Name	Equivalent Loads	
	DC21	DC22
S0	3.1	3.6
S1	3.1	3.6
EN	1.0	4.6

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DC21	5.7	TBD	17.6
DC22	7.5	TBD	22.9

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

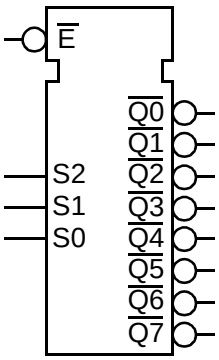
	Number of Equivalent Loads		1	2	4	5	7 (max)
DC21	From: Sx To: QN	t_{PLH} t_{PHL}	0.26 0.29	0.31 0.35	0.40 0.47	0.44 0.54	0.51 0.66
	From: EN To: QN	t_{PLH} t_{PHL}	0.40 0.39	0.44 0.46	0.52 0.58	0.56 0.64	0.64 0.75
	Number of Equivalent Loads		**1**	**3**	**6**	**10**	**13 (max)**
DC22	From: Sx To: QN	t_{PLH} t_{PHL}	0.23 0.34	0.30 0.44	0.39 0.58	0.51 0.75	0.59 0.86
	From: EN To: QN	t_{PLH} t_{PHL}	0.26 0.42	0.33 0.52	0.43 0.66	0.55 0.82	0.64 0.93

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

DC3x is a family of three-to-eight line decoder/demultiplexers with active low enable.

Logic Symbol



Truth Table

EN	S2	S1	S0	Q0N	Q1N	Q2N	Q3N	Q4N	Q5N	Q6N	Q7N
H	X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	L

Core Logic

HDL Syntax

Verilog ..... DC3x *inst_name* (Q0N, Q1N, Q2N, Q3N, Q4N, Q5N, Q6N, Q7N, EN, S0, S1, S2);

VHDL..... *inst_name* DC3x port map (Q0N, Q1N, Q2N, Q3N, Q4N, Q5N, Q6N, Q7N, EN, S0, S1, S2);

Pin Loading

Pin Name	Equivalent Loads	
	DC31	DC32
S0	5.4	5.7
S1	5.6	5.7
S2	5.4	5.3
EN	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DC31	12.0	TBD	41.4
DC32	16.2	TBD	59.7

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

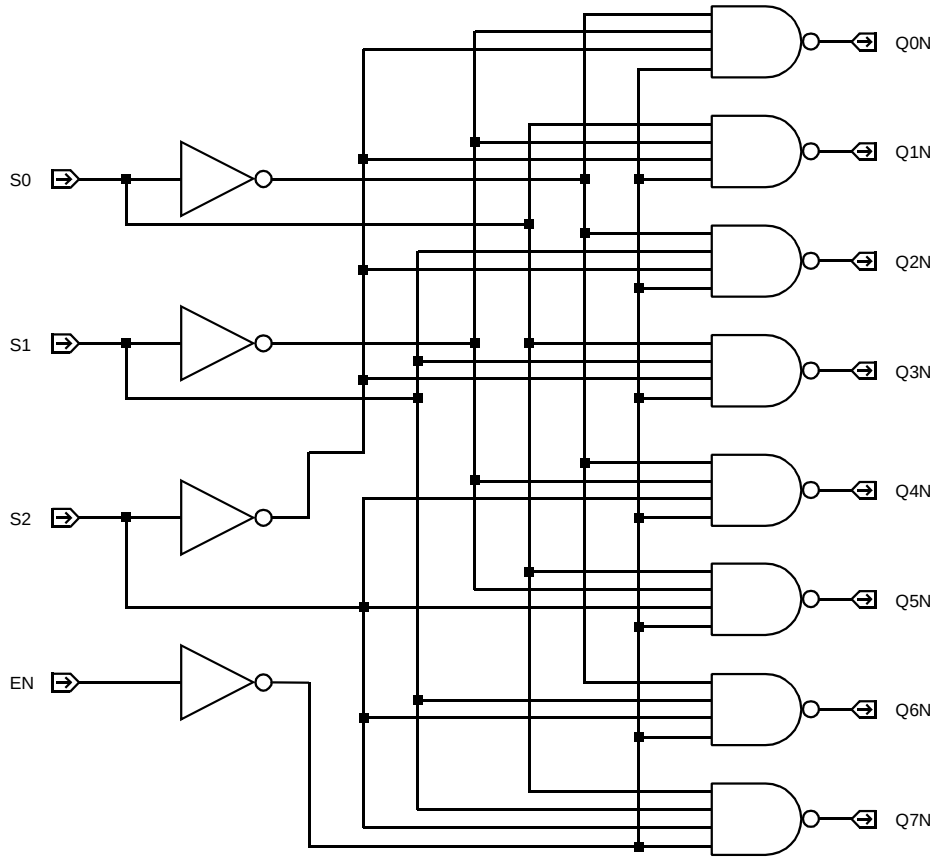
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	2	3	4	6 (max)
DC31	From: Sx To: QN	t_{PLH} t_{PHL}	0.34 0.38	0.39 0.45	0.44 0.53	0.49 0.60	0.59 0.75
	From: EN To: QN	t_{PLH} t_{PHL}	0.61 0.56	0.66 0.63	0.70 0.70	0.75 0.78	0.84 0.93
	Number of Equivalent Loads		**1**	**3**	**6**	**10**	**13 (max)**
DC32	From: Sx To: QN	t_{PLH} t_{PHL}	0.24 0.37	0.31 0.48	0.40 0.63	0.52 0.81	0.60 0.94
	From: EN To: QN	t_{PLH} t_{PHL}	0.83 0.92	0.89 1.03	0.98 1.17	1.10 1.35	1.19 1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

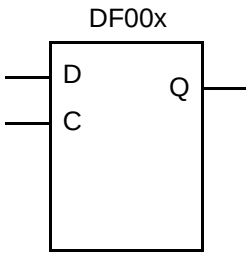
Logic Schematic



Description

DF00x is a family of static, master-slave D flip-flops without SET or RESET. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

D	C	Q
H	↑	H
L	↑	L
X	L	NC

NC = No Change

HDL Syntax

Verilog ..... DF00x *inst_name* (Q, C, D);

VHDL..... *inst_name*: DF00x port map (Q, C, D);

Pin Loading

Pin Name	Equivalent Loads	
	DF001	DF002
D	1.0	1.0
C	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF001	4.0	TBD	11.7
DF002	4.2	TBD	12.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

DF001	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: C	t_{PLH}	0.55	0.60	0.69	0.81	0.91
	To: Q	t_{PHL}	0.46	0.55	0.68	0.83	0.94
DF002	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: C	t_{PLH}	0.53	0.63	0.70	0.77	0.85
	To: Q	t_{PHL}	0.47	0.59	0.69	0.79	0.90

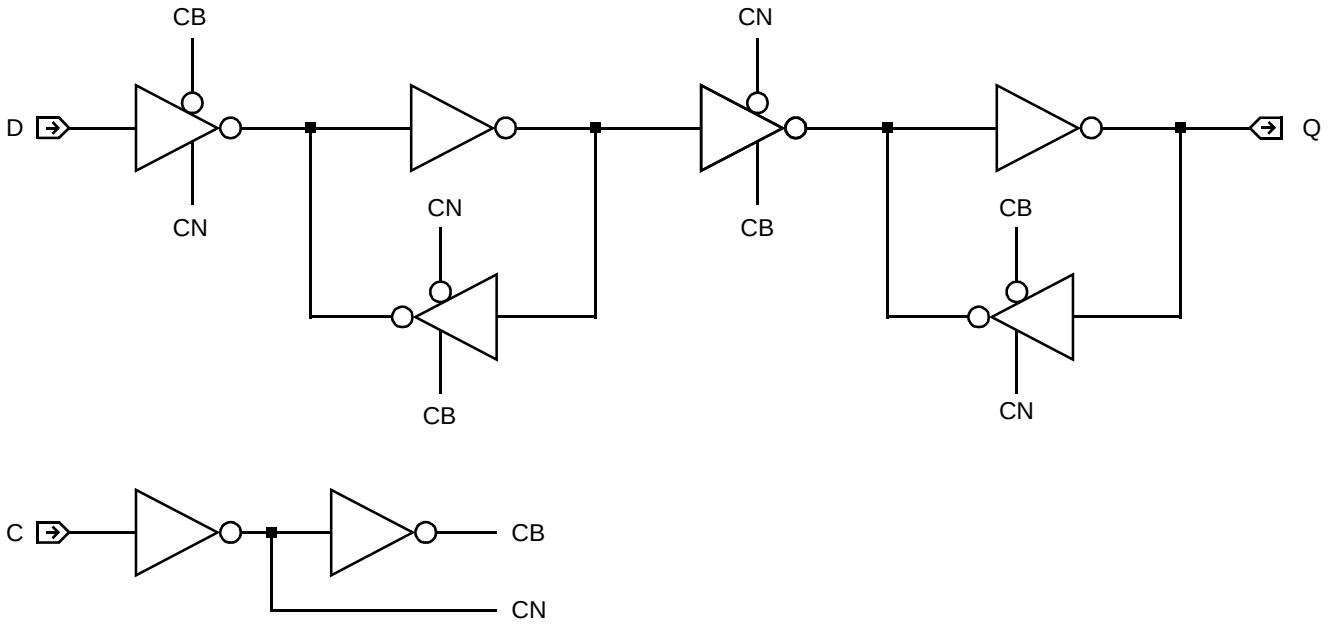
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DF001	Cell DF002
Min C Width	High	t_w	0.54	0.53
Min C Width	Low	t_w	0.57	0.54
Min D Setup		t_{su}	0.35	0.34
Min D Hold		t_h	0.17	0.16

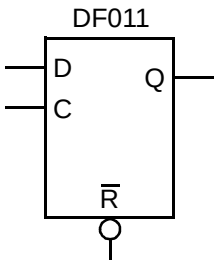
Logic Schematic



Description

DF011 is a static, master-slave D flip-flop. RESET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q
L	X	X	L
H	L	↑	L
H	H	↑	H
H	X	L	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	1.0
RN	1.1

Equivalent Gates 5.0

HDL Syntax

Verilog ..... DF011 *inst_name* (Q, C, D, RN);

VHDL..... *inst_name*: DF011 port map (Q, C, D, RN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	15.6	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.61 0.47	0.66 0.52	0.77 0.60	0.93 0.72	1.04 0.80
RN	Q	t_{PHL}	0.31	0.36	0.43	0.55	0.62

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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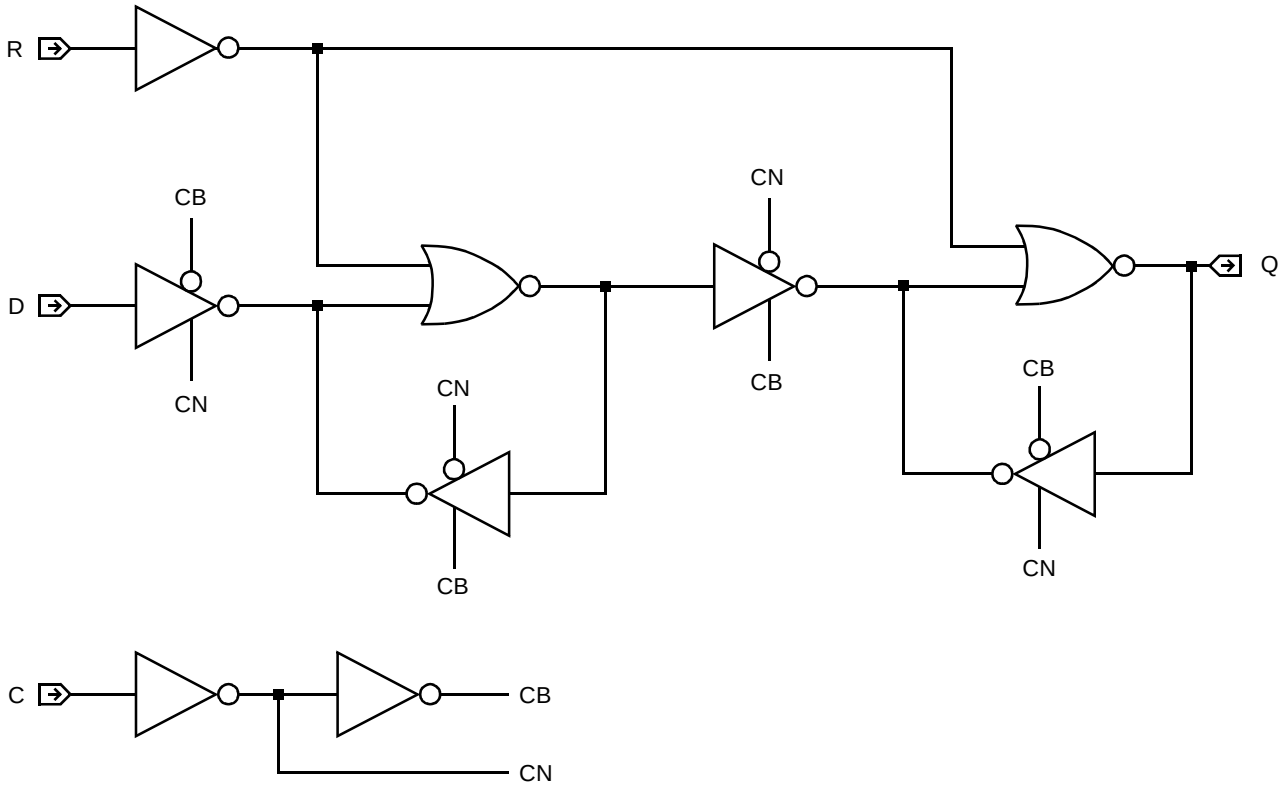
Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.61
Min C Width	Low	t_w	0.59
Min RN Width	Low	t_w	0.57
Min D Setup		t_{su}	0.36
Min D Hold		t_h	0.16
Min RN Setup		t_{su}	0.32
Min RN Hold		t_h	0.33

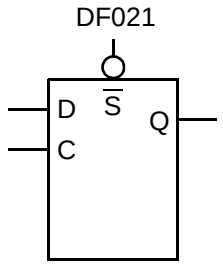
Logic Schematic



Description

DF021 is a static, master-slave D flip-flop. SET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q
L	X	X	H
H	L	↑	L
H	H	↑	H
H	X	L	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	1.0
SN	2.1

Equivalent Gates 4.5

HDL Syntax

Verilog.....DF021 *inst_name* (Q, C, D, SN);

VHDL..... *inst_name*: DF021 port map (Q, C, D, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	12.5	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.57 0.49	0.61 0.56	0.69 0.66	0.78 0.81	0.85 0.90
SN	Q	t_{PLH}	0.13	0.17	0.26	0.36	0.42

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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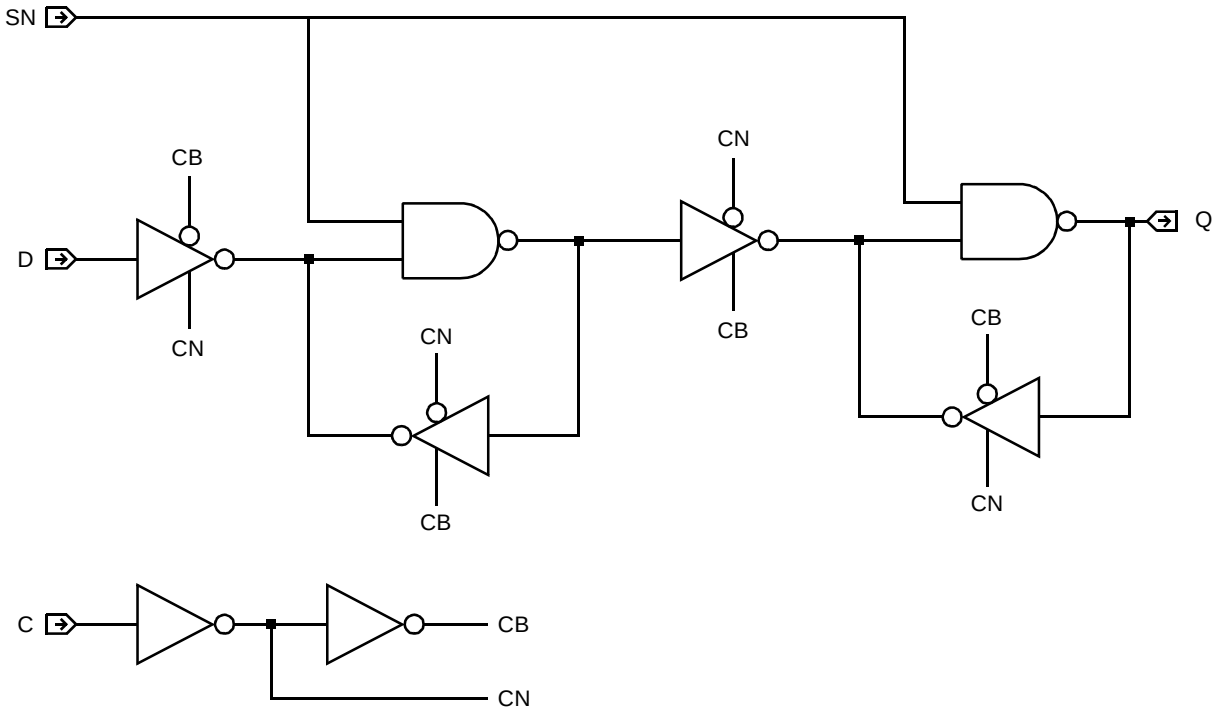
AMI5HS 0.5 micron CMOS Standard Cell

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.57
Min C Width	Low	t_w	0.58
Min SN Width	Low	t_w	0.71
Min D Setup		t_{su}	0.37
Min D Hold		t_h	0.16
Min SN Setup		t_{su}	0.17
Min SN Hold		t_h	0.58

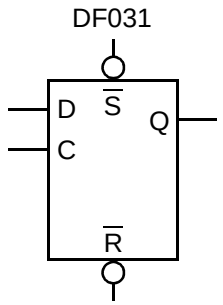
Logic Schematic



Description

DF031 is a static, master-slave D flip-flop. SET and RESET are asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q
L	L	X	X	IL
L	H	X	X	H
H	L	X	X	L
H	H	L	↑	L
H	H	H	↑	H
H	H	X	L	NC

NC = No Change
IL = Illegal

Pin Loading

	Equivalent Load
D	1.0
C	1.0
SN	2.1
RN	1.0

Core Logic

Equivalent Gates 6.0

HDL Syntax

Verilog ..... DF031 *inst_name* (Q, D, RN, SN);

VHDL..... *inst_name*: DF031 port map (Q, D, RN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	16.7	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.64 0.52	0.70 0.57	0.83 0.69	1.03 0.88	1.17 1.01
RN	Q	t_{PHL}	0.36	0.43	0.54	0.70	0.81
SN	Q	t_{PLH}	0.13	0.16	0.24	0.34	0.38

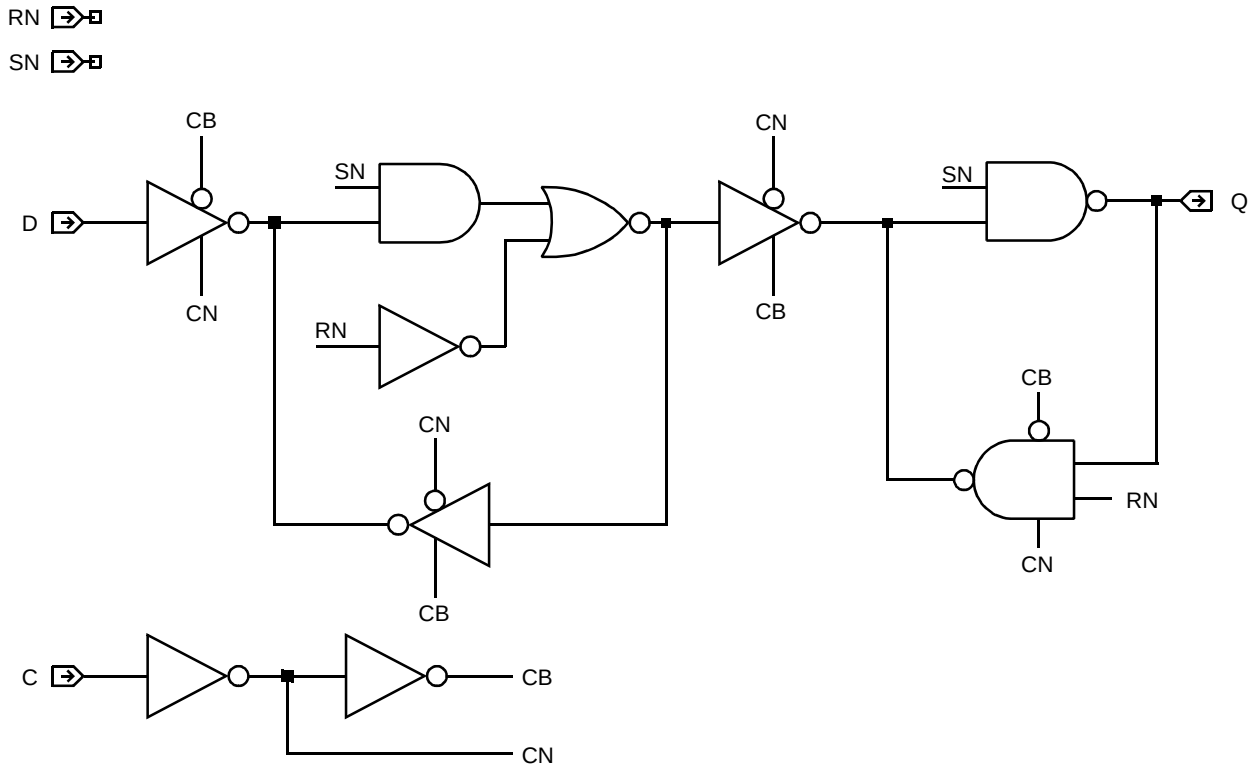
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.64
Min C Width	Low	t_w	0.61
Min RN Width	Low	t_w	0.60
Min SN Width	Low	t_w	0.67
Min D Setup		t_{su}	0.40
Min D Hold		t_h	0.16
Min RN Setup		t_{su}	0.36
Min RN Hold		t_h	0.33
Min SN Setup		t_{su}	0.21
Min SN Hold		t_h	0.54

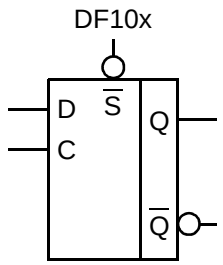
Logic Schematic



Description

DF10x is a family of static, master-slave D flip-flops. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

HDL Syntax

Verilog.....DF10x *inst_name* (Q, QN, C, D, SN);

VHDL..... *inst_name*: DF10x port map (Q, QN, C, D, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF101	DF102	DF104	DF106
D	1.0	1.0	1.0	1.0
C	1.0	1.0	1.0	1.0
SN	2.1	2.1	3.1	3.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static IDD (TJ = 85°C) (nA)	EQLpd (Eq-load)
DF101	5.5	TBD	15.8
DF102	5.7	TBD	17.9
DF104	8.0	TBD	29.2
DF106	9.2	TBD	35.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DF101	From: C To: Q	t_{PLH} t_{PHL}	0.59 0.53	0.66 0.63	0.76 0.77	0.88 0.93	0.97 1.05
	From: C To: QN	t_{PLH} t_{PHL}	0.68 0.79	0.73 0.89	0.81 1.00	0.94 1.13	1.04 1.22
	From: SN To: Q	t_{PLH}	0.73	0.81	0.91	1.03	1.12
	From: SN To: QN	t_{PHL}	0.28	0.38	0.50	0.65	0.76
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DF102	From: C To: Q	t_{PLH} t_{PHL}	0.60 0.53	0.70 0.68	0.77 0.80	0.84 0.90	0.92 1.02
	From: C To: QN	t_{PLH} t_{PHL}	0.78 0.89	0.86 0.98	0.92 1.06	0.98 1.13	1.04 1.22
	From: SN To: Q	t_{PLH}	0.85	0.95	1.02	1.09	1.15
	From: SN To: QN	t_{PHL}	0.30	0.42	0.52	0.62	0.73
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
DF104	From: C To: Q	t_{PLH} t_{PHL}	0.66 0.53	0.77 0.69	0.84 0.81	0.90 0.91	0.97 1.00
	From: C To: QN	t_{PLH} t_{PHL}	0.79 0.90	0.84 1.02	0.90 1.11	0.96 1.18	1.02 1.25
	From: SN To: Q	t_{PLH}	0.81	0.90	0.98	1.05	1.11
	From: SN To: QN	t_{PHL}	0.26	0.39	0.49	0.57	0.65
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
DF106	From: C To: Q	t_{PLH} t_{PHL}	0.70 0.60	0.81 0.77	0.88 0.88	0.94 0.98	0.99 1.06
	From: C To: QN	t_{PLH} t_{PHL}	0.93 1.03	0.98 1.12	1.03 1.21	1.09 1.29	1.16 1.36
	From: SN To: Q	t_{PLH}	0.98	1.06	1.13	1.19	1.24
	From: SN To: QN	t_{PHL}	0.31	0.43	0.53	0.62	0.69

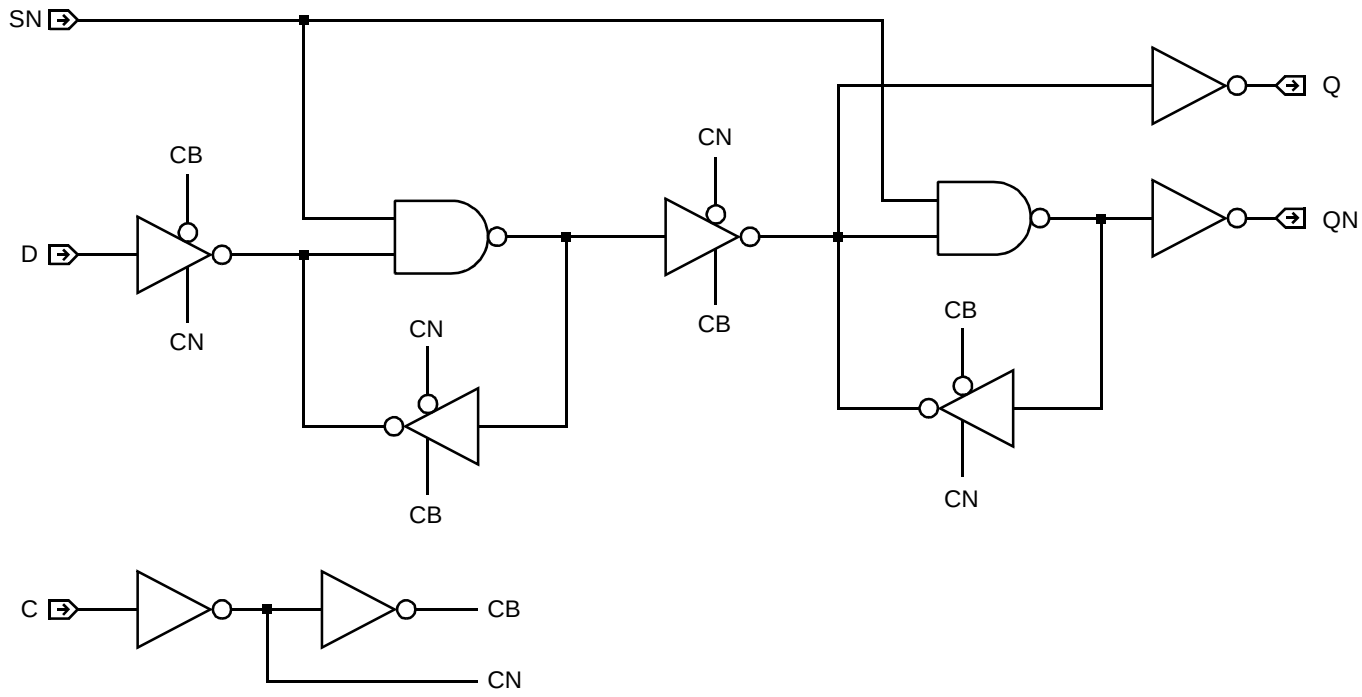
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF101	DF102	DF104	DF106
Min C Width	High	t_w	0.63	0.71	0.77	0.87
Min C Width	Low	t_w	0.58	0.58	0.67	0.67
Min SN Width		t_w	0.59	0.73	0.69	0.84
Min D Setup		t_{su}	0.37	0.36	0.40	0.41
Min D Hold		t_h	0.16	0.16	0.20	0.20
Min SN Setup		t_{su}	0.17	0.17	0.21	0.21
Min SN Hold		t_h	0.56	0.56	0.60	0.60

Logic Schematic



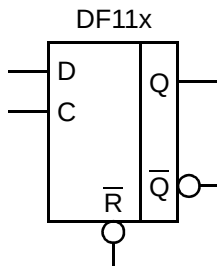
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

DF11x is a family of static, master-slave D flip-flops. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

HDL Syntax

Verilog.....DF11x *inst_name* (Q, QN, C, D, RN);

VHDL.....inst_DF11x : DF11x port map (Q, QN, C, D, RN);

Pin Loading

Pin Name	Equivalent Loads			
	DF111	DF112	DF114	DF116
D	1.0	1.0	1.0	1.0
C	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF111	6.0	TBD	18.4
DF112	6.2	TBD	21.3
DF114	8.5	TBD	33.3
DF116	9.8	TBD	39.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DF111	From: C To: Q	t_{PLH} t_{PHL}	0.57 0.51	0.64 0.62	0.73 0.75	0.86 0.92	0.95 1.04
	From: C To: QN	t_{PLH} t_{PHL}	0.64 0.82	0.68 0.92	0.76 1.04	0.88 1.19	0.98 1.30
	From: RN To: Q	t_{PHL}	0.93	1.05	1.19	1.36	1.49
	From: RN To: QN	t_{PLH}	0.38	0.45	0.55	0.66	0.75
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DF112	From: C To: Q	t_{PLH} t_{PHL}	0.61 0.54	0.71 0.68	0.79 0.80	0.87 0.90	0.95 1.02
	From: C To: QN	t_{PLH} t_{PHL}	0.72 1.00	0.79 1.12	0.86 1.21	0.93 1.29	1.02 1.38
	From: RN To: Q	t_{PHL}	1.07	1.21	1.33	1.43	1.55
	From: RN To: QN	t_{PLH}	0.39	0.47	0.54	0.61	0.69
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
DF114	From: C To: Q	t_{PLH} t_{PHL}	0.65 0.53	0.74 0.68	0.81 0.80	0.87 0.91	0.93 1.01
	From: C To: QN	t_{PLH} t_{PHL}	0.75 0.95	0.79 1.09	0.85 1.18	0.92 1.27	1.00 1.35
	From: RN To: Q	t_{PHL}	1.13	1.28	1.38	1.47	1.55
	From: RN To: QN	t_{PLH}	0.43	0.49	0.56	0.64	0.72
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
DF116	From: C To: Q	t_{PLH} t_{PHL}	0.69 0.60	0.80 0.77	0.88 0.89	0.94 0.99	0.99 1.06
	From: C To: QN	t_{PLH} t_{PHL}	0.86 1.09	0.90 1.23	0.97 1.33	1.03 1.41	1.10 1.48
	From: RN To: Q	t_{PHL}	1.29	1.45	1.56	1.64	1.72
	From: RN To: QN	t_{PLH}	0.47	0.53	0.60	0.67	0.74

AMI5HS 0.5 micron CMOS Standard Cell

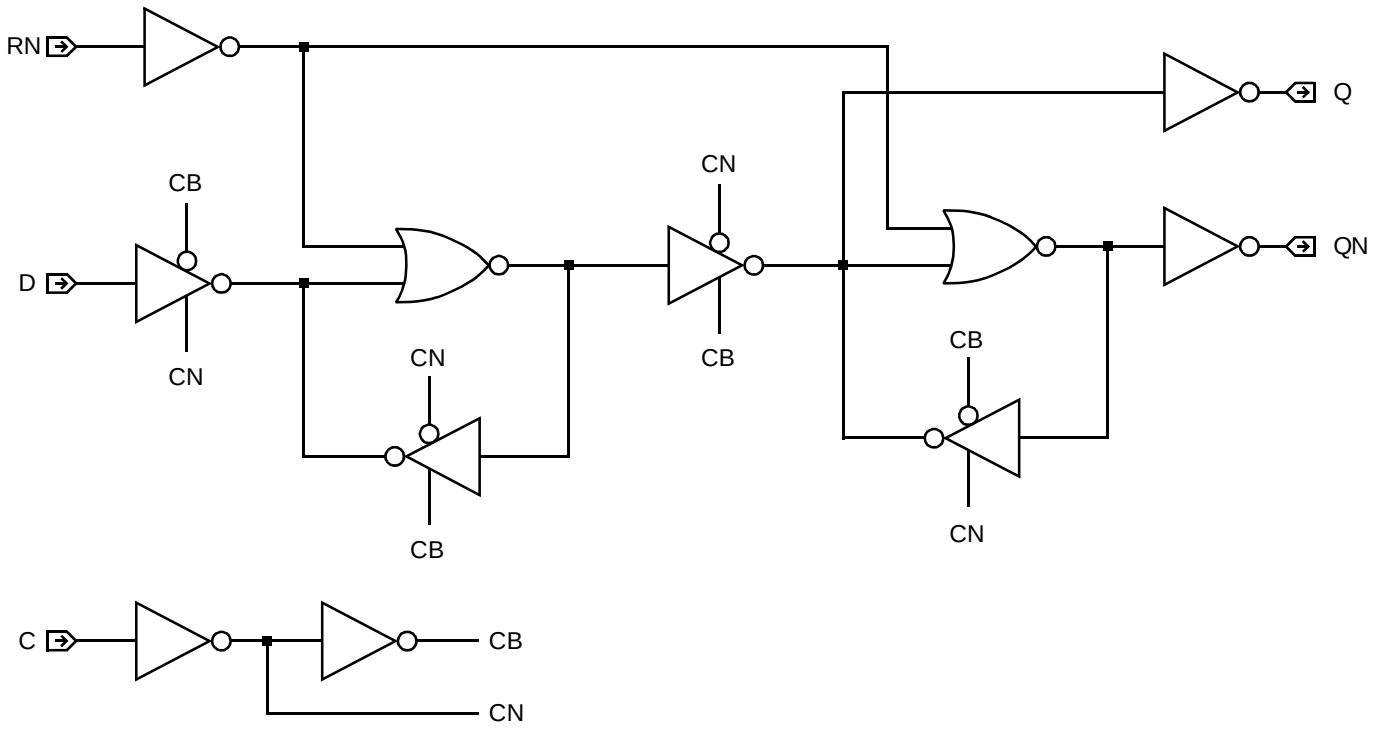
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF111	DF112	DF114	DF116
Min C Width	High	t_w	0.63	0.79	0.80	0.92
Min C Width	Low	t_w	0.57	0.59	0.66	0.66
Min RN Width		t_w	0.57	0.57	0.65	0.65
Min D Setup		t_{su}	0.37	0.36	0.41	0.41
Min D Hold		t_h	0.16	0.17	0.18	0.19
Min RN Setup		t_{su}	0.32	0.33	0.40	0.40
Min RN Hold		t_h	0.33	0.34	0.36	0.36

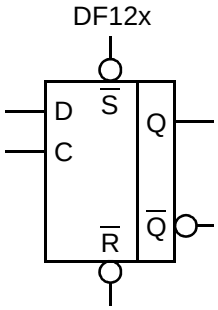
Logic Schematic



Description

DF12x is a family of static, master-slave D flip-flops. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

IL = Illegal NC = No Change

HDL Syntax

Verilog ..... DF12x *inst_name* (Q, QN, C, D, RN, SN);

VHDL..... *inst_name*: DF12x port map (Q, QN, C, D, RN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF121	DF122	DF124	DF126
D	1.0	1.0	1.0	1.0
C	1.0	1.0	1.0	1.0
SN	2.1	2.1	2.1	2.1
RN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF121	6.8	TBD	20.2
DF122	7.3	TBD	23.0
DF124	9.0	TBD	31.6
DF126	10.2	TBD	37.6

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DF121	From: C To: Q	t_{PLH} t_{PHL}	0.59 0.52	0.66 0.62	0.75 0.76	0.87 0.91	0.95 1.03
	From: C To: QN	t_{PLH} t_{PHL}	0.69 0.92	0.74 1.02	0.82 1.15	0.94 1.30	1.04 1.42
	From: SN To: Q	t_{PLH}	0.71	0.79	0.89	1.01	1.10
	From: SN To: QN	t_{PHL}	0.28	0.37	0.50	0.65	0.76
	From: RN To: Q	t_{PHL}	0.97	1.07	1.22	1.39	1.52
	From: RN To: QN	t_{PLH}	0.43	0.50	0.59	0.71	0.80
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DF122	From: C To: Q	t_{PLH} t_{PHL}	0.60 0.54	0.71 0.67	0.79 0.79	0.86 0.90	0.94 1.04
	From: C To: QN	t_{PLH} t_{PHL}	0.82 1.08	0.90 1.18	0.96 1.28	1.02 1.37	1.09 1.48
	From: SN To: Q	t_{PLH}	0.87	0.96	1.03	1.10	1.17
	From: SN To: QN	t_{PHL}	0.30	0.42	0.52	0.61	0.71
	From: RN To: Q	t_{PHL}	1.13	1.29	1.40	1.50	1.60
	From: RN To: QN	t_{PLH}	0.46	0.55	0.63	0.71	0.79

	Number of Equivalent Loads		1	10	20	30	40 (max)
DF124	From: C To: Q	t_{PLH} t_{PHL}	1.10 0.91	1.18 1.03	1.24 1.13	1.30 1.22	1.35 1.30
	From: C To: QN	t_{PLH} t_{PHL}	0.68 0.81	0.77 0.91	0.84 1.02	0.90 1.12	0.95 1.22
	From: SN To: Q	t_{PLH}	0.44	0.52	0.59	0.65	0.72
	From: SN To: QN	t_{PHL}	0.97	1.11	1.20	1.28	1.33
	From: RN To: Q	t_{PHL}	0.67	0.78	0.89	0.97	1.06
	From: RN To: QN	t_{PLH}	1.18	1.21	1.28	1.35	1.44
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
DF126	From: C To: Q	t_{PLH} t_{PHL}	1.18 0.98	1.26 1.14	1.32 1.24	1.37 1.32	1.42 1.38
	From: C To: QN	t_{PLH} t_{PHL}	0.78 0.92	0.85 1.06	0.92 1.15	0.99 1.23	1.05 1.30
	From: SN To: Q	t_{PLH}	0.51	0.59	0.65	0.72	0.79
	From: SN To: QN	t_{PHL}	1.05	1.20	1.31	1.41	1.49
	From: RN To: Q	t_{PHL}	0.76	0.87	0.98	1.08	1.16
	From: RN To: QN	t_{PLH}	1.28	1.31	1.38	1.45	1.54

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMERICAN MICROSYSTEMS, INC.

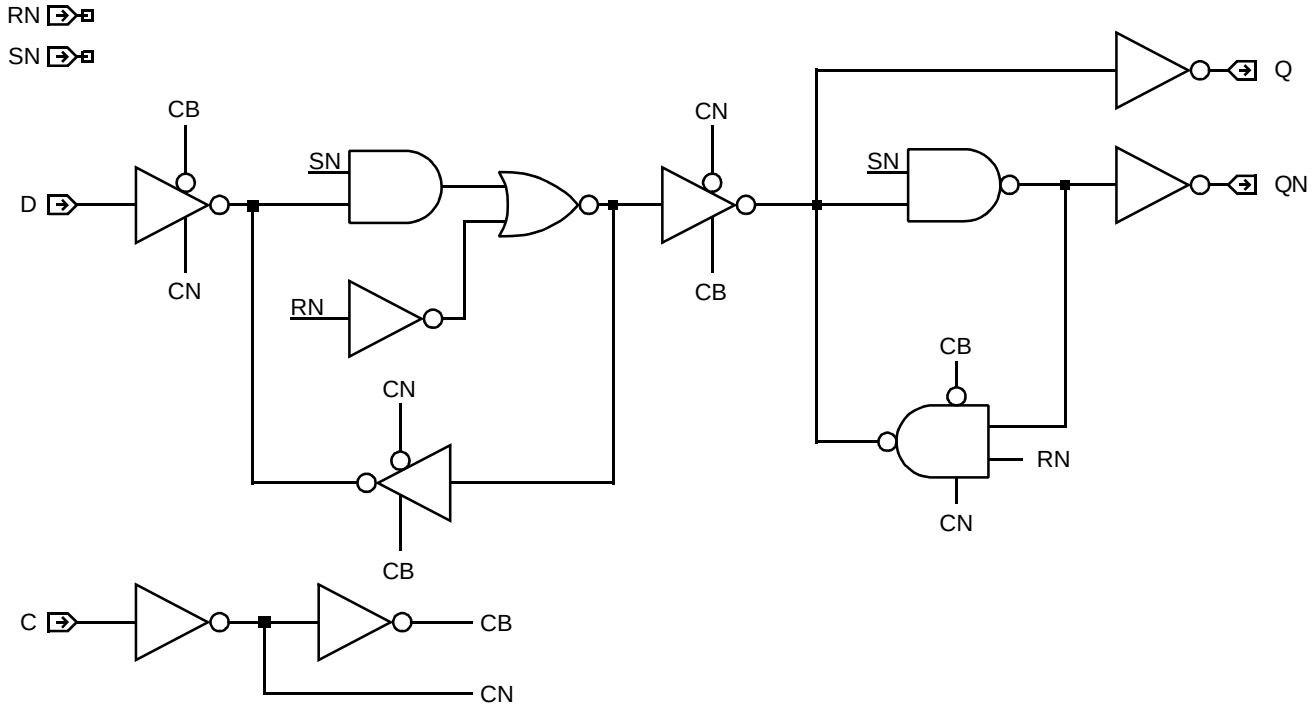
AMI5HS 0.5 micron CMOS Standard Cell

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF121	DF122	DF124	DF126
Min C Width	High	t_w	0.71	0.84	0.70	0.71
Min C Width	Low	t_w	0.61	0.61	0.61	0.61
Min RN Width	Low	t_w	0.60	0.60	0.60	0.60
Min SN Width	Low	t_w	0.59	0.73	0.60	0.60
Min D Setup		t_{su}	0.41	0.41	0.40	0.41
Min D Hold		t_h	0.17	0.17	0.17	0.17
Min RN Setup		t_{su}	0.36	0.36	0.36	0.36
Min RN Hold		t_h	0.34	0.34	0.33	0.34
Min SN Setup		t_{su}	0.21	0.21	0.21	0.21
Min SN Hold		t_h	0.55	0.55	0.54	0.54

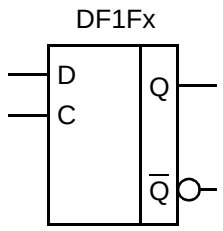
Logic Schematic



Description

DF1Fx is a family of static, master-slave D flip-flops without SET or RESET. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

D	C	Q	QN
X	X	L	H
L	↑	L	H
H	↑	H	L
X	L	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF1Fx *inst_name* (Q, QN, C, D);

VHDL..... *inst_name*: DF1Fx port map (Q, QN, C, D)

Pin Loading

Pin Name	Equivalent Loads			
	DF1F1	DF1F2	DF1F4	DF1F6
D	1.0	1.0	1.0	1.0
C	1.1	1.1	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF1F1	5.0	TBD	15.3
DF1F2	5.7	TBD	17.4
DF1F4	7.0	TBD	25.5
DF1F6	8.2	TBD	32.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DF1F1	From: C To: Q	t_{PLH} t_{PHL}	0.61 0.54	0.68 0.65	0.78 0.79	0.90 0.95	0.99 1.07
	From: C To: QN	t_{PLH} t_{PHL}	0.64 0.79	0.70 0.88	0.78 1.00	0.89 1.14	0.98 1.25
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DF1F2	From: C To: Q	t_{PLH} t_{PHL}	0.64 0.57	0.73 0.72	0.82 0.84	0.89 0.94	0.98 1.04
	From: C To: QN	t_{PLH} t_{PHL}	0.75 0.87	0.81 0.97	0.87 1.06	0.94 1.16	1.02 1.26
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
DF1F4	From: C To: Q	t_{PLH} t_{PHL}	0.92 0.85	1.00 0.95	1.07 1.05	1.12 1.14	1.17 1.22
	From: C To: QN	t_{PLH} t_{PHL}	0.59 0.70	0.68 0.83	0.75 0.94	0.81 1.03	0.87 1.13
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
DF1F6	From: C To: Q	t_{PLH} t_{PHL}	0.92 0.86	1.01 0.96	1.07 1.04	1.11 1.12	1.14 1.19
	From: C To: QN	t_{PLH} t_{PHL}	0.66 0.78	0.72 0.87	0.78 0.97	0.86 1.05	0.94 1.13

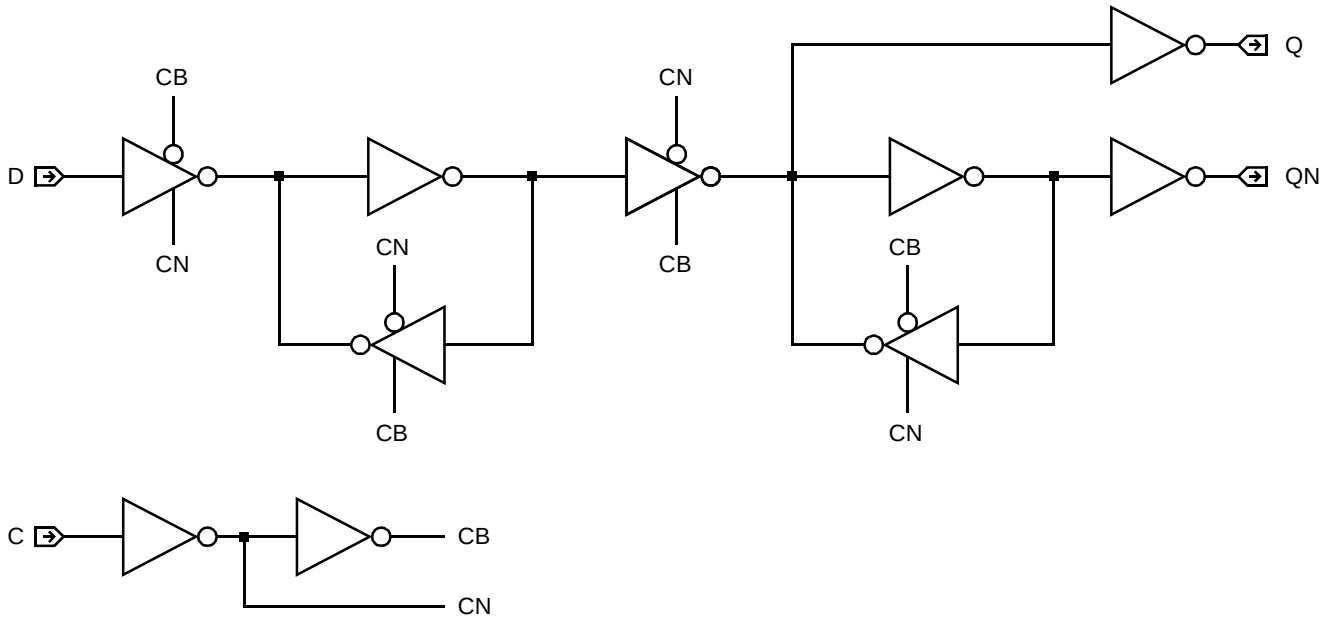
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DF1F1	DF1F2	DF1F4	DF1F6
Min C Width	High	t_w	0.63	0.72	0.59	0.63
Min C Width	Low	t_w	0.55	0.56	0.53	0.53
Min D Setup		t_{su}	0.34	0.35	0.33	0.33
Min D Hold		t_h	0.17	0.17	0.16	0.16

Logic Schematic



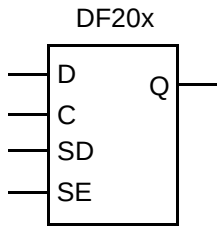
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

DF20x is a family of static, master-slave, multiplexed scan D flip-flops without SET or RESET. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	Q
↑	H	X	L	H
↑	L	X	L	L
↑	X	H	H	H
↑	X	L	H	L
L	X	X	X	NC

NC = No Change

HDL Syntax

Verilog ..... DF20x *inst_name* (Q, C, D, SD, SE);

VHDL..... *inst_name*: DF20x port map (Q, C, D, SD, SE);

Pin Loading

Pin Name	Equivalent Loads	
	DF201	DF202
C	1.0	1.0
D	1.0	1.0
SD	1.0	1.0
SE	2.1	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF201	5.7	TBD	17.0
DF202	5.5	TBD	16.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DF201	From: C	t_{PLH}	0.58	0.63	0.72	0.85	0.94
	To: Q	t_{PHL}	0.51	0.60	0.73	0.88	0.99
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DF202	From: C	t_{PLH}	0.55	0.63	0.70	0.77	0.84
	To: Q	t_{PHL}	0.48	0.62	0.72	0.81	0.91

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

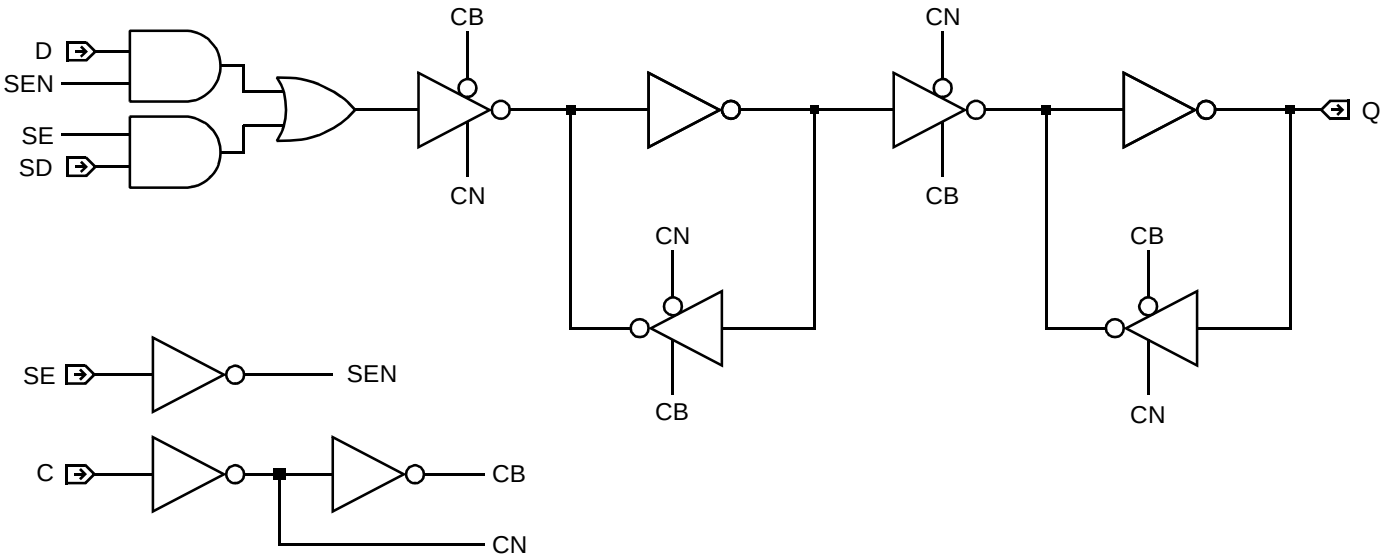
Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			DF201	DF202
Min C Width	High	t_w	0.58	0.54
Min C Width	Low	t_w	0.77	0.68
Min D Setup		t_{su}	0.63	0.57
Min D Hold		t_h	0.17	0.17
Min SD Setup		t_{su}	0.63	0.57
Min SD Hold		t_h	0.17	0.17
Min SE Setup		t_{su}	0.77	0.71
Min SE Hold		t_h	0.17	0.17

AMI5HS 0.5 micron CMOS Standard Cell

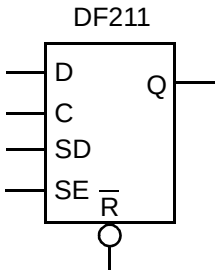
Logic Schematic



Description

DF211 is a static, master-slave, multiplexed scan D flip-flop. RESET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	Q
↑	H	H	X	L	H
↑	L	H	X	L	L
↑	X	H	H	H	H
↑	X	H	L	H	L
X	X	L	X	X	L
L	X	H	X	X	NC

NC = No Change

Pin Loading

	Equivalent Load
C	1.1
D	1.0
RN	1.0
SD	1.0
SE	2.1

Equivalent Gates 6.5

HDL Syntax

Verilog ..... DF211 *inst_name* (Q, C, D, RN, SD, SE);

VHDL..... *inst_name*: DF211 port map (Q, C, D, RN, SD, SE);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	19.9	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.61 0.48	0.66 0.53	0.76 0.62	0.93 0.74	1.04 0.82
RN	Q	t_{PHL}	0.33	0.38	0.46	0.57	0.65

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

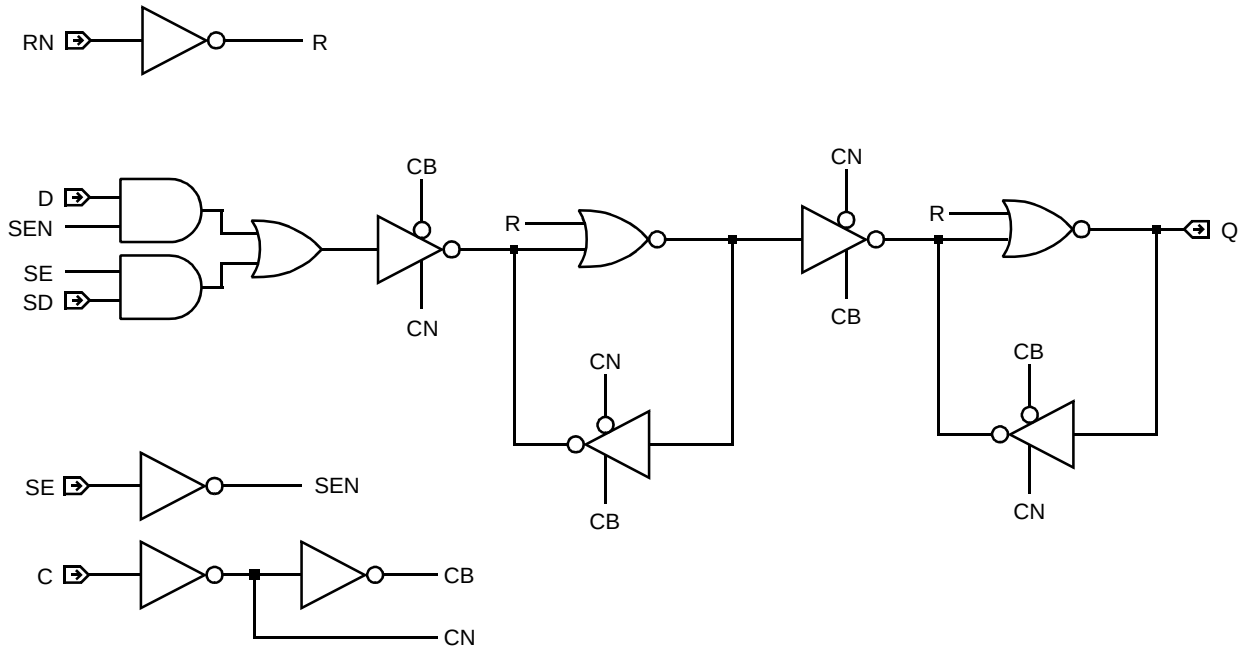
AMI5HS 0.5 micron CMOS Standard Cell

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.61
Min C Width	Low	t_w	0.74
Min RN Width	Low	t_w	0.58
Min D Setup		t_{su}	0.63
Min D Hold		t_h	0.17
Min SD Setup		t_{su}	0.63
Min SD Hold		t_h	0.17
Min SE Setup		t_{su}	0.75
Min SE Hold		t_h	0.17
Min RN Setup		t_{su}	0.32
Min RN Hold		t_h	0.35

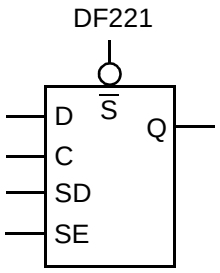
Logic Schematic



Description

DF221 is a static, master-slave, multiplexed scan D flip-flop. SET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	SN	Q
↑	H	X	L	H	H
↑	L	X	L	H	L
↑	X	H	H	H	H
↑	X	L	H	H	L
X	X	X	X	L	H
L	X	X	X	H	NC

NC = No Change

Pin Loading

	Equivalent Load
C	1.1
D	1.0
SD	1.0
SE	2.0
SN	2.1

Equivalent Gates 6.0

HDL Syntax

Verilog ..... DF221 *inst_name* (Q, C, D, SD, SE, SN);

VHDL..... *inst_name*: DF221 port map (Q, C, D, SD, SE, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	16.6	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.56 0.50	0.59 0.56	0.67 0.67	0.79 0.85	0.88 0.97
SN	Q	t_{PLH}	0.13	0.17	0.24	0.34	0.41

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

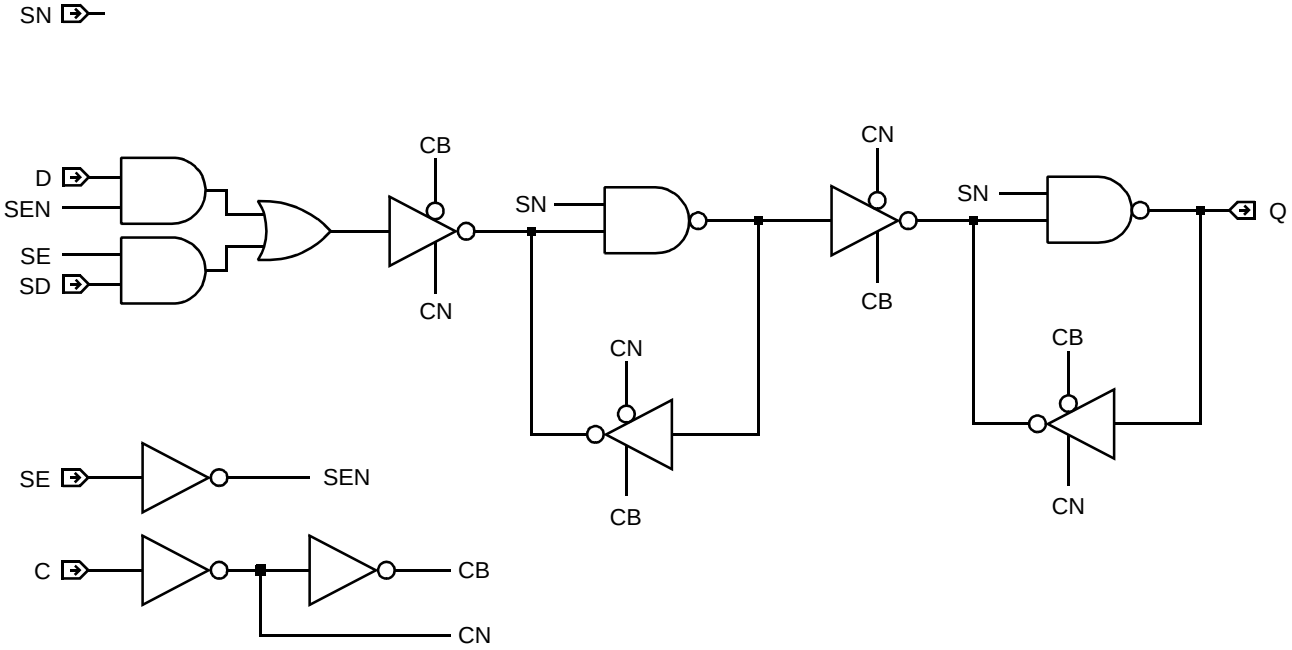
AMI5HS 0.5 micron CMOS Standard Cell

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.56
Min C Width	Low	t_w	0.79
Min SN Width	Low	t_w	0.50
Min D Setup		t_{su}	0.67
Min D Hold		t_h	0.17
Min SD Setup		t_{su}	0.67
Min SD Hold		t_h	0.17
Min SE Setup		t_{su}	0.81
Min SE Hold		t_h	0.17
Min SN Setup		t_{su}	0.17
Min SN Hold		t_h	0.55

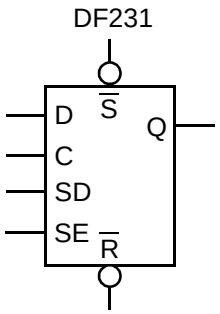
Logic Schematic



Description

DF231 is a static, master-slave, multiplexed scan D flip-flop. SET and RESET are asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	SN	Q
↑	H	H	X	L	H	H
↑	L	H	X	L	H	L
↑	X	H	H	H	H	H
↑	X	H	L	H	H	L
X	X	L	X	X	H	L
X	X	H	X	X	L	H
X	X	L	X	X	L	IL
L	X	H	X	X	H	NC

NC = No Change IL = Illegal Condition

Pin Loading

	Equivalent Load
C	1.0
D	1.0
RN	1.0
SD	1.0
SE	2.1
SN	2.1

Equivalent Gates 7.3

HDL Syntax

Verilog ..... DF231 *inst_name* (Q, C, D, RN, SD, SE, SN);

VHDL..... *inst_name*: DF231 port map (Q, C, D, RN, SD, SE, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	20.7	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Delay (ns) Number of Equivalent Loads 1	2	4	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.64 0.52	0.71 0.58	0.84 0.70	1.03 0.88	1.17 1.00
RN	Q	t_{PHL}	0.36	0.42	0.53	0.70	0.81
SN	Q	t_{PLH}	0.13	0.17	0.23	0.33	0.37

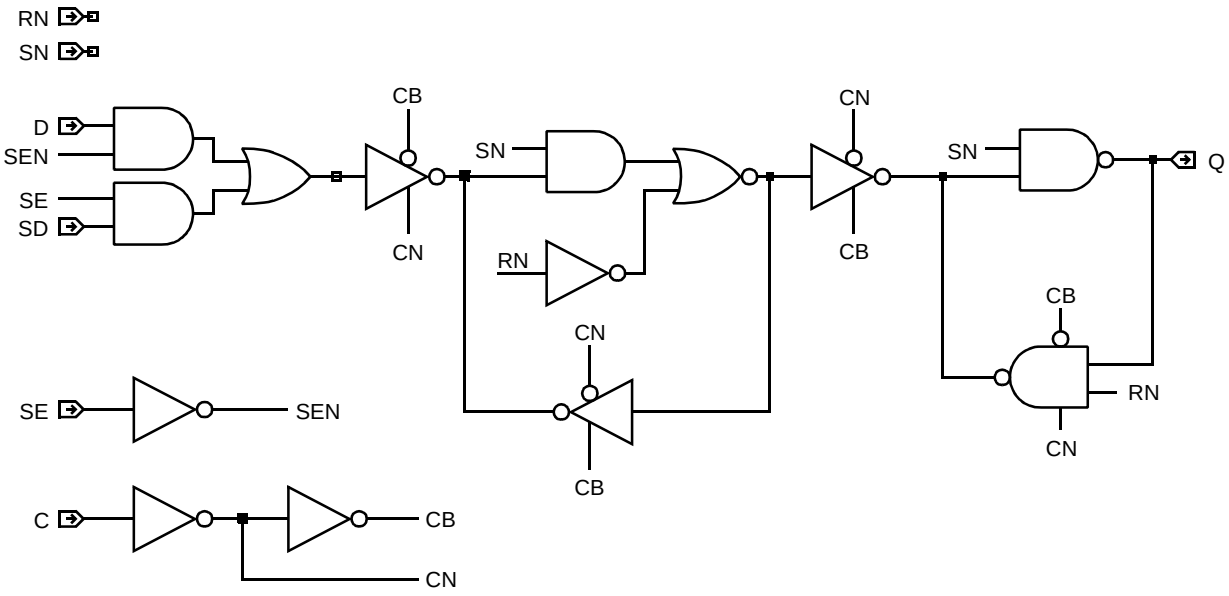
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.64
Min C Width	Low	t_w	0.77
Min RN Width	Low	t_w	0.61
Min SN Width	Low	t_w	0.50
Min D Setup		t_{su}	0.65
Min D Hold		t_h	0.17
Min SD Setup		t_{su}	0.65
Min SD Hold		t_h	0.17
Min SE Setup		t_{su}	0.78
Min SE Hold		t_h	0.17
Min RN Setup		t_{su}	0.37
Min RN Hold		t_h	0.35
Min SN Setup		t_{su}	0.21
Min SN Hold		t_h	0.56

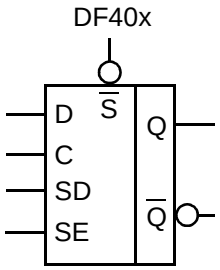
Logic Schematic



Description

DF40x is a family of static, master-slave, multiplexed scan D flip-flops. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	SN	Q	QN
↑	H	X	L	H	H	L
↑	L	X	L	H	L	H
↑	X	H	H	H	H	L
↑	X	L	H	H	L	H
X	X	X	X	L	H	L
L	X	X	X	H	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF40x *inst_name* (Q, QN, C, D, SD, SE, SN);

VHDL..... *inst_name*: DF40x port map (Q, QN, C, D, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF401	DF402	DF404	DF406
C	1.1	1.1	1.0	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1
SN	2.1	2.1	3.1	3.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF401	6.8	TBD	20.0
DF402	7.3	TBD	22.3
DF404	9.8	TBD	33.4
DF406	10.8	TBD	39.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DF401	From: C To: Q	t_{PLH} t_{PHL}	0.60 0.52	0.68 0.63	0.78 0.77	0.90 0.94	1.00 1.05
	From: C To: QN	t_{PLH} t_{PHL}	0.67 0.81	0.73 0.89	0.82 1.01	0.94 1.17	1.02 1.29
	From: SN To: Q	t_{PLH}	0.74	0.82	0.93	1.04	1.12
	From: SN To: QN	t_{PHL}	0.29	0.39	0.52	0.68	0.79
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DF402	From: C To: Q	t_{PLH} t_{PHL}	0.61 0.55	0.70 0.70	0.79 0.83	0.86 0.94	0.95 1.08
	From: C To: QN	t_{PLH} t_{PHL}	0.81 0.93	0.88 1.04	0.94 1.13	0.99 1.22	1.06 1.32
	From: SN To: Q	t_{PLH}	0.85	0.95	1.04	1.11	1.20
	From: S To: QN	t_{PHL}	0.32	0.45	0.56	0.66	0.77
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
DF404	From: C To: Q	t_{PLH} t_{PHL}	0.66 0.56	0.76 0.70	0.84 0.82	0.91 0.92	0.98 1.01
	From: C To: QN	t_{PLH} t_{PHL}	0.79 0.93	0.83 1.00	0.89 1.09	0.97 1.18	1.07 1.31
	From: SN To: Q	t_{PLH}	0.78	0.90	0.98	1.05	1.12
	From: SN To: QN	t_{PHL}	0.29	0.40	0.50	0.59	0.68

	Number of Equivalent Loads		1	14	29	44	58 (max)
DF406	From: C To: Q	t_{PLH} t_{PHL}	0.70 0.61	0.82 0.76	0.89 0.91	0.96 1.00	1.01 1.10
	From: C To: QN	t_{PLH} t_{PHL}	0.96 1.05	0.99 1.15	1.05 1.24	1.11 1.32	1.19 1.39
	From: SN To: Q	t_{PLH}	0.98	1.06	1.14	1.21	1.28
	From: SN To: QN	t_{PHL}	0.31	0.44	0.55	0.64	0.72

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

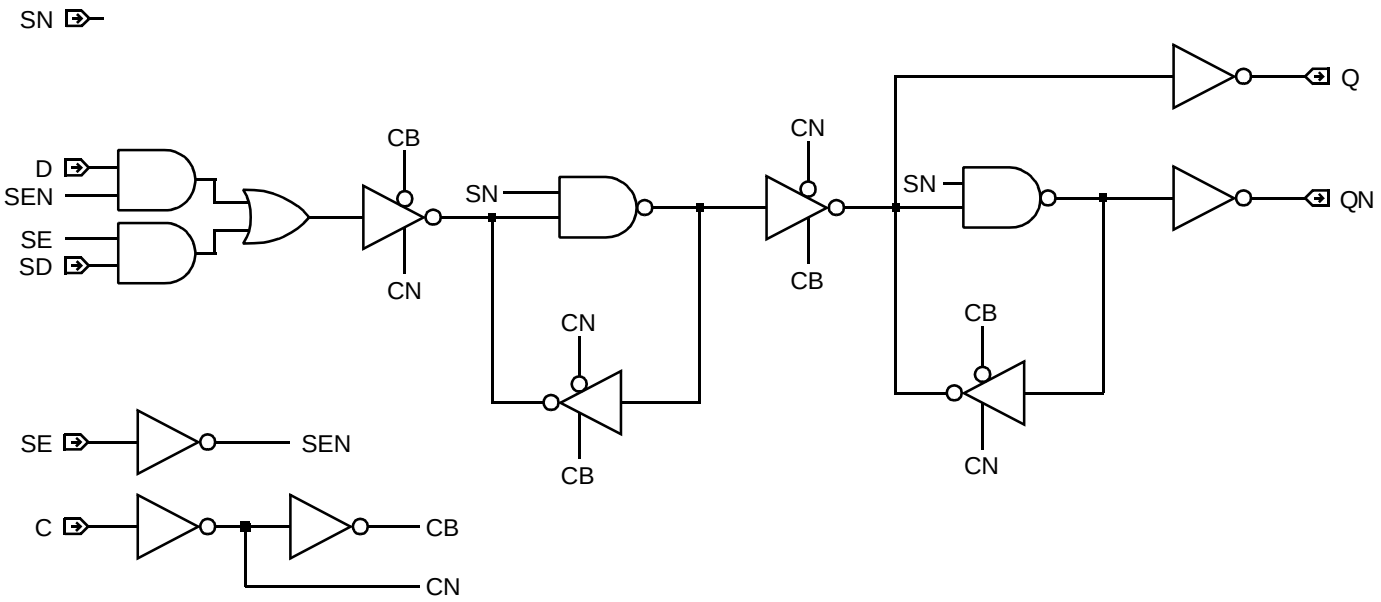
Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DF401	DF402	DF404	DF406
Min C Width	High	t_w	0.64	0.74	0.77	0.87
Min C Width	Low	t_w	0.77	0.79	0.85	0.86
Min SN Width	Low	t_w	0.59	0.74	0.70	0.86
Min D Setup		t_{su}	0.65	0.65	0.68	0.68
Min D Hold		t_h	0.17	0.17	0.19	0.19
Min SD Setup		t_{su}	0.65	0.65	0.68	0.68
Min SD Hold		t_h	0.17	0.17	0.19	0.19
Min SE Setup		t_{su}	0.77	0.77	0.81	0.81
Min SE Hold		t_h	0.17	0.17	0.19	0.19
Min SN Setup		t_{su}	0.18	0.18	0.22	0.22
Min SN Hold		t_h	0.56	0.56	0.61	0.60

AMI5HS 0.5 micron CMOS Standard Cell

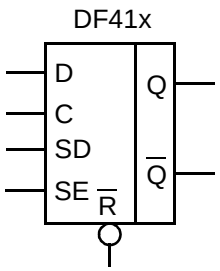
Logic Schematic



Description

DF41x is a family of static, master-slave, multiplexed scan D flip-flops. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	Q	QN
↑	H	H	X	L	H	L
↑	L	H	X	L	L	H
↑	X	H	H	H	H	L
↑	X	H	L	H	L	H
X	X	L	X	X	L	H
L	X	H	X	X	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF41x *inst_name* (Q, QN, C, D, RN, SD, SE);

VHDL..... *inst_name*: DF41x port map (Q, QN, C, D, RN, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	DF411	DF412	DF414	DF416
C	1.1	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
RN	1.1	1.0	1.0	1.0
SD	1.1	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF411	7.3	TBD	22.9
DF412	7.5	TBD	25.2
DF414	10.0	TBD	37.5
DF416	11.2	TBD	43.2

a. See page 2-13 for power equation.

Core Logic

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DF411	From: C To: Q	t_{PLH} t_{PHL}	0.60 0.50	0.67 0.61	0.77 0.74	0.89 0.90	0.97 1.03
	From: C To: QN	t_{PLH} t_{PHL}	0.64 0.85	0.71 0.94	0.80 1.07	0.92 1.22	1.01 1.32
	From: RN To: Q	t_{PHL}	0.94	1.05	1.19	1.36	1.49
	From: RN To: QN	t_{PLH}	0.40	0.47	0.57	0.69	0.79
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DF412	From: C To: Q	t_{PLH} t_{PHL}	0.60 0.55	0.71 0.71	0.79 0.83	0.87 0.93	0.95 1.04
	From: C To: QN	t_{PLH} t_{PHL}	0.76 0.97	0.83 1.08	0.90 1.17	0.97 1.26	1.04 1.37
	From: RN To: Q	t_{PHL}	1.09	1.26	1.37	1.46	1.56
	From: RN To: QN	t_{PLH}	0.40	0.49	0.57	0.63	0.72
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
DF414	From: C To: Q	t_{PLH} t_{PHL}	0.65 0.54	0.75 0.71	0.83 0.82	0.90 0.92	0.97 1.01
	From: C To: QN	t_{PLH} t_{PHL}	0.75 0.92	0.82 1.10	0.88 1.20	0.94 1.29	0.99 1.37
	From: RN To: Q	t_{PHL}	1.12	1.26	1.38	1.47	1.56
	From: RN To: QN	t_{PLH}	0.43	0.51	0.59	0.65	0.71

	Number of Equivalent Loads		1	14	29	44	58 (max)
DF416	From: C To: Q	t_{PLH} t_{PHL}	0.70 0.64	0.81 0.76	0.88 0.88	0.94 0.99	1.00 1.09
	From: C To: QN	t_{PLH} t_{PHL}	0.90 1.12	0.96 1.22	1.02 1.33	1.06 1.42	1.10 1.51
	From: RN To: Q	t_{PHL}	1.29	1.47	1.58	1.66	1.72
	From: RN To: QN	t_{PLH}	0.47	0.55	0.61	0.68	0.75

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Core Logic

Timing Constraints

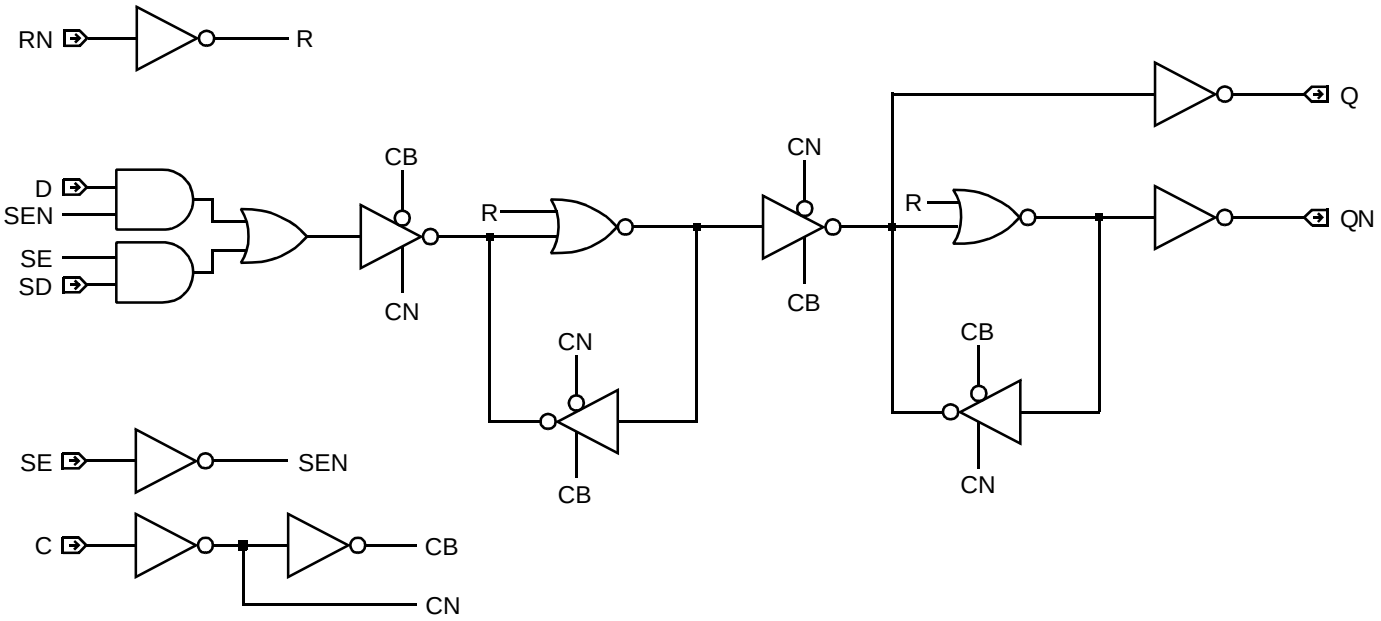
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DF411	DF412	DF414	DF416
Min C Width	High	t_w	0.66	0.76	0.81	0.93
Min C Width	Low	t_w	0.74	0.73	0.83	0.83
Min RN Width	Low	t_w	0.58	0.58	0.66	0.66
Min D Setup		t_{su}	0.61	0.62	0.66	0.66
Min D Hold		t_h	0.17	0.17	0.19	0.19
Min SD Setup		t_{su}	0.61	0.62	0.66	0.66
Min SD Hold		t_h	0.17	0.17	0.19	0.19
Min SE Setup		t_{su}	0.75	0.74	0.79	0.79
Min SE Hold		t_h	0.17	0.17	0.19	0.19
Min RN Setup		t_{su}	0.32	0.32	0.42	0.42
Min RN Hold		t_h	0.35	0.35	0.38	0.38

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

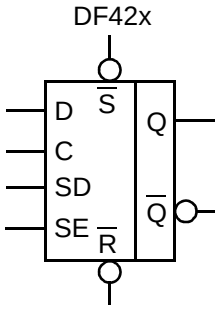
Logic Schematic



Description

DF42x is a family of static, master-slave, multiplexed scan D flip-flops. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	SN	Q	QN
↑	H	H	X	L	H	H	L
↑	L	H	X	L	H	L	H
↑	X	H	H	H	H	H	L
↑	X	H	L	H	H	L	H
X	X	L	X	X	H	L	H
X	X	H	X	X	L	H	L
X	X	L	X	X	L	IL	IL
L	X	H	X	X	H	NC	NC

NC = No Change IL = Illegal Condition

HDL Syntax

Verilog ..... DF421x *inst_name* (Q, QN, C, D, RN, SD, SE, SN);

VHDL..... *inst_name*: DF421x port map (Q, QN, C, D, RN, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF421	DF422	DF424	DF426
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1
SN	2.1	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF421	8.2	TBD	24.3

AMI5HS 0.5 micron CMOS Standard Cell

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF422	8.8	TBD	27.1
DF424	10.5	TBD	36.0
DF426	11.7	TBD	41.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DF421	From: C To: Q	t_{PLH} t_{PHL}	0.60 0.53	0.67 0.64	0.78 0.77	0.91 0.94	1.01 1.05
	From: C To: QN	t_{PLH} t_{PHL}	0.71 0.92	0.78 1.02	0.88 1.15	0.98 1.31	1.07 1.44
	From: RN To: Q	t_{PHL}	1.00	1.12	1.27	1.44	1.56
	From: RN To: QN	t_{PLH}	0.46	0.53	0.63	0.75	0.85
	From: SN To: Q	t_{PLH}	0.74	0.82	0.93	1.05	1.15
	From: SN To: QN	t_{PHL}	0.29	0.38	0.51	0.67	0.79
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DF422	From: C To: Q	t_{PLH} t_{PHL}	0.63 0.56	0.74 0.72	0.84 0.84	0.93 0.96	1.04 1.08
	From: C To: QN	t_{PLH} t_{PHL}	0.84 1.08	0.92 1.21	0.99 1.30	1.05 1.38	1.13 1.48
	From: RN To: Q	t_{PHL}	1.18	1.35	1.47	1.58	1.71
	From: RN To: QN	t_{PLH}	0.50	0.60	0.68	0.75	0.84
	From: SN To: Q	t_{PLH}	0.86	0.98	1.08	1.17	1.28
	From: SN To: QN	t_{PHL}	0.31	0.43	0.53	0.63	0.73

	Number of Equivalent Loads		1	10	20	30	40 (max)
DF424	From: C To: Q	t_{PLH} t_{PHL}	1.11 0.93	1.16 1.04	1.23 1.14	1.30 1.23	1.37 1.33
	From: C To: QN	t_{PLH} t_{PHL}	0.70 0.83	0.76 0.96	0.83 1.04	0.90 1.12	0.98 1.25
	From: RN To: Q	t_{PHL}	0.68	0.81	0.93	1.03	1.12
	From: RN To: QN	t_{PLH}	1.20	1.28	1.34	1.38	1.44
	From: SN To: Q	t_{PLH}	0.44	0.53	0.59	0.66	0.74
	From: SN To: QN	t_{PHL}	0.99	1.08	1.18	1.27	1.35
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
DF426	From: C To: Q	t_{PLH} t_{PHL}	1.17 1.02	1.26 1.13	1.31 1.24	1.37 1.33	1.43 1.43
	From: C To: QN	t_{PLH} t_{PHL}	0.79 0.94	0.88 1.06	0.95 1.16	1.00 1.24	1.07 1.32
	From: RN To: Q	t_{PHL}	0.76	0.87	0.98	1.08	1.17
	From: RN To: QN	t_{PLH}	1.28	1.35	1.41	1.46	1.53
	From: SN To: Q	t_{PLH}	0.51	0.59	0.65	0.72	0.79
	From: SN To: QN	t_{PHL}	1.08	1.20	1.30	1.39	1.47

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

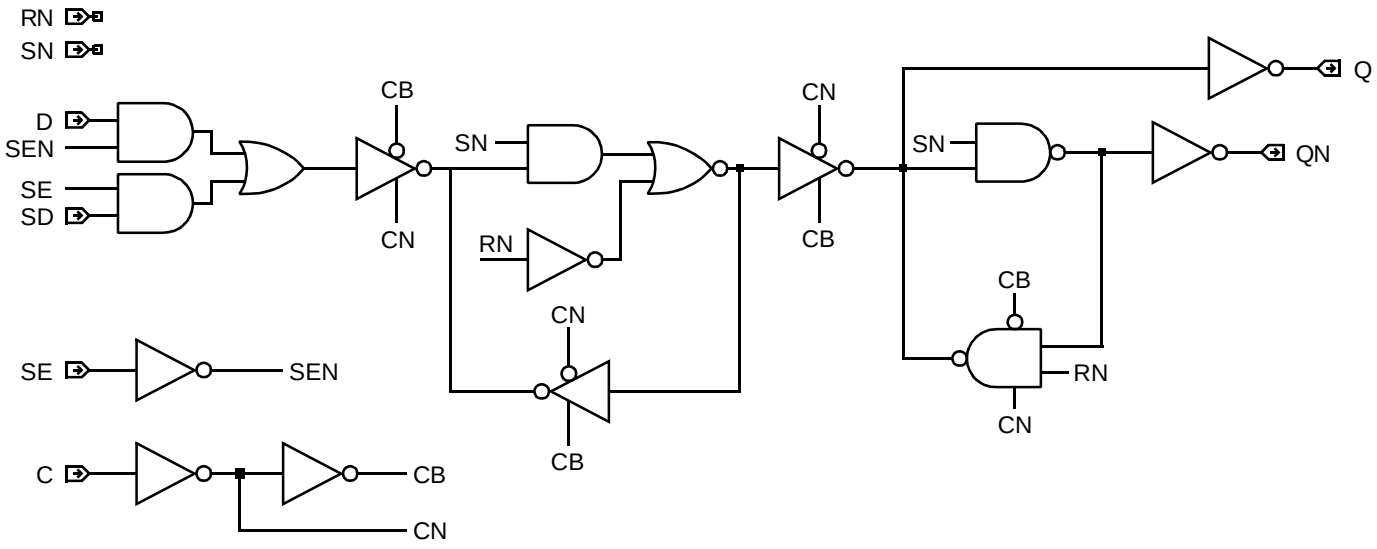
AMI5HS 0.5 micron CMOS Standard Cell

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF421	DF422	DF424	DF426
Min C Width	High	t_w	0.71	0.83	0.71	0.71
Min C Width	Low	t_w	0.77	0.78	0.77	0.78
Min RN Width	Low	t_w	0.63	0.65	0.61	0.62
Min SN Width	Low	t_w	0.59	0.73	0.59	0.60
Min D Setup		t_{su}	0.65	0.65	0.65	0.65
Min D Hold		t_h	0.17	0.17	0.17	0.17
Min SD Setup		t_{su}	0.65	0.65	0.65	0.65
Min SD Hold		t_h	0.17	0.17	0.17	0.17
Min SE Setup		t_{su}	0.78	0.78	0.78	0.78
Min SE Hold		t_h	0.17	0.17	0.17	0.17
Min RN Setup		t_{su}	0.37	0.37	0.37	0.36
Min RN Hold		t_h	0.35	0.35	0.35	0.35
Min SN Setup		t_{su}	0.22	0.22	0.21	0.22
Min SN Hold		t_h	0.56	0.56	0.56	0.56

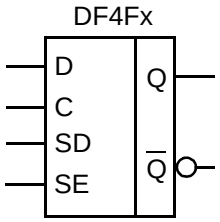
Logic Schematic



Description

DF4Fx is a family of static, master-slave, multiplexed scan D flip-flops without SET or RESET. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	Q	QN
↑	H	X	L	H	L
↑	L	X	L	L	H
↑	X	H	H	H	L
↑	X	L	H	L	H
L	X	X	X	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF4Fx *inst_name* (Q, QN, C, D, SD, SE);

VHDL..... *inst_name*: DF4Fx port map (Q, QN, C, D, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	DF4F1	DF4F2	DF4F4	DF4F6
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF4F1	6.2	TBD	18.9
DF4F2	6.8	TBD	21.2
DF4F4	8.5	TBD	29.7
DF4F6	9.8	TBD	36.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DF4F1	From: C To: Q	t_{PLH} t_{PHL}	0.58 0.52	0.65 0.64	0.75 0.77	0.87 0.93	0.96 1.04
	From: C To: QN	t_{PLH} t_{PHL}	0.62 0.75	0.68 0.83	0.76 0.95	0.87 1.09	0.96 1.19
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DF4F2	From: C To: Q	t_{PLH} t_{PHL}	0.60 0.54	0.70 0.69	0.79 0.81	0.86 0.91	0.95 1.04
	From: C To: QN	t_{PLH} t_{PHL}	0.73 0.82	0.80 0.93	0.86 1.03	0.93 1.11	1.01 1.21
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
DF4F4	From: C To: Q	t_{PLH} t_{PHL}	0.95 0.89	1.03 1.01	1.09 1.09	1.14 1.17	1.23 1.26
	From: C To: QN	t_{PLH} t_{PHL}	0.62 0.72	0.68 0.83	0.75 0.94	0.83 1.04	0.91 1.11
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
DF4F6	From: C To: Q	t_{PLH} t_{PHL}	0.97 0.90	1.02 1.00	1.08 1.09	1.15 1.15	1.22 1.21
	From: C To: QN	t_{PLH} t_{PHL}	0.68 0.83	0.76 0.94	0.83 1.02	0.88 1.10	0.93 1.18

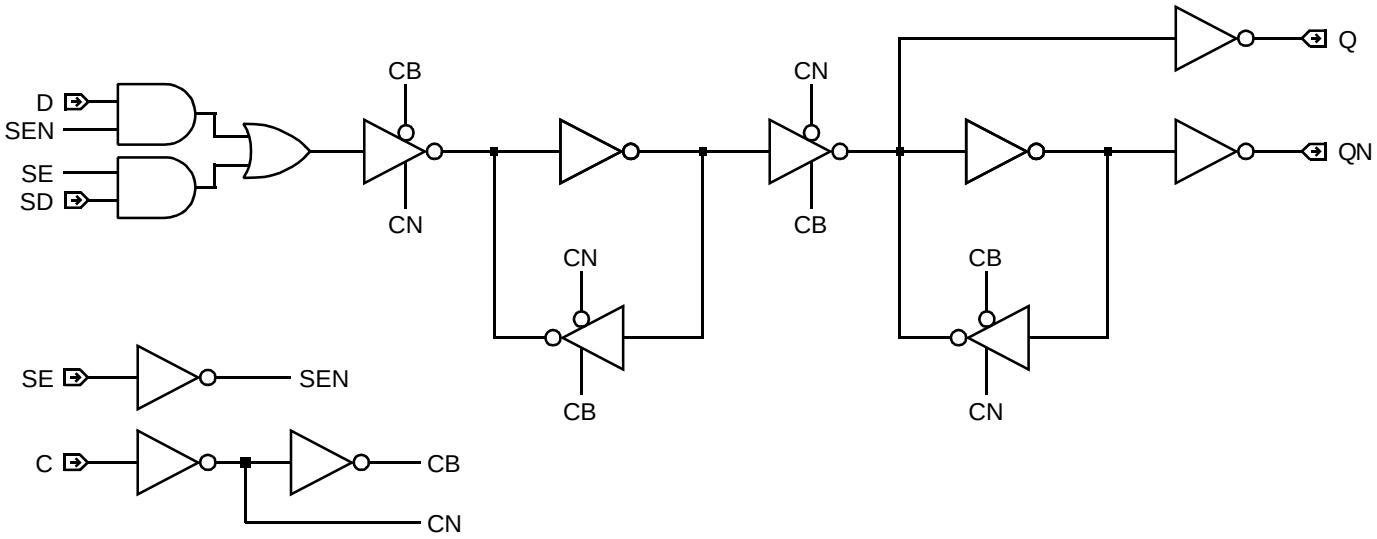
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF4F1	DF4F2	DF4F4	DF4F6
Min C Width	High	t_w	0.59	0.68	0.61	0.66
Min C Width	Low	t_w	0.71	0.71	0.71	0.71
Min D Setup		t_{su}	0.60	0.60	0.60	0.59
Min D Hold		t_h	0.17	0.17	0.17	0.17
Min SD Setup		t_{su}	0.60	0.60	0.60	0.59
Min SD Hold		t_h	0.17	0.17	0.17	0.17
Min SE Setup		t_{su}	0.72	0.72	0.72	0.72
Min SE Hold		t_h	0.17	0.17	0.17	0.17

Logic Schematic



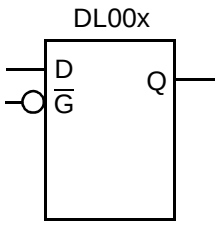
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

DL00x is a family of transparent, unbuffered D latch with active low gate transparency and without SET or RESET.

Logic Symbol



Truth Table

GN	D	Q
L	L	L
L	H	H
H	X	NC

NC = No Change

HDL Syntax

Verilog ..... DL00x *inst_name* (Q, D, GN);

VHDL..... *inst_name*: DL00x port map (Q, D, GN);

Pin Loading

Pin Name	Equivalent Loads	
	DL001	DL002
D	1.0	1.0
GN	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL001	2.5	TBD	5.6
DL002	2.8	TBD	6.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DL001	From: D To: Q	t_{PLH} t_{PHL}	0.30 0.35	0.37 0.45	0.47 0.57	0.59 0.72	0.68 0.83
	From: GN To: Q	t_{PLH} t_{PHL}	0.36 0.50	0.42 0.59	0.52 0.71	0.64 0.86	0.73 0.97
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DL002	From: D To: Q	t_{PLH} t_{PHL}	0.32 0.38	0.40 0.51	0.48 0.61	0.56 0.70	0.65 0.81
	From: GN To: Q	t_{PLH} t_{PHL}	0.38 0.51	0.48 0.64	0.55 0.74	0.62 0.84	0.69 0.96

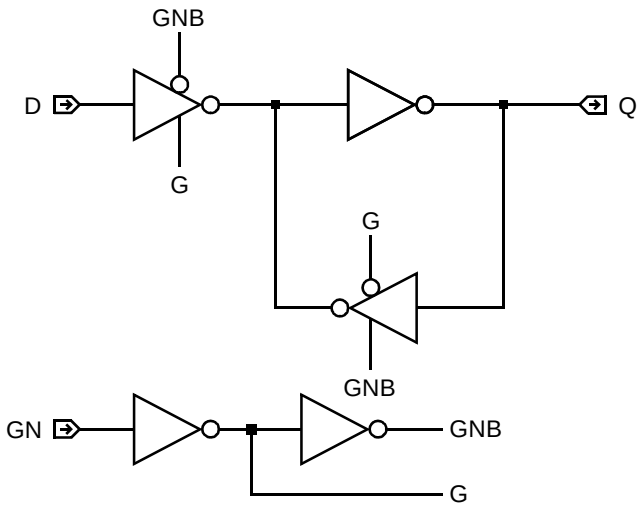
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DL001	Cell DL002
Min GN Width	Low	t_w	0.50	0.51
Min D Setup		t_{su}	0.35	0.37
Min D Hold		t_h	0.14	0.14

Logic Schematic



Core Logic

DL011

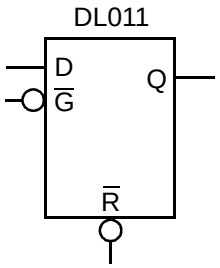
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

DL011 is a transparent, unbuffered D latch with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q
H	L	L	L
H	H	L	H
H	X	H	NC
L	X	X	L

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	1.0
RN	1.0

Core Logic

Equivalent Gates 3.2

HDL Syntax

Verilog ..... DL011 *inst_name* (Q, D, GN, RN);

VHDL..... *inst_name*: DL011 port map (Q, D, GN, RN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	7.8	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	4	7	9 (max)
D	Q	t_{PLH} t_{PHL}	0.35 0.37	0.40 0.42	0.51 0.51	0.68 0.63	0.80 0.70
GN	Q	t_{PLH} t_{PHL}	0.42 0.51	0.47 0.55	0.58 0.64	0.74 0.77	0.85 0.86
RN	Q	t_{PLH} t_{PHL}	0.29 0.26	0.35 0.31	0.46 0.39	0.61 0.51	0.72 0.58

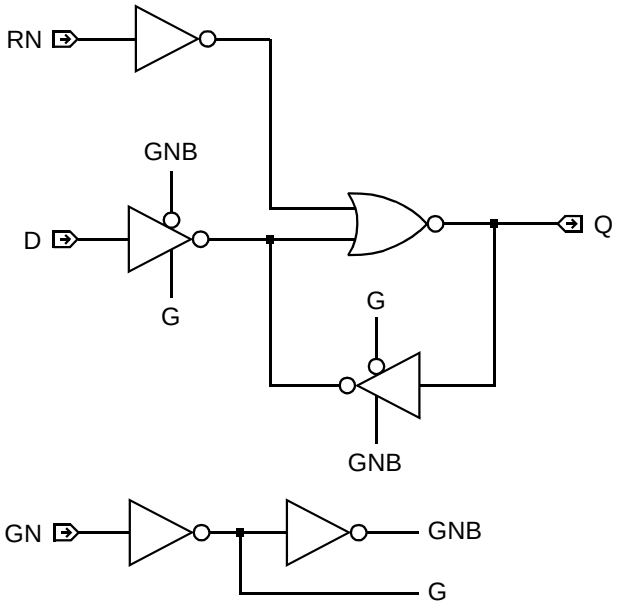
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min GN Width	Low	t_w	0.52
Min RN Width	Low	t_w	0.66
Min D Setup		t_{su}	0.37
Min D Hold		t_h	0.14
Min RN Setup		t_{su}	0.29
Min RN Hold		t_h	0.21

Logic Schematic



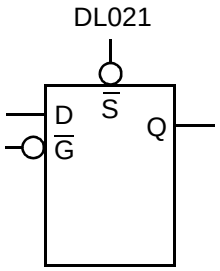
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

DL021 is a transparent, unbuffered D latch with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q
L	X	X	H
H	H	X	NC
H	L	L	L
H	L	H	H

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	1.0
SN	1.0

Equivalent Gates 2.8

HDL Syntax

Verilog ..... DL021 *inst_name* (Q, D, GN, SN);

VHDL..... *inst_name*: DL021 port map (Q, D, GN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	6.0	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	4	7	9 (max)
D	Q	t_{PLH} t_{PHL}	0.34 0.38	0.38 0.44	0.45 0.55	0.55 0.70	0.62 0.80
GN	Q	t_{PLH} t_{PHL}	0.40 0.54	0.44 0.59	0.52 0.70	0.61 0.85	0.67 0.95
SN	Q	t_{PLH} t_{PHL}	0.14 0.18	0.18 0.23	0.26 0.34	0.37 0.49	0.45 0.59

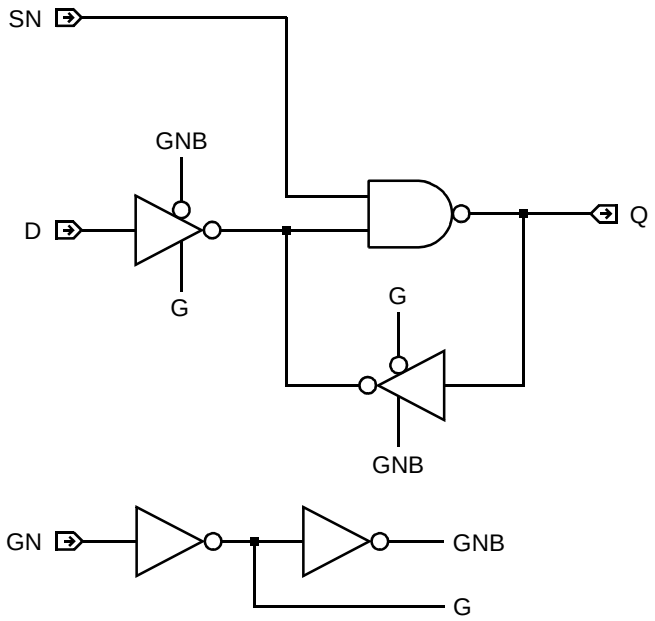
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min GN Width	Low	t_w	0.54
Min SN Width	Low	t_w	0.71
Min D Setup		t_{su}	0.39
Min D Hold		t_h	0.13
Min SN Setup		t_{su}	0.19
Min SN Hold		t_h	0.48

Logic Schematic



DL031

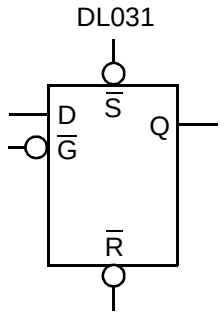
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

DL031 is a transparent, unbuffered D latches with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q
L	L	X	X	IL
L	H	X	X	H
H	L	X	X	L
H	H	X	H	NC
H	H	L	L	L
H	H	H	L	H

NC = No Change IL = Illegal

Pin Loading

	Equivalent Load
D	1.1
GN	1.0
SN	1.0
RN	1.1

Equivalent Gates 3.5

HDL Syntax

Verilog ..... DL031 *inst_name* (Q, D, GN, RN, SN);

VHDL..... *inst_name*: DL031 port map (Q, D, GN, RN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	7.2	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	4	7	9 (max)
D	Q	t_{PLH} t_{PHL}	0.44 0.49	0.49 0.56	0.57 0.67	0.68 0.83	0.75 0.93
GN	Q	t_{PLH} t_{PHL}	0.50 0.67	0.55 0.74	0.63 0.85	0.74 0.99	0.81 1.08
SN	Q	t_{PLH} t_{PHL}	0.15 0.20	0.19 0.25	0.26 0.35	0.36 0.49	0.43 0.60
RN	Q	t_{PLH} t_{PHL}	0.46 0.41	0.51 0.47	0.59 0.58	0.71 0.74	0.78 0.84

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMERICAN MICROSYSTEMS, INC.

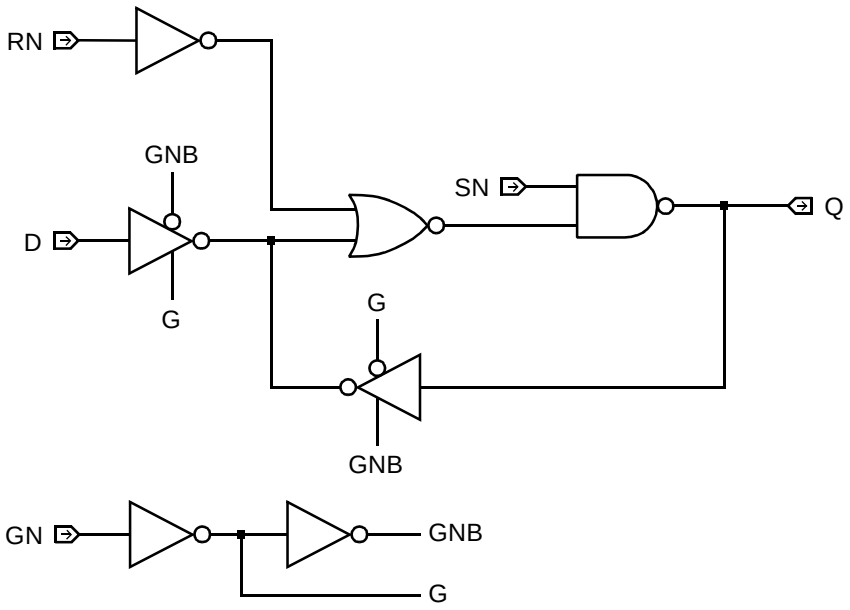
AMI5HS 0.5 micron CMOS Standard Cell

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min GN Width	Low	t_w	0.66
Min RN Width	Low	t_w	0.14
Min SN Width	Low	t_w	0.67
Min D Setup		t_{su}	0.49
Min D Hold		t_h	0.14
Min SN Setup		t_{su}	0.20
Min SN Hold		t_h	0.42
Min RN Setup		t_{su}	0.46
Min RN Hold		t_h	0.21

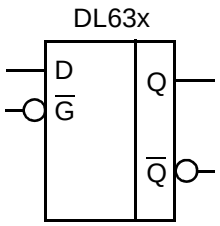
Logic Schematic



Description

DL63x is a family of transparent, buffered D latches with active low gate transparency and without SET or RESET.

Logic Symbol



Truth Table

D	GN	Q	QN
L	L	L	H
H	L	H	L
X	H	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DL63x *inst_name* (Q, QN, D, GN);

VHDL..... *inst_name*: DL63x port map (Q, QN, D, GN);

Pin Loading

Pin Name	Equivalent Loads			
	DL631	DL632	DL634	DL636
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL631	4.0	TBD	10.8
DL632	4.5	TBD	13.0
DL634	5.7	TBD	19.8
DL636	7.0	TBD	26.7

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DL631	From: D To: Q	t_{PLH} t_{PHL}	0.56 0.59	0.63 0.67	0.72 0.79	0.83 0.94	0.90 1.05
	From: D To: QN	t_{PLH} t_{PHL}	0.47 0.50	0.53 0.59	0.62 0.70	0.73 0.85	0.81 0.95
	From: GN To: Q	t_{PLH} t_{PHL}	0.62 0.73	0.68 0.80	0.77 0.92	0.88 1.08	0.97 1.20
	From: GN To: QN	t_{PLH} t_{PHL}	0.61 0.55	0.67 0.64	0.76 0.76	0.88 0.91	0.96 1.01
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DL632	From: D To: Q	t_{PLH} t_{PHL}	0.62 0.64	0.69 0.74	0.76 0.83	0.83 0.92	0.91 1.01
	From: D To: QN	t_{PLH} t_{PHL}	0.47 0.49	0.55 0.62	0.63 0.72	0.70 0.81	0.78 0.91
	From: GN To: Q	t_{PLH} t_{PHL}	0.68 0.80	0.75 0.89	0.82 0.99	0.89 1.08	0.97 1.18
	From: GN To: QN	t_{PLH} t_{PHL}	0.62 0.55	0.71 0.68	0.78 0.78	0.86 0.87	0.94 0.98
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
DL634	From: D To: Q	t_{PLH} t_{PHL}	0.70 0.77	0.75 0.84	0.82 0.95	0.89 1.04	0.96 1.11
	From: D To: QN	t_{PLH} t_{PHL}	0.51 0.49	0.57 0.60	0.64 0.70	0.70 0.78	0.77 0.86
	From: GN To: Q	t_{PLH} t_{PHL}	0.74 0.90	0.83 1.01	0.90 1.10	0.96 1.18	1.01 1.26
	From: GN To: QN	t_{PLH} t_{PHL}	0.63 0.56	0.70 0.64	0.77 0.74	0.84 0.84	0.92 0.93

	Number of Equivalent Loads		1	14	29	44	58 (max)
DL636	From: D To: Q	t_{PLH} t_{PHL}	0.73 0.75	0.78 0.86	0.84 0.95	0.90 1.03	0.96 1.09
	From: D To: QN	t_{PLH} t_{PHL}	0.54 0.54	0.63 0.67	0.70 0.76	0.77 0.85	0.82 0.93
	From: GN To: Q	t_{PLH} t_{PHL}	0.79 0.92	0.83 1.00	0.89 1.08	0.96 1.17	1.03 1.24
	From: GN To: QN	t_{PLH} t_{PHL}	0.70 0.60	0.77 0.71	0.84 0.79	0.91 0.89	0.97 0.99

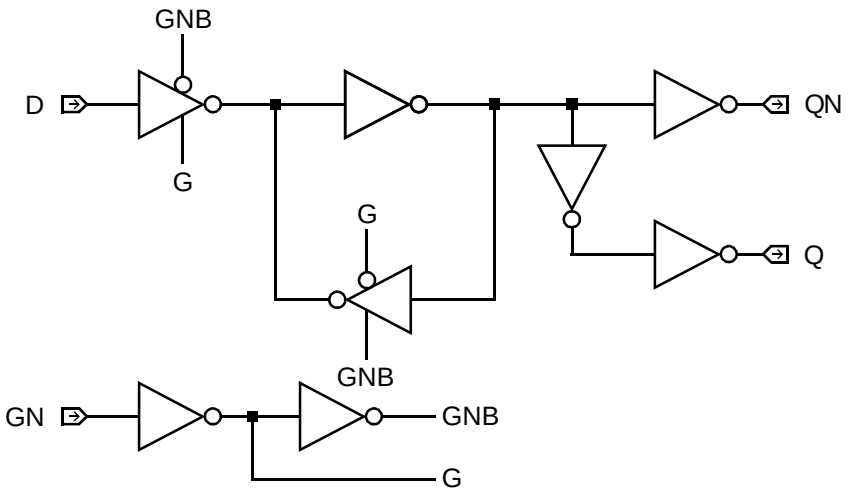
Delay will vary with input conditions. See page 2-Reference for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL631	DL632	DL634	DL636
Min GN Width	Low	t_w	0.52	0.55	0.59	0.64
Min D Setup		t_{su}	0.37	0.40	0.44	0.49
Min D Hold		t_h	0.14	0.14	0.14	0.14

Logic Schematic



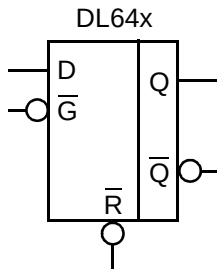
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

DL64x is a family of transparent, buffered D latches with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q	QN
H	L	L	L	H
H	H	L	H	L
H	X	H	NC	NC
L	X	X	L	H

NC = No Change

HDL Syntax

Verilog ..... DL64x *inst_name* (Q, QN, D, GN);

VHDL..... *inst_name*: DL64x port map (Q, QN, D, GN);

Pin Loading

Pin Name	Equivalent Loads			
	DL641	DL642	DL644	DL646
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL641	4.0	TBD	11.3
DL642	4.2	TBD	13.6
DL644	7.0	TBD	25.1
DL646	8.2	TBD	30.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DL641	From: D To: Q	t_{PLH} t_{PHL}	0.44 0.52	0.53 0.63	0.64 0.78	0.77 0.94	0.87 1.05
	From: D To: QN	t_{PLH} t_{PHL}	0.65 0.64	0.72 0.73	0.81 0.85	0.94 1.01	1.03 1.12
	From: GN To: Q	t_{PLH} t_{PHL}	0.50 0.67	0.59 0.79	0.70 0.93	0.83 1.09	0.92 1.20
	From: GN To: QN	t_{PLH} t_{PHL}	0.81 0.71	0.88 0.79	0.97 0.91	1.10 1.07	1.20 1.19
	From: RN To: Q	t_{PLH} t_{PHL}	0.46 0.37	0.55 0.48	0.66 0.62	0.80 0.78	0.90 0.90
	From: RN To: QN	t_{PLH} t_{PHL}	0.52 0.67	0.59 0.76	0.68 0.88	0.81 1.03	0.91 1.15
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DL642	From: D To: Q	t_{PLH} t_{PHL}	0.46 0.53	0.58 0.71	0.67 0.83	0.75 0.95	0.85 1.07
	From: D To: QN	t_{PLH} t_{PHL}	0.76 0.73	0.83 0.84	0.89 0.94	0.96 1.04	1.04 1.15
	From: GN To: Q	t_{PLH} t_{PHL}	0.54 0.70	0.65 0.86	0.74 0.98	0.82 1.08	0.90 1.19
	From: GN To: QN	t_{PLH} t_{PHL}	0.94 0.81	1.01 0.92	1.06 1.01	1.11 1.09	1.16 1.19
	From: RN To: Q	t_{PLH} t_{PHL}	0.48 0.38	0.60 0.53	0.70 0.65	0.78 0.74	0.88 0.85
	From: RN To: QN	t_{PLH} t_{PHL}	0.58 0.77	0.65 0.87	0.72 0.97	0.79 1.05	0.88 1.16

AMI5HS 0.5 micron CMOS Standard Cell

	Number of Equivalent Loads		1	10	20	30	40 (max)
DL644	From: D To: Q	t_{PLH} t_{PHL}	0.72 0.62	0.80 0.74	0.86 0.83	0.91 0.92	0.96 1.00
	From: D To: QN	t_{PLH} t_{PHL}	0.76 0.85	0.82 0.96	0.89 1.04	0.95 1.12	1.00 1.20
	From: GN To: Q	t_{PLH} t_{PHL}	0.76 0.75	0.85 0.87	0.92 0.97	0.98 1.07	1.04 1.17
	From: GN To: QN	t_{PLH} t_{PHL}	0.92 0.92	0.97 0.99	1.02 1.09	1.08 1.18	1.14 1.28
	From: RN To: Q	t_{PLH} t_{PHL}	0.64 0.51	0.70 0.62	0.77 0.72	0.84 0.81	0.92 0.89
	From: RN To: QN	t_{PLH} t_{PHL}	0.64 0.80	0.71 0.87	0.77 0.95	0.82 1.04	0.87 1.14
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
DL646	From: D To: Q	t_{PLH} t_{PHL}	0.74 0.66	0.81 0.74	0.85 0.81	0.89 0.87	0.92 0.92
	From: D To: QN	t_{PLH} t_{PHL}	0.85 0.97	0.89 1.03	0.92 1.08	0.95 1.12	0.98 1.16
	From: GN To: Q	t_{PLH} t_{PHL}	0.82 0.82	0.86 0.89	0.90 0.96	0.94 1.01	0.98 1.07
	From: GN To: QN	t_{PLH} t_{PHL}	0.99 1.03	1.03 1.06	1.06 1.11	1.10 1.17	1.12 1.24
	From: RN To: Q	t_{PLH} t_{PHL}	0.66 0.57	0.72 0.63	0.77 0.71	0.82 0.78	0.86 0.83
	From: RN To: QN	t_{PLH} t_{PHL}	0.72 0.88	0.75 0.94	0.79 1.00	0.83 1.06	0.87 1.12

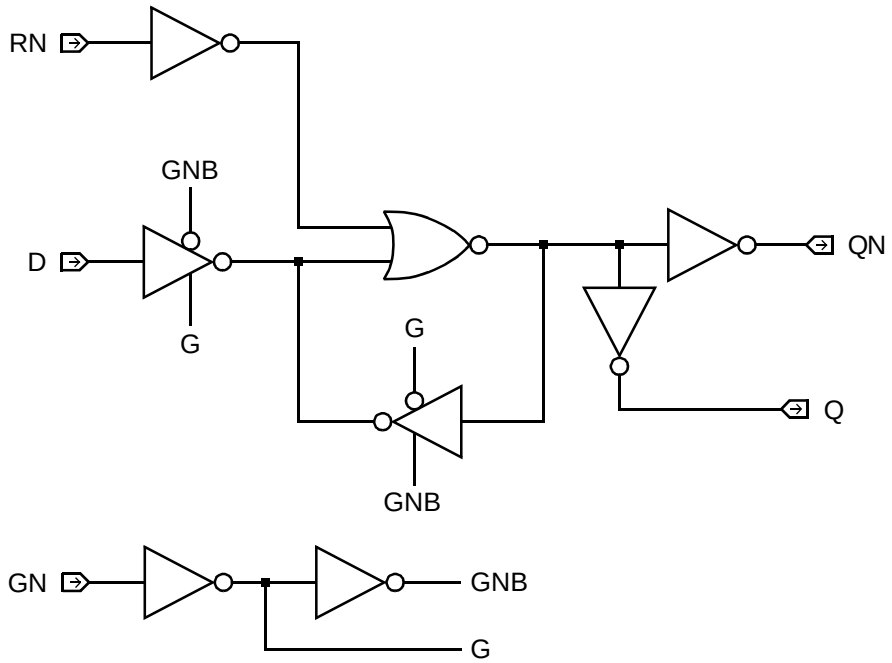
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL641	DL642	DL644	DL646
Min GN Width	Low	t_w	0.53	0.67	0.54	0.54
Min RN Width	Low	t_w	0.40	0.49	0.53	0.53
Min D Setup		t_{su}	0.53	0.67	0.39	0.39
Min D Hold		t_h	0.14	0.14	0.14	0.14
Min RN Setup		t_{su}	0.35	0.41	0.32	0.32
Min RN Hold		t_h	0.21	0.21	0.28	0.28

Logic Schematic



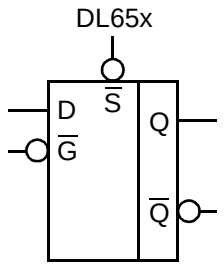
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

DL65x is a family of transparent, buffered D latches with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q	QN
L	X	X	H	L
H	H	X	NC	NC
H	L	L	L	H
H	L	H	H	L

NC = No Change

HDL Syntax

Verilog ..... DL65x *inst_name* (Q, QN, D, GN, SN);

VHDL..... *inst_name*: DL65x port map (Q, QN, D, GN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DL651	DL652	DL654	DL656
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0
SN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL651	4.5	TBD	11.2
DL652	4.7	TBD	13.6
DL654	6.5	TBD	23.3
DL656	7.7	TBD	29.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DL651	From: D To: Q	t_{PLH} t_{PHL}	0.61 0.64	0.67 0.72	0.75 0.84	0.87 0.99	0.96 1.11
	From: D To: QN	t_{PLH} t_{PHL}	0.52 0.54	0.59 0.63	0.68 0.75	0.79 0.90	0.88 1.00
	From: GN To: Q	t_{PLH} t_{PHL}	0.67 0.79	0.73 0.86	0.82 0.97	0.94 1.14	1.03 1.27
	From: GN To: QN	t_{PLH} t_{PHL}	0.67 0.60	0.74 0.69	0.83 0.81	0.94 0.96	1.02 1.06
	From: SN To: Q	t_{PLH} t_{PHL}	0.41 0.45	0.47 0.53	0.56 0.64	0.68 0.79	0.78 0.91
	From: SN To: QN	t_{PLH} t_{PHL}	0.31 0.34	0.39 0.44	0.49 0.56	0.60 0.72	0.68 0.82
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DL652	From: D To: Q	t_{PLH} t_{PHL}	0.68 0.70	0.74 0.80	0.81 0.90	0.88 0.99	0.97 1.10
	From: D To: QN	t_{PLH} t_{PHL}	0.52 0.54	0.61 0.67	0.69 0.77	0.76 0.87	0.84 0.98
	From: GN To: Q	t_{PLH} t_{PHL}	0.74 0.86	0.81 0.96	0.88 1.05	0.96 1.14	1.04 1.23
	From: GN To: QN	t_{PLH} t_{PHL}	0.67 0.60	0.77 0.74	0.85 0.84	0.92 0.93	0.99 1.03
	From: SN To: Q	t_{PLH} t_{PHL}	0.49 0.50	0.55 0.60	0.62 0.69	0.69 0.78	0.76 0.89
	From: SN To: QN	t_{PLH} t_{PHL}	0.32 0.34	0.41 0.48	0.49 0.59	0.56 0.68	0.65 0.78

	Number of Equivalent Loads		1	10	20	30	40 (max)
DL654	From: D To: Q	t_{PLH} t_{PHL}	0.62 0.67	0.68 0.76	0.76 0.86	0.84 0.96	0.92 1.06
	From: D To: QN	t_{PLH} t_{PHL}	0.79 0.77	0.87 0.87	0.93 0.96	0.98 1.05	1.03 1.14
	From: GN To: Q	t_{PLH} t_{PHL}	0.70 0.81	0.77 0.95	0.84 1.04	0.90 1.11	0.97 1.17
	From: GN To: QN	t_{PLH} t_{PHL}	0.94 0.85	0.98 0.92	1.05 1.01	1.12 1.11	1.20 1.21
	From: SN To: Q	t_{PLH} t_{PHL}	0.42 0.46	0.52 0.57	0.59 0.67	0.65 0.75	0.70 0.83
	From: SN To: QN	t_{PLH} t_{PHL}	0.57 0.59	0.64 0.69	0.70 0.77	0.76 0.85	0.81 0.92
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
DL656	From: D To: Q	t_{PLH} t_{PHL}	0.65 0.72	0.72 0.83	0.79 0.92	0.87 1.00	0.94 1.07
	From: D To: QN	t_{PLH} t_{PHL}	0.88 0.86	0.93 0.93	0.99 1.02	1.05 1.11	1.11 1.21
	From: GN To: Q	t_{PLH} t_{PHL}	0.73 0.87	0.81 0.98	0.87 1.07	0.93 1.15	0.98 1.22
	From: GN To: QN	t_{PLH} t_{PHL}	1.06 0.94	1.11 1.01	1.16 1.10	1.20 1.19	1.23 1.27
	From: SN To: Q	t_{PLH} t_{PHL}	0.48 0.50	0.55 0.60	0.61 0.70	0.68 0.79	0.74 0.87
	From: SN To: QN	t_{PLH} t_{PHL}	0.66 0.68	0.73 0.78	0.80 0.86	0.86 0.94	0.91 1.00

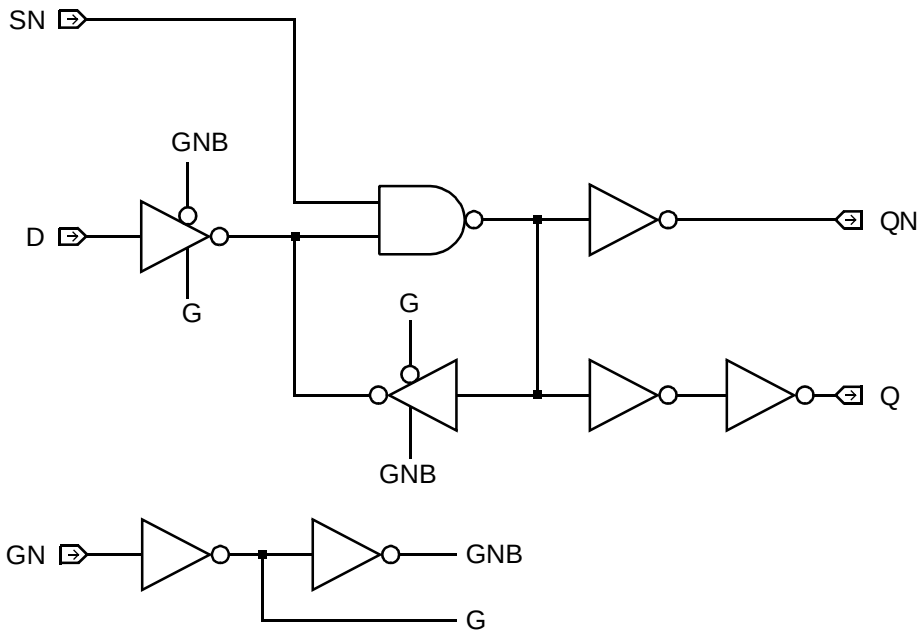
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL651	DL652	DL654	DL656
Min GN Width	Low	t_w	0.57	0.60	0.56	0.56
Min SN Width	Low	t_w	0.54	0.58	0.53	0.52
Min D Setup		t_{su}	0.41	0.45	0.41	0.41
Min D Hold		t_h	0.13	0.13	0.13	0.13
Min SN Setup		t_{su}	0.22	0.25	0.21	0.21
Min SN Hold		t_h	0.48	0.48	0.48	0.48

Logic Schematic



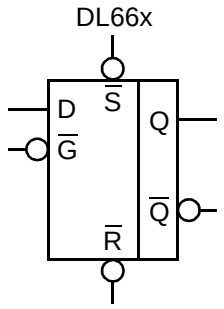
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

DL66x is a family of transparent, buffered D latches with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	X	H	NC	NC
H	H	L	L	L	H
H	H	H	L	H	L

IL = Illegal NC = No Change

HDL Syntax

Verilog ..... DL66x *inst_name* (Q, QN, D, GN, RN, SN);

VHDL..... *inst_name*: DL66x port map (Q, QN, D, GN, RN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DL661	DL662	DL664	DL666
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0
SN	1.0	1.0	2.0	2.0
RN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL661	4.5	TBD	13.3
DL662	5.0	TBD	15.5
DL664	8.5	TBD	30.1
DL666	9.5	TBD	35.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
DL661	From: D To: Q	t_{PLH} t_{PHL}	0.73 0.76	0.79 0.83	0.88 0.94	0.98 1.09	1.06 1.20
	From: D To: QN	t_{PLH} t_{PHL}	0.64 0.67	0.71 0.77	0.80 0.89	0.92 1.04	1.00 1.14
	From: GN To: Q	t_{PLH} t_{PHL}	0.80 0.92	0.85 0.98	0.93 1.08	1.05 1.24	1.14 1.37
	From: GN To: QN	t_{PLH} t_{PHL}	0.80 0.73	0.88 0.81	0.97 0.94	1.08 1.10	1.16 1.21
	From: SN To: Q	t_{PLH} t_{PHL}	0.42 0.44	0.48 0.52	0.56 0.64	0.69 0.79	0.78 0.90
	From: SN To: QN	t_{PLH} t_{PHL}	0.32 0.35	0.40 0.45	0.50 0.58	0.62 0.74	0.70 0.85
	From: R To: Q	t_{PLH} t_{PHL}	0.75 0.67	0.81 0.75	0.90 0.86	1.01 1.00	1.09 1.10
	From: RN To: QN	t_{PLH} t_{PHL}	0.55 0.70	0.61 0.80	0.71 0.92	0.82 1.07	0.91 1.18
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
DL662	From: D To: Q	t_{PLH} t_{PHL}	0.81 0.83	0.87 0.94	0.94 1.03	1.00 1.12	1.08 1.23
	From: D To: QN	t_{PLH} t_{PHL}	0.65 0.67	0.75 0.79	0.82 0.90	0.89 1.00	0.97 1.12
	From: GN To: Q	t_{PLH} t_{PHL}	0.86 1.02	0.92 1.10	0.99 1.18	1.06 1.26	1.15 1.36
	From: GN To: QN	t_{PLH} t_{PHL}	0.82 0.72	0.91 0.85	0.99 0.96	1.06 1.06	1.13 1.17
	From: SN To: Q	t_{PLH} t_{PHL}	0.50 0.53	0.57 0.63	0.64 0.72	0.70 0.81	0.78 0.91
	From: SN To: QN	t_{PLH} t_{PHL}	0.34 0.36	0.44 0.51	0.52 0.61	0.60 0.71	0.68 0.81
	From: RN To: Q	t_{PLH} t_{PHL}	0.83 0.76	0.88 0.85	0.95 0.95	1.01 1.04	1.10 1.14
	From: RN To: QN	t_{PLH} t_{PHL}	0.56 0.69	0.66 0.83	0.74 0.93	0.81 1.02	0.89 1.12

AMI5HS 0.5 micron CMOS Standard Cell

	Number of Equivalent Loads		1	10	20	30	40 (max)
DL664	From: D To: Q	t_{PLH} t_{PHL}	0.73 0.71	0.81 0.80	0.89 0.90	0.95 0.99	1.01 1.07
	From: D To: QN	t_{PLH} t_{PHL}	0.80 0.89	0.88 1.00	0.94 1.09	1.00 1.17	1.06 1.25
	From: GN To: Q	t_{PLH} t_{PHL}	0.80 0.85	0.86 0.95	0.93 1.04	1.00 1.13	1.06 1.21
	From: GN To: QN	t_{PLH} t_{PHL}	0.96 0.97	1.01 1.05	1.08 1.14	1.15 1.21	1.21 1.27
	From: SN To: Q	t_{PLH} t_{PHL}	0.35 0.44	0.42 0.53	0.49 0.62	0.56 0.71	0.62 0.82
	From: SN To: QN	t_{PLH} t_{PHL}	0.54 0.50	0.63 0.60	0.68 0.69	0.74 0.77	0.81 0.84
	From: RN To: Q	t_{PLH} t_{PHL}	0.64 0.54	0.71 0.65	0.79 0.75	0.85 0.84	0.90 0.95
	From: RN To: QN	t_{PLH} t_{PHL}	0.67 0.80	0.74 0.89	0.81 0.96	0.87 1.03	0.94 1.10
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
DL666	From: D To: Q	t_{PLH} t_{PHL}	0.76 0.74	0.82 0.85	0.89 0.94	0.97 1.02	1.04 1.08
	From: D To: QN	t_{PLH} t_{PHL}	0.92 0.97	0.97 1.06	1.03 1.15	1.09 1.24	1.14 1.31
	From: GN To: Q	t_{PLH} t_{PHL}	0.85 0.89	0.92 0.98	0.98 1.08	1.04 1.16	1.08 1.23
	From: GN To: QN	t_{PLH} t_{PHL}	1.04 1.03	1.10 1.10	1.16 1.18	1.22 1.27	1.27 1.36
	From: SN To: Q	t_{PLH} t_{PHL}	0.38 0.46	0.44 0.58	0.51 0.68	0.59 0.77	0.66 0.84
	From: SN To: QN	t_{PLH} t_{PHL}	0.63 0.59	0.70 0.67	0.77 0.76	0.83 0.85	0.87 0.94
	From: RN To: Q	t_{PLH} t_{PHL}	0.65 0.59	0.72 0.69	0.80 0.79	0.86 0.89	0.91 0.99
	From: RN To: QN	t_{PLH} t_{PHL}	0.77 0.87	0.82 0.94	0.89 1.03	0.94 1.12	1.00 1.21

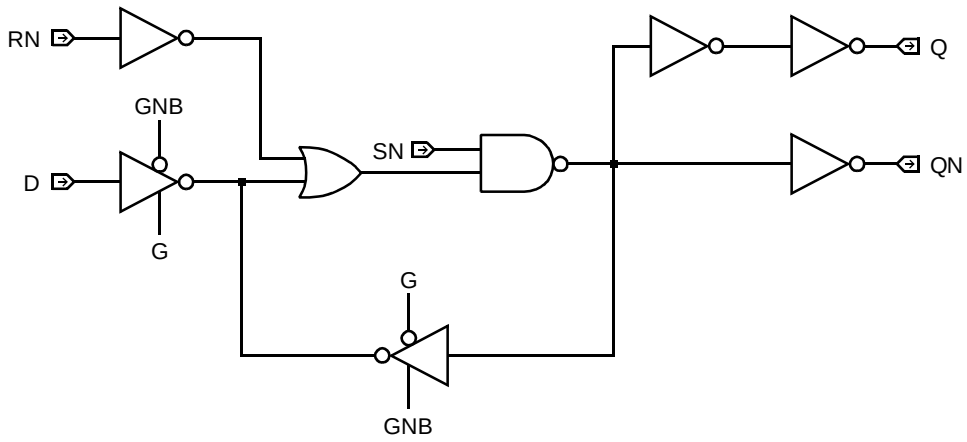
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

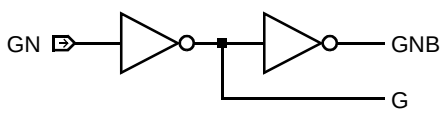
Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL661	DL662	DL664	DL666
Min GN Width	Low	t_w	0.69	0.73	0.59	0.58
Min RN Width	Low	t_w	0.45	0.49	0.31	0.31
Min SN Width	Low	t_w	0.50	0.55	0.60	0.60
Min D Setup		t_{su}	0.53	0.57	0.44	0.44
Min D Hold		t_h	0.14	0.14	0.13	0.13
Min SN Setup		t_{su}	0.22	0.27	0.19	0.19
Min SN Hold		t_h	0.43	0.43	0.56	0.56
Min RN Setup		t_{su}	0.49	0.52	0.34	0.34
Min RN Hold		t_h	0.22	0.21	0.35	0.35

Logic Schematic





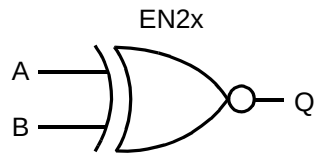
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

EN2x is a family of 2-input gates which perform the logical exclusive NOR (XNOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	H

HDL Syntax

Verilog ..... EN2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: EN2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	EN21	EN22	EN23	EN24	EN26
A	2.0	4.0	4.0	4.0	4.0
B	2.0	4.0	4.0	4.0	4.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
EN21	1.7	TBD	4.0
EN22	3.7	TBD	9.5
EN23	4.7	TBD	13.2
EN24	5.2	TBD	15.5
EN26	6.0	TBD	19.0

a. See page 2-13 for power equation.

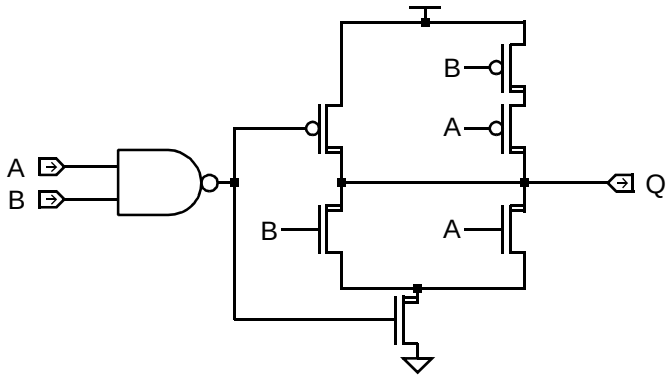
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

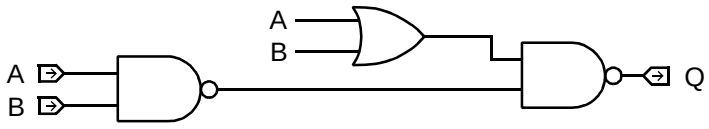
EN21	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.26 0.16	0.29 0.22	0.35 0.33	0.43 0.49	0.49 0.60
EN22	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.24 0.13	0.27 0.20	0.32 0.30	0.38 0.41	0.42 0.49
EN23	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.24 0.44	0.32 0.56	0.40 0.66	0.47 0.76	0.56 0.88
EN24	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.29 0.46	0.37 0.62	0.46 0.75	0.54 0.83	0.61 0.91
EN26	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.35 0.53	0.43 0.67	0.51 0.79	0.58 0.90	0.65 0.99

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



LOGICAL



Core Logic

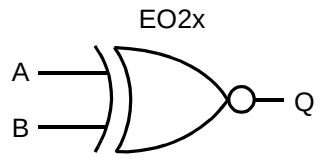
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

EO2x is a family of 2-input gates which perform the logical exclusive OR (XOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	L

HDL Syntax

Verilog ..... EO2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: EO2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	EO21	EO22	EO23	EO24	EO26
A	2.1	4.0	4.0	4.0	4.0
B	2.0	4.0	4.0	4.0	4.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
EO21	1.7	TBD	4.4
EO22	4.0	TBD	9.6
EO23	4.7	TBD	12.8
EO24	5.2	TBD	15.6
EO26	6.0	TBD	18.6

a. See page 2-13 for power equation.

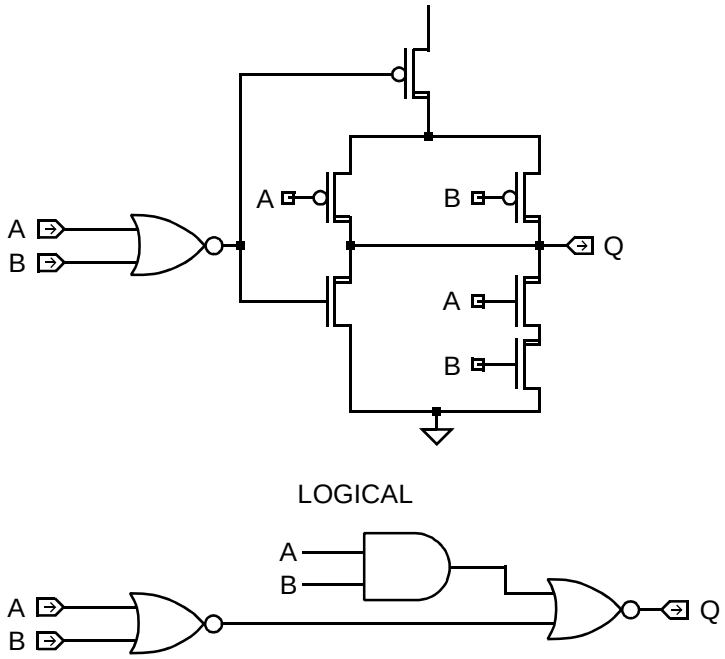
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

EO21	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.30 0.21	0.35 0.27	0.45 0.40	0.60 0.60	0.70 0.73
EO22	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.26 0.17	0.32 0.24	0.40 0.33	0.50 0.44	0.57 0.54
EO23	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.22 0.39	0.31 0.51	0.38 0.61	0.45 0.70	0.54 0.80
EO24	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.24 0.42	0.33 0.54	0.41 0.61	0.48 0.71	0.54 0.82
EO26	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.27 0.46	0.37 0.57	0.46 0.67	0.53 0.77	0.59 0.87

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



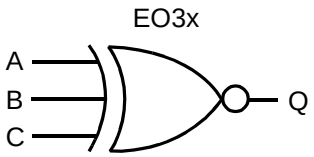
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

EO3x is a family of 3-input gates which perform the logical exclusive OR (XOR) function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

HDL Syntax

Verilog ..... EO3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: EO3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads				
	EO31	EO32	EO33	EO34	EO36
A	2.0	2.0	2.0	2.0	2.0
B	2.0	2.1	2.0	2.0	2.0
C	2.0	3.1	3.0	3.0	3.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
EO31	3.5	TBD	10.6
EO32	5.0	TBD	16.1
EO33	6.0	TBD	18.5
EO34	6.8	TBD	21.4
EO36	7.3	TBD	24.4

a. See page 2-13 for power equation.

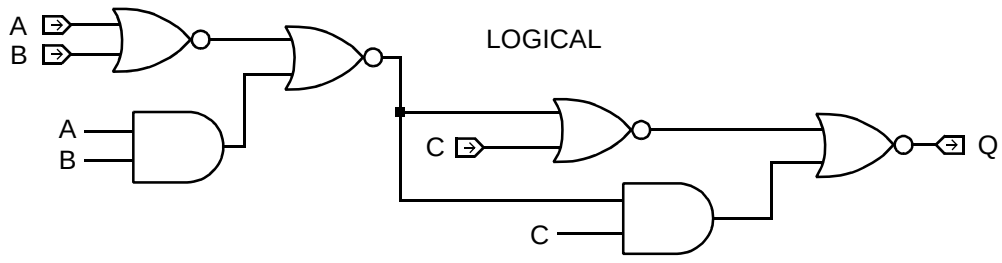
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

EO31	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.69 0.60	0.74 0.67	0.84 0.81	1.00 1.02	1.10 1.17
EO32	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.79 0.72	0.85 0.77	0.92 0.88	1.00 1.02	1.05 1.11
EO33	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.71 0.91	0.81 1.01	0.88 1.10	0.95 1.17	1.03 1.26
EO34	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.78 0.92	0.85 1.05	0.92 1.14	0.99 1.23	1.06 1.33
EO36	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.84 0.98	0.93 1.08	0.99 1.18	1.04 1.26	1.11 1.34

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



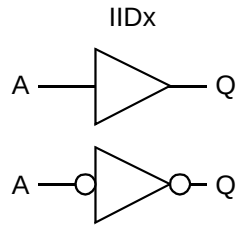
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

IIDx is a family of non-inverting clock drivers with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

HDL Syntax

Verilog ..... IIDx *inst_name* (Q, A);

VHDL..... *inst_name*: IIDx port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads				
	IID1	IID2	IID3	IID4	IID6
A	1.0	1.0	2.0	1.9	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IID1	1.0	TBD	2.5
IID2	1.2	TBD	3.5
IID3	2.0	TBD	5.5
IID4	2.2	TBD	6.6
IID6	2.5	TBD	9.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

IID1	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.20 0.20	0.26 0.28	0.34 0.41	0.46 0.56	0.55 0.67
IID2	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.21 0.23	0.30 0.35	0.38 0.45	0.46 0.55	0.55 0.67
IID3	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.17 0.17	0.25 0.27	0.33 0.37	0.39 0.45	0.46 0.54
IID4	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.21 0.19	0.27 0.29	0.33 0.38	0.39 0.46	0.45 0.54
IID6	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.22 0.20	0.29 0.31	0.35 0.41	0.42 0.50	0.47 0.57

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

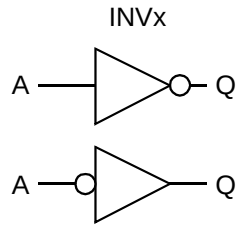
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

INVx is a family of inverters which perform the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

HDL Syntax

Verilog ..... INVx *inst_name* (Q, A);

VHDL..... *inst_name*: INVx port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads					
	INV1	INV2	INV3	INV4	INV5	INV6
A	1.0	1.9	2.9	3.9	4.9	5.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
INV1	0.8	TBD	0.8
INV2	1.0	TBD	1.6
INV3	1.2	TBD	1.7
INV4	1.5	TBD	1.8
INV5	2.0	TBD	2.5
INV6	2.0	TBD	3.0

a. See page 2-13 power equation

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

INV1	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.09 0.14	0.16 0.23	0.24 0.34	0.35 0.47	0.44 0.57
INV2	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.06 0.10	0.15 0.21	0.22 0.30	0.29 0.39	0.37 0.49
INV3	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.05 0.07	0.14 0.18	0.22 0.29	0.27 0.37	0.33 0.46
INV4	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.04 0.07	0.12 0.17	0.19 0.25	0.26 0.34	0.32 0.43
INV5	**Number of Equivalent Loads**		**1**	**12**	**24**	**37**	**49 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.04 0.06	0.12 0.19	0.19 0.29	0.25 0.37	0.30 0.43
INV6	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	0.04 0.05	0.10 0.18	0.17 0.30	0.23 0.38	0.30 0.45

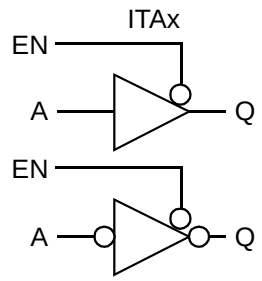
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI5HS 0.5 micron CMOS Standard Cell

Description

ITAx is a family of non-inverting internal tristate buffers with active low enable.

Logic Symbol



Truth Table

EN	A	Q
H	X	Z
L	L	L
L	H	H

Z = High Impedance

HDL Syntax

Verilog ..... ITAx *inst_name* (Q, A, EN);

VHDL..... *inst_name*: ITAx port map (Q, A, EN);

Pin Loading

Pin Name	Equivalent Loads			
	ITA1	ITA2	ITA4	ITA6
A	1.0	1.0	1.0	1.0
EN	1.5	2.1	3.2	4.4
Q	0.7	0.9	1.8	2.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITA1	1.7	TBD	4.2
ITA2	2.0	TBD	6.4
ITA4	3.0	TBD	11.1
ITA6	4.0	TBD	16.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	11	22	32	43 (max)
ITA1	From: A To: Q	t_{PLH} t_{PHL}	0.28 0.28	0.80 0.93	1.39 1.65	1.93 2.32	2.52 3.05
	From: EN To: Q	t_{ZH} t_{ZL}	0.16 0.19	0.72 0.87	1.27 1.59	1.78 2.24	2.35 2.97
	Number of Equivalent Loads		**1**	**17**	**34**	**50**	**67 (max)**
ITA2	From: A To: Q	t_{PLH} t_{PHL}	0.29 0.27	0.70 0.79	1.14 1.34	1.57 1.85	2.03 2.40
	From: EN To: Q	t_{ZH} t_{ZL}	0.14 0.14	0.56 0.68	0.98 1.23	1.39 1.75	1.83 2.29
	Number of Equivalent Loads		**1**	**28**	**57**	**86**	**114 (max)**
ITA4	From: A To: Q	t_{PLH} t_{PHL}	0.31 0.37	0.68 0.80	1.07 1.26	1.46 1.73	1.84 2.19
	From: EN To: Q	t_{ZH} t_{ZL}	0.08 0.16	0.50 0.65	0.85 1.11	1.19 1.57	1.52 2.02
	Number of Equivalent Loads		**1**	**40**	**80**	**121**	**161 (max)**
ITA6	From: A To: Q	t_{PLH} t_{PHL}	0.38 0.43	0.74 0.87	1.09 1.29	1.46 1.73	1.83 2.17
	From: EN To: Q	t_{ZH} t_{ZL}	0.05 0.17	0.50 0.64	0.83 1.07	1.13 1.52	1.42 1.97

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

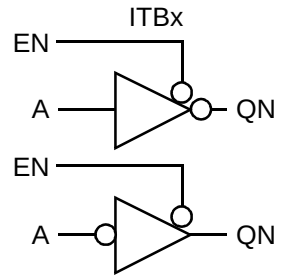
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			ITA1	ITA2	ITA4	ITA6
EN	Q	t_{HZ} t_{LZ}	0.12 0.14	0.12 0.16	0.12 0.22	0.12 0.27

Description

ITBx is a family of inverting internal tristate buffers with active low enable.

Logic Symbol



Truth Table

EN	A	QN
H	X	Z
L	L	H
L	H	L

Z = High Impedance

HDL Syntax

Verilog ..... ITBx *inst_name* (QN, A, EN);

VHDL..... *inst_name*: ITBx port map (QN, A, EN);

Pin Loading

Pin Name	Equivalent Loads			
	ITB1	ITB2	ITB4	ITB6
A	1.0	2.0	4.0	5.9
EN	1.5	2.1	3.2	4.4
QN	0.7	0.9	1.9	2.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITB1	1.2	TBD	2.5
ITB2	1.7	TBD	3.7
ITB4	2.8	TBD	6.5
ITB6	3.7	TBD	9.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	11	22	32	43 (max)
ITB1	From: A To: QN	t_{PLH} t_{PHL}	0.15 0.19	0.71 0.88	1.29 1.59	1.81 2.23	2.39 2.95
	From: EN To: QN	t_{ZH} t_{ZL}	0.17 0.17	0.72 0.85	1.27 1.57	1.78 2.23	2.36 2.96
	Number of Equivalent Loads		**1**	**17**	**34**	**50**	**67 (max)**
ITB2	From: A To: QN	t_{PLH} t_{PHL}	0.13 0.17	0.56 0.71	1.00 1.24	1.42 1.75	1.88 2.32
	From: EN To: QN	t_{ZH} t_{ZL}	0.08 0.15	0.57 0.68	0.99 1.22	1.35 1.74	1.74 2.30
	Number of Equivalent Loads		**1**	**28**	**57**	**86**	**114 (max)**
ITB4	From: A To: QN	t_{PLH} t_{PHL}	0.12 0.13	0.49 0.62	0.85 1.09	1.23 1.55	1.62 2.00
	From: EN To: QN	t_{ZH} t_{ZL}	0.06 0.15	0.54 0.64	0.92 1.13	1.24 1.60	1.51 2.06
	Number of Equivalent Loads		**1**	**40**	**80**	**121**	**161 (max)**
ITB6	From: A To: QN	t_{PLH} t_{PHL}	0.05 0.13	0.49 0.63	0.87 1.08	1.22 1.52	1.53 1.96
	From: EN To: QN	t_{ZH} t_{ZL}	0.12 0.13	0.48 0.63	0.81 1.08	1.15 1.53	1.48 1.96

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

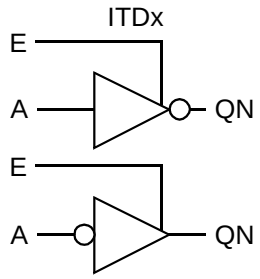
Delay (ns) From	To	Parameter	Cell ITB1	ITB2	ITB4	ITB6
EN	QN	t_{HZ} t_{LZ}	0.12 0.13	0.12 0.16	0.12 0.22	0.12 0.27

AMI5HS 0.5 micron CMOS Standard Cell

Description

ITD1x is a family of inverting internal tristate buffers with active high enable.

Logic Symbol



Truth Table

E	A	QN
L	X	Z
H	L	H
H	H	L

Z = High Impedance

HDL Syntax

Verilog ..... ITDx *inst_name* (QN, A, E);

VHDL..... *inst_name*: ITDx port map (QN, A, E);

Pin Loading

Pin Name	Equivalent Loads			
	ITD1	ITD2	ITD4	ITD6
A	1.0	2.0	4.0	5.9
E	1.4	1.8	2.6	3.5
QN	0.7	0.9	1.9	2.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITD1	1.2	TBD	2.7
ITD2	1.7	TBD	4.0
ITD4	2.8	TBD	7.1
ITD6	3.7	TBD	10.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	11	22	32	43 (max)
ITD1	From: A To: QN	t_{PLH} t_{PHL}	0.15 0.20	0.71 0.89	1.29 1.56	1.81 2.19	2.40 2.93
	From: E To: QN	t_{ZH} t_{ZL}	0.17 0.22	0.72 0.89	1.30 1.56	1.82 2.18	2.42 2.90
	Number of Equivalent Loads		**1**	**17**	**34**	**50**	**67 (max)**
ITD2	From: A To: QN	t_{PLH} t_{PHL}	0.13 0.14	0.57 0.69	1.01 1.23	1.42 1.74	1.87 2.29
	From: E To: QN	t_{ZH} t_{ZL}	0.15 0.08	0.59 0.75	1.03 1.29	1.46 1.78	1.91 2.32
	Number of Equivalent Loads		**1**	**28**	**57**	**86**	**114 (max)**
ITD4	From: A To: QN	t_{PLH} t_{PHL}	0.12 0.13	0.51 0.60	0.88 1.05	1.26 1.52	1.63 1.98
	From: E To: QN	t_{ZH} t_{ZL}	0.15 0.11	0.55 0.64	0.94 1.07	1.32 1.50	1.69 1.94
	Number of Equivalent Loads		**1**	**40**	**80**	**121**	**161 (max)**
ITD6	From: A To: QN	t_{PLH} t_{PHL}	0.10 0.06	0.44 0.61	0.72 1.05	1.00 1.48	1.27 1.89
	From: E To: QN	t_{ZH} t_{ZL}	0.21 0.13	0.58 0.60	0.93 1.00	1.29 1.42	1.64 1.88

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell ITD1	ITD2	ITD4	ITD6
E	QN	t_{HZ} t_{LZ}	0.14 0.07	0.19 0.07	0.29 0.07	0.39 0.07

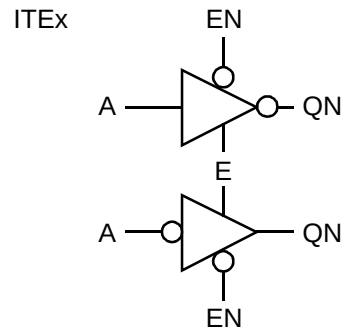
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

ITEx is a family of two-phase inverting internal tristate buffers.

Logic Symbol



Truth Table

EN	E	A	QN
H	L	X	Z
L	H	L	H
L	H	H	L
L	L	X	IL
H	H	X	IL

IL = Illegal

HDL Syntax

Verilog ..... ITEx *inst_name* (QN, A, E, EN);

VHDL..... *inst_name*: ITEx port map (QN, A, E, EN);

Pin Loading

Pin Name	Equivalent Loads			
	ITE1	ITE2	ITE4	ITE6
A	1.0	2.0	3.9	5.9
E	0.4	0.8	1.7	2.5
EN	0.6	1.1	2.3	3.4
QN	0.8	0.9	1.9	2.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITE1	1.0	TBD	1.3
ITE2	1.5	TBD	2.0
ITE4	2.2	TBD	4.1
ITE6	3.2	TBD	6.1

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	11	22	32	43 (max)
ITE1	From: A To: QN	t_{PLH} t_{PHL}	0.15 0.20	0.71 0.86	1.29 1.58	1.81 2.23	2.42 2.95
	From: EN To: QN	t_{ZH}	0.19	0.78	1.37	1.89	2.47
	From: E To: QN	t_{ZL}	0.25	0.94	1.62	2.25	2.97
	Number of Equivalent Loads		**1**	**17**	**34**	**50**	**67 (max)**
ITE2	From: A To: QN	t_{PLH} t_{PHL}	0.10 0.14	0.57 0.68	1.01 1.24	1.43 1.76	1.86 2.30
	From: EN To: QN	t_{ZH}	0.16	0.69	1.11	1.47	1.84
	From: E To: QN	t_{ZL}	0.16	0.76	1.27	1.74	2.24
	Number of Equivalent Loads		**1**	**28**	**57**	**86**	**114 (max)**
ITE4	From: A To: QN	t_{PLH} t_{PHL}	0.10 0.15	0.54 0.59	0.91 1.04	1.25 1.51	1.58 2.01
	From: EN To: QN	t_{ZH}	0.03	0.50	0.92	1.29	1.62
	From: E To: QN	t_{ZL}	0.17	0.67	1.10	1.52	1.93
	Number of Equivalent Loads		**1**	**40**	**80**	**121**	**161 (max)**
ITE6	From: A To: QN	t_{PLH} t_{PHL}	0.07 0.14	0.49 0.62	0.85 1.03	1.19 1.46	1.49 1.92
	From: EN To: QN	t_{ZH}	0.13	0.56	0.88	1.21	1.56
	From: E To: QN	t_{ZL}	0.08	0.63	1.06	1.46	1.84

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

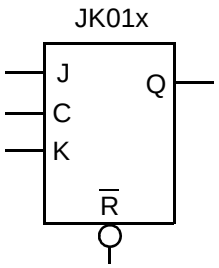
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			ITE1	ITE2	ITE4	ITE6
EN	QN	t_{ZH}	0.12	0.12	0.12	0.12
E	QN	t_{LZ}	0.07	0.07	0.07	0.07

Description

JK01x is a family of static, master-slave JK flip-flops. RESET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	J	K	C	Q(n+1)
L	X	X	X	L
H	L	L	↑	NC
H	L	H	↑	L
H	H	L	↑	H
H	H	H	↑	$\overline{Q(n)}$

NC = No Change

HDL Syntax

Verilog ..... JK01x *inst_name* (Q, C, J, K, RN);

VHDL..... *inst_name*: JK01x port map (Q, C, J, K, RN);

Pin Loading

Pin Name	Equivalent Loads	
	JK011	JK012
J	1.0	1.0
K	1.0	1.0
C	1.0	1.0
RN	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK011	6.5	TBD	22.1
JK012	7.3	TBD	24.9

a. See page 2-13 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	2	4	7	9 (max)
JK011	From: C To: Q	t_{PLH} t_{PHL}	0.72 0.63	0.77 0.69	0.88 0.79	1.05 0.94	1.17 1.04
	From: RN To: Q	t_{PHL}	0.32	0.37	0.45	0.57	0.64
	Number of Equivalent Loads		**1**	**3**	**6**	**10**	**13 (max)**
JK012	From: C To: Q	t_{PLH} t_{PHL}	0.74 0.65	0.79 0.72	0.87 0.80	0.98 0.89	1.06 0.95
	From: RN To: Q	t_{PHL}	0.33	0.38	0.45	0.54	0.60

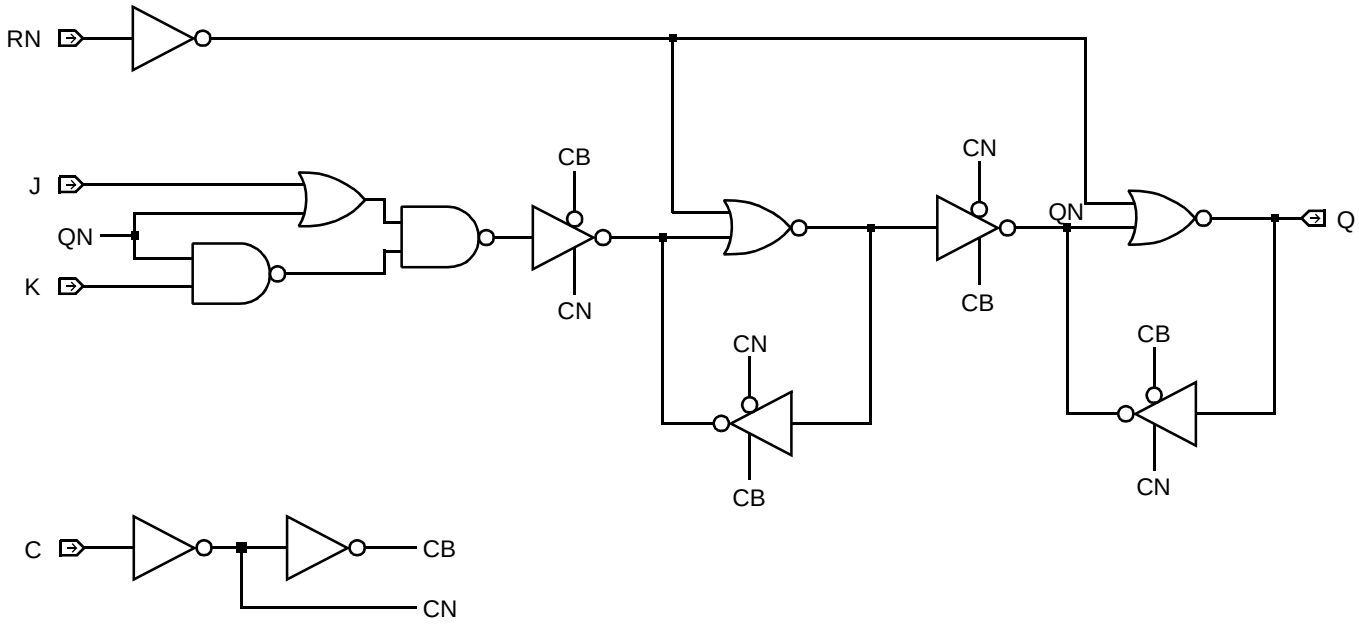
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			JK011	JK012
Min C Width	High	t_w	0.73	0.74
Min C Width	Low	t_w	0.68	0.67
Min RN Width	Low	t_w	0.58	0.63
Min J Setup		t_{su}	0.68	0.67
Min J Hold		t_h	0.17	0.17
Min K Setup		t_{su}	0.56	0.56
Min K Hold		t_h	0.17	0.17
Min RN Setup		t_{su}	0.32	0.36
Min RN Hold		t_h	0.35	0.35

Logic Schematic



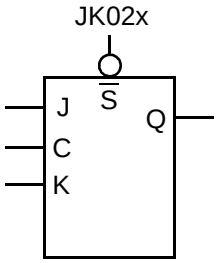
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

JK02x is a family of static, master-slave JK flip-flops. SET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	J	K	C	Q(n+1)
L	X	X	X	H
H	L	L	↑	NC
H	L	H	↑	L
H	H	L	↑	H
H	H	H	↑	$\overline{Q(n)}$

NC = No Change

HDL Syntax

Verilog ..... JK02x *inst_name* (Q, C, J, K, SN);

VHDL..... *inst_name*: JK02x port map (Q, C, J, K, SN);

Pin Loading

Pin Name	Equivalent Loads	
	JK021	JK022
J	1.0	1.0
K	1.0	1.0
C	1.0	1.0
SN	2.1	3.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK021	6.2	TBD	19.3
JK022	6.8	TBD	21.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	2	4	7	9 (max)
JK021	From: C To: Q	t_{PLH} t_{PHL}	0.70 0.63	0.74 0.70	0.82 0.82	0.95 0.99	1.04 1.10
	From: SN To: Q	t_{PLH}	0.13	0.17	0.24	0.35	0.42
	Number of Equivalent Loads		**1**	**3**	**6**	**10**	**13 (max)**
JK022	From: C To: Q	t_{PLH} t_{PHL}	0.71 0.65	0.76 0.72	0.82 0.81	0.89 0.92	0.95 1.00
	From: SN To: Q	t_{PLH}	0.09	0.14	0.20	0.26	0.31

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

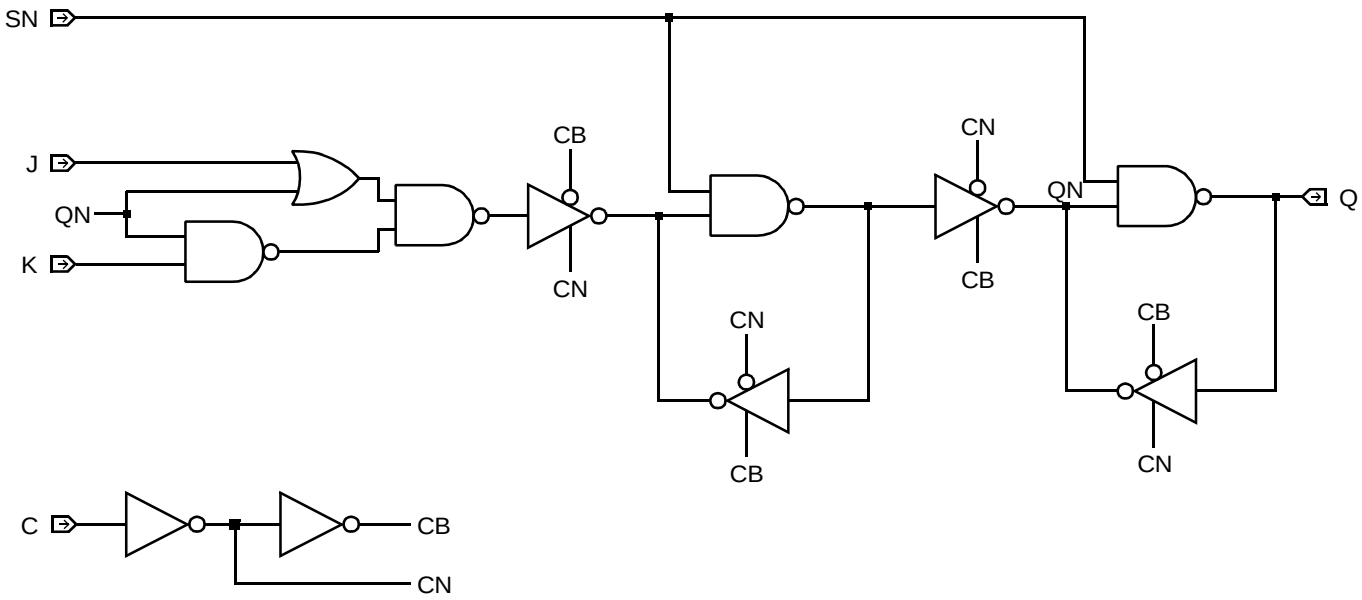
Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			JK021	JK022
Min C Width	High	t_w	0.70	0.72
Min C Width	Low	t_w	0.68	0.67
Min SN Width	Low	t_w	0.91	0.94
Min J Setup		t_{su}	0.68	0.67
Min J Hold		t_h	0.17	0.17
Min K Setup		t_{su}	0.56	0.56
Min K Hold		t_h	0.17	0.17
Min SN Setup		t_{su}	0.17	0.17
Min SN Hold		t_h	0.57	0.57

AMI5HS 0.5 micron CMOS Standard Cell

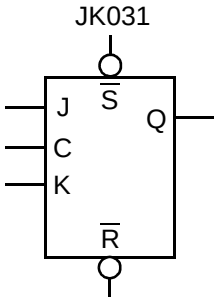
Logic Schematic



Description

JK031 is a static, master-slave JK flip-flop. SET and RESET are asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)
L	L	X	X	X	IL
L	H	X	X	X	L
H	L	X	X	X	H
H	H	L	L	↑	NC
H	H	L	H	↑	L
H	H	H	L	↑	H
H	H	H	H	↑	$\overline{Q(n)}$

IL = Illegal NC = No Change

Pin Loading

	Equivalent Load
J	1.0
K	1.0
C	1.0
SN	2.1
RN	1.0

Core Logic

Equivalent Gates 7.3

HDL Syntax

Verilog ..... JK031 *inst_name* (Q, C, J, K, RN, SN);

VHDL..... *inst_name*: JK031 port map (Q, C, J, K, RN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	24.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.79 0.68	0.87 0.76	1.00 0.89	1.18 1.06	1.29 1.17
RN	Q	t_{PHL}	0.36	0.42	0.55	0.73	0.84
SN	Q	t_{PLH}	0.13	0.17	0.23	0.33	0.39

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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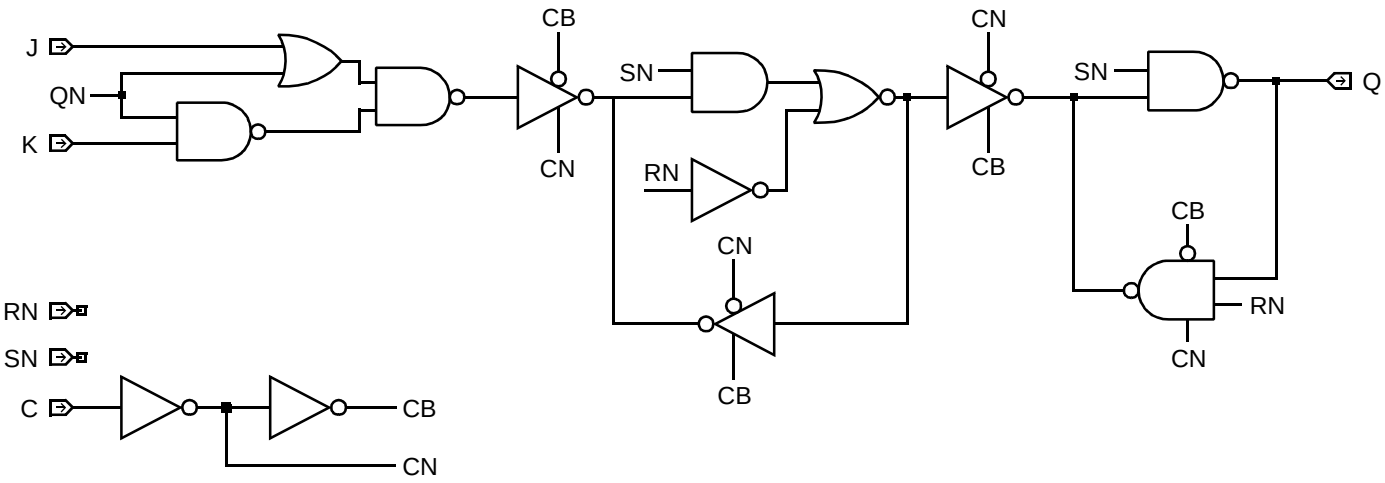
AMI5HS 0.5 micron CMOS Standard Cell

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.78
Min C Width	Low	t_w	0.72
Min RN Width	Low	t_w	0.61
Min SN Width	Low	t_w	0.90
Min J Setup		t_{su}	0.72
Min J Hold		t_h	0.17
Min K Setup		t_{su}	0.61
Min K Hold		t_h	0.17
Min RN Setup		t_{su}	0.37
Min RN Hold		t_h	0.34
Min SN Setup		t_{su}	0.21
Min SN Hold		t_h	0.57

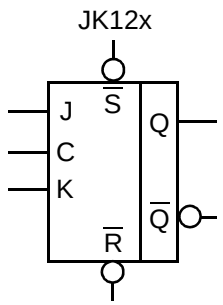
Logic Schematic



Description

JK12x is a family of static, master-slave JK flip-flops. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)	QN(n+1)
L	L	X	X	X	IL	IL
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	L	L	↑	NC	NC
H	H	L	H	↑	L	H
H	H	H	L	↑	H	L
H	H	H	H	↑	QN(n)	Q(n)

IL = Illegal NC = No Change

HDL Syntax

Verilog ..... JK12x *inst_name* (Q, QN, C, J, K, RN, SN);

VHDL..... *inst_name*: JK12x port map (Q, QN, C, J, K, RN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	JK121	JK122	JK124	JK126
J	1.0	1.0	1.0	1.0
K	1.0	1.0	1.0	1.0
C	1.0	1.0	1.0	1.0
SN	2.1	2.1	2.1	2.1
RN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK121	8.2	TBD	27.5
JK122	9.2	TBD	33.6
JK124	10.5	TBD	39.5

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
JK126	11.7	TBD	46.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
JK121	From: C To: Q	t_{PLH} t_{PHL}	0.71 0.67	0.78 0.78	0.89 0.93	1.01 1.11	1.11 1.24
	From: C To: QN	t_{PLH} t_{PHL}	0.85 1.05	0.92 1.15	1.01 1.28	1.10 1.43	1.17 1.53
	From: RN To: Q	t_{PHL}	1.24	1.38	1.55	1.74	1.88
	From: RN To: QN	t_{PLH}	0.45	0.52	0.61	0.73	0.81
	From: SN To: Q	t_{PLH}	0.95	1.04	1.15	1.28	1.37
	From: SN To: QN	t_{PHL}	0.28	0.38	0.51	0.66	0.77
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
JK122	From: C To: Q	t_{PLH} t_{PHL}	1.11 0.95	1.18 1.06	1.25 1.15	1.31 1.23	1.38 1.32
	From: C To: QN	t_{PLH} t_{PHL}	0.62 0.74	0.70 0.84	0.78 0.94	0.85 1.04	0.93 1.16
	From: RN To: Q	t_{PHL}	0.69	0.82	0.92	1.01	1.10
	From: RN To: QN	t_{PLH}	1.11	1.16	1.22	1.28	1.36
	From: SN To: Q	t_{PLH}	0.45	0.54	0.62	0.68	0.76
	From: SN To: QN	t_{PHL}	0.89	0.99	1.07	1.15	1.24

	Number of Equivalent Loads		1	10	20	30	40 (max)
JK124	From: C To: Q	t_{PLH} t_{PHL}	1.20 0.98	1.29 1.13	1.35 1.23	1.40 1.33	1.44 1.43
	From: C To: QN	t_{PLH} t_{PHL}	0.71 0.81	0.76 0.96	0.84 1.05	0.91 1.13	0.97 1.19
	From: RN To: Q	t_{PHL}	0.72	0.90	1.01	1.11	1.19
	From: RN To: QN	t_{PLH}	1.21	1.29	1.34	1.39	1.42
	From: SN To: Q	t_{PLH}	0.49	0.59	0.67	0.74	0.81
	From: SN To: QN	t_{PHL}	0.98	1.06	1.15	1.25	1.34
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
JK126	From: C To: Q	t_{PLH} t_{PHL}	1.36 1.14	1.45 1.28	1.51 1.39	1.56 1.49	1.60 1.60
	From: C To: QN	t_{PLH} t_{PHL}	0.82 0.98	0.89 1.10	0.96 1.19	1.02 1.27	1.07 1.34
	From: RN To: Q	t_{PHL}	0.87	1.03	1.14	1.23	1.31
	From: RN To: QN	t_{PLH}	1.09	1.17	1.23	1.28	1.32
	From: SN To: Q	t_{PLH}	0.63	0.70	0.78	0.85	0.92
	From: SN To: QN	t_{PHL}	0.86	0.98	1.09	1.19	1.28

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMERICAN MICROSYSTEMS, INC.

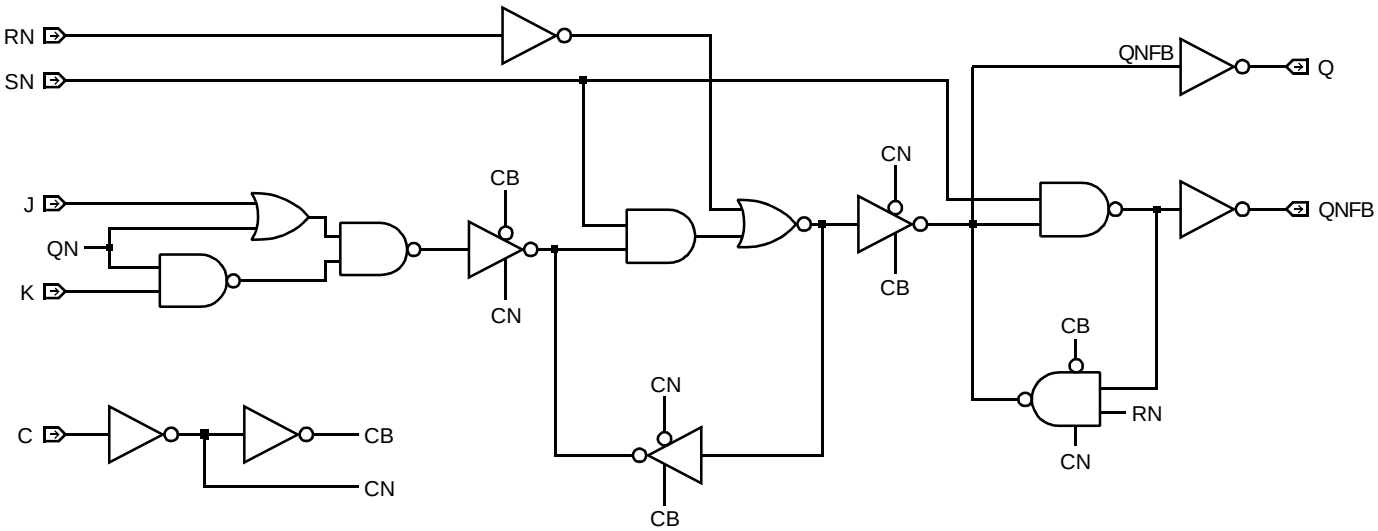
AMI5HS 0.5 micron CMOS Standard Cell

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			JK121	JK122	JK124	JK126
Min C Width	High	t_w	0.83	0.71	0.71	0.79
Min C Width	Low	t_w	0.72	0.72	0.72	0.72
Min RN Width	Low	t_w	0.61	0.61	0.61	0.61
Min SN Width	Low	t_w	0.79	0.59	0.59	0.48
Min J Setup		t_{su}	0.72	0.72	0.72	0.72
Min J Hold		t_h	0.17	0.17	0.17	0.18
Min K Setup		t_{su}	0.61	0.60	0.60	0.61
Min K Hold		t_h	0.17	0.17	0.17	0.18
Min RN Setup		t_{su}	0.37	0.37	0.38	0.37
Min RN Hold		t_h	0.34	0.34	0.34	0.35
Min SN Setup		t_{su}	0.21	0.21	0.21	0.21
Min SN Hold		t_h	0.56	0.57	0.57	0.58

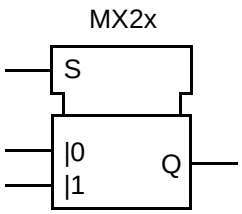
Logic Schematic



Description

MX2x is a family of two-to-one digital multiplexers.

Logic Symbol



Truth Table

S	I0	I1	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

HDL Syntax

Verilog ..... MX2x *inst_name* (Q, I0, I1, S);

VHDL..... *inst_name*: MX2x port map (Q, I0, I1, S);

Pin Loading

Pin Name	Equivalent Loads			
	MX21	MX22	MX24	MX26
I0	1.0	1.0	2.0	2.0
I1	1.0	1.0	2.0	2.0
S	1.5	1.5	4.0	4.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MX21	2.0	TBD	5.2
MX22	2.2	TBD	6.3
MX24	4.2	TBD	12.7
MX26	4.7	TBD	15.6

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

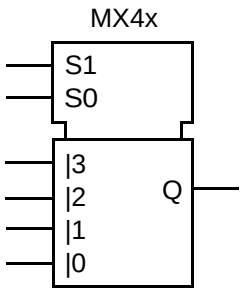
	Number of Equivalent Loads		1	3	6	10	13 (max)
MX21	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.30 0.33	0.38 0.43	0.48 0.56	0.60 0.72	0.69 0.84
	From: S To: Q	t_{PLH} t_{PHL}	0.42 0.50	0.49 0.59	0.58 0.71	0.69 0.86	0.77 0.98
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
MX22	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.34 0.36	0.45 0.50	0.53 0.62	0.60 0.72	0.68 0.84
	From: S To: Q	t_{PLH} t_{PHL}	0.44 0.52	0.54 0.66	0.62 0.77	0.69 0.87	0.78 0.98
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
MX24	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.32 0.35	0.40 0.50	0.48 0.60	0.54 0.68	0.61 0.76
	From: S To: Q	t_{PLH} t_{PHL}	0.36 0.43	0.44 0.57	0.51 0.68	0.59 0.78	0.68 0.88
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
MX26	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.37 0.39	0.46 0.52	0.54 0.62	0.61 0.73	0.69 0.83
	From: S To: Q	t_{PLH} t_{PHL}	0.41 0.51	0.48 0.66	0.56 0.78	0.64 0.87	0.72 0.96

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

MX4x is a family of four-to-one digital multiplexers.

Logic Symbol



Truth Table

I0	I1	I2	I3	S1	S0	Q
L	X	X	X	L	L	L
H	X	X	X	L	L	H
X	L	X	X	L	H	L
X	H	X	X	L	H	H
X	X	L	X	H	L	L
X	X	H	X	H	L	H
X	X	X	L	H	H	L
X	X	X	H	H	H	H

HDL Syntax

Verilog ..... MX4x *inst_name* (Q, I0, I1, I2, I3, S0, S1);

VHDL..... *inst_name*: MX4x port map (Q, I0, I1, I2, I3, S0, S1);

Pin Loading

Pin Name	Equivalent Loads			
	MX41	MX42	MX44	MX46
I0	1.1	1.0	1.0	1.0
I1	1.1	1.0	1.0	1.0
I2	1.0	1.0	1.0	1.0
I3	1.0	1.0	1.0	1.0
S0	3.2	3.2	3.2	3.3
S1	3.2	2.1	2.2	2.2

AMI5HS 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MX41	4.2	TBD	14.1
MX42	5.7	TBD	19.3
MX44	7.0	TBD	25.2
MX46	7.5	TBD	28.0

a. See page 2-13 for power equation.

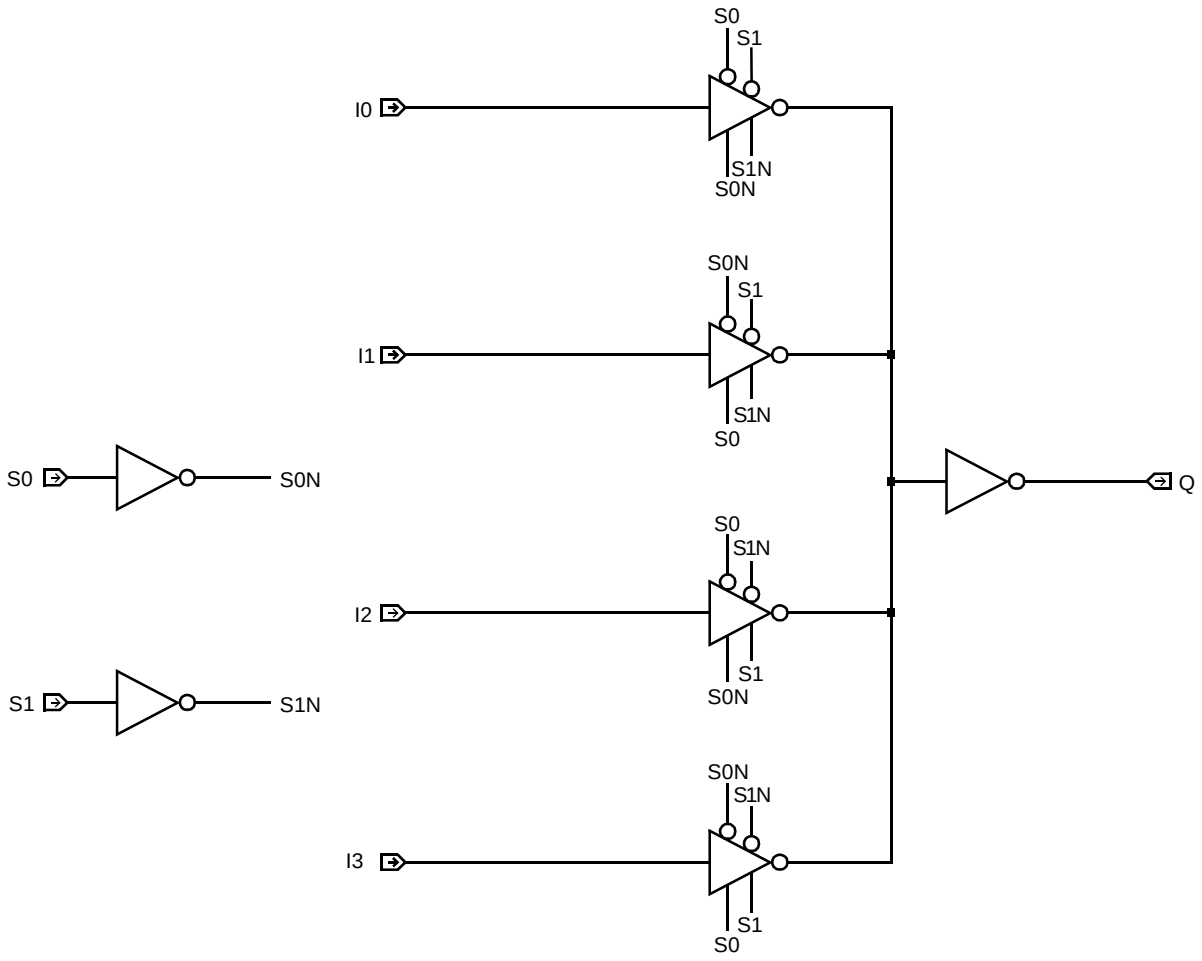
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
MX41	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.66 0.71	0.75 0.84	0.85 1.00	0.97 1.19	1.05 1.31
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.77 0.87	0.85 1.00	0.95 1.16	1.08 1.33	1.16 1.46
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
MX42	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.60 0.62	0.70 0.73	0.78 0.83	0.84 0.93	0.91 1.03
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.70 0.80	0.78 0.92	0.86 1.01	0.92 1.10	1.00 1.19
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
MX44	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.63 0.63	0.72 0.76	0.79 0.86	0.86 0.95	0.93 1.03
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.76 0.83	0.84 0.97	0.91 1.08	0.97 1.16	1.03 1.21
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
MX46	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.68 0.71	0.78 0.81	0.85 0.91	0.92 1.00	0.98 1.09
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.79 0.91	0.88 1.02	0.95 1.11	1.01 1.19	1.07 1.25

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



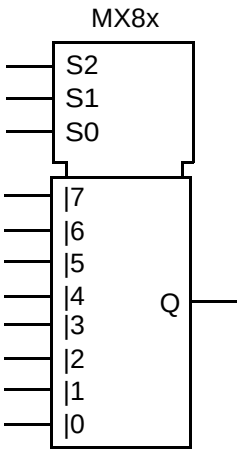
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

MX8x is a family of eight-to-one digital multiplexers.

Logic Symbol



Truth Table

S2	S1	S0	Q
L	L	L	I0
L	L	H	I1
L	H	L	I2
L	H	H	I3
H	L	L	I4
H	L	H	I5
H	H	L	I6
H	H	H	I7

HDL Syntax

Verilog ..... MX8x *inst_name* (Q, I0, I1, I2, I3, I4, I5, I6, I7, S0, S1, S2);

VHDL..... *inst_name*: MX8x port map (Q, I0, I1, I2, I3, I4, I5, I6, I7, S0, S1, S2);

Pin Loading

Pin Name	Equivalent Loads			
	MX81	MX82	MX84	MX86
I0	1.0	1.0	1.0	1.0
I1	1.0	1.0	1.0	1.0
I2	1.0	1.0	1.0	1.0
I3	1.1	1.1	1.1	1.1
I4	1.0	1.0	1.0	1.0
I5	1.0	1.0	1.0	1.0
I6	1.0	1.0	1.0	1.0
I7	1.0	1.0	1.0	1.0
S0	5.4	5.5	5.5	5.5
S1	3.2	3.3	3.3	3.3
S2	2.1	2.2	3.2	3.2

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MX81	9.2	TBD	33.1
MX82	11.2	TBD	43.3
MX84	10.5	TBD	42.1
MX86	11.2	TBD	45.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

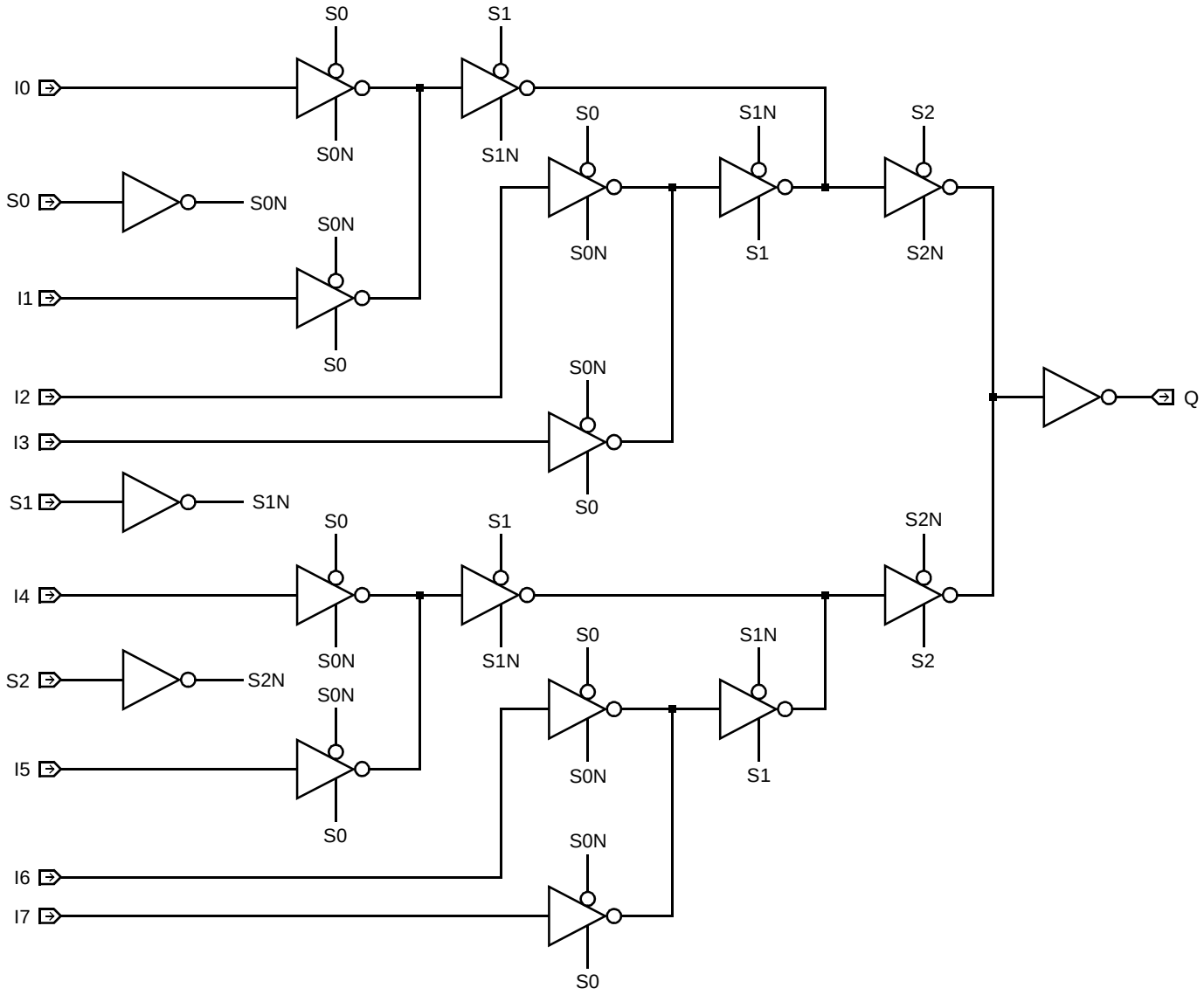
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
MX81	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.80 0.83	0.87 0.93	0.97 1.07	1.10 1.25	1.18 1.37
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.99 1.06	1.07 1.14	1.17 1.27	1.28 1.47	1.36 1.62
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
MX82	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.84 0.85	0.89 0.91	0.93 0.97	0.96 1.03	1.00 1.09
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	1.03 1.08	1.08 1.13	1.11 1.19	1.15 1.25	1.19 1.33
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
MX84	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.88 0.88	0.98 0.97	1.06 1.08	1.12 1.19	1.17 1.30
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	1.10 1.10	1.17 1.24	1.25 1.33	1.31 1.42	1.38 1.53
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
MX86	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.93 0.96	1.05 1.10	1.12 1.20	1.17 1.28	1.22 1.36
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	1.15 1.18	1.22 1.35	1.29 1.46	1.37 1.53	1.43 1.59

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI5HS 0.5 micron CMOS Standard Cell

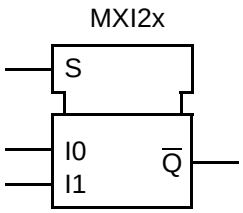
Logic Schematic



Description

MXI2x is a family of inverting two-to-one digital multiplexers.

Logic Symbol



Truth Table

S	I0	I1	QN
L	L	X	H
L	H	X	L
H	X	L	H
H	X	H	L

HDL Syntax

Verilog ..... MXI2x *inst_name* (QN, I0, I1, S);

VHDL..... *inst_name*: MXI2x port map (QN, I0, I1, S);

Pin Loading

Pin Name	Equivalent Loads			
	MXI21	MXI22	MXI24	MXI26
I0	1.0	1.0	1.0	1.0
I1	1.0	1.0	1.0	1.0
S	1.5	1.5	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MXI21	2.5	TBD	6.7
MXI22	2.8	TBD	7.9
MXI24	4.0	TBD	12.7
MXI26	5.0	TBD	18.7

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

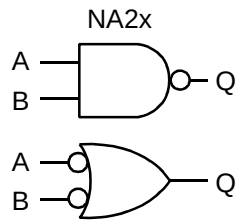
	Number of Equivalent Loads		1	3	6	10	13 (max)
MXI21	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.39 0.43	0.46 0.52	0.55 0.64	0.68 0.80	0.77 0.92
	From: S To: QN	t_{PLH} t_{PHL}	0.56 0.54	0.62 0.62	0.72 0.74	0.83 0.89	0.91 1.00
	Number of Equivalent Loads		**1**	**6**	**11**	**16**	**22 (max)**
MXI22	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.42 0.45	0.51 0.57	0.58 0.67	0.65 0.76	0.74 0.87
	From: S To: QN	t_{PLH} t_{PHL}	0.57 0.55	0.66 0.67	0.73 0.77	0.80 0.86	0.88 0.97
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
MXI24	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.41 0.50	0.50 0.61	0.58 0.72	0.66 0.82	0.73 0.92
	From: S To: QN	t_{PLH} t_{PHL}	0.56 0.57	0.66 0.68	0.73 0.79	0.80 0.89	0.87 0.98
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
MXI26	From: Any Ix Input To: QN	t_{PLH} t_{PHL}	0.40 0.48	0.49 0.60	0.57 0.69	0.64 0.77	0.71 0.84
	From: S To: QN	t_{PLH} t_{PHL}	0.57 0.53	0.66 0.64	0.72 0.75	0.78 0.85	0.84 0.93

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

NA2x is a family of 2-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	H
H	L	H
H	H	L

HDL Syntax

Verilog ..... NA2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: NA2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	NA21	NA22	NA23	NA24	NA26
A	1.0	2.0	3.9	2.0	2.0
B	1.0	1.9	3.9	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA21	1.0	TBD	1.1
NA22	1.5	TBD	2.4
NA23	3.2	TBD	5.2
NA24	4.0	TBD	11.6
NA26	4.2	TBD	14.2

a. See page 2-13 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

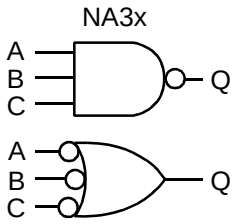
NA21	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.10 0.14	0.14 0.20	0.21 0.32	0.31 0.48	0.38 0.58
NA22	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.07 0.11	0.12 0.18	0.18 0.27	0.25 0.38	0.29 0.45
NA23	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.07 0.10	0.13 0.16	0.17 0.23	0.21 0.28	0.26 0.35
NA24	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.27 0.33	0.35 0.43	0.42 0.52	0.49 0.62	0.55 0.71
NA26	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.30 0.40	0.38 0.49	0.45 0.55	0.51 0.64	0.57 0.74

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

NA3x is a family of 3-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

HDL Syntax

Verilog ..... NA3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: NA3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads				
	NA31	NA32	NA33	NA34	NA36
A	1.0	1.9	2.0	2.0	2.0
B	1.0	1.9	2.0	1.9	2.0
C	1.0	2.0	2.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA31	1.2	TBD	1.7
NA32	2.2	TBD	3.2
NA33	3.7	TBD	9.0
NA34	4.5	TBD	13.0
NA36	5.2	TBD	15.9

a. See page 2-13 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

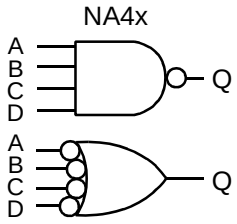
NA31	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.13 0.21	0.17 0.29	0.25 0.44	0.29 0.51	0.36 0.64
NA32	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.10 0.16	0.12 0.19	0.18 0.28	0.24 0.37	0.27 0.44
NA33	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.29 0.37	0.38 0.48	0.45 0.58	0.52 0.67	0.60 0.77
NA34	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.31 0.40	0.38 0.51	0.45 0.60	0.52 0.69	0.59 0.78
NA36	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.35 0.44	0.42 0.53	0.49 0.62	0.56 0.71	0.61 0.79

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

NA4x is a family of 4-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

HDL Syntax

Verilog ..... NA4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: NA4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads				
	NA41	NA42	NA43	NA44	NA46
A	1.0	2.0	1.9	1.9	1.9
B	1.0	2.0	1.9	1.9	1.9
C	1.0	2.0	1.9	1.9	1.9
D	1.0	2.1	1.9	1.9	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA41	1.5	TBD	2.3
NA42	2.8	TBD	3.9
NA43	4.7	TBD	10.7
NA44	5.2	TBD	14.5
NA46	6.0	TBD	17.6

a. See page 2-13 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

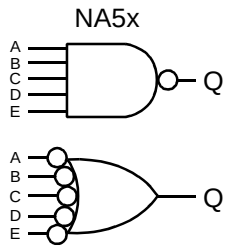
NA41	**Number of Equivalent Loads**		**1**	**2**	**3**	**4**	**6 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.15 0.23	0.20 0.30	0.25 0.36	0.29 0.43	0.37 0.56
NA42	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.11 0.17	0.14 0.21	0.19 0.28	0.25 0.38	0.29 0.45
NA43	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.32 0.41	0.41 0.52	0.49 0.62	0.56 0.71	0.63 0.82
NA44	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.34 0.44	0.41 0.55	0.48 0.63	0.54 0.71	0.61 0.79
NA46	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.38 0.47	0.45 0.59	0.51 0.68	0.57 0.76	0.64 0.83

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

NA5x is a family of 5-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

HDL Syntax

Verilog ..... NA5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: NA5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads				
	NA51	NA52	NA53	NA54	NA56
A	1.0	1.0	2.0	2.0	2.0
B	1.0	1.0	2.0	2.0	2.0
C	1.0	1.0	2.0	2.0	2.0
D	1.0	1.0	2.0	1.9	1.9
E	1.0	1.0	1.9	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA51	2.0	TBD	2.8
NA52	3.2	TBD	7.6
NA53	6.0	TBD	13.5
NA54	7.3	TBD	20.2
NA56	7.7	TBD	23.0

a. See page 2-13 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

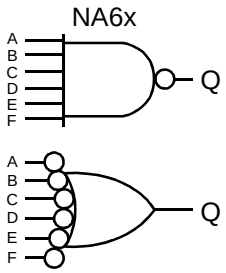
NA51	**Number of Equivalent Loads**		**1**	**2**	**3**	**4**	**6 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.16 0.24	0.22 0.33	0.27 0.40	0.32 0.48	0.41 0.65
NA52	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.33 0.43	0.40 0.52	0.50 0.65	0.62 0.80	0.70 0.91
NA53	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.31 0.45	0.40 0.57	0.47 0.68	0.54 0.77	0.62 0.88
NA54	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.33 0.48	0.40 0.59	0.47 0.68	0.53 0.78	0.60 0.89
NA56	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.57	0.43 0.68	0.50 0.77	0.57 0.87	0.63 0.95

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

NA6x is a family of 6-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
X	X	X	X	L	X	H
X	X	X	X	X	L	H
H	H	H	H	H	H	L

HDL Syntax

Verilog ..... NA6x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: NA6x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads				
	NA61	NA62	NA63	NA64	NA66
A	1.0	2.0	2.0	2.0	1.9
B	1.0	2.0	1.9	2.0	2.0
C	1.0	1.9	1.9	1.9	1.9
D	1.0	1.9	1.9	1.9	1.9
E	1.0	1.9	1.9	1.9	1.9
F	1.0	1.9	1.9	1.9	1.9

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AMI5HS 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA61	3.2	TBD	8.4
NA62	7.3	TBD	18.6
NA63	7.7	TBD	20.2
NA64	7.7	TBD	21.4
NA66	8.5	TBD	24.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

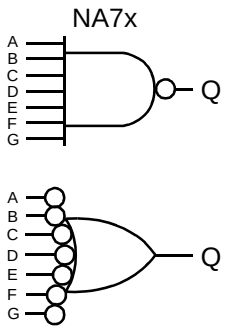
NA61	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.34 0.46	0.40 0.54	0.50 0.66	0.62 0.82	0.70 0.94
NA62	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.29 0.42	0.37 0.54	0.45 0.64	0.52 0.73	0.61 0.84
NA63	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.31 0.44	0.39 0.57	0.47 0.68	0.53 0.76	0.59 0.85
NA64	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.33 0.47	0.41 0.59	0.48 0.70	0.55 0.80	0.62 0.91
NA66	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.52	0.42 0.67	0.49 0.79	0.57 0.89	0.64 0.97

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

NA7x is a family of 7-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	X	X	X	X	X	X	H
X	L	X	X	X	X	X	H
X	X	L	X	X	X	X	H
X	X	X	L	X	X	X	H
X	X	X	X	L	X	X	H
X	X	X	X	X	L	X	H
X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	L

HDL Syntax

Verilog ..... NA7x *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: NA7x port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads				
	NA71	NA72	NA73	NA74	NA76
A	1.9	1.9	1.9	1.9	1.9
B	1.9	1.9	1.9	1.9	1.9
C	1.9	1.9	1.9	1.9	1.9
D	2.0	2.0	2.0	2.0	2.0
E	2.0	2.0	2.0	2.0	2.0
F	2.0	2.0	2.0	2.0	2.0
G	2.0	2.0	2.0	2.0	2.0

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA71	7.7	TBD	17.2
NA72	9.0	TBD	24.1
NA73	9.5	TBD	25.8
NA74	9.8	TBD	27.0
NA76	10.2	TBD	29.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

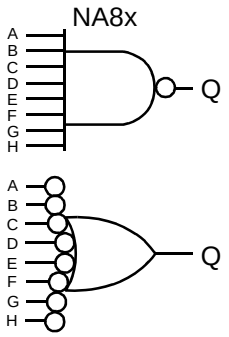
NA71	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.37 0.59	0.43 0.70	0.52 0.83	0.65 0.99	0.74 1.11
NA72	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.37 0.60	0.45 0.74	0.53 0.85	0.60 0.95	0.69 1.06
NA73	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.37 0.65	0.47 0.80	0.55 0.92	0.61 1.01	0.68 1.11
NA74	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.68	0.47 0.85	0.55 0.96	0.62 1.06	0.68 1.15
NA76	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.44 0.82	0.53 0.95	0.60 1.07	0.66 1.18	0.71 1.28

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

NA8x is a family of 8-input gates which perform the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

HDL Syntax

Verilog ..... NA8x *inst_name* (Q, A, B, C, D, E, F, G, H);

VHDL..... *inst_name*: NA8x port map (Q, A, B, C, D, E, F, G, H);

Pin Loading

Pin Name	Equivalent Loads				
	NA81	NA82	NA83	NA84	NA86
A	1.0	1.9	1.9	1.9	1.9
B	1.0	1.9	1.9	1.9	1.9
C	1.0	1.9	1.9	1.9	1.9
D	1.0	2.0	1.9	1.9	1.9
E	1.0	1.9	1.9	1.9	1.9
F	1.0	1.9	2.0	2.0	2.0
G	1.0	2.0	2.0	2.0	2.0
H	1.0	2.0	2.0	2.0	2.0

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NA81	4.0	TBD	9.3
NA82	9.8	TBD	25.5
NA83	10.0	TBD	27.2
NA84	10.2	TBD	28.3
NA86	10.8	TBD	31.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

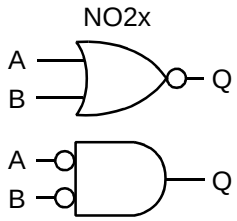
NA81	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.37 0.48	0.44 0.58	0.53 0.71	0.65 0.86	0.73 0.97
NA82	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.37 0.59	0.46 0.73	0.54 0.84	0.61 0.94	0.69 1.05
NA83	**Number of Equivalent Loads**		**1**	**8**	**16**	**23**	**31 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.38 0.64	0.47 0.79	0.54 0.91	0.61 0.99	0.67 1.08
NA84	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.68	0.49 0.82	0.56 0.91	0.63 1.02	0.68 1.17
NA86	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.44 0.76	0.51 0.91	0.59 1.04	0.66 1.15	0.72 1.25

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

NO2x is a family of 2-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	L

HDL Syntax

Verilog ..... NO2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: NO2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	NO21	NO22	NO23	NO24	NO26
A	1.0	2.0	3.9	2.0	2.0
B	1.0	2.0	3.9	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NO21	1.0	TBD	1.2
NO22	1.5	TBD	1.9
NO23	2.8	TBD	5.3
NO24	3.7	TBD	11.5
NO26	4.2	TBD	14.4

a. See page 2-13 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

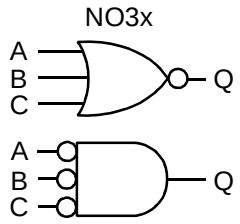
NO21	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.13 0.12	0.19 0.18	0.30 0.27	0.46 0.40	0.56 0.48
NO22	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.10 0.11	0.16 0.16	0.23 0.22	0.34 0.30	0.42 0.36
NO23	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.08 0.10	0.14 0.16	0.20 0.21	0.26 0.25	0.34 0.31
NO24	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.33 0.29	0.41 0.39	0.47 0.49	0.54 0.58	0.59 0.66
NO26	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.34 0.34	0.42 0.44	0.50 0.53	0.57 0.61	0.62 0.69

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

NO3x is a family of 3-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

HDL Syntax

Verilog ..... NO3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: NO3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads				
	NO31	NO32	NO33	NO34	NO36
A	1.0	2.0	2.0	2.0	2.0
B	1.0	2.0	2.0	2.0	2.0
C	1.0	2.0	2.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NO31	1.2	TBD	2.0
NO32	2.2	TBD	3.1
NO33	3.7	TBD	9.6
NO34	4.5	TBD	13.7
NO36	5.2	TBD	16.5

a. See page 2-13 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

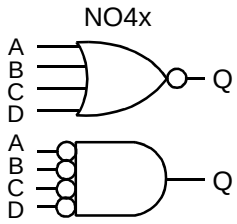
NO31	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.17 0.17	0.24 0.22	0.38 0.30	0.44 0.34	0.58 0.42
NO32	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.11 0.13	0.15 0.16	0.26 0.23	0.35 0.29	0.42 0.33
NO33	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.35 0.32	0.43 0.43	0.51 0.53	0.58 0.62	0.65 0.72
NO34	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.41 0.41	0.47 0.55	0.53 0.65	0.59 0.74	0.67 0.82
NO36	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.41 0.34	0.50 0.46	0.58 0.55	0.64 0.64	0.68 0.71

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

NO4x is a family of 4-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

HDL Syntax

Verilog ..... NO4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: NO4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads				
	NO41	NO42	NO43	NO44	NO46
A	1.0	1.0	2.0	2.0	2.0
B	1.0	1.0	2.0	2.0	2.0
C	1.0	1.0	2.0	2.0	2.0
D	1.0	1.0	2.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
NO41	1.5	TBD	2.4
NO42	2.8	TBD	7.3
NO43	4.2	TBD	11.2
NO44	5.0	TBD	15.0
NO46	5.7	TBD	18.1

a. See page 2-13 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

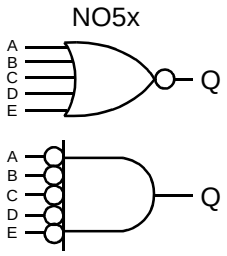
NO41	**Number of Equivalent Loads**		**1**	**2**	**3**	**4**	**6 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.18 0.17	0.26 0.22	0.34 0.27	0.42 0.31	0.60 0.39
NO42	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.37 0.38	0.44 0.47	0.52 0.59	0.64 0.75	0.74 0.86
NO43	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.34	0.46 0.46	0.54 0.55	0.61 0.64	0.69 0.74
NO44	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.44 0.32	0.50 0.42	0.56 0.52	0.63 0.61	0.71 0.70
NO46	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.50 0.40	0.54 0.49	0.59 0.58	0.67 0.67	0.76 0.75

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

NO5x is a family of 5-input gates which perform the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	H
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L

HDL Syntax

Verilog ..... NO5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: NO5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads				
	NO51	NO52	NO53	NO54	NO56
A	1.0	1.0	2.0	2.0	2.0
B	1.0	1.0	2.0	2.0	2.0
C	1.0	1.0	2.0	2.0	2.0
D	1.0	1.0	2.0	2.0	2.0
E	1.0	1.0	2.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static IDD (TJ = 85°C) (nA)	EQLpd (Eq-load)
NO51	2.0	TBD	3.1
NO52	3.2	TBD	7.9
NO53	5.7	TBD	14.2
NO54	7.0	TBD	20.4
NO56	7.5	TBD	23.3

a. See page 2-13 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

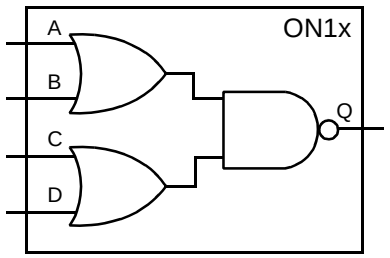
NO51	**Number of Equivalent Loads**		**1**	**2**	**3**	**4**	**6 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.18 0.22	0.28 0.27	0.38 0.33	0.48 0.38	0.68 0.49
NO52	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.37 0.39	0.44 0.48	0.53 0.60	0.65 0.75	0.72 0.86
NO53	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.35 0.37	0.44 0.49	0.52 0.59	0.59 0.68	0.67 0.78
NO54	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.38 0.36	0.46 0.48	0.52 0.58	0.59 0.67	0.67 0.75
NO56	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.41 0.40	0.50 0.52	0.58 0.60	0.64 0.69	0.70 0.77

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ON1x is a family of OR-NAND circuits consisting of two 2-input OR gates into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	L	H
All other combinations				L

HDL Syntax

Verilog ..... ON1x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: ON1x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	ON11	ON12	ON14	ON16
A	1.0	1.0	1.0	2.0
B	1.0	1.0	1.0	2.0
C	1.0	1.0	1.0	2.0
D	1.0	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON11	1.5	TBD	2.9
ON12	2.8	TBD	7.3
ON14	3.0	TBD	8.5
ON16	6.0	TBD	16.2

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

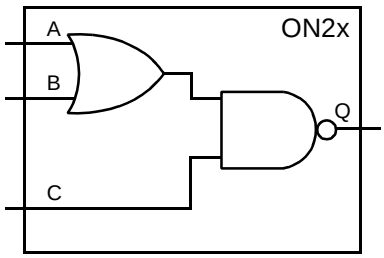
ON11	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.17 0.22	0.23 0.28	0.36 0.40	0.55 0.56	0.68 0.66
ON12	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.40	0.42 0.50	0.51 0.62	0.63 0.78	0.72 0.89
ON14	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.38 0.43	0.46 0.57	0.54 0.68	0.61 0.78	0.69 0.89
ON16	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.37 0.40	0.44 0.52	0.50 0.63	0.57 0.73	0.63 0.82

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ON2x is a familyof OR-NAND circuits consisting of one 2-input OR gate into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	Q
L	L	X	H
X	X	L	H
All other combinations			L

HDL Syntax

Verilog ..... ON2x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: ON2x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads			
	ON21	ON22	ON24	ON26
A	1.0	1.0	1.0	2.0
B	1.0	1.0	1.0	2.0
C	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON21	1.2	TBD	2.3
ON22	2.5	TBD	6.8
ON24	2.8	TBD	8.0
ON26	5.0	TBD	14.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

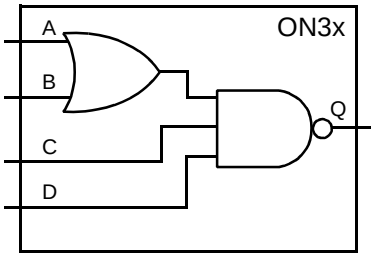
ON21	**Number of Equivalent Loads**		**1**	**2**	**4**	**7**	**9 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.18 0.20	0.25 0.26	0.37 0.37	0.54 0.53	0.67 0.64
ON22	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.39	0.42 0.49	0.52 0.62	0.63 0.78	0.72 0.89
ON24	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.38 0.43	0.47 0.56	0.55 0.67	0.62 0.77	0.69 0.88
ON26	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.38	0.42 0.52	0.49 0.63	0.56 0.73	0.63 0.82

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ON3x is a family of OR-NAND circuits consisting of a 2-input OR gate and two direct inputs into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	X	H
X	X	X	L	H
All other combinations				L

HDL Syntax

Verilog ..... ON3x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: ON3x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	ON31	ON32	ON34	ON36
A	1.0	1.0	1.0	2.0
B	1.0	1.0	1.0	2.0
C	1.0	1.0	1.0	1.9
D	1.0	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON31	1.5	TBD	2.6
ON32	2.8	TBD	7.2
ON34	3.0	TBD	8.4
ON36	5.7	TBD	16.2

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

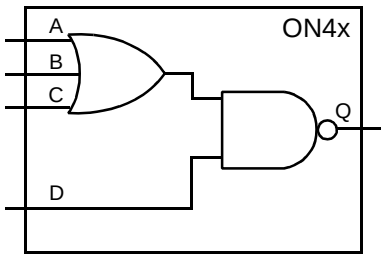
ON31	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.21 0.21	0.28 0.28	0.42 0.42	0.49 0.48	0.63 0.62
ON32	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.40	0.42 0.50	0.51 0.62	0.63 0.78	0.72 0.89
ON34	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.44	0.47 0.57	0.54 0.68	0.61 0.78	0.69 0.88
ON36	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.35 0.41	0.43 0.51	0.50 0.64	0.57 0.73	0.63 0.81

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ON4x is a family of OR-NAND circuits consisting of one 3-input OR gate into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	X	H
X	X	X	L	H
All other combinations				L

HDL Syntax

Verilog ..... ON4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: ON4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	ON41	ON42	ON44	ON46
A	1.0	1.0	1.0	2.0
B	1.0	1.0	1.0	2.0
C	1.0	1.0	1.0	2.0
D	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON41	1.5	TBD	3.0
ON42	2.8	TBD	7.6
ON44	3.0	TBD	8.7
ON46	5.5	TBD	15.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

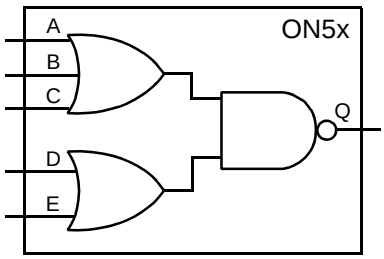
ON41	**Number of Equivalent Loads**		**1**	**2**	**4**	**5**	**7 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.23 0.22	0.32 0.29	0.49 0.41	0.57 0.48	0.73 0.60
ON42	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.43 0.43	0.49 0.52	0.58 0.65	0.71 0.81	0.80 0.92
ON44	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.46 0.46	0.54 0.59	0.62 0.70	0.69 0.80	0.78 0.92
ON46	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.40 0.30	0.48 0.47	0.55 0.62	0.62 0.73	0.69 0.83

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ON5x is a family of OR-NAND circuits consisting of one 3-input OR gate and one 2-input OR gate into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	X	X	H
X	X	X	L	L	H
All other combinations					L

HDL Syntax

Verilog ..... ON5x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: ON5x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	ON52	ON54	ON56
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON52	3.0	TBD	8.0
ON54	3.2	TBD	9.1
ON56	6.5	TBD	17.2

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

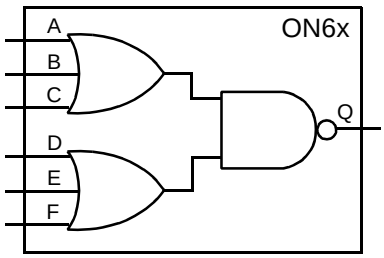
ON52	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.43 0.42	0.50 0.52	0.59 0.64	0.71 0.79	0.79 0.92
ON54	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.46 0.46	0.54 0.59	0.61 0.70	0.68 0.80	0.77 0.91
ON56	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.41 0.41	0.49 0.53	0.56 0.65	0.62 0.75	0.68 0.84

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ON6x is a family of OR-NAND circuits consisting of two 3-input OR gates into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	L	X	X	X	H
X	X	X	L	L	L	H
All other combinations						L

HDL Syntax

Verilog ..... ON6x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ON6x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	ON62	ON64	ON66
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON62	3.2	TBD	8.6
ON64	3.7	TBD	9.8
ON66	7.0	TBD	18.1

a. See page 2-13 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

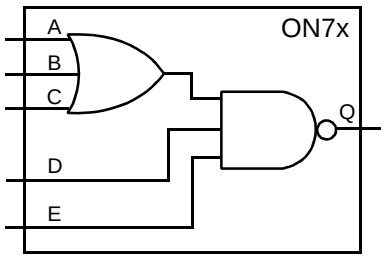
ON62	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.43 0.42	0.48 0.51	0.57 0.64	0.71 0.80	0.81 0.92
ON64	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.46 0.46	0.55 0.59	0.63 0.70	0.69 0.80	0.77 0.92
ON66	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.42 0.41	0.48 0.53	0.55 0.64	0.62 0.74	0.70 0.84

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ON7x is a family of OR-NAND circuits consisting of one 3-input OR gate into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
All other combinations					L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Core Logic

HDL Syntax

Verilog ..... ON7x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: ON7x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	ON72	ON74	ON76
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	1.9
E	1.0	1.0	1.9

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON72	3.0	TBD	7.9
ON74	3.2	TBD	9.0
ON76	6.2	TBD	17.2

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

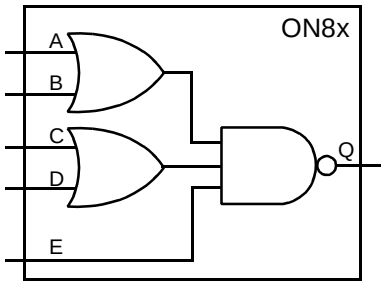
ON72	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.43 0.42	0.49 0.52	0.58 0.64	0.70 0.80	0.79 0.91
ON74	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.46 0.46	0.54 0.59	0.62 0.70	0.69 0.80	0.77 0.92
ON76	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.42 0.40	0.49 0.54	0.55 0.65	0.62 0.75	0.70 0.83

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ON8x is a family of OR-NAND circuits consisting of two 2-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	X	X	X	H
X	X	L	L	X	H
X	X	X	X	L	H
All other combinations					L

HDL Syntax

Verilog ..... ON8x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: ON8x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	ON82	ON84	ON86
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON82	3.7	TBD	9.7
ON84	4.0	TBD	10.9
ON86	7.3	TBD	20.2

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

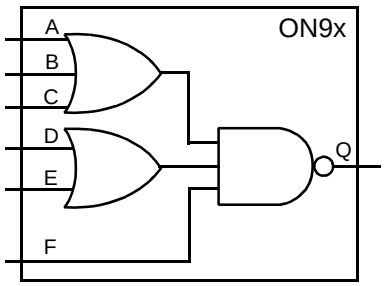
ON82	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.47	0.46 0.58	0.56 0.72	0.68 0.91	0.78 1.04
ON84	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.40 0.52	0.50 0.68	0.58 0.80	0.64 0.91	0.72 1.03
ON86	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.46	0.44 0.61	0.51 0.73	0.59 0.83	0.66 0.92

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ON9x is a family of OR-NAND circuits consisting of one 3-input OR gate and one 2-input OR gate into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	L	X	X	X	H
X	X	X	L	L	X	H
X	X	X	X	X	L	H
All other combinations						L

HDL Syntax

Verilog ..... ON9x *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ON9x port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	ON92	ON94	ON96
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON92	4.0	TBD	10.4
ON94	4.2	TBD	11.5
ON96	7.7	TBD	21.2

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

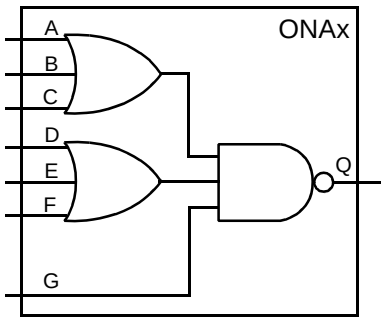
ON92	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.46 0.50	0.53 0.62	0.62 0.76	0.75 0.93	0.85 1.05
ON94	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.49 0.55	0.58 0.70	0.65 0.82	0.72 0.93	0.80 1.05
ON96	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.44 0.48	0.52 0.63	0.58 0.75	0.64 0.86	0.70 0.96

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ONAx is a family of OR-NAND circuits consisting of two 3-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	L	L	X	X	X	X	H
X	X	X	L	L	L	X	H
X	X	X	X	X	X	L	H
All other combinations							L

HDL Syntax

Verilog ..... ONAx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ONAx port map (Q, A, B, C, D, E, F, G;)

Pin Loading

Pin Name	Equivalent Loads		
	ONA2	ONA4	ONA6
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0
G	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONA2	4.2	TBD	11.0
ONA4	4.5	TBD	12.1
ONA6	8.2	TBD	22.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ONA2	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.46 0.50	0.53 0.60	0.62 0.74	0.74 0.92	0.83 1.04
ONA4	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.48 0.54	0.57 0.68	0.65 0.81	0.72 0.93	0.80 1.07
ONA6	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.46 0.49	0.52 0.62	0.57 0.74	0.64 0.85	0.72 0.95

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

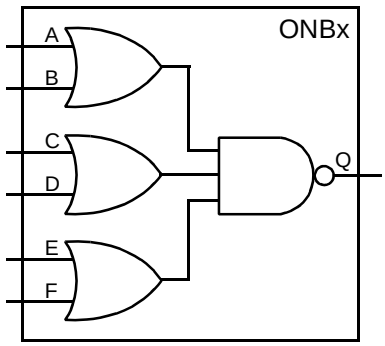
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

ONBx is a family of OR-NAND circuits consisting of three 2-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	X	X	X	X	H
X	X	L	L	X	X	H
X	X	X	X	L	L	H
All other combinations						L

HDL Syntax

Verilog ..... ONBx *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ONBx port map (Q, A, B, C, D, E, F)

Pin Loading

Pin Name	Equivalent Loads		
	ONB2	ONB4	ONB6
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONB2	3.7	TBD	10.2
ONB4	4.0	TBD	11.4
ONB6	8.0	TBD	21.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ONB2	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.38 0.47	0.45 0.58	0.55 0.73	0.67 0.91	0.76 1.04
ONB4	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.41 0.53	0.49 0.67	0.57 0.80	0.65 0.91	0.73 1.04
ONB6	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.37 0.47	0.44 0.62	0.51 0.72	0.59 0.83	0.66 0.93

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

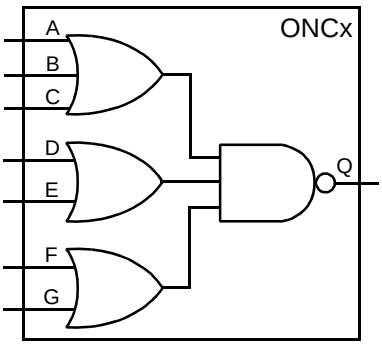
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

ONCx is a family of OR-NAND circuits consisting of one 3-input OR gate and two 2-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	L	L	X	X	X	X	H
X	X	X	L	L	X	X	H
X	X	X	X	X	L	L	H
All other combinations							L

HDL Syntax

Verilog ..... ONCx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ONCx port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads		
	ONC2	ONC4	ONC6
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0
G	1.0	1.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONC2	4.2	TBD	10.8
ONC4	4.5	TBD	12.0

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONC6	8.5	TBD	22.6

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

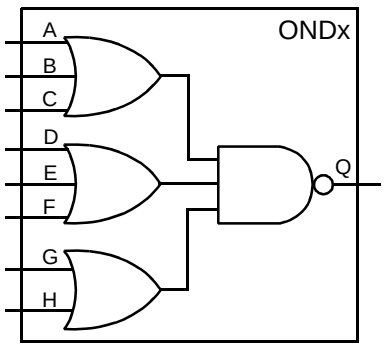
ONC2	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.46 0.49	0.52 0.60	0.61 0.74	0.73 0.92	0.83 1.05
ONC4	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.49 0.55	0.58 0.71	0.66 0.83	0.73 0.93	0.82 1.05
ONC6	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.43 0.50	0.52 0.65	0.59 0.76	0.65 0.86	0.71 0.95

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ONDx is a family of OR-NAND circuits consisting of two 3-input OR gates and one 2-input OR gate into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
L	L	L	X	X	X	X	X	H
X	X	X	L	L	L	X	X	H
X	X	X	X	X	X	L	L	H
All other combinations								L

HDL Syntax

Verilog ..... ONDx *inst_name* (Q, A, B, C, D, E, F, G, H);

VHDL..... *inst_name*: ONDx port map (Q, A, B, C, D, E, F, G, H);

Pin Loading

Pin Name	Equivalent Loads		
	OND2	OND4	OND6
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0
G	1.0	1.0	2.0
H	1.0	1.0	2.0

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OND2	4.5	TBD	11.5
OND4	4.7	TBD	12.7
OND6	9.0	TBD	23.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

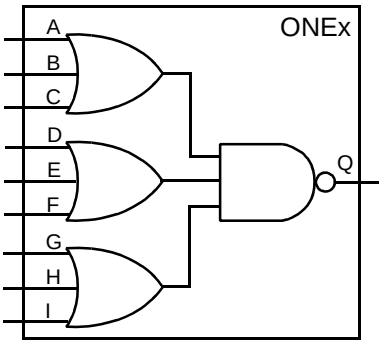
OND2	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.46 0.50	0.52 0.61	0.61 0.76	0.73 0.94	0.83 1.06
OND4	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.49 0.55	0.59 0.70	0.66 0.82	0.73 0.93	0.81 1.05
OND6	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.43 0.49	0.51 0.64	0.59 0.75	0.65 0.85	0.70 0.95

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ONEx is a family of OR-NAND circuits consisting of three 3-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Q
L	L	L	X	X	X	X	X	X	H
X	X	X	L	L	L	X	X	X	H
X	X	X	X	X	X	L	L	L	H
All other combinations									L

HDL Syntax

Verilog ..... ONEx *inst_name* (Q, A, B, C, D, E, F, G, H, I);

VHDL..... *inst_name*: ONEx port map (Q, A, B, C, D, E, F, G, H, I);

Pin Loading

Pin Name	Equivalent Loads		
	ONE2	ONE4	ONE6
A	1.0	1.0	2.0
B	1.0	1.0	2.0
C	1.0	1.0	2.0
D	1.0	1.0	2.0
E	1.0	1.0	2.0
F	1.0	1.0	2.0
G	1.0	1.0	2.0
H	1.0	1.0	2.0
I	1.0	1.0	2.0

AMI5HS 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONE2	5.0	TBD	12.2
ONE4	5.2	TBD	13.4
ONE6	9.2	TBD	24.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

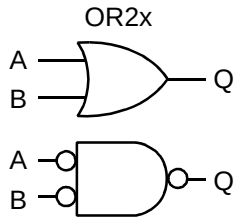
ONE2	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.46 0.50	0.54 0.61	0.63 0.76	0.75 0.93	0.84 1.05
ONE4	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.49 0.55	0.59 0.69	0.66 0.81	0.73 0.92	0.80 1.06
ONE6	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.45 0.49	0.52 0.63	0.58 0.74	0.65 0.84	0.71 0.93

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

OR2x is a family of 2-input gates which perform the logical OR function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	H

HDL Syntax

Verilog ..... OR2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: OR2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads			
	OR21	OR22	OR24	OR26
A	1.0	1.0	2.0	2.0
B	1.0	1.0	2.0	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OR21	1.2	TBD	2.9
OR22	1.5	TBD	4.0
OR24	3.0	TBD	8.7
OR26	3.7	TBD	11.5

a. See page 2-13 for power equation.

Core Logic

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

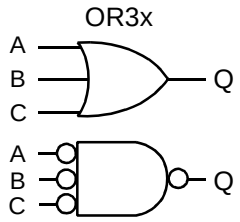
OR21	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.21 0.27	0.28 0.36	0.36 0.49	0.48 0.65	0.57 0.77
OR22	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.23 0.31	0.32 0.45	0.39 0.56	0.46 0.66	0.54 0.76
OR24	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.20 0.27	0.28 0.40	0.34 0.50	0.40 0.60	0.48 0.70
OR26	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.24 0.35	0.31 0.46	0.38 0.56	0.45 0.67	0.50 0.77

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

OR3x is a family of 3-input gates which perform the logical OR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

HDL Syntax

Verilog ..... OR3x *inst_name* (Q, A, B);

VHDL..... *inst_name*: OR3x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads			
	OR31	OR32	OR34	OR36
A	1.0	1.0	2.0	3.0
B	1.0	1.0	2.0	3.0
C	1.0	1.0	2.0	3.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OR31	1.5	TBD	3.6
OR32	2.0	TBD	4.7
OR34	4.0	TBD	10.4
OR36	5.2	TBD	14.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

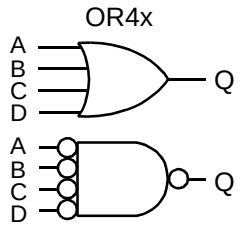
OR31	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.23 0.33	0.30 0.45	0.39 0.59	0.51 0.75	0.60 0.87
OR32	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.24 0.39	0.33 0.53	0.41 0.65	0.48 0.77	0.56 0.90
OR34	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.21 0.35	0.29 0.48	0.36 0.63	0.44 0.73	0.51 0.82
OR36	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.21 0.34	0.28 0.49	0.35 0.60	0.42 0.70	0.48 0.78

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

OR4x is a family of 4-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

HDL Syntax

Verilog ..... OR4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: OR4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	OR41	OR42	OR44	OR46
A	1.0	1.0	3.0	3.0
B	1.0	1.0	3.0	3.0
C	1.0	1.0	3.0	3.0
D	1.0	1.0	3.0	3.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OR41	2.0	TBD	4.1
OR42	2.2	TBD	5.2
OR44	5.5	TBD	14.6
OR46	6.0	TBD	17.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

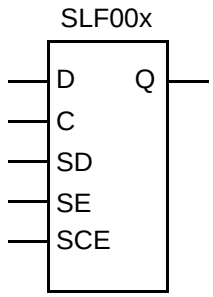
OR41	**Number of Equivalent Loads**		**1**	**3**	**6**	**10**	**13 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.23 0.38	0.30 0.49	0.39 0.64	0.51 0.82	0.60 0.94
OR42	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.28 0.45	0.37 0.62	0.44 0.74	0.51 0.86	0.60 0.98
OR44	**Number of Equivalent Loads**		**1**	**10**	**20**	**30**	**40 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.21 0.34	0.28 0.49	0.35 0.61	0.42 0.71	0.48 0.82
OR46	**Number of Equivalent Loads**		**1**	**14**	**29**	**44**	**58 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.22 0.38	0.30 0.53	0.38 0.67	0.44 0.79	0.50 0.90

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

SLF00x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low.

Logic Symbol



Truth Table

C	D	SD	SE	SCE	Q
↑	H	X	L	L	H
↑	L	X	L	L	L
↑	X	H	H	L	H
↑	X	L	H	L	L
L	X	X	X	L	NC
L	H	X	L	H	H
L	L	X	L	H	L
L	X	H	H	H	H
L	X	L	H	H	L
H	X	X	X	H	NC

NC = No Change

HDL Syntax

Verilog ..... SLF00x *inst_name* (Q, C, D, SCE, SD, SE);

VHDL..... *inst_name*: SLF00x port map (Q, C, D, SCE, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	SLF001	SLF002	SLF004	SLF006
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1
SCE	2.0	2.0	2.0	2.0

AMI5HS 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF001	8.0	TBD	26.5
SLF002	8.8	TBD	30.9
SLF004	9.5	TBD	33.7
SLF006	10.0	TBD	36.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
SLF001	From: C To: Q	t_{PLH} t_{PHL}	0.99 1.18	1.06 1.29	1.17 1.44	1.31 1.60	1.42 1.72
	From: D To: Q	t_{PLH} t_{PHL}	0.89 1.05	0.98 1.15	1.09 1.29	1.21 1.47	1.29 1.60
	From: SCE To: Q	t_{PLH} t_{PHL}	0.76 0.89	0.84 1.00	0.95 1.14	1.08 1.31	1.18 1.43
	From: SD To: Q	t_{PLH} t_{PHL}	0.90 1.04	0.97 1.16	1.07 1.30	1.22 1.46	1.33 1.58
	From: SE To: Q	t_{PLH} t_{PHL}	0.97 1.18	1.04 1.29	1.14 1.43	1.29 1.60	1.40 1.71
SLF002	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: C To: Q	t_{PLH} t_{PHL}	0.95 1.12	1.03 1.23	1.10 1.33	1.17 1.42	1.24 1.53
	From: D To: Q	t_{PLH} t_{PHL}	0.86 1.03	0.95 1.15	1.03 1.25	1.10 1.34	1.18 1.43
	From: SCE To: Q	t_{PLH} t_{PHL}	0.69 0.83	0.79 0.96	0.87 1.07	0.95 1.16	1.04 1.27
	From: SD To: Q	t_{PLH} t_{PHL}	0.90 1.00	0.98 1.12	1.05 1.22	1.11 1.30	1.18 1.40
	From: SE To: Q	t_{PLH} t_{PHL}	0.95 1.14	1.03 1.26	1.10 1.36	1.16 1.45	1.25 1.55

	Number of Equivalent Loads		1	10	20	30	40 (max)
SLF004	From: C To: Q	t_{PLH} t_{PHL}	1.01 1.17	1.10 1.30	1.16 1.39	1.22 1.48	1.27 1.55
	From: D To: Q	t_{PLH} t_{PHL}	0.87 1.09	0.95 1.22	1.05 1.31	1.13 1.39	1.20 1.45
	From: SCE To: Q	t_{PLH} t_{PHL}	0.64 0.88	0.80 1.04	0.93 1.14	1.00 1.22	1.05 1.30
	From: SD To: Q	t_{PLH} t_{PHL}	0.91 1.03	1.01 1.16	1.08 1.27	1.14 1.37	1.18 1.46
	From: SE To: Q	t_{PLH} t_{PHL}	1.00 1.20	1.08 1.33	1.15 1.42	1.22 1.50	1.28 1.58
	Number of Equivalent Loads		**1**	**14**	**29**	**44**	**58 (max)**
SLF006	From: C To: Q	t_{PLH} t_{PHL}	1.06 1.24	1.14 1.36	1.21 1.46	1.27 1.56	1.32 1.64
	From: D To: Q	t_{PLH} t_{PHL}	0.96 1.13	1.05 1.27	1.13 1.37	1.20 1.46	1.26 1.53
	From: SCE To: Q	t_{PLH} t_{PHL}	0.82 0.96	0.87 1.12	0.95 1.22	1.04 1.31	1.13 1.38
	From: SD To: Q	t_{PLH} t_{PHL}	0.99 1.13	1.05 1.26	1.13 1.36	1.21 1.44	1.28 1.52
	From: SE To: Q	t_{PLH} t_{PHL}	1.07 1.27	1.17 1.38	1.22 1.48	1.27 1.58	1.30 1.66

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF001	SLF002	SLF004	SLF006
Min C Width	High	t_w	1.08	1.07	1.14	1.21
Min C Width	Low	t_w	0.74	0.79	0.79	0.79
Min D Setup		t_{su}	0.61	0.66	0.66	0.66
Min D Hold		t_h	0.15	0.15	0.15	0.15
Min SD Setup		t_{su}	0.61	0.66	0.66	0.66
Min SD Hold		t_h	0.15	0.15	0.15	0.15
Min SE Setup		t_{su}	0.73	0.78	0.78	0.78
Min SE Hold		t_h	0.15	0.15	0.15	0.15

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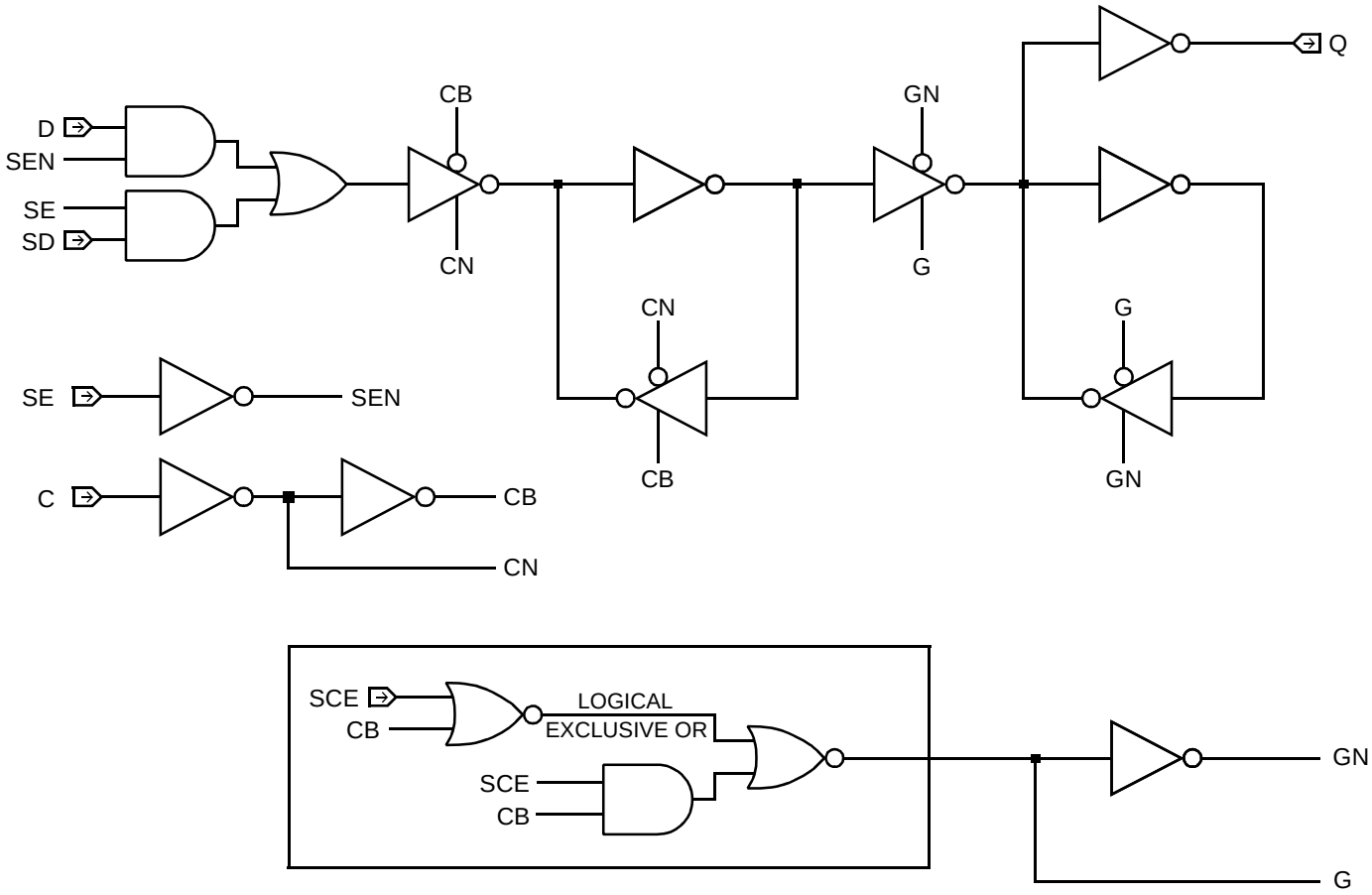
Delay (ns) From To	Parameter	Cell			
		SLF001	SLF002	SLF004	SLF006
Min SCE Setup	t_{su}	0.84	0.83	0.90	0.97
Min SCE Hold	t_h	0.91	0.92	0.96	1.00

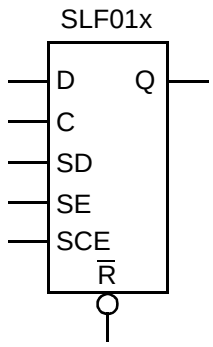
Logic Schematic



Description

SLF01x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low. RESET is asynchronous and active low.

Logic Symbol



Truth Table

RN	C	D	SD	SE	SCE	Q
H	↑	H	X	L	L	H
H	↑	L	X	L	L	L
H	↑	X	H	H	L	H
H	↑	X	L	H	L	L
H	L	X	X	X	L	NC
H	L	H	X	L	H	H
H	L	L	X	L	H	L
H	L	X	H	H	H	H
H	L	X	L	H	H	L
H	H	X	X	X	H	NC
L	X	X	X	X	X	L

NC = No Change

HDL Syntax

Verilog ..... SLF01x *inst_name* (Q, C, D, RN, SCE, SD, SE);

VHDL..... *inst_name*: SLF01x port map (Q, C, D, RN, SCE, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	SLF011	SLF012	SLF014	SLF016
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1
SCE	2.0	2.0	2.0	2.0

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AMI5HS 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF011	8.8	TBD	30.3
SLF012	9.8	TBD	34.7
SLF014	10.2	TBD	37.6
SLF016	11.0	TBD	39.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
SLF011	From: C To: Q	t_{PLH} t_{PHL}	0.98 1.18	1.05 1.27	1.15 1.40	1.27 1.58	1.36 1.72
	From: D To: Q	t_{PLH} t_{PHL}	0.95 1.08	1.03 1.20	1.12 1.33	1.24 1.49	1.33 1.59
	From: RN To: Q	t_{PLH} t_{PHL}	0.72 0.90	0.79 1.03	0.88 1.17	1.01 1.33	1.10 1.44
	From: SCE To: Q	t_{PLH} t_{PHL}	0.75 0.90	0.81 1.01	0.90 1.14	1.04 1.31	1.14 1.42
	From: SD To: Q	t_{PLH} t_{PHL}	0.98 1.06	1.05 1.16	1.14 1.29	1.27 1.47	1.37 1.59
	From: SE To: Q	t_{PLH} t_{PHL}	1.05 1.19	1.13 1.30	1.23 1.44	1.34 1.60	1.41 1.71

	Number of Equivalent Loads		1	6	11	16	22 (max)
SLF012	From: C To: Q	t_{PLH} t_{PHL}	0.99 1.15	1.06 1.28	1.13 1.37	1.19 1.45	1.27 1.54
	From: D To: Q	t_{PLH} t_{PHL}	0.99 1.04	1.08 1.14	1.14 1.24	1.20 1.34	1.26 1.45
	From: RN To: Q	t_{PLH} t_{PHL}	0.73 1.10	0.81 1.27	0.88 1.39	0.96 1.50	1.05 1.62
	From: SCE To: Q	t_{PLH} t_{PHL}	0.69 0.84	0.78 0.96	0.86 1.06	0.94 1.16	1.02 1.28
	From: SD To: Q	t_{PLH} t_{PHL}	1.01 1.01	1.09 1.12	1.16 1.22	1.21 1.31	1.28 1.42
	From: SE To: Q	t_{PLH} t_{PHL}	1.07 1.16	1.15 1.29	1.22 1.38	1.28 1.46	1.35 1.55
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
SLF014	From: C To: Q	t_{PLH} t_{PHL}	1.06 1.20	1.13 1.31	1.20 1.42	1.26 1.52	1.32 1.61
	From: D To: Q	t_{PLH} t_{PHL}	1.05 1.11	1.14 1.22	1.20 1.32	1.25 1.42	1.29 1.51
	From: RN To: Q	t_{PLH} t_{PHL}	0.78 1.36	0.89 1.50	0.96 1.64	1.02 1.78	1.06 1.92
	From: SCE To: Q	t_{PLH} t_{PHL}	0.77 0.91	0.89 1.03	0.99 1.14	1.08 1.23	1.17 1.32
	From: SD To: Q	t_{PLH} t_{PHL}	1.04 1.10	1.12 1.22	1.20 1.31	1.27 1.40	1.35 1.47
	From: SE To: Q	t_{PLH} t_{PHL}	1.11 1.23	1.19 1.36	1.26 1.45	1.32 1.52	1.37 1.59

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	Number of Equivalent Loads		1	14	29	44	58 (max)
SLF016	From: C To: Q	t_{PLH} t_{PHL}	1.36 1.40	1.41 1.48	1.48 1.56	1.54 1.65	1.62 1.74
	From: D To: Q	t_{PLH} t_{PHL}	1.36 1.30	1.44 1.38	1.49 1.47	1.52 1.56	1.54 1.64
	From: RN To: Q	t_{PLH} t_{PHL}	1.10 0.58	1.18 0.66	1.23 0.77	1.28 0.86	1.31 0.95
	From: SCE To: Q	t_{PLH} t_{PHL}	1.11 1.14	1.18 1.25	1.25 1.33	1.30 1.40	1.34 1.45
	From: SD To: Q	t_{PLH} t_{PHL}	1.34 1.28	1.42 1.36	1.48 1.45	1.53 1.53	1.57 1.61
	From: SE To: Q	t_{PLH} t_{PHL}	1.44 1.40	1.52 1.47	1.57 1.56	1.61 1.65	1.64 1.74

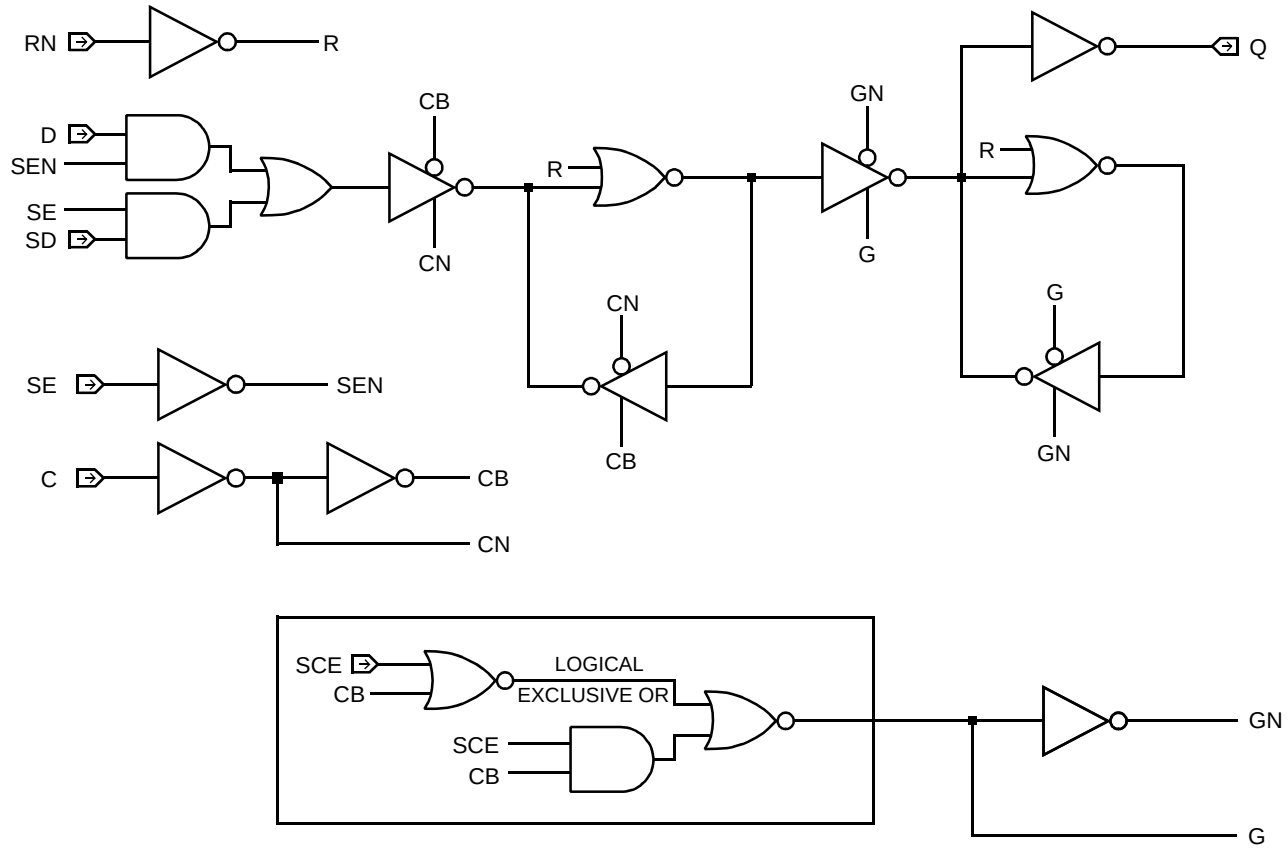
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.05.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF011	SLF012	SLF014	SLF016
Min C Width	High	t_w	1.10	1.08	1.15	1.10
Min C Width	Low	t_w	0.76	0.81	0.81	0.76
Min RN Width	Low	t_w	0.59	0.62	0.62	0.58
Min D Setup		t_{su}	0.63	0.68	0.68	0.62
Min D Hold		t_h	0.15	0.15	0.15	0.15
Min SD Setup		t_{su}	0.63	0.68	0.68	0.62
Min SD Hold		t_h	0.15	0.15	0.15	0.15
Min SE Setup		t_{su}	0.75	0.81	0.81	0.75
Min SE Hold		t_h	0.15	0.15	0.15	0.15
Min SCE Setup		t_{su}	0.86	0.85	0.92	0.87
Min SCE Hold		t_h	0.91	0.92	0.96	0.86
Min RN Setup		t_{su}	0.32	0.37	0.37	0.32
Min RN Hold		t_h	0.34	0.34	0.34	0.34

Logic Schematic



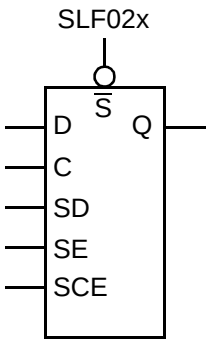
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

SLF02x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low. SET is asynchronous and active low.

Logic Symbol



Truth Table

SN	C	D	SD	SE	SCE	Q
H	↑	H	X	L	L	H
H	↑	L	X	L	L	L
H	↑	X	H	H	L	H
H	↑	X	L	H	L	L
H	L	X	X	X	L	NC
H	L	H	X	L	H	H
H	L	L	X	L	H	L
H	L	X	H	H	H	H
H	L	X	L	H	H	L
H	H	X	X	X	H	NC
L	X	X	X	X	X	H

NC = No Change

HDL Syntax

Verilog ..... SLF02x *inst_name* (Q, C, D, SCE, SD, SE, SN);

VHDL..... *inst_name*:SLF02x port map (Q, C, D, SCE, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	SLF021	SLF022	SLF024	SLF026
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1
SCE	2.0	2.0	2.0	2.0
SN	2.0	2.1	2.1	2.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF021	8.2	TBD	27.1
SLF022	9.2	TBD	31.7
SLF024	9.8	TBD	34.5
SLF026	10.2	TBD	36.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	3	6	10	13 (max)
SLF021	From: C To: Q	t_{PLH} t_{PHL}	0.99 1.18	1.07 1.28	1.17 1.42	1.28 1.59	1.36 1.70
	From: D To: Q	t_{PLH} t_{PHL}	0.92 1.07	1.00 1.16	1.09 1.30	1.20 1.48	1.28 1.61
	From: SCE To: Q	t_{PLH} t_{PHL}	0.79 0.86	0.87 0.97	0.96 1.11	1.08 1.27	1.17 1.38
	From: SD To: Q	t_{PLH} t_{PHL}	0.94 1.06	1.03 1.18	1.12 1.31	1.22 1.47	1.29 1.57
	From: SE To: Q	t_{PLH} t_{PHL}	1.01 1.18	1.10 1.27	1.19 1.41	1.29 1.59	1.35 1.72
	From: SN To: Q	t_{PLH} t_{PHL}	0.65 0.61	0.74 0.74	0.84 0.91	0.95 1.11	1.03 1.25

AMI5HS 0.5 micron CMOS Standard Cell

	Number of Equivalent Loads		1	6	11	16	22 (max)
SLF022	From: C To: Q	t_{PLH} t_{PHL}	0.96 1.16	1.04 1.25	1.11 1.35	1.17 1.45	1.24 1.58
	From: D To: Q	t_{PLH} t_{PHL}	0.94 1.06	1.01 1.19	1.08 1.29	1.15 1.38	1.22 1.47
	From: SCE To: Q	t_{PLH} t_{PHL}	0.74 0.83	0.83 0.97	0.91 1.08	0.98 1.17	1.05 1.28
	From: SD To: Q	t_{PLH} t_{PHL}	0.96 1.03	1.05 1.15	1.11 1.25	1.17 1.34	1.24 1.45
	From: SE To: Q	t_{PLH} t_{PHL}	1.03 1.17	1.11 1.27	1.17 1.37	1.24 1.47	1.31 1.60
	From: SN To: Q	t_{PLH} t_{PHL}	0.82 0.56	0.94 0.72	1.03 0.85	1.10 0.98	1.18 1.12
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
SLF024	From: C To: Q	t_{PLH} t_{PHL}	1.02 1.23	1.10 1.37	1.17 1.46	1.23 1.53	1.31 1.59
	From: D To: Q	t_{PLH} t_{PHL}	0.98 1.12	1.02 1.23	1.09 1.33	1.18 1.43	1.28 1.53
	From: SCE To: Q	t_{PLH} t_{PHL}	0.80 0.90	0.88 1.03	0.96 1.14	1.03 1.23	1.10 1.31
	From: SD To: Q	t_{PLH} t_{PHL}	0.99 1.12	1.10 1.26	1.17 1.36	1.23 1.44	1.28 1.51
	From: SE To: Q	t_{PLH} t_{PHL}	1.07 1.25	1.14 1.39	1.21 1.48	1.28 1.56	1.35 1.63
	From: SN To: Q	t_{PLH} t_{PHL}	1.01 0.60	1.13 0.78	1.22 0.92	1.30 1.04	1.36 1.15

	Number of Equivalent Loads		1	14	29	44	58 (max)
SLF026	From: C To: Q	t_{PLH} t_{PHL}	1.25 1.44	1.31 1.49	1.37 1.58	1.44 1.69	1.51 1.80
	From: D To: Q	t_{PLH} t_{PHL}	1.18 1.33	1.26 1.41	1.32 1.50	1.37 1.58	1.41 1.66
	From: SCE To: Q	t_{PLH} t_{PHL}	1.04 1.15	1.11 1.26	1.17 1.34	1.23 1.41	1.29 1.47
	From: SD To: Q	t_{PLH} t_{PHL}	1.20 1.33	1.27 1.37	1.33 1.45	1.39 1.56	1.43 1.68
	From: SE To: Q	t_{PLH} t_{PHL}	1.28 1.47	1.31 1.58	1.37 1.65	1.46 1.70	1.55 1.75
	From: SN To: Q	t_{PLH} t_{PHL}	0.43 0.85	0.51 0.97	0.59 1.09	0.65 1.19	0.71 1.28

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

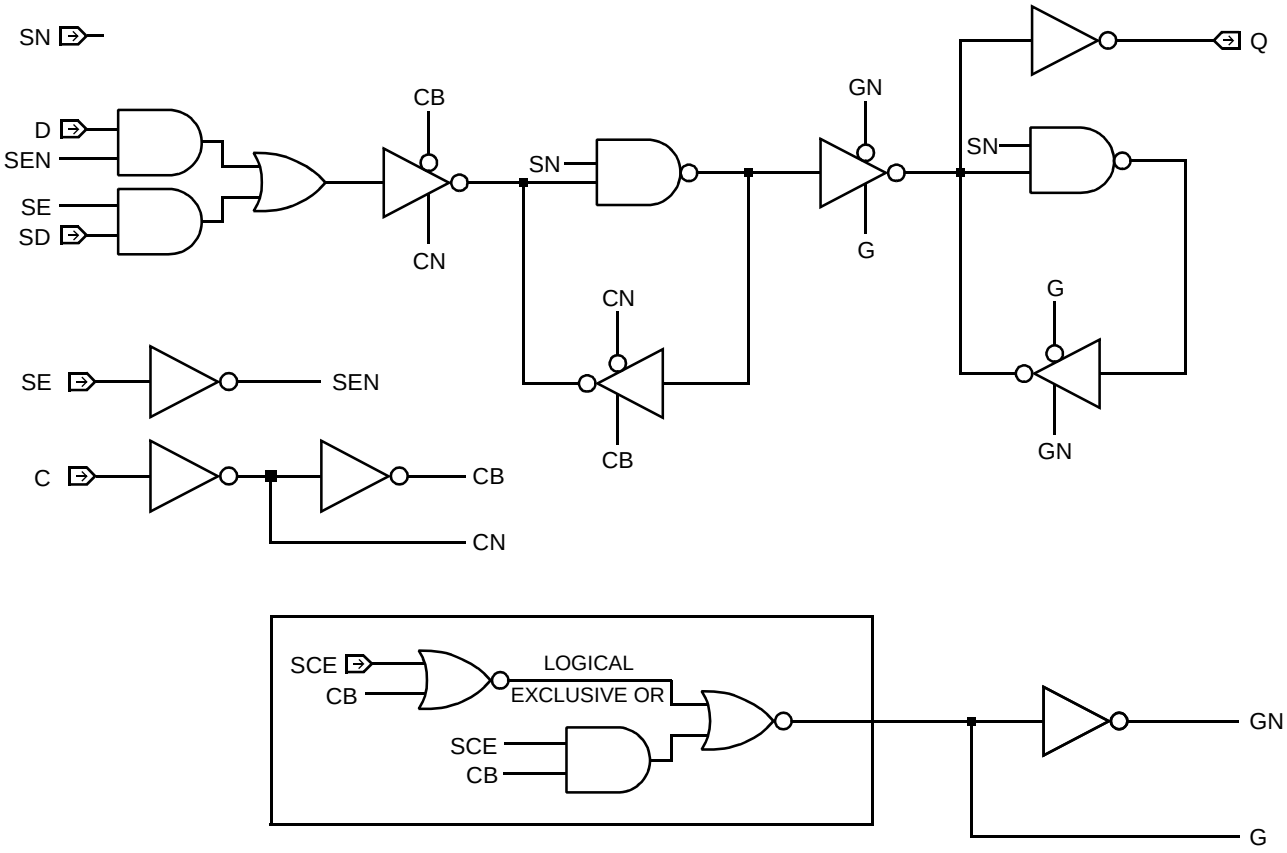
Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			SLF021	SLF022	SLF024	SLF026
Min C Width	High	t_w	1.07	1.09	1.16	1.11
Min C Width	Low	t_w	0.77	0.82	0.82	0.77
Min SN Width	Low	t_w	0.50	0.55	0.55	0.50
Min D Setup		t_{su}	0.64	0.69	0.69	0.64
Min D Hold		t_h	0.15	0.15	0.15	0.15
Min SD Setup		t_{su}	0.64	0.69	0.69	0.64
Min SD Hold		t_h	0.15	0.15	0.15	0.15
Min SE Setup		t_{su}	0.77	0.82	0.82	0.77
Min SE Hold		t_h	0.15	0.15	0.15	0.15
Min SCE Setup		t_{su}	0.84	0.86	0.93	0.87
Min SCE Hold		t_h	0.89	0.92	0.96	0.86
Min SN Setup		t_{su}	0.18	0.22	0.22	0.18
Min SN Hold		t_h	0.61	0.61	0.61	0.61

AMI5HS 0.5 micron CMOS Standard Cell

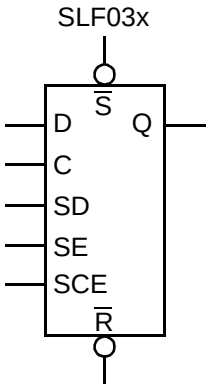
Logic Schematic



Description

SLF03x is a family of static, master-slave, multiplexed scan latch, D flip-flops. When SCE is low it is a D flip-flop with the output buffered and changes state on the rising edge of the clock. When SCE is high it is a D latch that is transparent when C is low. SET and RESET are asynchronous and active low.

Logic Symbol



Truth Table

RN	SN	C	D	SD	SE	SCE	Q
H	H	↑	H	X	L	L	H
H	H	↑	L	X	L	L	L
H	H	↑	X	H	H	L	H
H	H	↑	X	L	H	L	L
H	H	L	X	X	X	L	NC
H	H	L	H	X	L	H	H
H	H	L	L	X	L	H	L
H	H	L	X	H	H	H	H
H	H	L	X	L	H	H	L
H	H	H	X	X	X	H	NC
H	L	X	X	X	X	X	H
L	X	X	X	X	X	X	L

NC = No Change

HDL Syntax

Verilog ..... SLF03x *inst_name* (Q, C, D, RN, SCE, SD, SE, SN);

VHDL..... *inst_name*: SLF03x port map (Q, C, D, RN, SCE, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	SLF031	SLF032	SLF034	SLF036
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1
SCE	2.0	2.0	2.0	2.0
SN	2.1	2.1	2.1	2.1

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
SLF031	9.5	TBD	31.8
SLF032	10.5	TBD	36.3
SLF034	11.0	TBD	39.2
SLF036	11.5	TBD	42.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	6	11	16	22 (max)
SLF031	From: C To: Q	t_{PLH} t_{PHL}	1.08 1.23	1.25 1.47	1.39 1.67	1.53 1.85	1.70 2.06
	From: D To: Q	t_{PLH} t_{PHL}	1.05 1.11	1.21 1.34	1.35 1.54	1.50 1.73	1.67 1.96
	From: RN To: Q	t_{PLH} t_{PHL}	0.79 0.92	0.97 1.18	1.14 1.42	1.29 1.63	1.47 1.88
	From: SCE To: Q	t_{PLH} t_{PHL}	0.84 0.87	1.03 1.13	1.19 1.34	1.33 1.53	1.50 1.75
	From: SD To: Q	t_{PLH} t_{PHL}	1.07 1.09	1.22 1.33	1.37 1.55	1.51 1.76	1.68 2.00
	From: SE To: Q	t_{PLH} t_{PHL}	1.14 1.20	1.32 1.44	1.47 1.66	1.60 1.87	1.74 2.10
	From: SN To: Q	t_{PLH} t_{PHL}	0.65 0.64	0.84 0.94	1.01 1.22	1.16 1.49	1.34 1.79

	Number of Equivalent Loads		1	6	11	16	22 (max)
SLF032	From: C To: Q	t_{PLH} t_{PHL}	1.09 1.20	1.18 1.30	1.24 1.39	1.30 1.49	1.36 1.61
	From: D To: Q	t_{PLH} t_{PHL}	1.08 1.11	1.17 1.23	1.23 1.32	1.29 1.41	1.35 1.51
	From: RN To: Q	t_{PLH} t_{PHL}	0.82 1.13	0.92 1.29	0.99 1.42	1.06 1.53	1.14 1.65
	From: SCE To: Q	t_{PLH} t_{PHL}	0.82 0.83	0.92 0.96	1.00 1.07	1.08 1.16	1.17 1.28
	From: SD To: Q	t_{PLH} t_{PHL}	1.07 1.08	1.15 1.21	1.23 1.30	1.31 1.39	1.40 1.48
	From: SE To: Q	t_{PLH} t_{PHL}	1.16 1.22	1.23 1.35	1.29 1.44	1.36 1.52	1.45 1.61
	From: SN To: Q	t_{PLH} t_{PHL}	0.84 0.61	0.95 0.78	1.03 0.91	1.10 1.03	1.18 1.16
	Number of Equivalent Loads		**1**	**10**	**20**	**30**	**40 (max)**
SLF034	From: C To: Q	t_{PLH} t_{PHL}	1.13 1.27	1.20 1.41	1.27 1.50	1.34 1.58	1.41 1.65
	From: D To: Q	t_{PLH} t_{PHL}	1.12 1.17	1.16 1.31	1.23 1.41	1.31 1.49	1.41 1.56
	From: RN To: Q	t_{PLH} t_{PHL}	0.87 1.43	0.97 1.60	1.05 1.73	1.11 1.83	1.15 1.92
	From: SCE To: Q	t_{PLH} t_{PHL}	0.92 0.91	1.01 1.02	1.08 1.13	1.13 1.23	1.17 1.33
	From: SD To: Q	t_{PLH} t_{PHL}	1.13 1.15	1.25 1.29	1.30 1.38	1.35 1.45	1.39 1.51
	From: SE To: Q	t_{PLH} t_{PHL}	1.19 1.27	1.27 1.36	1.34 1.47	1.41 1.58	1.47 1.70
	From: SN To: Q	t_{PLH} t_{PHL}	1.04 0.66	1.19 0.84	1.27 0.97	1.32 1.08	1.37 1.17

AMI5HS 0.5 micron CMOS Standard Cell

	Number of Equivalent Loads		1	14	29	44	58 (max)
SLF036	From: C To: Q	t_{PLH} t_{PHL}	1.19 1.32	1.24 1.44	1.31 1.55	1.39 1.64	1.48 1.73
	From: D To: Q	t_{PLH} t_{PHL}	1.19 1.21	1.28 1.31	1.34 1.42	1.39 1.53	1.43 1.63
	From: RN To: Q	t_{PLH} t_{PHL}	0.92 1.65	1.00 1.78	1.09 1.94	1.17 2.09	1.24 2.24
	From: SCE To: Q	t_{PLH} t_{PHL}	0.93 0.96	1.03 1.11	1.11 1.22	1.19 1.30	1.25 1.37
	From: SD To: Q	t_{PLH} t_{PHL}	1.16 1.19	1.27 1.32	1.35 1.42	1.42 1.51	1.47 1.58
	From: SE To: Q	t_{PLH} t_{PHL}	1.26 1.34	1.32 1.43	1.39 1.54	1.47 1.64	1.54 1.74
	From: SN To: Q	t_{PLH} t_{PHL}	1.25 0.75	1.35 0.90	1.46 1.03	1.55 1.15	1.63 1.25

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

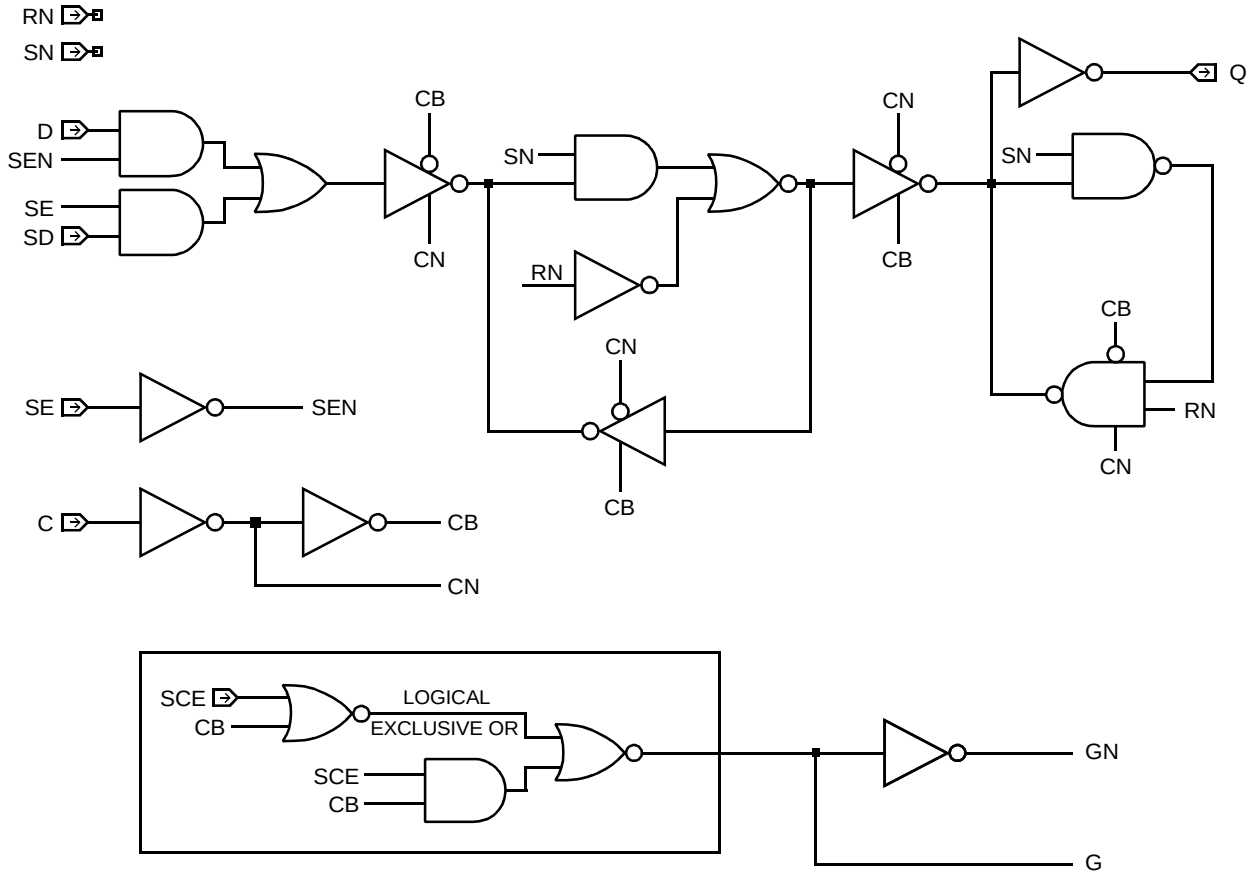
Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell SLF031	SLF032	SLF034	SLF036
Min C Width	High	t_w	1.11	1.12	1.19	1.26
Min C Width	Low	t_w	0.79	0.85	0.85	0.85
Min RN Width	Low	t_w	0.62	0.66	0.66	0.66
Min SN Width	Low	t_w	0.50	0.54	0.54	0.54
Min D Setup		t_{su}	0.66	0.73	0.73	0.73
Min D Hold		t_h	0.15	0.15	0.15	0.15
Min RN Setup		t_{su}	0.37	0.43	0.43	0.43
Min RN Hold		t_h	0.34	0.34	0.34	0.34
Min SCE Setup		t_{su}	0.89	0.89	0.97	1.04
Min SCE Hold		t_h	0.90	0.92	0.96	1.01
Min SD Setup		t_{su}	0.66	0.73	0.73	0.73
Min SD Hold		t_h	0.15	0.15	0.15	0.15
Min SE Setup		t_{su}	0.79	0.85	0.85	0.85
Min SE Hold		t_h	0.15	0.15	0.15	0.15

Delay (ns) From / To	Parameter	Cell			
		SLF031	SLF032	SLF034	SLF036
Min SN Setup	t_{su}	0.21	0.26	0.26	0.26
Min SN Hold	t_h	0.61	0.61	0.61	0.61

Logic Schematic



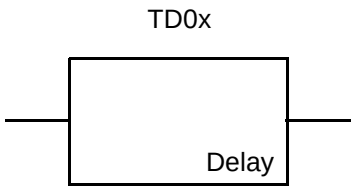
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

TD0x is a family of non-inverting time delays.

Logic Symbol



Truth Table

A	Q
L	L
H	H

HDL Syntax

Verilog ..... TD0x *inst_name* (Q, A);

VHDL..... *inst_name*: TD0x port map (Q, A);

Pin Loading

Pin Name	Equivalent Loads		
	TD02	TD03	TD08
A	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
TD02	3.7	TBD	10.0
TD03	4.2	TBD	11.4
TD08	6.5	TBD	20.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

TD02	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	2.23 2.30	2.27 2.43	2.33 2.48	2.40 2.52	2.50 2.55
TD03	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	3.22 3.35	3.25 3.48	3.31 3.55	3.39 3.61	3.51 3.67
TD08	**Number of Equivalent Loads**		**1**	**6**	**11**	**16**	**22 (max)**
	From: A To: Q	t_{PLH} t_{PHL}	8.64 8.70	8.70 8.74	8.78 8.81	8.86 8.91	8.96 9.08

PORA

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

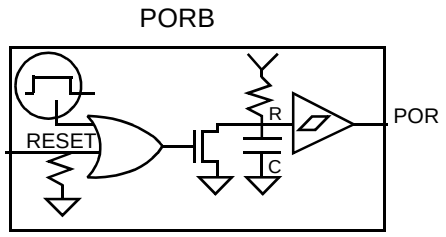
Description

PORB is a power-on-reset.

When power is applied, the POR output is asserted low for at least 2 microseconds after the logic circuits become operational. The active high RESET input also drives the POR signal to its active low state. Since the PORB is a corner function cell the RESET pin must be driven through the core.

For proper operation, user-designed external circuitry must provide a V_{DD} power slew rate of at least one volt per microsecond. This ensures that the reset pulse will be properly output when V_{DD} falls to zero and immediately returns to its valid range.

Logic Symbol



Truth Table

RESET	POR
L	H
H	L

Pin Loading

	Load
RESET	5.9 eql

HDL Syntax

Verilog ..... PORB *inst_name* (RESET, POR);

VHDL..... *inst_name*: PORB port map (RESET, POR);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	1673.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
RESET	POR	t_{PLH}	13854.71				
RESET	POR	t_{PHL}	10.19				

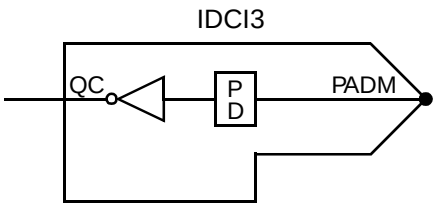
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

SECTION 4
PAD LOGIC

Description

IDCI3 is an inverting, CMOS-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	H
H	L

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDCI3 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCI3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	12.7	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	0.62 0.72	0.76 0.87	0.85 0.98	0.92 1.06	0.98 1.14

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

IDCR0

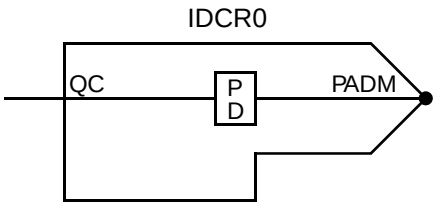
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

IDCR0 is a non-buffered, resistive analog interface input piece with ESD protection.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDCR0 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCR0 port map (QC, PADM);

Pad Logic

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	2.1	Eq-load

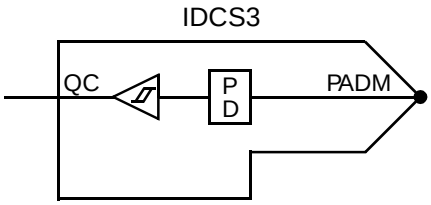
See page 2-13 for power equation.

Note: This special purpose, “resistive input” pad is not intended for use as a general input pad.

Description

IDCS3 is a non-inverting, CMOS-level Schmitt trigger input buffer piece with voltage hysteresis.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDCS3 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	17.0	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	1.37 1.01	1.49 1.19	1.58 1.30	1.65 1.39	1.72 1.47

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

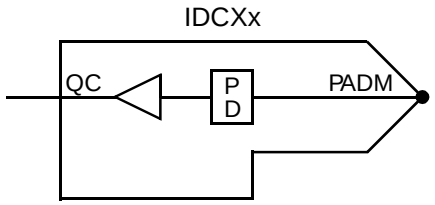
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

IDCXx is a family of non-inverting, CMOS-level input buffer pieces.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDCXx *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCXx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDCX3	IDCX6
PADM (pF)	4.90	4.90

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDCX3	0.0	TBD	10.4
IDCX6	0.0	TBD	18.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

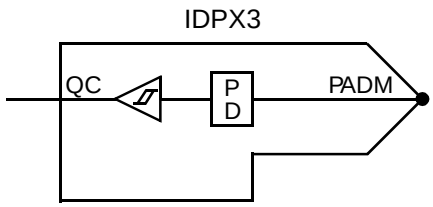
	Number of Equivalent Loads		1	11	22	32	43 (max)
IDCX3	From: PADM	t_{PLH}	0.63	0.79	0.90	1.00	1.09
	To: QC	t_{PHL}	0.63	0.76	0.88	0.98	1.07
	Number of Equivalent Loads		**1**	**11**	**22**	**32**	**43 (max)**
IDCX6	From: PADM	t_{PLH}	0.60	0.69	0.75	0.80	0.86
	To: QC	t_{PHL}	0.61	0.66	0.73	0.81	0.90

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

IDPX3 is a non-inverting, PCI-level input buffer piece. IDPX3 is for the 33MHz PCI ODPSXE16 piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDPX3 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDPX3 port map (QC, PADM);

Pin Loading

Pin Name	Load
	IDPX3
PADM (pF)	4.90

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDPX3	0.0	TBD	12.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	11	22	32	43 (max)
IDPX3	From: PADM	t_{PLH}	0.58	0.75	0.86	0.94	1.02
	To: QC	t_{PHL}	0.71	0.82	0.95	1.07	1.20

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

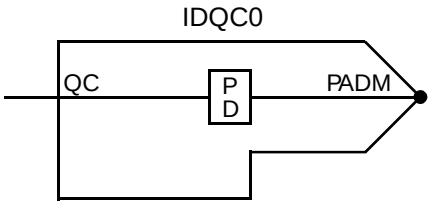
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

IDQC0 is a non-buffered, resistive crystal oscillator input receiver piece with ESD protection.

Logic Symbol



Truth Table

PADM	QO
L	L
H	H

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDQC0 *inst_name* (QO, PADM);

VHDL..... *inst_name*: IDQC0 port map (QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	2.1	Eq-load

See page 2-13 for power equation.

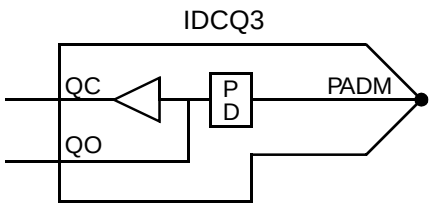
Design Notes:

The IDQC0 cell is for backward compatibility with existing oscillator methodologies.

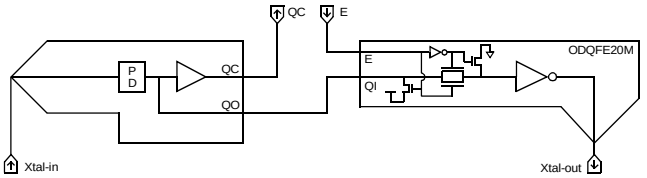
Description

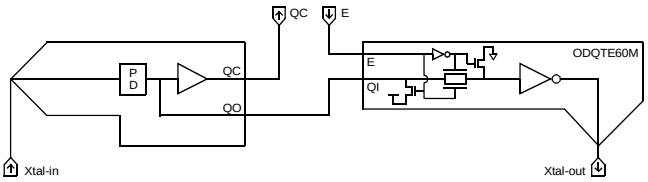
IDQC3 is a crystal oscillator input receiver pad piece with a non-inverting, CMOS-level clock input. QO is the output to either the ODQFE20M or the ODQTE60M. PADM is the bond pad from the Xtal-in.

Logic Symbol



The Possible Logic Schematic Combinations





Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load
PADM	4.90 pF

Pad Logic

HDL Syntax

Verilog ..... IDQC3 *inst_name (*QC, QO, PADM);

VHDL..... *inst_name*: IDQC3 port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	11.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	0.65 0.65	0.79 0.79	0.90 0.91	0.99 1.00	1.10 1.08
PADM	QO	t_{PLH} t_{PHL}	0.00 0.00				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

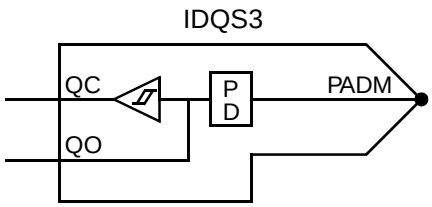
Design Notes:

The IDQC3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of either the ODQFE20M or the ODQTE60M oscillator output driver pad pieces. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

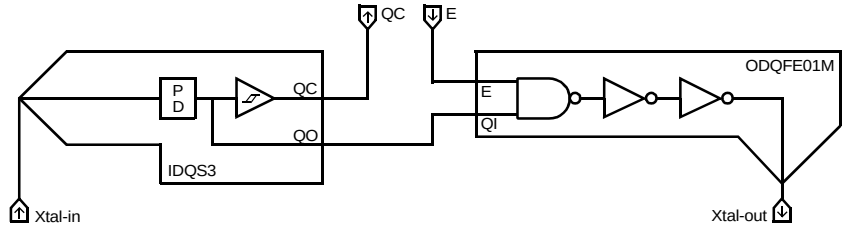
Description

IDQS3 is a crystal oscillator input receiver pad piece. QC is a non-inverting, CMOS-level schmitt trigger clock input buffer. QO is the output to the ODQFE01M. PADM is the bond pad from the Xtal-in.

Logic Symbol



Logic Schematic



Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load	
PADM	4.90	pF

HDL Syntax

Verilog ..... IDQS3 *inst_name* (QC, QO, PADM);

VHDL..... *inst_name*: IDQS3 port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	18.0	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	1.37 1.02	1.49 1.17	1.59 1.30	1.66 1.39	1.73 1.49
PADM	QO	t_{PLH} t_{PHL}	0.00 0.00				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

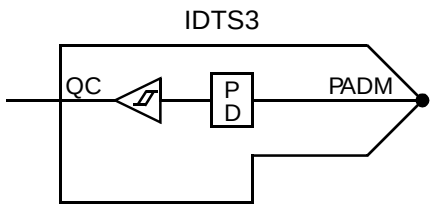
Design Notes:

The IDQS3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of the ODQFE01M oscillator output driver pad piece. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

Description

IDTS3 is a non-inverting, TTL-level Schmitt input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDTS3 inst_IDTS3 (QC, PADM);

VHDL..... inst_IDTS3 : IDTS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	15.8	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	0.99 1.72	1.03 1.89	1.11 2.02	1.20 2.12	1.33 2.21

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

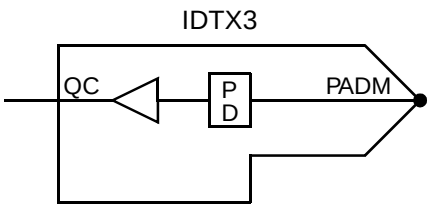
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

IDTX3 is a non-inverting, TTL-level, input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDTX3 *inst_name (*QC, PADM);

VHDL..... *inst_name*: IDTX3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	10.4	Eq-load

See page 2-13 for power equation.

Input Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

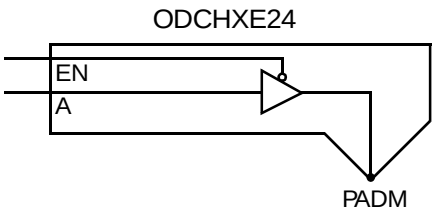
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	0.53 0.72	0.67 0.87	0.78 0.99	0.89 1.10	1.00 1.22

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODCHXE24 is a high performance, 24 mA, non-inverting, CMOS-level, tristate output buffer piece with active low enable.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Pin Loading

	Load
A	3.5 eql
EN	6.5 eql
PADM	4.93 pF

HDL Syntax

Verilog ..... ODCHXE24 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCHXE24 port map (PADM, A, EN);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	297.0	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	1.00 0.57	1.46 1.38	2.10 1.82	3.41 2.65	4.76 3.55
EN	PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.06 1.02 0.86 0.99	1.33 1.35	2.00 1.78	3.33 2.63	4.65 3.53

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

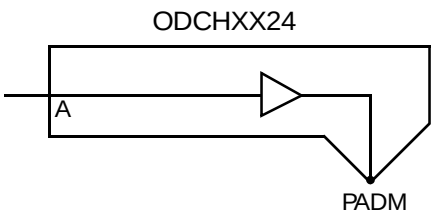
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

ODCHXX24 is a high performance, 24 mA, non-inverting, TTL-level output buffer piece.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

Pin Loading

	Load
A	14.5 eql

HDL Syntax

Verilog ..... ODCHXX24 *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCHXX24 port map (PADM, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	249.7	Eq-load

See page 2-13 for power equation.

Output Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

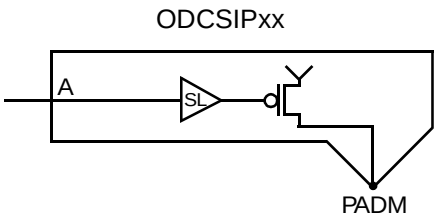
Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH}	0.67	1.13	1.78	3.10	4.42
		t_{PHL}	0.70	1.05	1.49	2.35	3.22

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODCSIPxx is a family of 4 to 8 mA, inverting, CMOS-level output buffer pieces with P-channel open-drains (pull-up) and controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	H
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODCSIPxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSIPxx port map (PADM, A);

Pin Loading

Pin Name	Load		
	ODCSIP04	ODCSIP08	ODCSIP12
A (eq-load)	4.1	4.1	4.1
PADM (pF)	4.94	4.94	4.94

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSIP04	4	TBD	190.5
ODCSIP08	8	TBD	203.6
ODCSIP12	12	TBD	216.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODCSIP04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	2.64	6.29	11.51	21.93	32.36
ODCSIP08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.75	3.62	6.31	11.65	16.94
ODCSIP12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.60	2.88	4.68	8.26	11.86

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

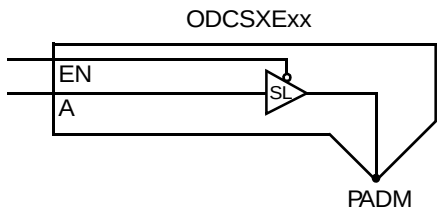
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Cell		
From	**To**		**ODCSIP04**	**ODCSIP08**	**ODCSIP12**
A	PADM	t_{HZ}	0.78	1.01	1.23

Description

ODCSXExx is a family of 4 to 16 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCSXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCSXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load			
	ODCSXE04	ODCSXE08	ODCSXE12	ODCSXE16
A (eq-load)	2.3	2.3	2.3	2.3
EN (eq-load)	6.9	6.9	6.9	6.9
PADM (pF)	4.94	4.94	4.94	4.94

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSXE04	4	TBD	218.9
ODCSXE08	8	TBD	240.3
ODCSXE12	12	TBD	261.1
ODCSXE16	16	TBD	283.9

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCSXE04	From: A To: PADM	t_{PLH} t_{PHL}	3.23 3.03	6.83 6.71	12.02 12.06	22.08 22.73	31.52 33.29
	From: EN To: PADM	t_{ZH} t_{ZL}	2.93 2.88	6.57 6.64	11.74 11.91	21.76 22.47	31.25 33.18
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE08	From: A To: PADM	t_{PLH} t_{PHL}	2.33 2.17	4.22 4.05	6.89 6.75	12.17 12.18	17.43 17.62
	From: EN To: PADM	t_{ZH} t_{ZL}	2.24 1.92	4.17 3.84	6.85 6.54	12.13 11.96	17.34 17.41
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE12	From: A To: PADM	t_{PLH} t_{PHL}	2.12 1.87	3.37 3.14	5.20 4.97	8.84 8.54	12.37 12.03
	From: EN To: PADM	t_{ZH} t_{ZL}	1.82 1.68	3.11 2.96	4.89 4.74	8.45 8.28	12.08 11.85
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE16	From: A To: PADM	t_{PLH} t_{PHL}	1.67 2.03	2.25 2.88	3.03 4.09	4.47 6.67	5.84 9.37
	From: EN To: PADM	t_{ZH} t_{ZL}	1.38 1.74	1.94 2.60	2.70 3.86	4.14 6.46	5.54 9.13

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

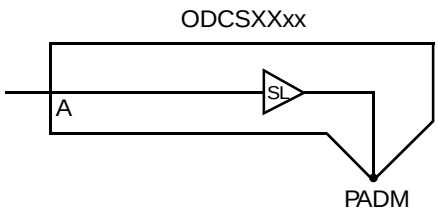
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell ODCSXE04	ODCSXE08	ODCSXE12	ODCSXE16
EN	PADM	t_{HZ} t_{LZ}	0.82 0.86	1.04 1.04	1.27 1.20	1.53 1.38

Description

ODCSXXxx is a family of 4 to 24 mA, non-inverting, CMOS-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCSXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSXXxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODCSXX04	ODCSXX08	ODCSXX12	ODCSXX16	ODCSXX24
A (eq-load)	9.3	9.3	9.3	9.3	11.4

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSXX04	4	TBD	198.6
ODCSXX08	8	TBD	220.0
ODCSXX12	12	TBD	240.8
ODCSXX16	16	TBD	263.6
ODCSXX24	24	TBD	282.3

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

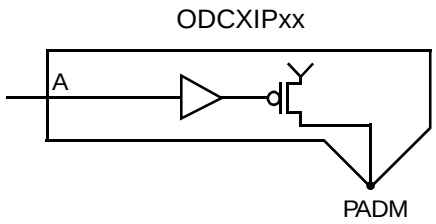
	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCSXX04	From: A	t_{PLH}	2.46	6.09	11.15	20.96	30.46
	To: PADM	t_{PHL}	2.44	6.13	11.43	22.05	32.67
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXX08	From: A	t_{PLH}	1.50	3.36	6.05	11.29	16.36
	To: PADM	t_{PHL}	1.64	3.50	6.19	11.60	17.04
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXX12	From: A	t_{PLH}	1.35	2.58	4.36	7.94	11.51
	To: PADM	t_{PHL}	1.47	2.58	4.31	7.87	11.40
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXX16	From: A	t_{PLH}	1.29	2.19	3.51	6.18	8.80
	To: PADM	t_{PHL}	1.44	2.30	3.56	6.13	8.75
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXX24	From: A	t_{PLH}	1.31	2.20	3.50	6.12	8.76
	To: PADM	t_{PHL}	1.12	1.71	2.55	4.26	6.01

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODCXIPxx is a family of 1 to 8 mA, inverting, CMOS-level, output buffer pieces with P-channel, open-drains (pull-up).

Logic Symbol



Truth Table

A	PADM
L	H
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODCXIPxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCXIPxx port map (PADM, A);

Pin Loading

Pin Name	Load			
	ODCXIP01	ODCXIP02	ODCXIP04	ODCXIP08
A (eq-load)	2.8	2.8	2.8	3.9
PADM (pF)	4.92	4.92	4.92	4.93

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static IDD (TJ = 85°C) (nA)	EQLpd (Eq-load)
ODCXIP01	1	TBD	148.8
ODCXIP02	2	TBD	153.6
ODCXIP04	4	TBD	162.0
ODCXIP08	8	TBD	178.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODCXIP01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{ZH}	4.73	6.87	8.98	12.13	17.31
ODCXIP02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{ZH}	2.54	6.19	8.78	11.38	16.61
ODCXIP04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.75	3.62	6.26	11.57	16.92
ODCXIP08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.33	2.26	3.59	6.24	8.91

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

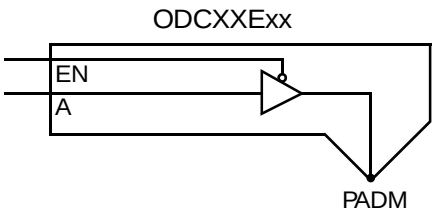
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			ODCXIP01	**ODCXIP02**	**ODCXIP04**	**ODCXIP08**
APADM		t_{HZ}	1.04	0.89	1.05	1.38

Description

ODCXXExx is a family of 1 to 24 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCXXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCXXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load						
	ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12	ODCXXE16	ODCXXE24
A (eq-load)	5.6	7.9	7.9	2.3	2.3	2.3	2.3
EN (eq-load)	4.0	5.3	5.3	5.5	5.5	5.5	5.5
PADM (pF)	4.92	4.92	4.93	4.93	4.93	4.93	4.93

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXXE01	1	TBD	154.9
ODCXXE02	2	TBD	164.2
ODCXXE04	4	TBD	174.8
ODCXXE08	8	TBD	223.0
ODCXXE12	12	TBD	243.9
ODCXXE16	16	TBD	268.0
ODCXXE24	24	TBD	279.9

a. See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Capacitive Load (pF)		15	25	35	50	75 (max)
ODCXXE01	From: A To: PADM	t_{PLH} t_{PHL}	4.70 4.92	6.77 7.09	8.86 9.26	12.04 12.53	17.40 18.02
	From: EN To: PADM	t_{ZH} t_{ZL}	4.94 4.98	7.05 7.06	9.16 9.18	12.32 12.44	17.58 18.06
	Capacitive Load (pF)		**15**	**50**	**75**	**100**	**150 (max)**
ODCXXE02	From: A To: PADM	t_{PLH} t_{PHL}	2.53 2.55	6.22 6.27	8.83 8.94	11.42 11.60	16.58 16.89
	From: EN To: PADM	t_{ZH} t_{ZL}	2.75 2.62	6.39 6.32	8.97 8.96	11.57 11.61	16.83 16.96
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCXXE04	From: A To: PADM	t_{PLH} t_{PHL}	1.65 1.82	3.57 3.58	6.27 6.20	11.58 11.51	16.83 16.77
	From: EN To: PADM	t_{ZH} t_{ZL}	1.85 1.72	3.67 3.62	6.29 6.25	11.61 11.49	16.98 16.82
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCXXE08	From: A To: PADM	t_{PLH} t_{PHL}	1.86 1.57	2.79 2.48	4.08 3.78	6.73 6.39	9.43 8.99
	From: EN To: PADM	t_{ZH} t_{ZL}	1.51 1.40	2.48 2.31	3.83 3.58	6.49 6.17	9.14 8.83
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCXXE12	From: A To: PADM	t_{PLH} t_{PHL}	1.22 1.61	1.93 2.21	2.87 3.03	4.69 4.74	6.46 6.53
	From: EN To: PADM	t_{ZH} t_{ZL}	1.48 1.26	2.20 1.93	3.12 2.83	4.91 4.59	6.72 6.31
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCXXE16	From: A To: PADM	t_{PLH} t_{PHL}	2.12 1.59	2.36 2.07	3.04 2.75	4.47 4.07	5.74 5.34
	From: EN To: PADM	t_{ZH} t_{ZL}	1.53 1.33	2.13 1.86	2.86 2.56	4.23 3.89	5.55 5.18
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCXXE24	From: A To: PADM	t_{PLH} t_{PHL}	1.87 1.53	2.37 1.91	3.07 2.43	4.45 3.39	5.80 4.22
	From: EN To: PADM	t_{ZH} t_{ZL}	1.42 1.26	2.04 1.71	2.78 2.26	4.14 3.22	5.48 4.09

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell					
			ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12	ODCXXE16
EN	PADM	t_{HZ}	1.45	1.20	1.59	1.24	1.62	2.01
		t_{LZ}	0.41	0.38	0.55	1.09	1.30	1.60

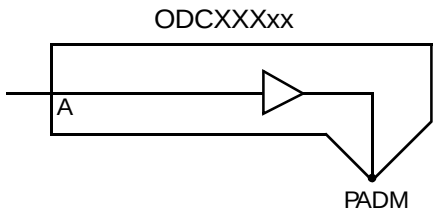
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

ODCXXXxx is a family of 1 to 24 mA, non-inverting, CMOS-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCXXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCXXXxx port map (PADM, A);

Pin Loading

Pin Name	Load						
	ODCXXX01	ODCXXX02	ODCXXX04	ODCXXX08	ODCXXX12	ODCXXX16	ODCXXX24
A (eq-load)	4.3	4.3	6.2	8.3	8.2	8.2	10.3

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXXX01	1	TBD	149.5
ODCXXX02	2	TBD	155.0
ODCXXX04	4	TBD	165.6
ODCXXX08	8	TBD	189.8
ODCXXX12	12	TBD	210.7
ODCXXX16	16	TBD	234.8
ODCXXX24	24	TBD	248.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODCXXX01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	4.55 4.71	6.53 6.90	8.68 9.09	11.93 12.37	17.07 17.81
ODCXXX02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.46 2.77	6.13 6.39	8.76 9.02	11.37 11.68	16.53 17.05
ODCXXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.45 1.52	3.31 3.43	5.97 6.09	11.30 11.35	16.62 16.64
ODCXXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.17 1.22	2.11 2.12	3.45 3.41	6.11 6.00	8.76 8.61
ODCXXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To PADM	t_{PLH} t_{PHL}	1.15 1.20	1.85 1.86	2.80 2.74	4.61 4.47	6.36 6.19
ODCXXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.29 1.33	1.83 1.85	2.54 2.56	3.91 3.90	5.24 5.15
ODCXXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.27 1.09	1.80 1.51	2.51 2.02	3.87 2.94	5.17 3.81

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

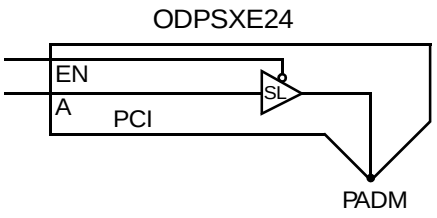
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

ODPSXE24 is a 33 MHz PCI, non-inverting, tristate buffer piece with active low enable and controlled slew rate output.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Pin Loading

	Load
A	8.2 pF
EN	5.5 pF
PADM	4.93 pF

HDL Syntax

Verilog ..... ODPSXE24 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODPSXE24 port map (PADM, A, EN);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	229.2	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

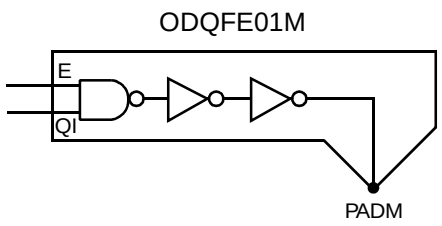
Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	1.50 2.08	1.92 2.70	2.41 3.62	3.33 5.52	4.28 7.49
EN	PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	3.47 2.49 1.41 1.46	 1.83 2.37	 2.37 3.45	 3.42 5.46	 4.43 7.46

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

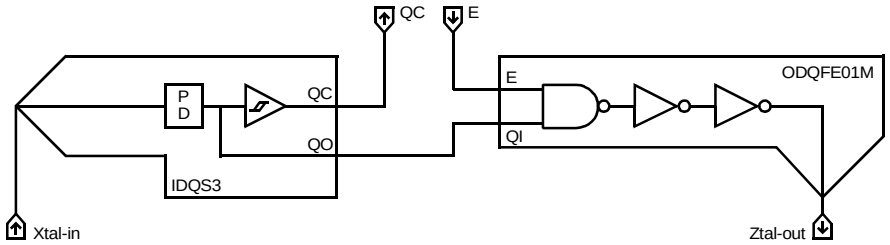
Description

ODQFE01M is a fundamental mode, enabled crystal oscillator, output driver pad piece that runs over a frequency range of 32 kHz - 1 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
L	H	H
H	H	L
H	L	X

Pin Loading

	Load
E	4.0 eql
QI	3.2 eql

Pad Logic

HDL Syntax

Verilog ..... ODQFE01M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQFE01M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	151.7	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
E	PADM	t_{PLH} t_{PHL}	4.93 5.52	6.91 7.71	9.09 9.90	12.33 13.18	17.45 18.61
QI	PADM	t_{PLH} t_{PHL}	4.96 5.56	7.06 7.75	9.17 9.95	12.33 13.25	17.59 18.66

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

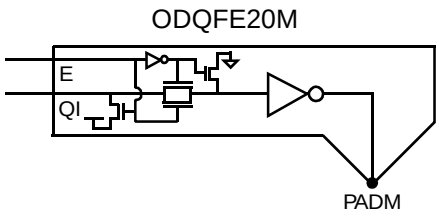
Design Notes:

The ODQFE01M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQS3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

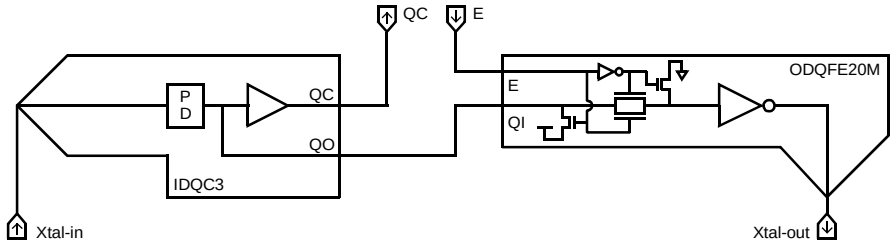
Description

ODQFE20M is a fundamental mode, enabled crystal oscillator, output buffer pad piece that runs over a frequency range of 1 MHz - 20 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to the Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
H	L	X
H	H	L
L	H	H

Pin Loading

	Load
E	6.5 eql
QI	5.5 eql

Pad Logic

HDL Syntax

Verilog ..... ODQFE20M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQFE20M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	165.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
E	PADM	t_{PLH} t_{PHL}	3.40 2.46	7.03 6.17	9.59 8.85	12.18 11.53	17.46 16.78
QI	PADM	t_{PLH} t_{PHL}	2.40 2.51	6.00 6.18	8.60 8.81	11.21 11.46	16.40 16.80

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

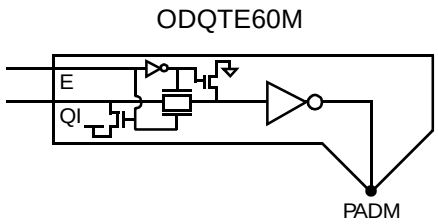
Design Notes:

The ODQFE20M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

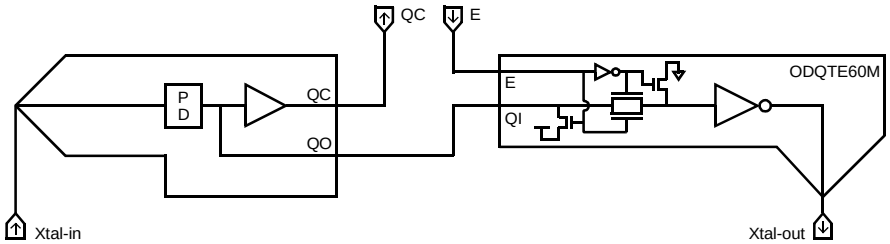
Description

ODQTE60M is an enabled crystal oscillator, output driver pad piece that runs over a frequency range of 20 - 60 MHz. QI is the input from the IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
H	L	X
H	H	L
L	H	H

Pin Loading

	Load
E	6.5 eql
QI	5.5 eql

Pad Logic

HDL Syntax

Verilog ..... ODQTE60M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQTE60M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	176.1	Eq-load

See page 2-13 for power equation.

AMI5HS 0.5 micron CMOS Standard Cell

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	50	100	200	300 (max)
E	PADM	t_{PLH} t_{PHL}	2.78 1.53	4.63 3.37	7.29 6.01	12.61 11.28	17.93 16.57
QI	PADM	t_{PLH} t_{PHL}	1.53 1.54	3.38 3.43	6.03 6.06	11.33 11.30	16.64 16.60

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

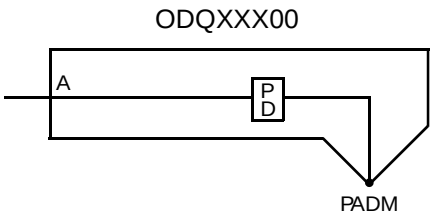
Design Notes:

The ODQTE60M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

Description

ODQXXX00 is a non-buffered, resistive analog crystal oscillator output pad piece with ESD protection.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

Pin Loading

	Load
A	2.4 eql

HDL Syntax

Verilog ..... ODQXXX00 *inst_name* (PADM, A);

VHDL..... *inst_name*: ODQXXX00 port map (PADM, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	137.5	Eq-load

See page 2-13 for power equation.

ODTHXE24

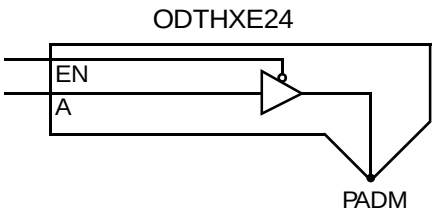
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

ODTHXE24 is a high performance, 24 mA, non-inverting, TTL-level, tristate output buffer piece with active low enable.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Pin Loading

	Load
A	3.5 eql
EN	6.5 eql
PADM	4.93 pF

HDL Syntax

Verilog ..... ODTHXE24 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODTHXE24 port map (PADM, A, EN);

Pad Logic

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	297.0	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

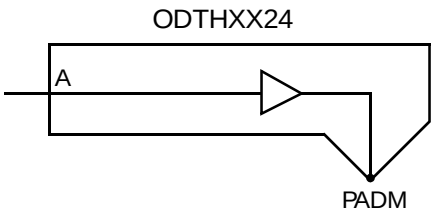
Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	0.89 1.19	1.17 1.64	1.55 2.30	2.26 3.60	2.94 4.91
EN	PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.06 1.02 0.70 1.10	 0.96 1.59	 1.32 2.27	 2.03 3.59	 2.74 4.88

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODTHXX24 is a high performance,24 mA, non-inverting, TTL-level output buffer piece.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

Pin Loading

	Load
A	14.5 eql

HDL Syntax

Verilog **.....** ODTHXX24 *inst_name* (PADM, A);

VHDL*.....* *inst_name*: ODTHXX24 port map (PADM, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	249.7	Eq-load

See page 2-13 for power equation.

Output Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH}	0.54	0.81	1.16	1.84	2.57
		t_{PHL}	0.84	1.30	1.95	3.25	4.56

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

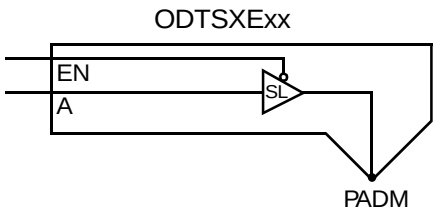
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

ODTSXExx is a family of 4 to 24 mA, non-inverting, TTL-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog **.....** ODTSXExx *inst_name* (PADM, A, EN);

VHDL*.....* *inst_name*: ODTSXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load				
	ODTSXE04	ODTSXE08	ODTSXE12	ODTSXE16	ODTSXE24
A (eq-load)	2.3	2.3	2.3	2.3	2.3
EN (eq-load)	6.9	6.9	6.9	6.9	6.9
PADM (pF)	4.94	4.94	4.94	4.94	4.94

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTSXE04	4	TBD	218.9
ODTSXE08	8	TBD	240.3
ODTSXE12	12	TBD	261.1
ODTSXE16	16	TBD	283.9
ODTSXE24	24	TBD	302.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODTSXE04	From: A To: PADM	t_{PLH} t_{PHL}	2.53 4.24	4.23 9.70	7.00 17.28	12.66 32.07	18.22 46.58
	From: EN To: PADM	t_{ZH} t_{ZL}	1.65 3.99	3.91 9.44	6.79 16.99	12.31 31.78	18.00 46.36
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTSXE08	From: A To: PADM	t_{PLH} t_{PHL}	1.82 2.62	2.84 5.68	4.27 9.82	7.12 17.67	9.98 25.18
	From: EN To: PADM	t_{ZH} t_{ZL}	1.46 2.53	2.51 5.45	3.97 9.54	6.83 17.43	9.65 24.94
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTSXE12	From: A To: PADM	t_{PLH} t_{PHL}	1.71 2.61	2.43 4.23	3.40 6.93	5.32 12.29	7.25 17.32
	From: EN To: PADM	t_{ZH} t_{ZL}	1.42 1.96	2.14 3.96	3.11 6.72	5.03 12.01	6.96 17.11
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTSXE16	From: A To: PADM	t_{PLH} t_{PHL}	1.73 2.15	2.28 3.52	3.02 5.54	4.45 9.49	5.85 13.31
	From: EN To: PADM	t_{ZH} t_{ZL}	1.39 1.91	1.96 3.36	2.70 5.34	4.13 9.23	5.55 13.16
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTSXE24	From: A To: PADM	t_{PLH} t_{PHL}	1.72 1.96	2.26 2.90	3.01 4.22	4.45 6.84	5.87 9.47
	From: EN To: PADM	t_{ZH} t_{ZL}	1.48 1.63	2.04 2.59	2.78 3.94	4.22 6.58	5.63 9.19

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell				
			ODTSXE04	**ODTSXE08**	**ODTSXE12**	**ODTSXE16**	**ODTSXE24**
EN	PADM	t_{HZ} t_{LZ}	0.82 0.86	1.04 1.04	1.27 1.20	1.53 1.38	1.42 1.46

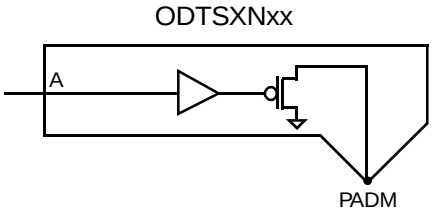
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

ODTSXNxx is a family of 4 to 24 mA, non-inverting, TTL-level, output buffer pieces with N-channel open-drains (pull-down) and controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	Z

Z = High Impedance

HDL Syntax

Verilog **.....** ODTSXNxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODTSXNxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODTSXN04	ODTSXN08	ODTSXN12	ODTSXN16	ODTSXN24
A (eq-load)	8.1	8.1	8.1	8.1	8.1
PADM (pF)	4.90	4.90	4.90	4.90	4.90

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTSXN04	4	TBD	164.3
ODTSXN08	8	TBD	172.6
ODTSXN12	12	TBD	180.2
ODTSXN16	16	TBD	188.3
ODTSXN24	24	TBD	200.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODTSXN04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{ZL}	3.28	8.54	15.91	30.44	44.81

ODTSXN08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	2.02	4.79	8.62	16.16	23.65
ODTSXN12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.45	3.36	5.94	10.94	15.84
ODTSXN16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.16	2.62	4.58	8.31	11.90
ODTSXN24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.03	2.00	3.34	5.92	8.40

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Cell				
From	**To**		**ODTSXN04**	**ODTSXN08**	**ODTSXN12**	**ODTSXN16**	**ODTSXN24**
A	PADM	t_{LZ}	0.80	0.93	1.05	1.19	1.37

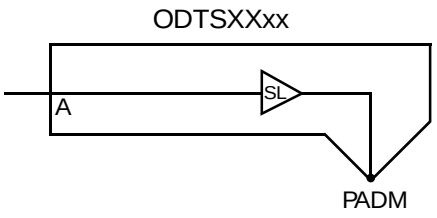
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

ODTSXXxx is a family of 4 to 24 mA, non-inverting, TTL-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog **.....** ODTSXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODTSXXxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODTSXX04	ODTSXX08	ODTSXX12	ODTSXX16	ODTSXX24
A (eq-load)	9.3	9.3	9.3	9.3	11.4

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTSXX04	4	TBD	198.6
ODTSXX08	8	TBD	220.0
ODTSXX12	12	TBD	240.8
ODTSXX16	16	TBD	263.6
ODTSXX24	24	TBD	282.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODTSXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	1.51	3.44	6.21	11.80	17.44
	To: PADM	t_{PLH}	3.60	8.97	16.46	31.17	45.68
ODTSXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	1.01	2.03	3.46	6.29	9.16
	To: PADM	t_{PLH}	2.19	5.12	9.13	16.85	24.39
ODTSXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	0.97	1.63	2.58	4.49	6.41
	To: PADM	t_{PLH}	1.82	3.72	6.37	11.54	16.57
ODTSXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	1.01	1.52	2.22	3.62	5.05
	To: PADM	t_{PLH}	1.60	2.98	4.96	8.83	12.60
ODTSXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	1.07	1.55	2.25	3.65	5.05
	To: PADM	t_{PLH}	1.31	2.20	3.52	6.14	8.73

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

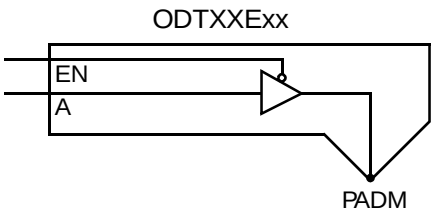
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

ODTXXExx is a family of 1 to 24 mA, non-inverting, TTL-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Z = High Impedance

HDL Syntax

Verilog **.....** ODTXXExx *inst_name* (PADM, A, EN);

VHDL*.....* *inst_name*: ODTXXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load						
	ODTXXE01	ODTXXE02	ODTXXE04	ODTXXE08	ODTXXE12	ODTXXE16	ODTXXE24
A (eq-load)	5.6	7.9	7.9	2.3	2.3	2.3	2.3
EN (eq-load)	4.0	5.3	5.3	5.5	5.5	5.5	5.5
PADM (pF)	4.92	4.92	4.93	4.93	4.93	4.93	4.93

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTXXE01	1	TBD	154.9
ODTXXE02	2	TBD	164.2
ODTXXE04	4	TBD	174.8
ODTXXE08	8	TBD	223.0
ODTXXE12	12	TBD	243.9
ODTXXE16	16	TBD	268.0
ODTXXE24	24	TBD	279.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Capacitive Load (pF)		15	25	35	50	75 (max)
ODTXXE01	From: A To: PADM	t_{PLH} t_{PHL}	2.85 7.15	3.95 10.42	5.07 13.74	6.76 18.76	9.64 27.24
	From: EN To: PADM	t_{ZH} t_{ZL}	2.85 7.28	4.03 10.47	5.21 13.71	6.93 18.69	9.67 27.25
	Capacitive Load (pF)		**15**	**50**	**75**	**100**	**150 (max)**
ODTXXE02	From: A To: PADM	t_{PLH} t_{PHL}	1.59 3.67	3.57 9.28	4.97 13.29	6.37 17.31	9.18 25.37
	From: EN To: PADM	t_{ZH} t_{ZL}	1.75 3.62	3.77 9.32	5.18 13.36	6.57 17.37	9.31 25.36
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTXXE04	From: A To: PADM	t_{PLH} t_{PHL}	1.02 2.27	2.19 5.06	3.66 9.01	6.47 17.01	9.36 24.98
	From: EN To: PADM	t_{ZH} t_{ZL}	1.33 2.68	2.36 5.09	3.81 9.03	6.68 17.08	9.52 25.00
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTXXE08	From: A To: PADM	t_{PLH} t_{PHL}	1.47 1.55	2.02 2.90	2.76 4.87	4.19 8.83	5.61 12.75
	From: EN To: PADM	t_{ZH} t_{ZL}	1.32 1.64	1.82 3.05	2.53 5.01	3.96 8.94	5.39 12.91
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTXXE12	From: A To: PADM	t_{PLH} t_{PHL}	1.53 1.73	1.96 2.65	2.48 3.98	3.46 6.62	4.43 9.22
	From: EN To: PADM	t_{ZH} t_{ZL}	1.23 1.48	1.67 2.45	2.22 3.77	3.22 6.42	4.14 9.05
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTXXE16	From: A To: PADM	t_{PLH} t_{PHL}	1.55 1.87	1.91 2.58	2.36 3.57	3.14 5.52	3.85 7.48
	From: EN To: PADM	t_{ZH} t_{ZL}	1.25 1.44	1.64 2.23	2.09 3.27	2.87 5.27	3.59 7.22
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTXXE24	From: A To: PADM	t_{PLH} t_{PHL}	1.70 1.70	2.00 2.26	2.39 2.99	3.15 4.34	3.89 5.61
	From: EN To: PADM	t_{ZH} t_{ZL}	1.31 0.69	1.68 2.03	2.13 2.78	2.91 4.11	3.60 5.47

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

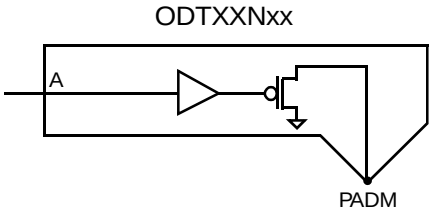
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell						
			ODTXXE01	ODTXXE02	ODTXXE04	ODTXXE08	ODTXXE12	ODTXXE16	ODTXXE24
EN	PADM	t_{HZ}	1.45	1.20	1.59	1.24	1.62	2.01	2.01
		t_{LZ}	0.41	0.38	0.55	1.09	1.30	1.60	1.96

Description

ODTXXNxx is a family of 1 to 24 mA, non-inverting, TTL-level, output buffer pieces with N-channel, open-drains (pull-down).

Logic Symbol



Truth Table

A	PADM
L	L
H	Z

Z = High Impedance

HDL Syntax

Verilog **.....** ODTXXNxx *inst_name* (PADM, A);

VHDL*.....* *inst_name*: ODTXXNxx port map (PADM, A);

Pin Loading

Pin Name	Load						
	ODTXXN01	ODTXXN02	ODTXXN04	ODTXXN08	ODTXXN12	ODTXXN16	ODTXXN24
A (eq-load)	4.3	4.3	4.3	8.3	8.3	8.3	8.3
PADM (pF)	4.90	4.90	4.91	4.90	4.91	4.91	4.91

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTXXN01	1	TBD	141.7
ODTXXN02	2	TBD	143.5
ODTXXN04	4	TBD	147.6
ODTXXN08	8	TBD	156.9
ODTXXN12	12	TBD	163.7
ODTXXN16	16	TBD	173.1
ODTXXN24	24	TBD	184.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODTXXN01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{ZL}	6.55	9.90	13.24	18.24	26.55
ODTXXN02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{ZL}	3.25	9.06	13.05	17.03	25.12
ODTXXN04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.93	4.75	8.75	16.74	24.70
ODTXXN08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.17	2.55	4.52	8.47	12.40
ODTXXN12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.99	1.95	3.28	5.92	8.56
ODTXXN16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.96	1.73	2.74	4.72	6.70
ODTXXN24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.84	1.49	2.23	3.56	4.90

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

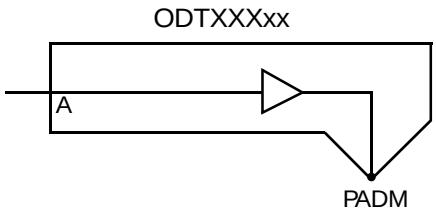
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell						
			ODTXXN01	**ODTXXN02**	**ODTXXN04**	**ODTXXN08**	**ODTXXN12**	**ODTXXN16**	**ODTXXN24**
A	PADM	t_{LZ}	0.23	0.31	0.48	0.56	0.74	1.02	1.35

Description

ODTXXXxx is a family of 1 to 24 mA, non-inverting, TTL-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODTXXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODTXXXxx port map (PADM, A);

Pin Loading

Pin Name	Load						
	ODTXXX01	ODTXXX02	ODTXXX04	ODTXXX08	ODTXXX12	ODTXXX16	ODTXXX24
A (eq-load)	4.3	4.3	6.2	8.3	8.2	8.2	10.3

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTXXX01	1	TBD	149.5
ODTXXX02	2	TBD	155.0
ODTXXX04	4	TBD	165.6
ODTXXX08	8	TBD	189.8
ODTXXX12	12	TBD	210.7
ODTXXX16	16	TBD	234.8
ODTXXX24	24	TBD	248.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Capacitive Load (pF)		15	25	35	50	75 (max)
ODTXXX01	From: A	t_{PLH}	2.52	3.69	4.86	6.58	9.33
	To: PADM	t_{PHL}	7.11	10.44	13.76	18.75	27.11

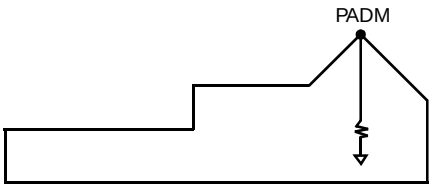
AMI5HS 0.5 micron CMOS Standard Cell

ODTXXX02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.63 3.87	3.59 9.51	4.99 13.53	6.38 17.54	9.20 25.55
ODTXXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.02 2.18	2.04 4.90	3.46 8.88	6.31 16.87	9.18 24.84
ODTXXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.91 1.50	1.45 2.87	2.15 4.82	3.57 8.75	5.02 12.69
ODTXXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.97 1.40	1.37 2.35	1.87 3.66	2.85 6.27	3.84 8.91
ODTXXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.10 1.59	1.41 2.33	1.80 3.33	2.58 5.29	3.34 7.24
ODTXXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.05 1.26	1.39 1.80	1.80 2.53	2.54 3.88	3.27 5.17

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

PLD3 is an active pull-down buffer piece.

Logic Symbol	Truth Table	Pin Loading
PLD3  	N/A	N/A

HDL Syntax

Verilog ..... PLD3 *inst_name* (PADM);

VHDL..... *inst_name*: PLD3 port map (PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	149.8	Eq-load

See page 2-13 for power equation.

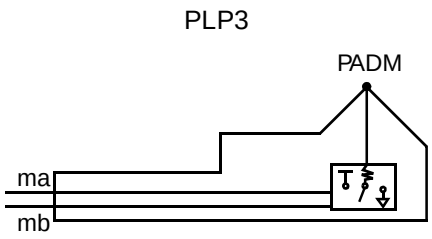
AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

PLP3 is a programmable pull-up/pull-down buffer piece.

Logic Symbol



Truth Table

MA	MB	PADM Function
L	L	Pull-down
H	H	Pull-up
H	L	Tristate
L	H	Tristate

Pin Loading

	Load
MA	2.1 eql
MB	1.8 eql

HDL Syntax

Verilog ..... PLP3 *inst_name* (PADM, MA, MB);

VHDL..... *inst_name*: PLP3 port map (PADM, MA, MB);

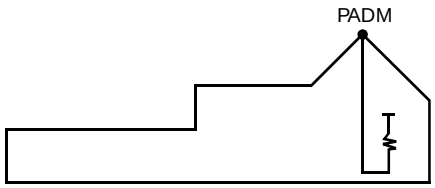
Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	146.8	Eq-load

See page 2-13 for power equation.

Description

PLU3 is an active pull-up buffer piece.

Logic Symbol	Truth Table	Pin Loading
PLU3 PADM 	N/A	N/A

HDL Syntax

Verilog ..... PLU3 *inst_name* (PADM);

VHDL..... *inst_name*: PLU3 port map (PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	149.7	Eq-load

See page 2-13 for power equation.

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

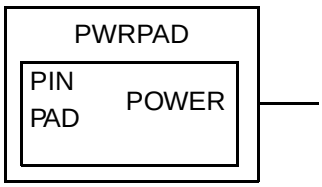
PWRPAD

AMERICAN MICROSYSTEMS, INC.

AMI5HS 0.5 micron CMOS Standard Cell

Description

PWRPAD is a generic power pad used to define the connection of a chip power pin to logical buses in the device. For more information on power and ground buses, as well as PWRPAD usage see “Interconnect Load Estimation” on page 2-15.



PWRPAD has the following parameters:

- LVDD: this parameter receives a string value that defines the name of the power supply that PWRPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that PWRPAD connects to.

Verilog Syntax

```
defparam SUPPLY_5V.LVDD = "PAD_5V",
         SUPPLY_5V.CONTACT = "IPWR,OPWR1";
PWRPAD SUPPLY_5V (.PADM(VDD_5V));
```

VHDL syntax

```
SUPPLY_5V : PWRPAD generic map (LVDD => "PAD_5V", CONTACT => "IPWR,OPWR1")
         port map (PADM => VDD_5V);
```

Bolt syntax

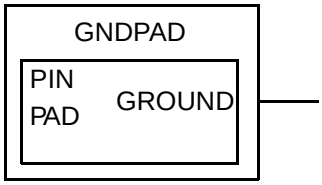
```
PWRPAD/SUPPLY_5V VDD_5V (LVDD='PAD_5V' CONTACT="IPWR,OPWR1");
```

where:

- SUPPLY_5V is the instance name for PWRPAD
- PAD_5V is the name of the supply
- IPWR, OPWR1 are logical buses (see section ...)
- VDD_5V is the chip port name

Description

GNDPAD is a generic ground pad used to define the connection of a chip ground pin to logical buses in the device. For more information on power and ground buses, as well as GNDPAD usage see “Interconnect Load Estimation” on page 2-15.



GNDPAD has the following parameters:

- LVSS: this parameter receives a string value that defines the name of the ground that GNDPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that GNDPAD connects to.

Verilog syntax

```
defparam GROUND1.LVSS = "VSS",
         GROUND1.CONTACT = "CGND,OGND";
GNDPAD GROUND1 (.PADM(VSS1));
```

VHDL syntax

```
GROUND1 : GNDPAD generic map (LVSS => "VSS", CONTACT => "CGND,OGND")
         port map (PADM => VSS1);
```

Bolt syntax

```
.GNDPAD/GROUND1 VSS1 (LVSS='VSS' CONTACT="CGND,OGND");
```

where:

- GROUND1 is the instance name for GNDPAD
- VSS is the name of the supply
- CGND,OGND are logical buses (see section ...)
- VSS1 is the chip port name

SECTION 5
MEGACELLS

Megacell Overview

AMI provides a wide selection of megacells to simplify the design of complex gate array and standard cell ASICs. AMI's megacells provide industry standard functions that are proven in silicon. Using megacells may reduce design time and cost, board space, system costs, and power requirements while increasing reliability and performance.

AMI's megacells are complex blocks of logic that implement a digital function. The function is often compatible to a standard product, such as an 8051. Other times, the function is more generic—a configurable PCI controller, for example. Most of AMI's megacells are "soft" or "firm" cores. Soft megacells are HDL based in an RTL form. They are technology independent and can be customized for specific applications. Synthesis is performed by the customer to create a firm core (a netlist) based on the customer's specifications. AMI's firm megacells are netlist based in Verilog or VHDL. The netlist based megacells can be customized by the end user. Scan test may be inserted at the netlist level if desired.

AMI's megacells are broken down into cores (8051 and 6502 code compatibles, etc.), peripherals (UARTs, SCSI controllers, timers, RTCs, etc.), datapath (multipliers, adders, shifters, etc.), and FIFOs. AMI core processors and peripherals duplicate the function of industry standard parts. Datapath and FIFO megacells are developed using parameterized logic synthesizers.

Advantages of Megacells

The advantages of using megacells in ASIC design include 1) decreased design time and cost by providing large building blocks that are the equivalent of standard products and functions; 2) reduced power consumption in comparison to the standard product that the megacell replaces; 3) reduced printed circuit board space, capacitance, and power (to get signals on and off ICs) because several functions can be put on a single die; 4) improved reliability and lower system costs because of decreased part and pin counts; and 5) improved performance compared to the original standard product because the megacell is typically implemented in a more advanced process technology.

AMI's firm megacells provide flexibility for design changes, testability, fault grading, design checking, process selection, and design implementation as a gate array or standard cell. Firm megacells are easily ported to new processes as they become available.

AMI's megacells are built with fully static logic and no internal tristates.

Megacell characteristics and functions can be changed as needed. For example, to change the initial conditions of the MGMC32 output ports, the output port flip-flop in each port cell is changed from a set type of flop to a reset type of flop.

Gate count can be minimized by deleting unused functions. If a timer or UART is not being used, it can be deleted to lower the gate count. Simulations must validate the correct implementation of the design change.

Firm megacells with a netlist implementation benefit from design checking software that checks all the circuitry for flip-flop set up and hold times, asynchronous race conditions, and test vector fault coverage. Behavioral models, which are frequently used with hard megacells, bypass these checks.

Processor Cores and Peripherals

Core processor and peripheral megacells duplicate the function of industry standard parts. AMI's megacell data sheets give a short overview, define the cell pinout, and outline any functional differences between AMI's megacell and the industry standard part. The standard device data sheets provide detailed functional information.

Table 1: Processor Cores

MEGACELL	FUNCTION
MG29C01	4-bit microprocessor slice
MG29C10	Microprogram controller/sequencer
MG65C02	8-bit microprocessor
M8042	8-bit slave microcontroller
M8048	8-bit microcontroller
MGMC32	8051 compatible processor
MGMC32FB	8051FB compatible processor
MGMC32SD	Reduced function MGMC32
M320C25	16-bit fixed point DSP
M320C50	16-bit fixed point DSP

AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Table 2: Processor Cores

MEGACELL	FUNCTION
MG1468C18	Real-time clock
M16C450	UART
M16C550	UART
M6402	UART
M6845	CRT controller
M765A	Floppy disk controller
M8251A	Communication interface USART
M8253	Programmable interval timer
M82530	Serial communications controller
MG82C37A	Programmable DMA controller
MG82C50A	Asynchronous comm. element
MG82C54	Programmable interval timer
MG82C55A	Programmable peripheral interface
MG82C59A	Programmable interrupt controller
M8490	SCSI controller
M85C30	Serial communications controller
M8868A	UART
M91C36	Digital data separator
M91C360	Digital data separator
MFDC	Floppy disk controller
MGI2CSL	I^2C Serial bus slave transceiver
MI2C	I^2C Bus interface

Datapath and FIFOs

Most datapath and FIFO megacells are produced using parameterized synthesizers. The synthesizers create various megacell sizes and speeds that are optimized for either minimum delay or gate count, or designed to meet a specified delay.

These synthesizers produce firm megacell netlists and are available on various workstations. AMI's datapath and FIFO data sheets contain a functional description, a pin description, and sample equivalent gate counts with sample delays.

Table 3: Datapath

MEGACELL	FUNCTION
MGAxxyyDv	Adder
MGAxxyyEv	Adder-subtractor
MGBxxyyAv	Barrel/arithmetic shifter
MGBxxBv	Barrel shifter
MGBxxyyCv	Arithmetic shifter
MGCDxxAv	Decrement Counter
MGCUxxAv	Increment Counter
MGCxxAv	2-function binary comparator
MGCxxBv	6-function binary comparator
MGDxxAv	Decrementer
MGIxxAv	Incrementer
MGIxxBv	Incrementer/decrementer
MGMxxyyDv	Signed/unsigned multiplier
MGMxxyyEv	Multiplier-accumulator
MGSxxyyAv	Signed/unsigned subtractor

Table 4: FIFOs

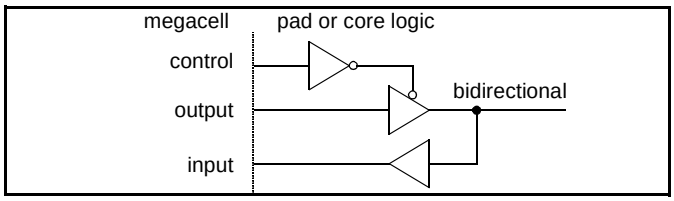
MEGACELL	FUNCTION
MGFxxyyC1	Fall-through FIFO (latch-based)
MGFxxxxyyD	Synchronous FIFO (dual-port RAM based)
MGFxxxxyyE	Asynchronous FIFO (dual-port RAM based)

Bidirectional Pins

Many of AMI's megacells are functional equivalents of standard products which have bidirectional pins. A bidirectional pin can be either an input or an output. To simplify operation and reduce the possibility of excess current on AMI's megacells, bidirectional pins are split into three pins: input, output and control.

If it is necessary to recombine these three pins into a single bidirectional pin, use the logic in the following figure "Split-Pins to Bidirectional-Pin Logic." If the bidirectional pin is to become a pin on the ASIC, this logic can come from a pad cell. Often the control pin controls a bank of bidirectional pins.

Split-Pins to Bidirectional-Pin Logic



Testing

Testing of megacells in ASICs usually requires additional logic to simplify testing. Direct or multiplexed input and output pins for controlling and observing the megacell simplify testing and system debugging. Most of AMI's megacells are scan testable, meaning they can be tested by inserting scan and using ATPG vectors.

If some pins on the ASIC are multiplexed between their normal function and a megacell function, a test-mode must apply the simulation patterns to the megacell. When enabled by this test mode, the megacell pins are connected to the pins of the ASIC. Simulation patterns are then run to develop a test or to verify the functionality of the megacell.

A test-mode can be implemented by 1) using an otherwise unused pin; 2) determining an unused condition in normal operation in two or three ASIC pins and using this condition to enable the test-mode; or 3) writing to an unused register bit in a bus-oriented design.

Timing

The electrical and timing characteristics of AMI's megacells depend on the process, layout, and implementation. Delays for megacells in ASICs are estimated using a logic simulator and delay calculator. Post-layout simulations using actual capacitance numbers provide more accurate timing characteristics.

Datapath megacells are designed to meet the application's timing requirements. The delays may change slightly when the megacells are incorporated into the ASIC.

AMI's processor cores and peripheral megacells have simple pin-to-pin relationships with all input changes expected on the cycle boundary. Functional timing diagrams are available for megacells that have more complex timing relationships.

Electrical Characteristics

AMI's megacells do not have any direct external connections to the pins of an ASIC. All necessary connections are made with pad buffers external to the megacell. The pad buffers, selected by the system designer, establish the DC electrical characteristics of the ASIC.

All inputs to the megacells are one to four logical loads. All outputs are buffered so that loading on a given pin will not affect the internal operation.

AMERICAN MICROSYSTEMS, INC.

MG29C01
4-Bit Microprocessor

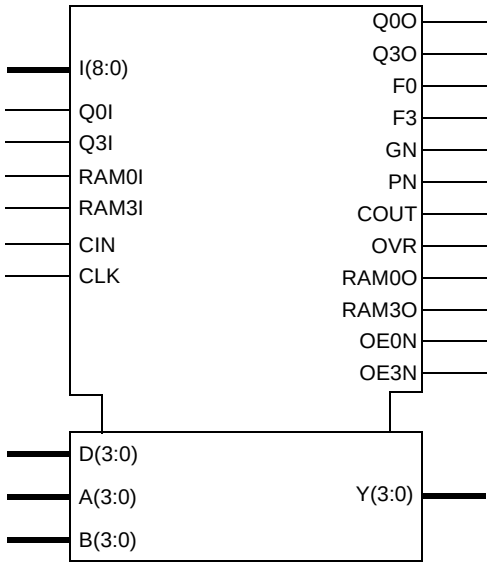
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 2901
- 4-Bit cascadable bit-slice
- Eight function ALU including addition, two subtraction and five logic operations on two operands
- Microprogrammable with three groups of three bits each for ALU function, destination control and source operand
- Two address architecture provides independent access to two working registers
- Five source ports for data selection
- Four status flags including carry, zero, overflow and sign
- Equivalent gates:
  Standard Cell - 810; Gate Array - 1000

LOGIC SYMBOL

MG29C01



Description

MG29C01 is a high-performance 4-bit cascadable microprocessor.

The MG29C01 offers the designer a simple and methodical approach to designing bit-slice microprocessors, high-speed ALUs and boolean machines.

The MG29C01 consists of a fast ALU, a 16-word by 4-bit two port RAM and the required decoding, multiplexing and shifting circuits. The microinstruction word consists of nine bits divided into three groups. Bits 0-2 select the ALU source operads. Bits 3-5 select the ALU function and bits 6-8 select the destination register.

The ALU allows for several arithmetic functions which include: unsigned addition and subtraction, two's complement and one's complement addition and subtraction, and decrementing. The ALU also produces the status bits: overflow, carry-out, F0. Boolean functions offered include: AND, OR, XOR, XNOR, INVERT, PASS, ZERO, and MASK.

The MG29C01 also includes a 16-word by 4-bit register, a 4-bit Q register, and various sources for the ALU.

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
I(8:0)	Input	The nine instruction lines.
CIN	Input	Carry in to the ALU.
CLK	Input	The clock input.
D(3:0)	Input	Data inputs. These data may be selected as one of the ALU sources. D(0) is the LSB.
A(3:0)	Input	The address inputs to the register stack, used to select which register's contents are available through the A port. A(0) is the LSB.
B(3:0)	Input	The address inputs to the register stack used to select which registers contents are available through the B port. B(0) is the LSB.
Q0O, Q3O Q0I, Q3I	I/O	The input and output shift lines for the LSB and MSB of the Q register, allow for shift up and shift down operations. Q3 is the MSB. Q0O is valid when OE0N is low and Q3O is valid when OE3N is low.
F0	Output	Becomes active when all four ALU outputs are low.
F3	Output	The most significant ALU output bit.
GN, PN	Output	The generate and propagate outputs of the ALU, can be used to for carry look-ahead.
COUT	Output	Carry out of the ALU.
OVR	Output	Overflow. Indicates the result of an arithmetic two's complement operation has overflowed into the sign bit.
OE0N	Output	A low on this pin indicates Q0O and RAM0O are valid.
OE3N	Output	A low on this pin indicates Q3O and RAM3O are valid.
RAM0O, RAM3O RAM0I, RAM3I	I/O	The input and output shift lines for the LSB and MSB of the register stack, allow for shift up and shift down operations. RAM3 is the MSB. RAM0O is valid when OE0N is low and RAM3O is valid when OE3N is low.
Y(3:0)	Output	Data outputs. These outputs are connected to either ALU or A port of the register stack.

AMERICAN MICROSYSTEMS, INC.

MG29C10
12-Bit Microprogram Controller

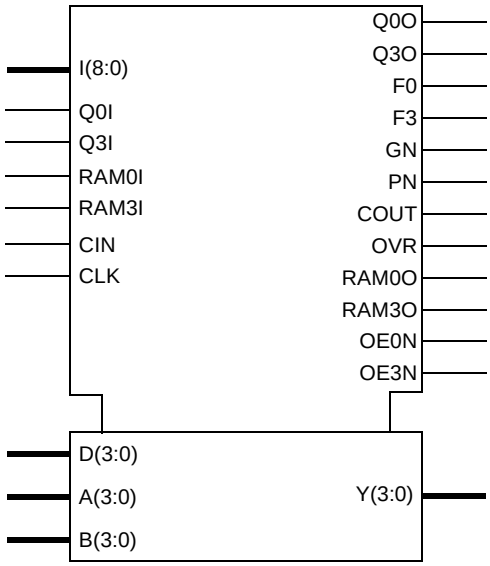
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 2901
- 4-Bit cascadable bit-slice
- Eight function ALU including addition, two subtraction and five logic operations on two operands
- Microprogrammable with three groups of three bits each for ALU function, destination control and source operand
- Two address architecture provides independent access to two working registers
- Five source ports for data selection
- Four status flags including carry, zero, overflow and sign
- Equivalent gates:
  Standard Cell - 810; Gate Array - 1000

LOGIC SYMBOL

MG29C01



Description

MG29C10 is a high-performance 12-bit microprogram controller. It functions as an address sequencer for controlling the execution of microinstructions in microprogram memory.

It also controls conditional branching to any microinstruction within its 4096 word range. There are nine levels of subroutine nesting with return linkage and looping capability provided by a last-in, first-out stack.

The MG29C10 has four sources for providing the 12-bit address during each microinstruction. These four sources are as follows:

1. A direct external input.
2. A register/counter (R) which retains data loaded during an earlier microinstruction.
3. The last-in, first-out stack/file (F).
4. The address counter/register which usually increments the addresses.

The MG29C10 consists of six functional blocks: an instruction PLA, a multiplexer, a register/counter, a zero detector, a 9-word by 12-bit stack, a microprogram counter register, and an incrementer.

Pin Description

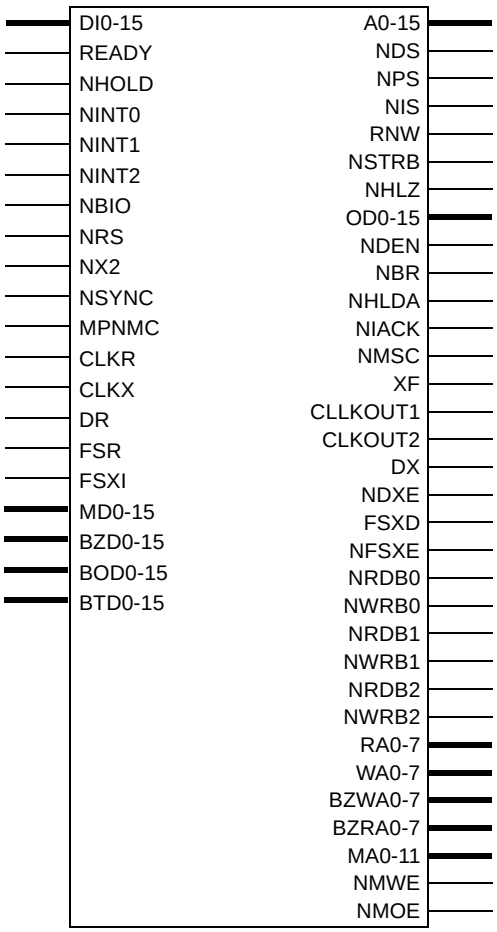
SIGNAL	TYPE	SIGNAL DESCRIPTIONS
CCN	Input	Used as test input criterion. Active low.
CCENN	Input	Enables CCN. Active low.
CI	Input	Carry input to the low order of the microprogram counter.
RLDN	Input	Forces loading of register/counter regardless of instruction or condition. Active low.
CLK	Input	Master input clock.
D(11:0)	Input	Direct data input to register/counter and multiplexer. D(0) is the LSB.
I(3:0)	Input	Instruction inputs. I(0) is the LSB.
FULLN	Output	Goes low when the internal stack is full. Active low.
PLN	Output	Used to select #1 source (usually a pipeline register) as the direct input source.
MAPN	Output	Used to select #2 source (usually a mapping ROM or PLA) as the direct input source.
VECTN	Output	Used to select #3 source (usually an interrupt starting address) as the direct input source.
Y(11:0)	Output	Address to microprogram memory. Y(0) is the LSB.

Features

- Functionally compatible with the industry standard
- 32-bit ALU/accumulator
- 16 X 16 parallel multiplier
- 16-bit shifter
- Up to 64k words of program memory
- Up to 64k words of data memory
- 16-bit timer
- Serial port
- Equivalent gates: 17,000

LOGIC SYMBOL

M320C25



Description

M320C25 is a digital signal processor with separate data and program memory, both of which may be up to 64k words. It has a 16-bit shifter, a 16 X 16 bit parallel multiplier and a 32-bit ALU/accumulator. Instructions are pipelined and it can perform single-cycle multiply/accumulate instructions. It contains a 16-bit timer, eight auxiliary registers, an eight-level hardware stack, sixteen input and sixteen output channels, and a serial port. It is fully compatible, including instructions execution times, with industry standard devices.

The M32C25 contains no RAM or ROM but provides functional interconnect signals for connecting to memory blocks. If internal program memory is required, a single port RAM (or ROM) block of up to 4k X 16 may be connected to the M320C25 (also the 256 X 16 internal data RAM block 0 may be configured as program memory). If internal data memory is required 1,2 or 3 blocks of dual-port RAM may be connected to the M320C25. Block 0 and 1 can be up to 256 X 16 and block 2 up to 32 X 16.

M320C50
DSP

AMERICAN MICROSYSTEMS, INC.

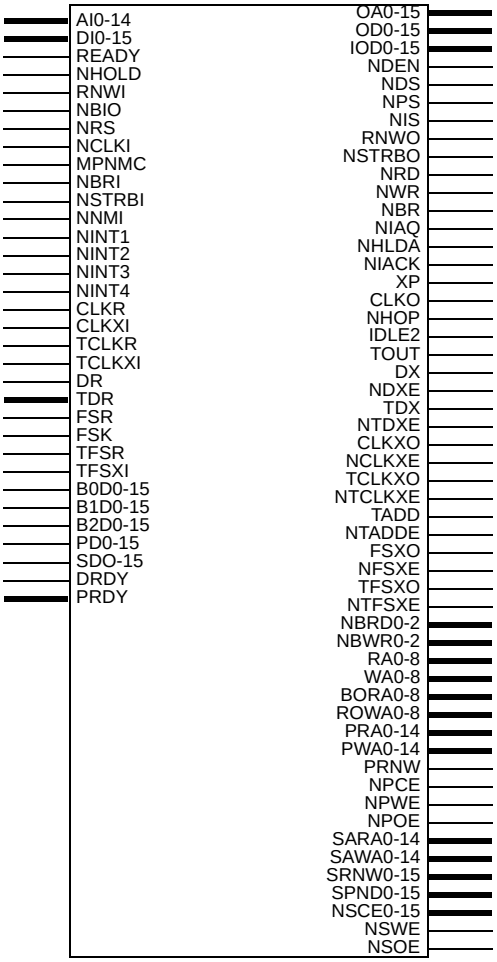
Digital Soft Megacells

Features

- Functionally compatible with the industry standard
- 32-bit ALU/accumulator
- 16 X 16 parallel multiplier
- 16-bit shifter
- 16-bit parallel logic space
- Up to 64k words each of program and data memory
- 64K I/O space
- Interrupt controller
- Serial port and TDM serial port
- Equivalent gates: 40,000

LOGIC SYMBOL

M320C50



Description

M320C50 is a digital signal processor with separate data and program memory. The program memory may be up to 64k words. The data memory may be up to 64k words, up to 32 words of which may be global access. It has 64k 16-bit I/O ports, sixteen of which are memory mapped. The central ALU has a 32-bit arithmetic logic unit, a 32-bit accumulator and accumulator buffer, a 16-bit scaling shifter, and a 16 X 16 parallel multiplier. A separate parallel logic unit can perform bit manipulations on any data memory location or control/status register. It has eight auxiliary registers, an eight level hardware stack, and a four stage instruction pipeline. The M320C50 contains no ROM or RAM but provides functional interconnect signals for connecting to memory blocks.

Peripherals are controlled through 28 memory-mapped registers and consists of: a timer, a serial port, a time-division-multiplexed serial port, a programmable wait-state generator, an interrupt controller, and the I/O ports.

The M320C50 is compatible, including instructions execution times, with industry standard devices.

AMERICAN MICROSYSTEMS, INC.

MG65C02
8-Bit Core Microprocessor

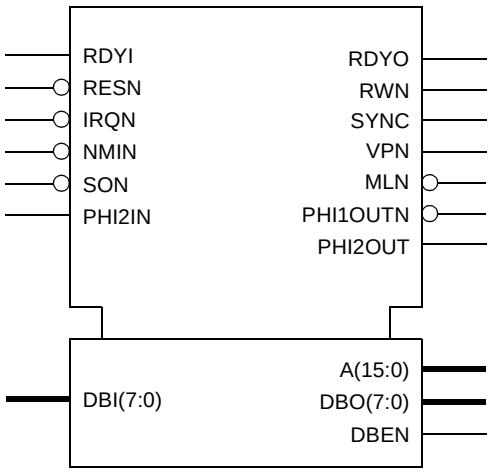
Digital Soft Megacells

Features

- High-performance, schematic-based megacell
- Functional compatibility with the industry standard 6502
- 8-Bit Microprocessor
- Fully Static Design
- 0-33 MHz Operation
- 64 kbytes Program Address Space
- Enhanced Instruction Set
- Supports Bit Manipulation
- 72 instructions and 212 opcodes
- 15 address modes
- Interrupt Capability
- Equivalent gates:
  Standard Cell - 2,950; Gate Array - 3,850

LOGIC SYMBOL

MG65C02



Description

MG65C02 is an 8-bit microprocessor which is compatible with the industry standard W65C02S. It has been designed to be compatible with both the original NMOS 6502 and the newer CMOS variations from various vendors.

The MG65C02 runs all 6502 opcodes as well as the new Enhanced Instruction set which include the new bit manipulation opcodes - RMB, SMB, BBR, BBS, and WAI and STP instructions. The latest functions are also incorporated in the MG65C02 such as Bus Enable, Vector-Pull, and Memory Lock. It accesses 65 kbytes of addressable Memory. It is fully static allowing the external clock to stop in either state. Operation frequency follows a range of 0 MHz, for low power or standby modes, to more than 25 MHz for high speed applications.

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
A0-A15	O	Address to memory.
DBO0-DBO7	O	Data bus output. Valid when DBEN is high.
DBI0-DBI7	I	Data bus Input. Should be valid when DBEN is low.
DBEN	O	Data Bus Enable.
RDYI	I	Ready Input, active low. Stops the internal clock.
RDYO	O	Ready Output. The WAI instruction uses this pin to bring RDYI low.
RESN	I	Active low Reset.
IRQN	I	Active low Interrupt.
NMIN	I	Active low Non-maskable interrupt.
SON	I	Active low sets the overflow bit in the status word.
RWN	O	Read/Write. Active low for write.
SYNC	O	Synchronize. Active during opcode fetch cycle.
VPN	O	Vector Pull, active low. Low during interrupt vector access.
MLN	O	Memory Lock, active low. Low during Read-Modify-Write (RMW) portion of RMW instructions.
PHI2IN	I	Clock.
PHI1OUTN	O	Clock. Out of phase with C2IN.
PHI2OUT	O	Clock. In phase with PHI2IN. It also goes high with the STP instruction.

AMERICAN MICROSYSTEMS, INC.

M8042
8-Bit Slave Microcontroller

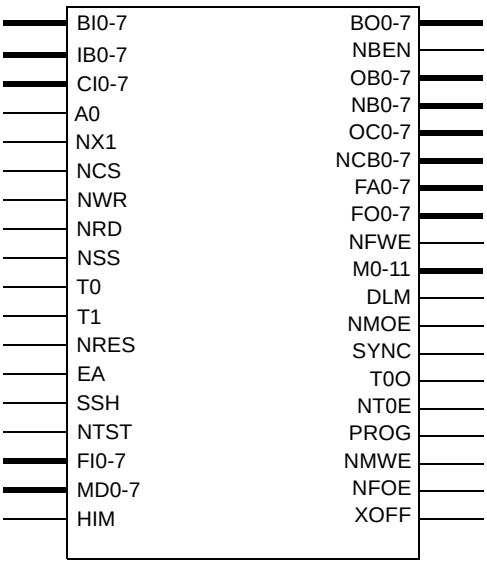
Digital Soft Megacells

Features

- Functionally compatible with the industry standard 8042
- Uses AMI's ASIC Standard Library for technology independence
- Up to 256 bytes of data memory
- Up to 4K bytes of program memory
- Memory down-load mode
- 8-bit timer/counter
- DMA, interrupt or polled operation supported
- Power saving modes
- Equivalent gates (does not include RAM or ROM): Standard Cell - 2,750; Gate Array - 3,500

LOGIC SYMBOL

M8042



Description

M8042 is an 8-bit slave microcontroller. This microcode-free design is software compatible with industry standard discrete devices. It can address data RAM of up to 256 bytes and program RAM or ROM of up to 4K bytes. If program memory is implemented with RAM a special down-load mode is available to program the RAM. An 8-bit timer/counter and 18 I/O pins are available.

Data is transferred between the M8042 and a master CPU through separate input and output data bus buffers. Communication can be controlled by two DMA handshaking lines or by interrupts.

The M8042 has two power saving modes; soft power down mode and hard power down mode. In soft power down mode the clock to the ALU is stopped but the timer/counter and interrupts are still active. In hard power down mode the clock to the entire M8042 is stopped.

Signals are present that allow the end user to choose the appropriate memory block for each implementation. This allows memory size to be configured, and if necessary, the program memory block may be implemented as "down-loadable" RAM.

As no I/O cells are included in the design, all bidirectional lines (the Data Bus, the Port1 and Port2 buses) are split into input and output sections, and have associated control lines for enabling and disabling 3-state buffers where appropriate. There are individual enable lines for each of the Port1 and Port2 outputs. This allows implementation of the 'quasi-bidirectional' pins feature of the original device.

There is only one clock input (NX1), this is again due to the fact that there are no I/O cells in the design. The output of a suitable crystal oscillator I/O cell should be connected to this input. XOFF (which is high true) is used to disable the oscillator I/O cell in power saving mode.

This megacell requires the use of ROM and RAM which can be ordered from the AMI Memory group.

A per-use fee is associated with this megacell. Contact the factory for more information.

M8048
8-Bit Microcontroller

AMERICAN MICROSYSTEMS, INC.

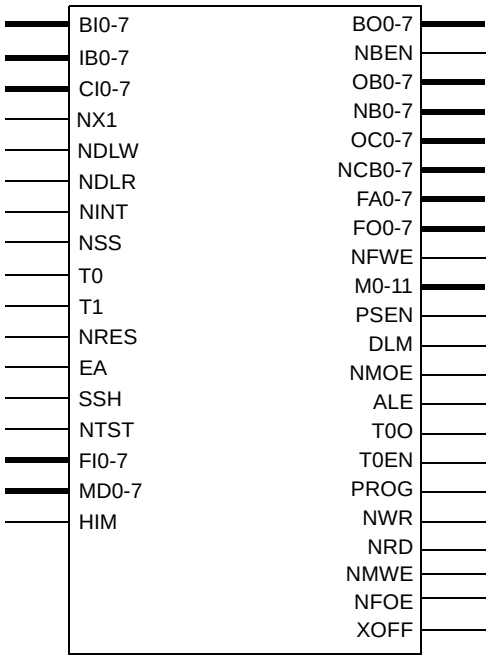
Digital Soft Megacells

Features

- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Up to 256 bytes of data memory
- Up to 4K bytes of RAM or ROM program memory
- Memory down-load mode
- 8-bit timer/counter
- Power saving modes
- Equivalent gates:
  Standard Cell - 2,770; Gate Array - 3,470

LOGIC SYMBOL

M8048



Description

M8048 is an 8-bit microcontroller. This microcode-free design is software compatible (including instruction execution times) with industry standard discrete devices. It can address data RAM of up to 256 bytes and program RAM or ROM of up to 4k bytes. If program memory is implemented with RAM a special down-load mode is available to program the RAM. An 8-bit timer/counter and 27 I/O lines are available, and both internal and external interrupts are supported.

The M8048 has two power saving modes; soft power down mode and hard power down mode. In soft power down mode the clock to the ALU is stopped but the timer/counter and interrupts are still active. In hard power down mode the clock to the entire M8048 is stopped.

A per-use fee is associated with this megacell. Contact the factory for more information.

AMERICAN MICROSYSTEMS, INC.

MGMC32 Family
8-Bit Core Microcontrollers

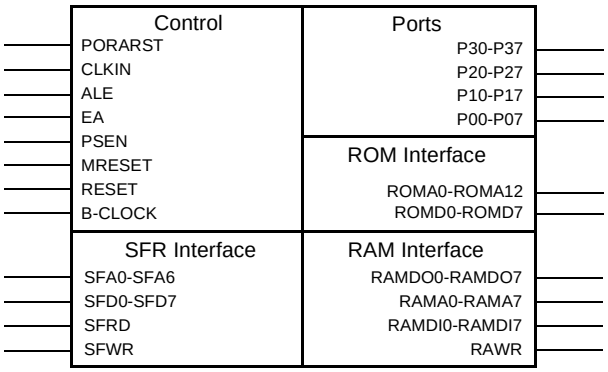
Digital Soft Megacells

Features

- Functionally compatible with the industry standard 8051 family.
- Several configurations to choose from; including PCA and reduced-function options.
- Schematic-based, uses the ASIC Standard Library for technology independence.
- Fully Static Design
- Low Standby Current At Full Supply Voltage.
- 64 kilobytes of Data and Program Address Space.
- Boolean Processor and serial port.
- Access To Special Function Register Bus.

LOGIC SYMBOL

MGMC31



Description

MGMC32 ASIC microcontroller family is a set of 8-bit microcontrollers that is functionally compatible with the industry standard 8052 and 8052FB. All members of the MGMC32 family are built around the same core processor and use the same instruction set. They differ only in the number and types of peripherals. None of these controllers contain ROM or RAM, any desired memory can be added.

All controllers are supported by a multiple source, two level interrupt capability. The core processor supports up to 256 bytes of scratchpad RAM and up to 64K of ROM. The size of the internal ROM may be adjusted to meet a specific application.

MGMC32

The basic MGMC32 contains four 8-bit parallel ports, two external interrupt sources, three timer/counters, a serial port, and power management. It is compatible with the 8052.

MGMC32SD

The MGMC32SD removes the serial port.

MGMC32FB

This configuration add a programmable-counter array, and a watchdog timer to the MGMC32. It is compatible with the industry standard 8052FB.

These configurations duplicate existing microcontrollers and will meet the requirements of most applications. However, the MGMC32 is not limited to just these configurations. The internal SFR bus has been made available to the designer. This allows the designer to place their own application into the SFR address space where it may be directly operated on by the 8051 instruction set.

Since the MGMC32 microcontrollers are in AMI's ASIC Standard Library, their AC and DC characteristics depend on the process that they are manufactured in. The process determines both the strengths of the output buffers and type of input buffer desired for each pin. Processes for low voltage operation at supplies of 3 volts or less are available. The process also provides for the maximum processor speed. The fully static design allows the clock to be stopped at any time and in either state to minimize power.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
P30-P37	IO	Port 3.
P20-P27	IO	Port 2.
P10-P17	IO	Port 1.
P00-P07	IO	Port 0.
RESET	I	Reset. Resets to location 0 only.
PORARST	I	Initializes the Power On Reset.
MRESET	I	Master Reset.
EA	IO	External Address. IO used with some In Circuit Emulators.
ALE	IO	Address Latch Enable.Is an input for special modes during reset.
PSEN	IO	Program Store Enable. Enables external ROM fetch. Is an input for special modes during reset.
CLKIN	I	Clock input.
B-CLOCK	O	Buffered Clock. Runs at half the XTAL2I frequency. Can clock synchronous memories.
ROMA0-ROMA12	O	ROM Address Bus.
ROMD0-ROMD7	I	ROM Data Bus.
SFA0-SFA6	O	Special Function Register Address Bus.
SFD0-SFD7	IO	Special Function Data Bus.
SFRD	O	Special Function Write Strobe.
SFWR	O	Special Function Read Strobe.
RAMA0-RAMA7	O	Scratchpad RAM Address Bus.
RAMDO0-RAMDO7	O	Scratchpad RAM Data Out Bus.
RAMDI0-RAMDI7	I	Scratchpad RAM Data In Bus.
RAWR	O	Scratchpad RAM Write.
RARD	O	Scratchpad RAM Read.

Equivalent Gates (does not include ROM or RAM)

	STANDARD CELL	GATE ARRAY
MGMC32SD	7,370	9,200
MGMC32	8,800	11,000
MGMC32FB	11,720	14,750

AMERICAN MICROSYSTEMS, INC.

MG1468C18
Real-Time Clock

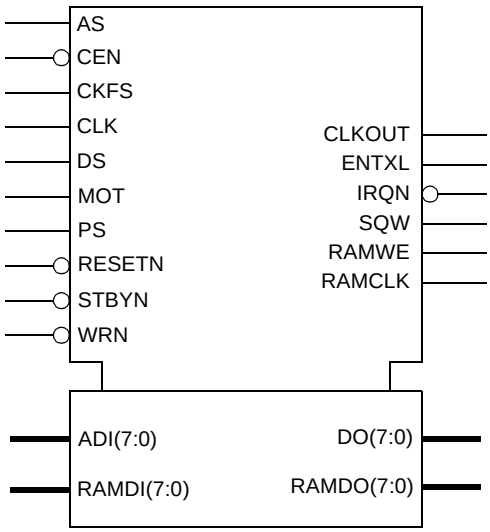
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell
- Functionally compatible with the industry standard 146818
- 12- or 24-hour clock with a.m and p.m. mode
- Leap year and end-of-month recognition
- Programmable alarm
- Equivalent gates: (does not include RAM) Standard Cell - 2,000; Gate Array - 2,500

LOGIC SYMBOL

MG1468C18



Description

MG1468C18 Real-Time Clock is a peripheral device which may be used with various processors/computers. It combines these features: a complete time-of-day clock with alarm and one hundred year calendar; and a programmable periodic interrupt and square wave generator.

The Real-Time Clock is designed for use as a battery powered element, including all the common backed-up functions such as RAM, time and calendar.

The megacell has been partitioned with battery backup application in mind. For purposes of electrical isolation the multiplexed address and data bus is split into input and output sides. The split avoids any possible conduction paths which result when the outputs of the tristate buffers in a portion of the chip, which could be without power, are connected to active or tristate outputs of powered circuits.

If not using battery backup, it is possible to configure the megacell to appear to the rest of the ASIC as if the data bus were bidirectional using ENTXL.

This megacell requires the use of an external 64-byte by 8-bit RAM with outputs always enabled. This RAM, in the correct process, can be ordered from the AMI Memory group.

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
ADI(7:0)	Input	Multiplexed bidirectional address and data bus. May be combined with the DO(7:0) bus using the ENTXL signal.
AS	Input	Address strobe. The falling edge of AS latches the address from the ADI bus.
CEN	Input	Chip enable, active low.
CKFS	Input	Selects the output frequency of CLKOUT. When CKFS=1, the frequency of CLKOUT will equal CLK. When CKFS=0. the frequency of CLKOUT will equal CLK/4.
CLK	Input	Time-base input for the time functions of the Real-TIme Clock.
CLKOUT	Output	Output at the time-base frequency divided by 1 or 4.
DO(7:0)	Output	Data output bus. May be combined with the ADI(7:0) bus using the ENTXL signal.
DS	Input	Data Strobe. The DS signal is used with the WRN signal to latch write data from the ADI bus and output data to the DO bus.
ENTXL	Output	Input/Output bus control. Used to create a multiplexed address/data bus external to the RTC. When ENTXL = 0, this external bus should be put in output mode, indicating a read cycle. If ENTXL = 1, the bus should be in a high-impedance state, allowing external drive.
IRQN	Output	Interrupt request, active low. Signifies an interrupt condition is present.
MOT	Input	Allows selection between Motorola (MOT=1) and Intel (MOT=0) bus timing.
PS	Input	Power sense. Used to control the Valid RAM and Time bit in register D.
RAMCLK	Output	RAM clock. An output from the megacell used to clock timed RAMs.
RAMDI(7:0)	Input	RAM data into the megacell.
RAMDO(7:0)	Output	RAM data coming out of the megacell.
RAMWE	Output	RAM write enable.
RESETN	Input	Megacell reset active low. Does not affect the clock, calendar or RAM functions.
STBYN	Input	Stand by, active low. Prevents access to the RTC.
SQW	Output	Square wave output from one of the 15 taps provided by the 22 internal-divider stages.
WRN	Input	Write enable, active low. Used with the DS pin to read and write data.

AMERICAN MICROSYSTEMS, INC.

M16C450
UART

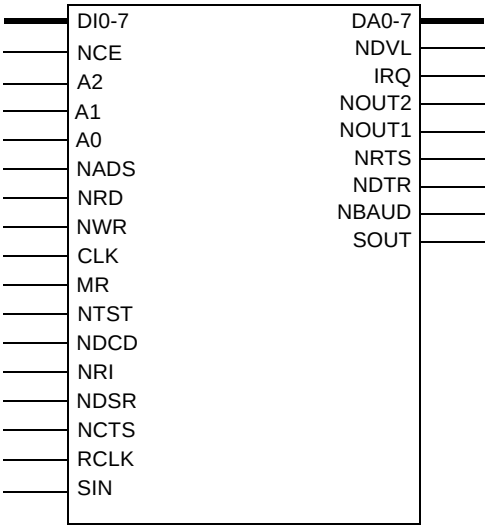
Digital Soft Megacells

Features

- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Programmable word length, stop bits and parity
- Programmable baud rate generator
- Interrupt generator
- Loop-back mode
- Scratch register
- Equivalent gates:
  Standard Cell - 1,700; Gate Array - 2,250

LOGIC SYMBOL

M16C450



Description

M16C450 is a universal asynchronous receiver/transmitter (UART) which is fully programmable by an 8-bit CPU interface. It supports word lengths from five to eight bits, an optional parity bit and one or two stop bits. If enabled the parity can be odd, even or forced to a defined state. A 16-bit programmable baud rate generator and an 8-bit scratch register are included. Eight modem control lines and a diagnostic loop-back mode are provided.

An interrupt can be generated from any one of 10 sources.

Transmission is initiated by writing the data to be sent to the Transmitter Holding Register. The data will then be transferred to the Transmit Shift Register together with a start bit and parity and stop bits as determined by the Line Control Register. The bits to be transmitted are then clocked out of the transmit shift register by the transmit clock (NBAUD) which comes from the baud rate generator.

If enabled, an interrupt will be generated when the Transmitter Holding Register becomes empty.

Data is clocked into the receiver by the receive clock (RCLK). The receive clock should be 16 times the baud rate of the received data. A filter is used to remove spurious inputs which last for less than two periods of RCLK. When the complete word has been clocked into the receiver the data bits are transferred to the Receiver Buffer Register to be read by the CPU. The receiver also checks for a stop bit and for correct parity as determined by the Line Control Register.

If enabled, an interrupt will be generated when the data has been transferred to the Receiver Buffer Register. Interrupts can also be generated for incorrect parity or a missing stop bit (frame error).

The output modem control lines; NRTS, NDTR, NOUT1 and NOUT2 can be set or cleared by writing to the Modem Control Register. The current status of the input modem control line; NDCD, NRI, NDSR and NCTS can be read from the Modem Status Register. Bit 2 of this register will be set if the NRI modem status line has changed from low to high since the register was last read.

If enabled, an interrupt will be generated when NDSR, NCTS, NRI or NCD are asserted.

A per-use fee is associated with this megacell. Contact the factory for more information.

M6402
UART

AMERICAN MICROSYSTEMS, INC.

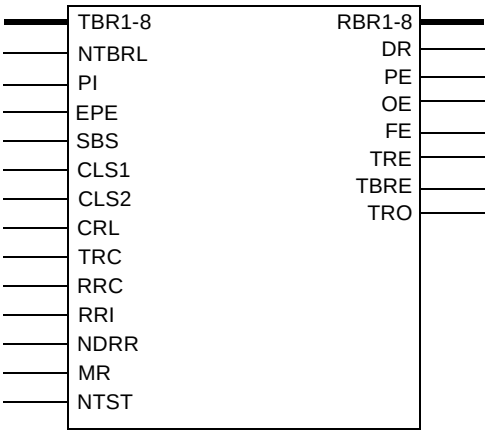
Digital Soft Megacells

Features

- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Programmable word length, stop bits and parity
- Double-buffered receiver and transmitter
- Overrun, parity and framing error detection
- Equivalent gates:
  Standard Cell - 580; Gate Array - 750

LOGIC SYMBOL

M6402



Description

M6402 is a full–duplex universal asynchronous receiver/transmitter (UART). It supports word lengths from five to eight bits, an optional parity bit and one or two stop bits. It can detect overrun, parity and framing errors in the received character.

The M6402 differs from the M8868A in that the master reset clears the TRE output to "0" and does not initialize the receive buffer.

A per-use fee is associated with this megacell. Contact the factory for more information.

AMERICAN MICROSYSTEMS, INC.

M6845
CRT Controller

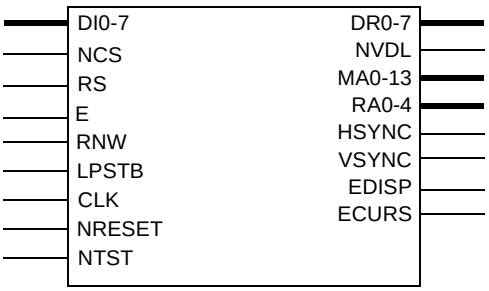
Digital Soft Megacells

Features

- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Alphanumeric, semi-graphic and full-graphic capability
- Alphanumeric screen formats of up to 16K characters
- Programmable horizontal and vertical sync pulses
- Programmable cursor format and blink rate
- Light pen register
- Interlaced or non-interlaced scan modes
- Equivalent gates:
  Standard Cell - 2,100; Gate Array - 2,700

LOGIC SYMBOL

M6845



Description

M6845 is a highly programmable controller designed to generate the timing and control signals necessary to meet a wide range of CRT (Cathode Ray Tube) based video controllers. It is programmed by an 8-bit CPU interface. It can address a character memory of up to 16K, which can represent one or more pages of characters. It can provide hardware scrolling through pages in multiple page setups. The position and width of the horizontal and vertical sync pulses are fully programmable, as is the size location and blink rate of the cursor.

The horizontal counter is clocked by the CLK input and counts from 0 up to the value stored in the Horizontal Total register. The counter output is used by the horizontal sync block to generate the HSYNC pulse, as defined by the Horizontal Sync. Position and Sync. Width registers, and by the display address generator block to produce the character memory address.

The raster counter is incremented by the horizontal counter and is used to count scan lines. The output is available on the row address lines (RA0-4).

The vertical counter is incremented by the raster counter and is used to count character lines. The output is used by the vertical sync block to generate the VSYNC pulse, as defined by the Vertical Sync. Position and Sync. Width registers, and by the display address generator block to produce the display memory address.

The frame counter is incremented by the vertical counter and is used to count display frames. The output is used by the cursor control block to blink the cursor at a rate determined by register 10.

By using both the display memory address and the row address an address space of 512K is available for use in graphic displays.

Addresses are provided during retrace to provide refresh for dynamic RAMs.

The light pen register will latch the display memory address when the LPSTB line goes high.

A per-use fee is associated with this megacell. Contact the factory for more information.

M765A
Floppy Disk Controller

AMERICAN MICROSYSTEMS, INC.

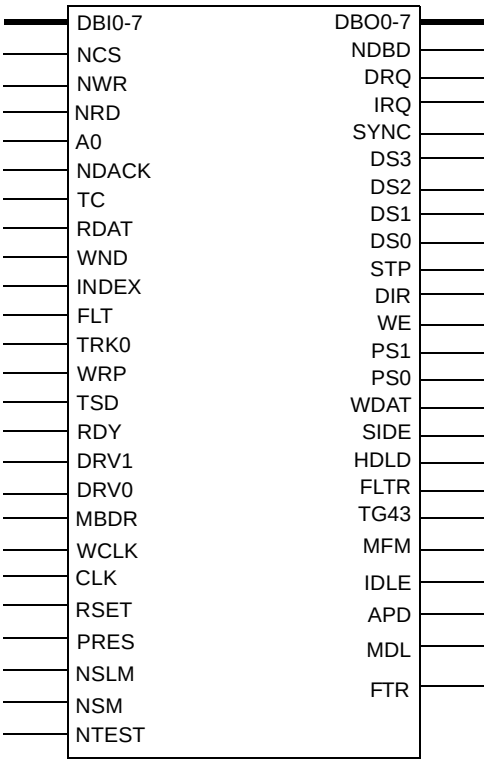
Digital Soft Megacells

Features

- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- IBM System 3740 format
- IBM System 34 format Perpendicular recording format Data rates up to 1.25 Mbps
- Directly addresses 256 tracks
- 255 step recalibrate command
- Programmable write precompensation
- 16 byte FIFO
- Equivalent gates:
  Standard Cell - 7,100; Gate Array - 9,300

LOGIC SYMBOL

M765A



Description

M765A is a floppy disk controller which also supports tape drives. This microcode-free design is compatible with industry standard discrete devices. It supports IBM System 3740 (FM), IBM System 34 (MFM), Perpendicular 500K BPS and Perpendicular 1M BPS formats. It supports 4 Mb floppy drives and is capable of data rates up to 1.25 Mbps. It provides drive select and motor signals, and supports drives with tunnel erase heads. It has programmable write precompensation and a 16 byte data FIFO. It can directly address 256 tracks and has the ability to access an unlimited number. The recalibrate command can step 255 tracks.

The M765A can be connected to a M91C360, or similar, data separator to form a complete floppy disk controller.

A per-use fee is associated with this megacell. Contact the factory for more information.

AMERICAN MICROSYSTEMS, INC.

M8251A
Serial Communication Interface

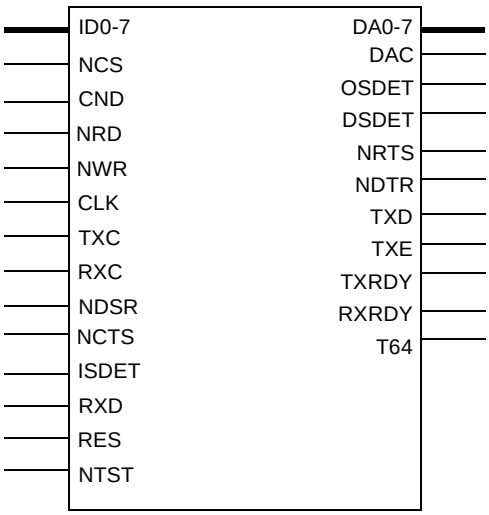
Digital Soft Megacells

Features

- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Synchronous and asynchronous operation
- Full duplex, double buffered transmitter and receiver
- Internal or external character synchronization
- 1X, 16X and 64X clock modes
- Framing, parity and overrun error detection
- Equivalent gates:
  Standard Cell - 1,500; Gate Array - 2,000

LOGIC SYMBOL

M8251A



Description

M8251A is a universal synchronous/asynchronous receiver/transmitter (USART) communications interface. It supports asynchronous communications with five to eight data bits, parity and one, one and a half, or two stop bits. It can provide automatic break detection. It supports synchronous communications with one or two SYNC characters, with internal or external SYNC detection. Both the transmit and receive data paths are double buffered. It has four modem control lines.

The M8251A is fully programmable by an 8-bit CPU interface.

The operating mode of the M8251A is programmed by writing to the mode control registers and SYNC registers, using the 8-bit CPU interface. Transmission can then begin by writing to the transmit buffer. Data is clocked out of the transmitter by the transmit clock (TXC), which can be 1, 16 or 64 times the baud rate. The data stream is clocked into the receiver by the receive clock (RXC), which can be 1, 16 or 64 times the baud rate. In synchronous mode character reception will not begin until the SYNC character, or characters, are detected. When each character has been received it is transferred to the receive buffer to be read by the CPU interface.

The M8251A has output signals to indicate when the transmit buffer is empty (TXRDY), when the receive buffer is full (RXRDY) and when the SYNC characters have been detected (OSDET, DSDET). Two input (NDSR, NCTS) and two output (NRTS, NDTR) modem control signals are also provided. A further input (ISDET) is provided for use with an external SYNC detector.

A per-use fee is associated with this megacell. Contact the factory for more information.

M8253
Programmable Interval Timer

AMERICAN MICROSYSTEMS, INC.

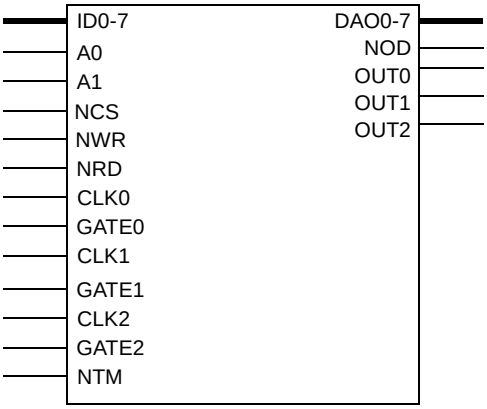
Digital Soft Megacells

Features

- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Three independent 16-bit counters
- Binary or BCD counting
- Six counter modes
- Equivalent gates:
  Standard Cell - 2,500; Gate Array - 3,250

LOGIC SYMBOL

M8253



Description

M8253 contains three independent 16-bit timer/counters that can be programmed over a common 8-bit CPU interface. It can be used for timing external events, producing fixed delays or producing repetitive waveforms. The current value of each of the counters can be latched and read back over the CPU interface.

A per-use fee is associated with this megacell. Contact the factory for more information.

AMERICAN MICROSYSTEMS, INC.

M82530
Serial Communications Controller

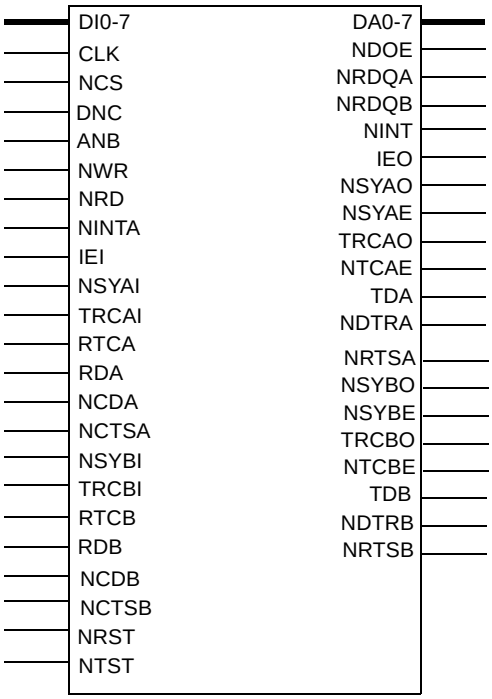
Digital Soft Megacells

Features

- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Asynchronous and synchronous modes
- MONOSYNC, BISYNC and SDLC supported
- SDLC loop-mode supported
- NRZ, NRZI and FM encoding/decoding
- Two independent full-duplex channels
- Digital phase-locked loop for each channel
- Baud rate generator for each channel
- Local loop-back and automatic echo modes
- Equivalent gates:
  Standard Cell - 9,400; Gate Array - 12,200

LOGIC SYMBOL

M82530



Description

M82530 serial communications controller has two independent full-duplex channels which support asynchronous, bit synchronous (SDLC, HDLC and SDLC loop mode) and byte synchronous (MONOSYNC, BISYNC) communication modes. NRZ, NRZI and FM data encoding/decoding are supported. The M82530 includes a baud rate generator and a digital phase-locked loop for each channel. Two diagnostic modes: local loop-back and automatic echo are available. The M82530 is fully programmable by an 8-bit system interface, which includes a six source interrupt controller. The interrupt controller has external signals that allow it to be daisy-chained with other interrupt controllers.

Each of the two identical channels in the M82530 contain a transmitter, a receiver, a baud rate generator, a digital phase-locked loop and a clock selector. The clock selector provides the clocks for the transmitter and the receiver blocks. The clocks can be programmed to come from one of two external clocks, from the baud rate generator, or derived from the receiver data stream by the phase-locked loop. In addition to the two serial communication channels there is a common 8-bit system interface and a six source interrupt controller.

The transmitter has a transmit shift register into which data to be transmitted is loaded. This data is loaded from the transmit buffer, sync characters and flags are loaded automatically from the sync registers. In SDLC mode a zero insertion block will insert zeros into long strings of ones. A CRC generator produces a CRC check word for appending to message blocks. The output data stream then passes to a data encoder block which can produce NRZ, NRZI or FM encoded formats. The final output selector allows the output to come from the receiver in diagnostic or loop modes.

The receiver input selector allows the received data stream to come from the transmitter in diagnostic modes or through a 1-bit delay, which is required in SDLC loop mode. The input stream then passes to a decoder to convert it into NRZ format. The data stream then goes into the receive data shift register. The receive data shift register can be extended to 16-bits for detecting 16-bit sync characters, and can automatically delete the extra zeros that were inserted into the data stream in SDLC mode. A CRC checker can be used in synchronous modes. The received data characters are transferred to the receive data FIFO and parity, frame or CRC errors are transferred to the receive error FIFO.

A per-use fee is associated with this megacell. Contact the factory for more information.

MG82C37A
Programmable DMA Controller

AMERICAN MICROSYSTEMS, INC.

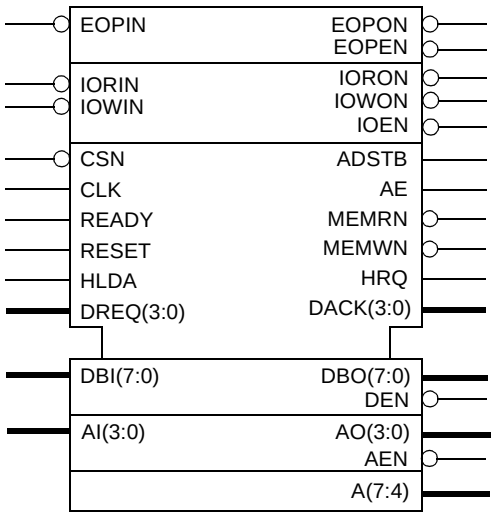
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 8237/8237A
- Compatible with 8080/85, 8086/88, 80286/386 and 68000 µP families
- Four independent maskable DMA channels with autoinitialize capability
- Memory-to-memory transfer
- Fixed or rotating DMA request priority
- Independent polarity control for DREQ and DACK signals
- Address increment or decrement selection
- Cascadable to any number of channels
- Equivalent gates:
  Standard Cell - 3,000; Gate Array - 3,800

LOGIC SYMBOL

MG82C37A



Description

MG82C37A is a high-performance, programmable Direct Memory Access (DMA) controller offering functional compatibility with the industry standard 8237/8237A. It features four channels, each independently programmable, and is cascadable to any number of channels. Each channel can be programmed to autoinitialize following DMA termination.

In addition, the MG82C37A supports both memory-to-memory transfer capability and memory block initialization, as well as a programmable transfer mode.

The MG82C37A is designed to improve system performance by allowing external devices to transfer data directly with system memory. High speed and very low-power consumption make it an ideal component for aerospace and defense applications. The low-power consumption also makes it an attractive addition in portable systems or systems with low-power standby modes.

The MG82C37A DMA controller is a state-driven address and control signal generator designed to accelerate data transfer in systems by moving data from an I/O device to memory, or memory to an I/O device. Data transfers are direct, rather than being stored enroute in a temporary register.

The MG82C37A also mediates memory-to-memory block transfers and will move data from a single location to a memory block. Temporary storage of data is required, but the transfer rate is significantly faster than CPU processes. The device provides operating modes to carry out both single byte and block transfers of data.

The organization of the MG82C37A is composed of three logic blocks, a series of internal registers and a counter section. The logic blocks include the Timing Control, Command Control and Priority Encoder circuits.

The Timing Control block generates internal timing signals from the clock input and produces external control signals.

Command Control decodes incoming instructions from the CPU, and the Priority Encoder block regulates DMA channel priority.

The internal registers hold internal states and instructions from the CPU. Addresses and word counts are computed in the counter section.

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
AI(3:0)	I	Input address bus. During Idle Cycle, addresses which control register to be loaded or read.
AO(3:0)	O	Low output address bus. During active Cycle, lower 4 bits of the transfer address.
AEN	O	Control line used to determine when AO(3:0) and A(7:4) is valid. Active low.
A(7:4)	O	High Address Bus. During active Cycle, upper 4 bits of the transfer address.
ADSTB	O	Address Strobe. Controls latching of the upper address byte.
AE	O	Address Enable. Enables the higher order address byte onto the system address bus.
CLK	I	Clock Input. May be stopped for standby operation.
CSN	I	Chip Select, active low.
DACK(3:0)	O	DMA Acknowledge. Informs a peripheral that the requested DMA transfer has been granted.
DBI(7:0)	I	Data Bus input ports.
DBO(7:0)	O	Data Bus output ports.
DEN	O	Control line, active low. Used to determine when DBO(7:0) is valid.
DREQ(3:0)	I	DMA Request. DMA service is requested by activation of the channel from a specific device.
EOPIN	I	End of Process, active low. Force termination of DMA.
EOPON	O	Indicates when DMA is finished.
EOPEN	O	Control line used to determine when EOPON is valid. Active low.
HLDA	I	Hold Acknowledge. Indicates the CPU has released control of the system buses.
HRQ	O	Hold Request. Requests control of the system buses. HRQ is issued following a request for DMA service (DREQ) from a peripheral, and is acknowledged by the HLDA signal.
IORIN IORON	I O	I/O Read, active low. Idle Cycle: CPU input control signal for reading the Control Registers. Active Cycle: Output control signal to read data from a peripheral device during a DMA cycle.
IOWIN IOWON	I O	I/O Write, active low. Idle Cycle: CPU input control signal for loading the control registers. Active Cycle: Output control signal to load data to a peripheral device during a DMA cycle.
IOEN	O	Control line active low. Indicates when IORON, IOWON, MEMRN and MEMWN are valid.
MEMRN	O	Memory Read, active low. MG82C37A reads data from a selected memory address during a DMA Read or Memory-to-Memory transfer. Valid when IOEN is low.
MEMWN	O	Memory Write, active low. MG82C37A writes data to a selected memory address during a DMA Write or Memory-to-Memory transfer. Valid when IOEN is low.
READY	I	Extends the Memory Read and Write pulse widths to accommodate slow I/O peripherals.
RESET	I	Reset. Asynchronous signal clears internal registers and puts the MG82C37A in Idle Cycle.

MG82C50A
Async. Communication Element

AMERICAN MICROSYSTEMS, INC.

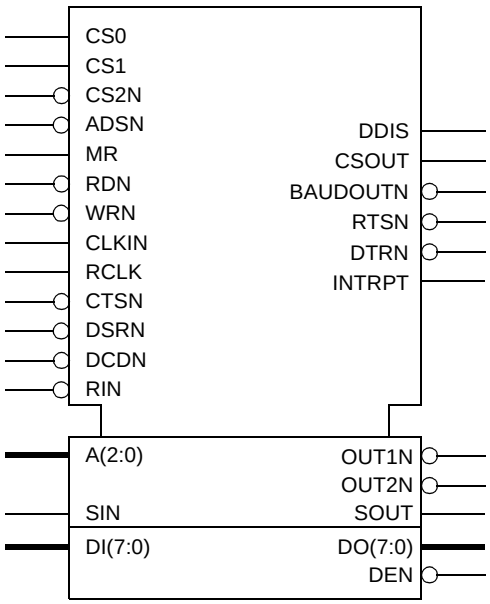
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 8250
- Single megacell UART/BRG
- On chip baud rate generator 1 to 65535 Divisor generates the BAUDOUTN (16x) clock
- Prioritized interrupt mode
- Microprocessor bus oriented interface
- Modem interface
- Line break generation and detection
- Loopback mode
- Double buffered transmitter and receiver
- Equivalent gates:
  Standard Cell - 2,000; Gate Array - 2,500

LOGIC SYMBOL

MG82C50



Description

MG82C50A Asynchronous Communications Element (ACE) is a high-performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single megacell. The device supports data rate from DC to 625K baud (0-10MHz clock). It is functionally compatible with the industry standard 8250.

The ACE receiver circuitry converts start, data, stop and parity bits into a parallel data word. The transmitter circuitry converts a parallel data word into serial form and appends the start, parity and stop bits. The word length is programmable to 5, 6, 7 or 8 data bits. Stop bit selection provides a choice of 1, 1.5 or 2 stop bits.

The Baud Rate Generator divides the clock frequency by a divisor programmable from 1 to 216-1 to provide standard RS-232C baud rates. The BAUDOUT programmable clock output provides a buffered oscillator or a 16x (16 times the data rate) baud rate clock for general purpose system use.

To meet the system requirements of a CPU interfacing to an asynchronous channel, the modem control signals RTSN, CTSN, DSRN, RIN, DCDN are provided.

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
RDN	I	Read, active low. Causes the register selected by A(2:0) to be output to D(7:0).
WRN	I	Write, active low. Causes data from the data bus D(7:0) to be input to the MG82C50A.
DI(7:0) DO(7:0)	I O	Data Bus inputs and outputs, DI(0) and DO(0) are the LSBs.
DEN	O	Control line used to determine when DO(7:0) is valid. Active low.
A(2:0)	I	Register Select. Selects the internal registers during CPU bus operations. A(0) is the LSB.
CLKIN	I	Clock in. Clock connection for the internal Baud Rate Generator.
SOUT	O	Serial Data Output. Serial data output from the MG82C50A transmitter circuitry.
CTSN	I	Clear to Send, active low. Indicates that data on SOUT can be transmitted.
DSRN	I	Data Set Ready, active low. Indicates the modem is ready to exchange data.
DTRN	O	Data Terminal Ready, active low. Indicates to that the MG82C50A is ready to receive data.
RTSN	O	Request to Send, active low. Indicates data is ready to transmit. In half duplex operations, RTS is used to control the direction of the line.
BAUDOUTN	O	Baud out clock. Rate is the CLKIN frequency divided by the specified divisor in the BSR.
OUT1N,OUT2N	O	Outputs 1and 2, active low. Asserted by setting MCR(2,3) high. Inactive during loop mode.
RIN	I	Ring Indicator, active low. Indicates that a telephone ringing signal has been received by the modem or data set.
DCDN	I	Data Carrier Detect, active low. Indicates that the data carrier has been detected by the modem or data set.
MR	I	Master Reset. Forces the MG82C50A into an idle mode.
INTRPT	O	Interrupt Request. Goes active when an interrupt has occurred if enabled by the IER.
SIN	I	Serial Data Input. Serial data input from the communication line or modem to the MG82C50A receiver circuits. Disabled when operating in the loop mode.
CS0,CS1,CS2N	I	Chip Selects. Enables WRN and RDN. Latched by the ADSN input.
CSOUT	O	Chip Select Out. Indicates the megacell has been selected by active CS0, CS1 and CS2N.
DDIS	O	Driver Disable. Used to disable an external transceiver when the CPU is reading data.
ADSN	I	Address Strobe, active low. Latches A(2:0) and CS0, CS1 and CS2N inputs.
RCLK	I	Baud Rate Clock. This input is the 16x Baud Rate Clock for the receiver section of the MG82C50A. This input may be provided from the BAUDOUT output or an external clock.

MG82C54
Programmable Interval Timer

AMERICAN MICROSYSTEMS, INC.

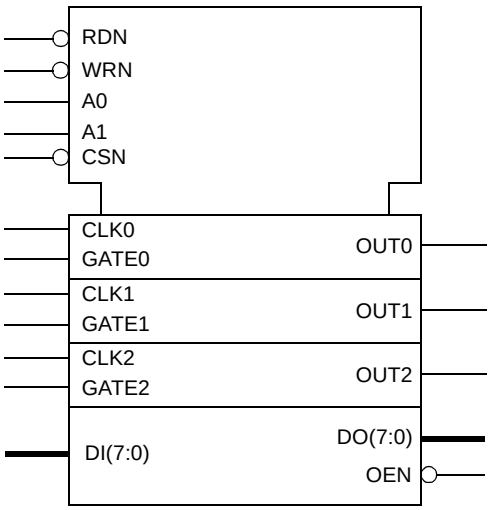
Digital Soft Megacells

Features

- A high-performance, low-power megacell featuring functional compatibility with the industry standard 8254
- Available in several AMI process technologies
- Three independent 16-Bit counters
- Six programmable counter modes
- Status read-back command
- Binary or BCD counting
- Equivalent gates:
  Standard Cell - 2,150; Gate Array - 2,800

LOGIC SYMBOL

MG82C54



Description

MG82C54 is a counter/timer megacell that includes complete functional compatibility with the industry standard 8254. Designed for fast operation, it has three independently programmable 16-bit counters and six programmable counter modes. Counting can be performed in both binary and BCD formats. Speed will depend on what AMI process technology is chosen.

The MG82C54 offers a very flexible, hardware solution to the generation of accurate time delays in microprocessor systems. A general purpose, multi-timing element, it can be used to implement event counters, elapsed time indicators, waveform generators plus a host of other functions.

Major functional blocks include read/write logic, control word register, and three programmable counters.

The read/write logic block generates internal control signals for the different functional blocks using address and control information obtained from the system. The active LOW signals, CSN, RDN and WRN are used to select the MG82C54 for operation, read a counter, and write to a counter (or the control word register) respectively. CSN must be LOW for RDN or WRN to be recognized.

The inputs A0 and A1are used to select the control word register, or one of the three counters that is to be written to or read from. A0 and A1 connect directly to the corresponding signals of the microprocessor address bus, while CS is derived from the address bus using either a linear select method, or an address decoder device.

The MG82C54 has a control word register which is a write only register. It is selected by the read/write logic block when A0 and A1=1. When CSN and WRN are LOW, data are written into the MG82C54 control word register. Control word data are interpreted as a number of different commands which are used to program the various device functions. For example, status information is available with the Read-Back Command.

The MG82C54 contains three identical, independent counter blocks. Each counter provides the same functions, but can be programmed to operate in different modes relative to each other. A typical counter contains the following functional elements: control logic, counter, output latches, count registers and status register.

The low-power consumption of the MG82C54 makes it ideally suited to portable systems or those with low-power standby modes.

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
A1,A0	I	Address. Used to select the Control Word Register (for read or write operations), or one of the three Counters. Normally connected to the system address bus.
CLK0	I	Clock input of counter 0.
CLK1	I	Clock input of counter 1.
CLK2	I	Clock input of counter 2.
CSN	I	Chip select, active low. Enables the MG82C54 to respond to RDN and WRN signals.
DI(7:0)	I	Input data bus.
DO(7:0)	O	Output data bus.
OEN	O	Output enable, active low. Output is low when valid output data is on DO bus.
GATE0	I	Gate input of counter 0.
GATE1	I	Gate input of counter 1.
GATE2	I	Gate input of counter 2.
OUT0	O	Output of counter 0.
OUT1	O	Output of counter 1.
OUT2	O	Output of counter 2.
RDN	I	Read Control, active low. Used to enable the MG82C54 for read operations by the CPU.
WRN	I	Write Control, active low. Used to enable the MG82C54 to be written to by the CPU.

MG82C55A
Programmable Peripheral Interface

AMERICAN MICROSYSTEMS, INC.

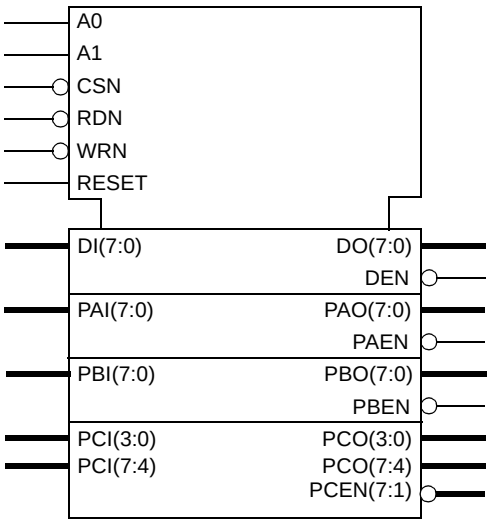
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 8255A
- Supports 8086/8088 and 80186/188 microprocessors
- 24 programmable I/O pins
- Direct bit set/reset capability
- Bidirectional bus operation
- Enhanced control word read capability
- Equivalent gates:
  Standard Cell - 700; Gate Array - 900

LOGIC SYMBOL

MG82C55A



Description

MG82C55A Programmable Peripheral Interface is a high speed, low power CMOS megacell offering functional compatibility with the industry standard 8255A. It is a general purpose I/O component which interfaces peripheral equipment to the microcomputer system bus usually without extra logic.

The MG82C55A has 24 I/O lines grouped as three 8-bit ports (A,B and C), in two control groups (A and B). Group A consists of port A and port C upper (7:4), while group B consists of port B and port C lower (3:0). Group A has three operating modes, (0,1,2) while group B has two (0,1). The operating modes are:

Mode 0: One 8-bit and one 4-bit uni-directional port, without handshaking.

Mode 1: One 8-bit uni-directional port with handshaking.

Mode 2: One 8-bit bi-directional port with handshaking.

For any modes other than mode 0, lines from port C are used as handshaking lines for ports A and B. Port A has latched inputs and latched outputs while ports B and C have unlatched inputs and latched outputs.

The system CPU has full access to the MG82C55A's control register which completely controls the megacell's configuration. When the control word register is read bit D7 will always be a logic ONE to indicate control word mode information.

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
A1,A0	I	Address. These input signals, in conjunction with RDN and WRN, control the selection of one of the three ports or the control word registers.
CSN	I	Chip Select, active low. Enables the MG82C55A to respond to RDN and WRN signals. RDN and WRN are ignored otherwise.
DI(7:0) DO(7:0)	I O	Data Bus.
DEN	O	Control line, active low. Used to determine when DBO(7:0) is valid.
PAI(7:0) PAO(7:0)	I O	Port A. An 8-bit data output latch and an 8-bit data input buffer.
PAEN	O	Control line, active low. Used to determine when PAO(7:0) is valid.
PBI(7:0) PBO(7:0)	I O	Port B. An 8-bit data output latch and an 8-bit data input buffer.
PBEN	O	Control line, active low. Used to determine when PBO(7:0) is valid.
PCI(3:0) PCO(3:0)	I O	Port C, Pins (3:0). Lower nibble of an 8-bit data output latch and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.
PCI(7:4) PCO(7:4)	I O	Port C, Pins(7:4). Upper nibble of Port C.
PCEN(7:1)	O	Control line, active low. Used to determine when PCO(7:0) is valid. PCEN(1) controls PCO(1:0).
RESET	I	Reset. A high on this input clears the control register and all ports are set to the input mode.
RDN	I	Read Control, active low. This input is low during CPU read operations.
WRN	I	Write Control, active low. This input is low during CPU write operations.

MG82C59A
Programmable Interrupt Controller

AMERICAN MICROSYSTEMS, INC.

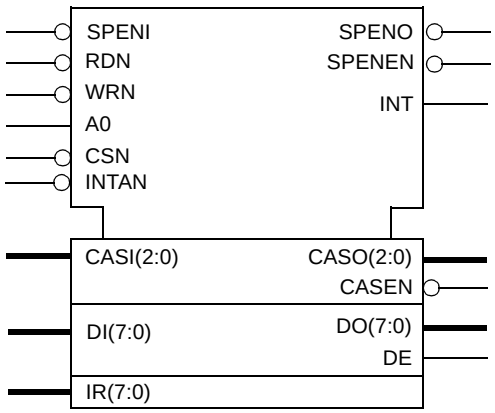
Digital Soft Megacells

Features

- A high-performance, low-power megacell featuring functional compatibility with the industry standard 8259/ 8259A
- Eight level priority controller
- Expandable to 64 levels
- Programmable interrupt modes, with each interrupt maskable
- Edge- or level-triggered interrupt request inputs
- Polling operation
- Equivalent gates:
  Standard Cell - 1,450; Gate Array - 2,000

LOGIC SYMBOL

MG82C59A



Description

MG82C59A is a high-performance, completely programmable interrupt controller. It can process eight interrupt request inputs, assigning a priority level to each one, and is cascadable up to 64 interrupt requests. Individual interrupting sources are maskable. Its two modes of operation (Call and Vector) allow it to be used with virtually all 8000 and 80000 type processors, as well as with 68000 family microprocessors.

Acting as an overall peripherals manager, its functions include:

- Accepting interrupt requests from assorted peripheral devices
- Determining which is the highest priority
- Establishing whether or not the new interrupt is of a higher priority than any interrupts which might be currently being serviced, and if so,
- Issuing an interrupt to the CPU
- Then providing the CPU with the interrupt service routine address of the interrupting peripheral

Each peripheral device usually has a specific interrupt service routine which is particular to its operational or functional requirements within the system. The MG82C59A can be programmed to hold a pointer to the service routine addresses associated with each of the peripheral devices under its control. Thus when a peripheral interrupt is passed through to the CPU, the MG82C59A can set the CPU Program Counter to the interrupt service routine required. These pointers (or vectors) are addresses in a vector table.

The MG82C59A is intended to run in one of two major operational modes, according to the type of CPU being used in the system. The CALL Mode is used for 8085 type microprocessor systems, while the VECTOR Mode is reserved for those systems using more sophisticated processors such as the 8088/86, 80286/386 or 68000 family.

In either mode, the MG82C59A can manage up to eight interrupt request levels individually, with a maximum capability of up to 64 interrupt request levels when cascaded with other MG82C59As. A selection of priority modes is also available such that interrupt requests can be processed in a number of different ways to meet the requirements of a variety of system configurations.

Priority modes can be changed or reconfigured dynamically at any time during system operation using the operation command words (OCWs), allowing the overall interrupt structure to be defined for a complete system. Note that the MG82C59A is programmed by the system software as an I/O peripheral.

The MG82C59A's high-performance and very low-power consumption makes it useful in portable systems and systems with low-power standby modes.

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
A0	I	A0 Address Line. Acts in conjunction with the CSN, WRN and RDN signals. It is used to decipher various command words written by the CPU, and Status information read by the CPU. It is typically connected to the CPU - A0 address line.
CSN	I	Chip Select, active low. Used to enable RDN and WRN communication between the CPU and the MG82C59A. Note that INTAN functions are independent of CSN.
INTAN	I	Interrupt Acknowledge. Signal used to enable the MG82C59A interrupt vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
WRN	I	Write, active low. Used to enable the MG82C59A to accept command words from the CPU, when CSN is LOW.
RDN	I	Read, active low. Used to enable the MG82C59A to output status information onto the data bus for the CPU, when CS is LOW.
IR(7:0)	I	Interrupt Requests. Asynchronous input signals, an interrupt request is executed by raising an IR input, and holding it HIGH until it is acknowledged (Edge Triggered Mode), or just by a HIGH level on an IR input (Level Triggered Mode).
CASI(2:0) CASO(2:0)	I O	Cascade Lines. The CAS lines are used as a private bus by a MG82C59A master to control multiple MG82C59A slaves. The master uses only CASO(2:0). The slaves use CASI(2:0).
CASEN	O	Control line used to determine when CASO(2:0) is valid. Active low.
SPENI SPENO	I O	Slave Program/Enable Buffer. Dual function control signal. When in the Buffered Mode, SPENO is used to control buffer transceivers. When not in the Buffered Mode, SPENI is used to designate a master (SP = 1) or a slave (SP = 0).
SPENEN	O	Control line used to determine when SPENO is valid. Active low.
DI(7:0) DO(7:0)	I O	Data Bus. 8-Bit data bus for the transfer of control, status and interrupt vector information.
DE	O	Control line used to determine when DO(7:0) is valid. Active high.
INT	O	Interrupt. This signal goes HIGH when a valid interrupt request is asserted.

M8490
SCSI Controller

AMERICAN MICROSYSTEMS, INC.

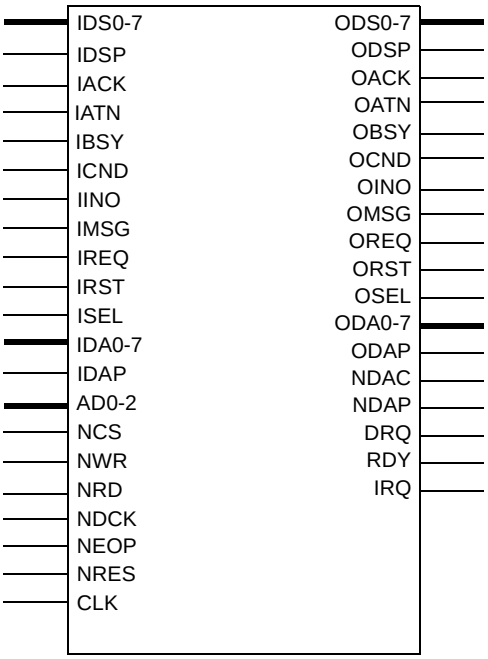
Digital Soft Megacells

Features

- Functionally compatible with the industry standard
- Compatible with ANSI SCSI-II
- Initiator or target mode
- Provides arbitration and bus clear/free/settle delays
- Enhanced arbitration mode
- Generates 9 separate interrupts
- Compatible with 5380 SCSI controller
- Equivalent gates:
  Standard Cell - 1,200; Gate Array - 1,500

LOGIC SYMBOL

M8490



Description

M8490 is a Small Computer Systems Interface (SCSI) controller. It can control 8-bit asynchronous communication over an ANSI SCSI-II bus. It has an 8-bit CPU interface through which the local processor can program it to act as initiator or target on the SCSI bus, and can control all phases of data transfers by writing to command registers within the M8490. It can generate up to 9 separate interrupts to signal to the local processor when commands have been completed or errors have occurred. Bus clear, free and settle delays, and optionally arbitration delays, can be generated automatically from an external clock. Signals are provided to allow data to be transferred to, and from, the M8490 by DMA.

The M8490 is 5380 compatible, applications currently using the 5380 controller should be able to use the M8490 with out software changes. The M8490 has additional features not found in the 5380 making it more attractive for new designs, these additional features are:- CPU parity, programmable CPU and SCSI parity, loop back mode, enhanced arbitration and interrupt support.

The CPU interface block provides an 8-bit interface to the twelve internal registers that control the M8490. The registers control the operation of the SCSI bus controller, the DMA controller and the interrupt controller. The data transferred over the SCSI bus is also written and read by the CPU interface.

The DMA controller block provides an alternative means of writing data to the Output Data register, or reading data from the Input Data Register. When DMA is enabled the M8490 requests a DMA cycle by asserting DRQ high. When the request is acknowledged by asserting NDACK low then reads or writes will be directed to the IDS or ODS register respectively. A DMA transfer is terminated by asserting NEOP low during the last DMA transfer.

The interrupt controller can generate interrupts to signal the completion of a DMA transfer, the completion of arbitration, the selection of the M8490 or an error condition. The source of the interrupt can be found by reading the RPI register.

The SCSI controller block provides access to the SCSI bus. Internal timers are used to provide bus free, bus clear and bus settle delays, and to time the arbitration period.

A per-use fee is associated with this megacell. Contact the factory for more information.

AMERICAN MICROSYSTEMS, INC.

M85C30
Serial Communications Controller

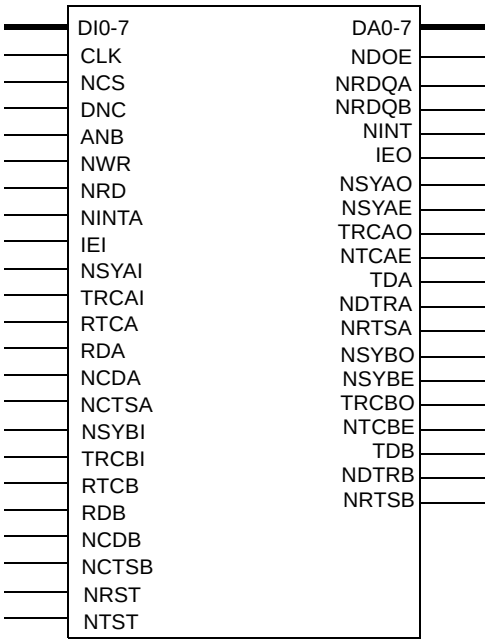
Digital Soft Megacells

Features

- Functionally compatible with the industry standard
- Asynchronous and synchronous modes
- MONOSYNC, BISYNC and SDLC supported
- SDLC loop-mode supported
- NRZ, NRZI and FM encoding/decoding
- Two independent full-duplex channels
- Digital phase-locked loop for each channel
- Baud rate generator for each channel
- Local loop-back and automatic echo modes
- SDLC Frame counter and status FIFO
- Equivalent gates:
  Standard Cell - 12,700; Gate Array - 16,500

LOGIC SYMBOL

M85C30



Description

M85C30 serial communications controller has two independent full-duplex channels which support asynchronous, bit synchronous (SDLC, HDLC and SDLC loop mode) and byte synchronous (MONOSYNC, BISYNC) communication modes. NRZ, NRZI and FM data encoding/decoding are supported.

It includes a baud rate generator and a digital phase-locked loop for each channel. Two diagnostic modes: local loopback and automatic echo are available. A character counter and a 10 X 19-bit frame status FIFO are available in SDLC mode.

The M85C30 is fully programmable by an 8-bit system interface, which includes a six source interrupt controller. The interrupt controller has external signals that allow it to be daisy-chained with other interrupt controllers.

A per-use fee is associated with this megacell. Contact the factory for more information.

M8868A
UART

AMERICAN MICROSYSTEMS, INC.

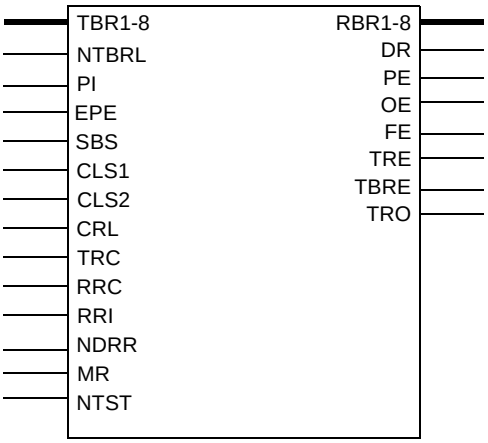
Digital Soft Megacells

Features

- Functionally compatible with the industry standard
- Programmable word length, stop bits and parity
- Double-buffered receiver and transmitter
- Overrun, parity and framing error detection
- Equivalent gates:
  Standard Cell - 600; Gate Array - 760

LOGIC SYMBOL

M8868A



Description

M8868A is a full-duplex universal asynchronous receiver/transmitter (UART). It supports word lengths from five to eight bits, an optional parity bit and one or two stop bits. It can detect overrun, parity and framing errors in the received character.

The M8868A differs from the M6402 in that the master reset sets the TRE output to “1” and clears the receive buffer.

A per-use fee is associated with this megacell. Contact the factory for more information.

AMERICAN MICROSYSTEMS, INC.

M91C36
Digital Data Separator

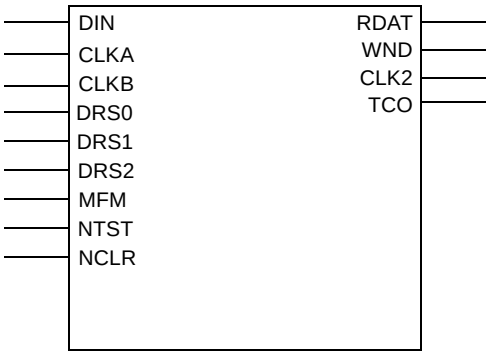
Digital Soft Megacells

Features

- Functionally compatible with the industry standard
- Data rates up to 1.25 Mbps
- 75% Jitter tolerance
- ±6.25% Frequency range
- Equivalent gates:
  Standard Cell - 800; Gate Array - 1,100

LOGIC SYMBOL

M91C36



Description

M91C36 is a digital data separator for use with a floppy disk controller. It takes the “raw” FM or MFM data pulses from a disk drive and outputs a clock at the bit rate and data pulses synchronized to that clock. These signals can then go to a floppy disk controller, such as the MFDC, M765A or similar, for decoding. Three control lines, and the FM/MFM control line, together with a clock (typically 48 or 60 MHz) determine the data rate. This data rate can be up to 1.25 Mbps.

The M91C36 contains a clock selector block and a second order digital phase-locked loop which locks to the frequency and phase of the input data pulses.

The clock selector block produces an internal reference clock 16 times the cycle rate of the phase-locked loop (32 times the data rate). This internal reference clock determines the resolution to which the inputs and outputs are sampled, however the phase and frequency errors are calculated to a much higher resolution (12 bits and 8 bits respectively). This allows very high performance without using a very high clock speed.

The WND output is toggled at the end of every cycle of the phase-locked loop (twice per bit period). If a data pulse occurred at the DIN input during a cycle an active high pulse, lasting two periods of the internal reference clock and synchronized to WND, appears at the RDAT output.

Unlike an analogue data separator the performance of a digital data separator, such as the M91C36, is independent of the data rate. Its performance at 1.25 Mbps (with an internal clock of 40 MHz) is the same as its performance at 250 Kbps (with an internal clock of 8 MHz).

A per-use fee is associated with this megacell. Contact the factory for more information.

M91C360
Digital Data Separator

AMERICAN MICROSYSTEMS, INC.

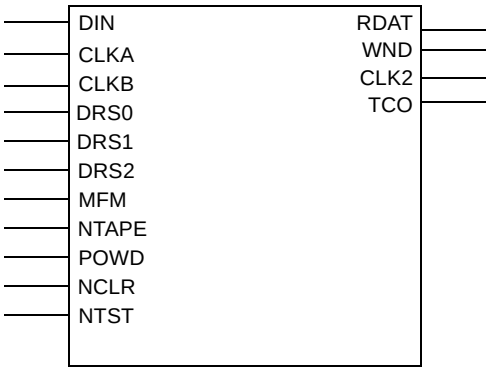
Digital Soft Megacells

Features

- Functionally compatible with the industry standard
- Data rates up to 1.25 Mbps
- Floppy disk or tape
- Power saving mode
- Equivalent gates:
  Standard Cell - 950; Gate Array - 1,250

LOGIC SYMBOL

M91C360



Description

M91C360 is a digital data separator for use with a floppy disk or tape controller. It takes the “raw” FM or MFM data pulses from a disk or tape drive and outputs a clock at the bit rate and data pulses synchronized to that clock. These signals can then go to a floppy disk controller, such as the MFDC, M765A or similar, for decoding.

Three control lines, and the FM/MFM control line, together with a clock (typically 48 or 60 MHz) determine the data rate. This data rate can be up to 1.25 Mbps.

The M91C360 can be configured for use with tape drives. This will increase the frequency range of the data separator at the cost of a slight reduction in jitter performance.

The M91C360 can be placed in a power-down mode which will stop the internal clock to reduce power when not in use.

The M91C360 contains a clock selector block and a second order digital phase-locked loop which locks to the frequency and phase of the input data pulses.

The clock selector block produces an internal reference clock 16 times the cycle rate of the phase-locked loop (32 times the data rate). This internal reference clock determines the resolution to which the inputs and outputs are sampled, however the phase and frequency errors are calculated to a much higher resolution (12 bits and 8 bits respectively). This allows very high performance without using a very high clock speed.

The WND output is toggled at the end of every cycle of the phase-locked loop (twice per bit period). If a data pulse occurred at the DIN input during a cycle an active high pulse, lasting two periods of the internal reference clock and synchronized to WND, appears at the RDAT output.

Unlike an analogue data separator the performance of a digital data separator, such as the M91C360, is independent of the data rate. Its performance at 1.25 Mbps (with an internal clock of 40 MHz) is the same as its performance at 250 Kbps (with an internal clock of 8 MHz).

A per-use fee is associated with this megacell. Contact the factory for more information.

AMERICAN MICROSYSTEMS, INC.

MFDC
Floppy Disk Controller

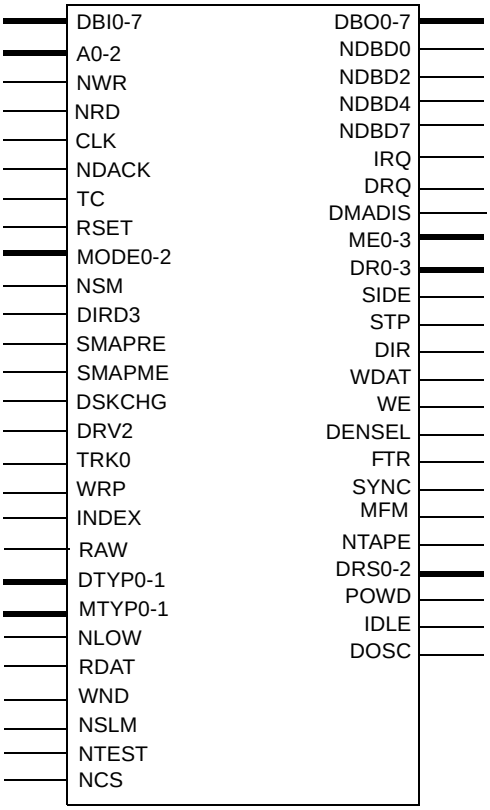
Digital Soft Megacells

Features

- Functionally compatible with the industry standard
- IBM System 3740 format
- IBM System 34 format
- Perpendicular recording format
- Data rates up to 1.25 Mbps
- Directly addresses 256 tracks
- 255 step recalibrate command
- Programmable write precompensation
- 16 byte FIFO
- Enhanced power-saving features
- Equivalent gates:
  Standard Cell - 8,100; Gate Array - 10,500

LOGIC SYMBOL

MFDC



Description

MFDC is a floppy disk controller which uses the M765A floppy disk controller core and includes the interface circuitry required in IBM PC compatible systems. It includes power saving features which are software compatible with the 82077SL. These include a clock disable signal, immediate auto-powerdown, low-latency awakening and a power-saving state for the write precompensator. The MFDC also contains multiplexers for swapping the default drive control outputs under software control.

The MFDC can be combined with the M91C360 digital data separator (or another data separator) to form a complete 82077SL compatible PC and PS/2™ floppy disk subsystem.

All references in this document to the 'core' or 'M765A' refer to the M765A Floppy Disk Controller that is incorporated in the MFDC net list.

PS/2™ is a trademark of IBM Corporation.

The MFDC uses the M765A core and provides additional interfacing logic for a PC compatible system. The additional blocks added to the M765A core are:

I/O BUFFERING. This block provides a PC compatible CPU interface and access to additional registers outside the M765Acore. The polarity of control signals can also be inverted by this block.

CLOCK GENERATOR. This block produces three clocks for the M765A core from the 24/30 MHz input clock to the MFDC.The frequency of the clocks to the M765A core are set by the data rate selected.

DRIVE MAPPING. This block controls the mapping of the logical drive numbers from the M765A core to the physical drive numbers coming from the MFDC.

WRITE PRECOMPENSATION. This block applies precompensation to the data stream coming from the M765A core. The amount of precompensation is determined by the delay period and data rate.

POWERDOWN CONTROLLER. This block can provide either direct or automatic powerdown which will stop internal clocks to save power.

A per-use fee is associated with this megacell. Contact the factory for more information.

MGI2CSL
I2C Serial Bus Slave Transceiver

AMERICAN MICROSYSTEMS, INC.

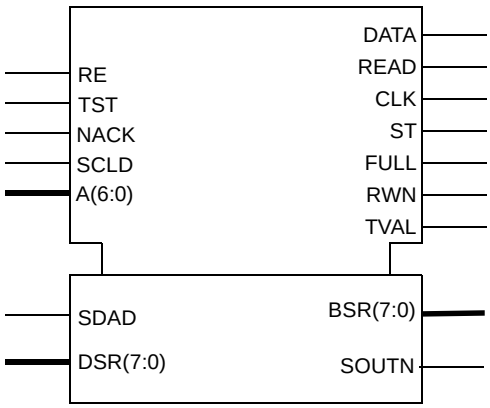
Digital Soft Megacells

Features

- Phillips licensed I2C slave transceiver
- Supports normal (100kbit/s) and fast (400kbit/s) modes when used with appropriate pads
- Supports 7-bit addressing
- Schematic-based, uses the ASIC Standard Library for technology independence
- Equivalent gates:
  Standard Cell - 210; Gate Array - 250

LOGIC SYMBOL

MGI2CSL



Description

MGI2CSL megacell implements an I2C serial to 8-bit parallel bidirectional I/O port. The MGI2CSL is designed to provide I2C bus handshaking and protocol support for a slave port. The seven bit port address is externally programmable from the A(6:0) bus. Port addresses are assigned by Phillips.

Received data is not latched. Received data is available on the BSR bus during the one clock cycle that FULL is HI. Data must be captured by the external logic during this time or it will be lost. FULL transitions on the falling edge of clock.

Because it is a minimal configuration it operates in slave mode only and does not support any of the following: clock stretching for slow peripherals, general call addressing, or ten-bit extended addressing. The MGI2CSL does support both normal (0 - 100kbit/s) and fast (0 - 400kbit/s) modes when used with appropriate pads. Contact the factory for pad selection and availability.

Phillips has represented to AMI that purchase of AMI's I2C components conveys a license under the Phillips I2C Patent Rights to use these components in an I2C system. Provided that the system conforms to the I2C Standard Specification as defined by Phillips.

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
SCLD	I	Input from bus clock line.
SDAD	I	Input from bus data line.
RE	I	Reset, active high.
TST	I	Test mode, active high.
NACK	I	When high, suppresses transmission of acknowledge signal.
A(6:0)	I	Programs 7-bit address that the cell responds to. Address are assigned by Phillips.
DSR(7:0)	I	Parallel data input for serial out.
SOUTN	O	Serial data out to bus driver.
TVAL	O	Transmission valid. Goes high when port has received a valid address.
RWN	O	Status of read/write bit. Indicates whether master is reading or writing to this port. High indicates a read, a low indicates a write.
FULL	O	High indicates shift register full. BSR bus must be read before the next falling edge of CLK.
ST	O	High Indicates reception of start signal from bus or reset on RE.
CLK	O	Follows bus clock while transmission is valid.
READ	O	RWN delayed by one clock.
DATA	O	A high level indicates when in DATA mode. A low indicates ADDRESS mode.
BSR(7:0)	O	Parallel data out from serial in.

MI2C
I2C Bus Interface

AMERICAN MICROSYSTEMS, INC.

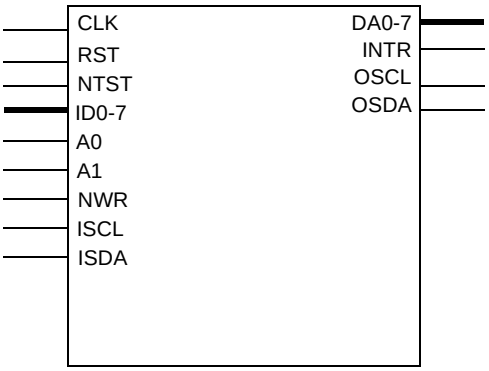
Digital Soft Megacells

Features

- Functionally compatible with the industry standard
- Master or slave operation
- Multi-master systems supported
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Equivalent gates:
  Standard Cell - 1,200; Gate Array - 1,450

LOGIC SYMBOL

MI2C



Description

MI2C provides an interface between a microprocessor and an I2C bus. It can operate in master or slave mode and performs arbitration in master mode to allow it to operate in multi-master systems. In slave mode it can interrupt the processor when it recognizes its own 7-bit address or the general call address. A clock divider is provided to allow operation from a wide range of input clock frequencies.

A per-use fee is associated with this megacell. Contact the factory for more information.

MGAxxyyDv Adder

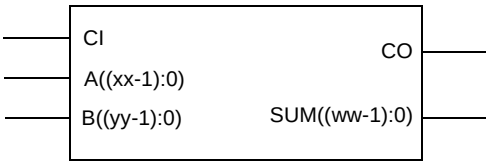
Digital Soft Megacells

Features

- High-performance, Schematic-based megacell Word length for inputs A and B are user definable
- Selects multiple architectures for size and speed efficiency
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGAxxyyDv



Description

MGAxxyyDv adder synthesizer builds xx-bit by yy-bit adders. Input operands are A and B with an input carry CI to produce the output SUM with a carry-out CO.

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead.

Inputs A and B and output SUM can be interpreted to be either in the two's complement or unsigned number format. The SUM output is the same format as the inputs; its size is the same as the largest of inputs A or B.

In the name, "xx" represents the A input size and "yy" represents the B input size. The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit by 20-bit adder optimized for minimum delay would be named MGA2420D2.

Functional Description

A	B	CI	SUM	CO
A	B	0	A + B	carry-out
A	B	1	A + B + 1	carry-out

Contact the factory for information on specific speeds and sizes or to have an Adder built.

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
CI	Input	Carry in, active high.	1
A((xx-1):0)	Input	A Data inputs. A(0) is the LSB.	width > 0
B((yy-1):0)	Input	B Data inputs. B(0) is the LSB.	width > 0
CO	Output	Carry out, active high.	1
SUM((ww-1):0)	Output	SUM Data outputs. SUM(0) is the LSB.	width > 0

Equivalent Gates

CELL NAME	EQ GATES
MGA0808D1	62
MGA0808D2	144
MGA1212D1	92
MGA1212D2	217

MGAxxyyEv Adder/Subtractor

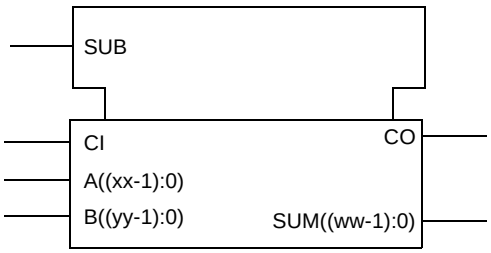
Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Word length for inputs A and B are user definable
- Selects multiple architectures for size and speed efficiency
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGAxxyyEv



Description

MGAxxyyEv adder/subtractor synthesizer builds xx-bit by yy-bit adder/subtractors. This megacell either adds (SUB=0) or subtracts (SUB=1) depending on the value of SUB. Input operands are A and B with an input carry CI and a subtract control line SUB. The outputs are SUM and carry-out CO.

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead.

Inputs A and B and output SUM can be interpreted to be either in the two's complement or unsigned number format. The SUM output is the same format as the inputs; its size is the same as the largest of inputs A or B.

In the name, "xx" represents the A input size and "yy" represents the B input size. The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit by 20-bit adder/subtractor optimized for minimum delay would be named MGS2420A2.

Functional Description

SUB	A	B	CI	SUM	CO
0	A	B	0	A + B	carry-out
0	A	B	1	A + B + 1	carry-out
1	A	B	0	A - B	carry-out
1	A	B	1	A - B - 1	carry-out

Contact the factory for information on specific speeds and sizes or to have an Adder/Subtractor built.

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
SUB	Input	Subtract control. Megacell subtracts when this input is high.	1
CI	Input	Carry in, active high.	1
A((xx-1):0)	Input	A Data inputs. A(0) is the LSB.	width > 0
B((yy-1):0)	Input	B Data inputs. B(0) is the LSB.	width > 0
CO	Output	Carry out, active high.	1
SUM((ww-1):0)	Output	SUM Data outputs. SUM(0) is the LSB.	width > 0

Equivalent Gates

CELL NAME	EQ GATES
MGA0808E1	82
MGA0808E2	168
MGA1212E1	120
MGA1212E2	288

AMERICAN MICROSYSTEMS, INC.

MGBxxAv
Barrel/Arithmetic Shifter

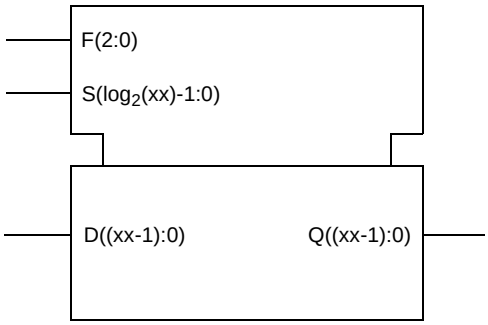
Digital Soft Megacells

Features

- Schematic-based megacell synthesizer
- Word length is definable
- High-speed flash shift operations
- Logical and arithmetic shifts available

LOGIC SYMBOL

MGBxxAv



Description

The MGBxxAv barrel/arithmetic shifter synthesizer builds barrel/arithmetic shifters which provide various shift functions for a data word size of “xx” bits. The shifts are performed completely through combinational logic which allows for very fast operations. Commonly used logical and arithmetic shift functions are available.

The user has flexibility in specifying the word size. Within the name shown above, the “xx” represents the size of the data word. The size of the S bus is equal to log2(xx).

The “v” represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, an 8-bit shifter optimized for minimum gate count would be named MGB08A1.

The S inputs select the number of bits to be shifted. For a right circular shift, the S inputs select the number of bits to be shifted. For a left circular shift, the two’s compliment of the number of bits to be shifted is placed on the S inputs. In the case of an 8-bit shifter, for example, an input select value of two (010) operating on the input 00001100 will generate the output 00000011, a right shift of two bits. If S has the value of seven (111) the output would become 00011000, which would represent a right shift of seven or a left shift of one.

The type of shift function is controlled by the F inputs and are as described in the following table.

Shift Functions

F(2)	F(1)	F(0)	FUNCTION
0	0	0	Logic shift with zeros fill
0	0	1	Logic shift with ones fill
0	1	x	Arithmetic shift with sign extend
1	0	x	Logical shift with D0 fill
1	1	x	Left of Right circular shift

Sample Truth Tables(MGB04Av):

Logical shift with zeros fill, F(2:0) = 000

S(1:0)	Q(3)	Q(2)	Q(1)	Q(0)
00	D(3)	D(2)	D(1)	D(0)
01	0	D(3)	D(2)	D(1)
10	0	0	D(3)	D(2)
11	0	0	0	D(3)

Logical shift with ones fill, F(2:0) = 001

S(1:0)	Q(3)	Q(2)	Q(1)	Q(0)
00	D(3)	D(2)	D(1)	D(0)
01	1	D(3)	D(2)	D(1)
10	1	1	D(3)	D(2)
11	1	1	1	D(3)

Logical shift with D(0) fill, F(2:0) = 10x

S(1:0)	Q(3)	Q(2)	Q(1)	Q(0)
00	D(3)	D(2)	D(1)	D(0)
01	D(0)	D(3)	D(2)	D(1)
10	D(0)	D(0)	D(3)	D(2)
11	D(0)	D(0)	D(0)	D(3)

Arithmetic shift with sign extend, F(2:0) = 01x

S(1:0)	Q(3)	Q(2)	Q(1)	Q(0)
00	D(3)	D(2)	D(1)	D(0)
01	D(3)	D(3)	D(2)	D(1)
10	D(3)	D(3)	D(3)	D(2)
11	D(3)	D(3)	D(3)	D(3)

Left or Right circular shift, F(2:0) = 11x

S(1:0)	Q(3)	Q(2)	Q(1)	Q(0)
00	D(3)	D(2)	D(1)	D(0)
01	D(0)	D(3)	D(2)	D(1)
10	D(1)	D(0)	D(3)	D(2)
11	D(2)	D(1)	D(0)	D(3)

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
F(2:0)	Input	Function inputs. These inputs determine the type of shift to be performed.	3
S($\log_2$(xx)-1:0)	Input	Shift inputs. Specifies the number of position to be shifted.	width = $\log_2$(xx)
D((xx-1):0)	Input	Data inputs. D(0) is the LSB.	width > 0
Q((xx-1):0)	Output	Data outputs. Q(0) is the LSB.	width > 0

Equivalent Gates

CELL NAME	EQ GATES
MGB08A1	110
MGB08A2	133
MGB12A1	207
MGB12A2	250

AMERICAN MICROSYSTEMS, INC.

MGBxxBv Barrel Shifter

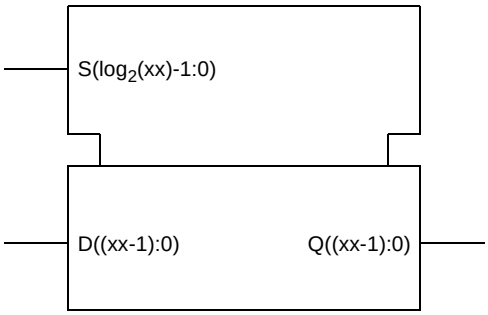
Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Word length is definable
- High-speed flash barrel shift operations
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGBxxBv



Description

MGBxxBv barrel shifter synthesizer builds barrel shifters which provide various shift functions for a data word size of “xx” bits. The shifts are performed completely through combinational logic which allows for very fast operations. Shifted data wraps around from the MSB to the LSB.

The S inputs select the number of bits to be shifted from the D inputs to the Q outputs. In the case of an 8-bit shifter, for example, an input select value of two (010) operating on the input 00001100 will generate the output 00110000, a left shift of two bits. If S has the value of seven (111), the output would become 00000110.

The user has flexibility in specifying the word size. Within the name shown above, the “xx” represents the size of the data word. The size of the S bus must be less than or equal to log2(xx). For example, if xx = 8, the size of the S bus must be equal to or less than 3. If not all shift combinations are needed, the size of the S bus can be reduced to save logic.

The “v” represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, an 8-bit shifter optimized for minimum gate count would be named MGB08B1.

Contact the factory for information on specific speeds and sizes or to have a Shifter built.

Sample Truth Table

S(1:0)	Q(3)	Q(2)	Q(1)	Q(0)
00	D(3)	D(2)	D(1)	D(0)
01	D(2)	D(1)	D(0)	D(3)
10	D(1)	D(0)	D(3)	D(2)
11	D(0)	D(3)	D(2)	D(1)

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
S($\log_2$(xx)-1:0)	Input	Shift inputs. Specifies the number of position to be shifted.	width ≤ $\log_2$(xx)
D((xx-1):0)	Input	Data inputs. D(0) is the LSB.	width > 0
Q((xx-1):0)	Output	Data outputs. Q(0) is the LSB.	width > 0

Equivalent Gates

CELL NAME	EQ GATES
MGB08B1	77
MGB08B2	80
MGB12B1	155
MGB12B2	200

AMERICAN MICROSYSTEMS, INC.

MGBxxyyCv Arithmetic Shifter

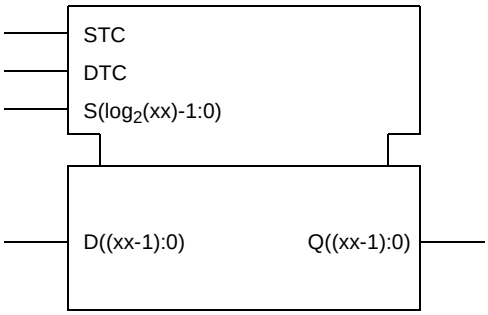
Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Word length is definable
- High-speed flash arithmetic shift operations
- Two's complement or unsigned shift control and data
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGBxxyyCv



Description

MGBxxyyCv arithmetic shifter synthesizer builds arithmetic shifters which provide various shift functions for a data word size of "xx" bits. The shifts are performed completely through combinational logic which allows for very fast operations.

The input data D is shifted left or right by the number of bits specified by the control input S. When the control signal STC is '0', S is interpreted as an unsigned positive number and the shifter performs only left shift operations.

When STC is '1', S is a two's complement number. If S is negative, a right shift is performed. If S is positive, a left shift is performed.

The input data D is interpreted as an unsigned number when DTC is '0' or a two's complement number when DTC is '1'. The type of D is only significant for right shift operations where zero padding is done on the MSBs for unsigned data and sign extension is done for two's complement data.

The user has flexibility in specifying the word size. Within the name shown above, the "xx" represents the size of the data word and "yy" represents the size of the S bus.The size of the S bus is equal to log2(xx).

The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example an 8-bit shifter optimized for minimum gate count would be named MGB0803C1.

Sample Truth Table (MGB0402Cv):

S(1:0)	STC	DTC	Q(3)	Q(2)	Q(1)	Q(0)
00	0	x	D(3)	D(2)	D(1)	D(0)
01	0	x	D(2)	D(1)	D(0)	0
10	0	x	D(1)	D(0)	0	0
11	0	x	D(0)	0	0	0
00	1	x	D(3)	D(2)	D(1)	D(0)
01	1	x	D(2)	D(1)	D(0)	0
10	1	0	0	0	D(3)	D(2)
11	1	0	0	D(3)	D(2)	D(1)
10	1	1	D(3)	D(3)	D(3)	D(2)
11	1	1	D(3)	D(3)	D(2)	D(1)

Contact the factory for information on specific speeds and sizes or to have a Shifter built.

MGBxxyyCv
Arithmetic Shifter

AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
STC	Input	Determines whether S is interpreted as unsigned or two's complement.	1
DTC	Input	Determines whether D is interpreted as unsigned or two's complement.	1
S($\log_2$(xx)-1:0)	Input	Shift inputs. Specifies the number of position to be shifted.	width < $\log_2$(xx)
D((xx-1):0)	Input	Data inputs. D(0) is the LSB.	width > 0
Q((xx-1):0)	Output	Data outputs. Q(0) is the LSB.	width > 0

Equivalent Gates

CELL NAME	EQ GATES
MGB0803C1	130
MGB0803C2	175
MGB1204C1	223
MGB1204C2	320

AMERICAN MICROSYSTEMS, INC.

MGCDxxAv Decrement Counter

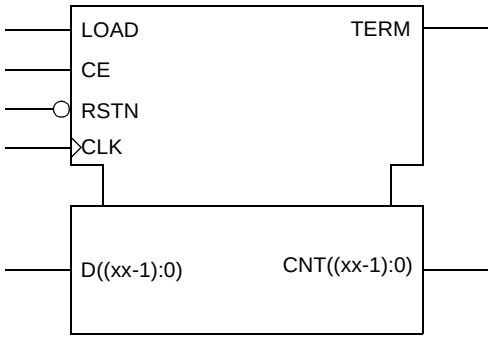
Digital Soft Megacells

Features

- High-performance, HDL-based megacell synthesizer
- Counter size is definable
- Includes terminal count when count is zero
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGCDxxAv



Description

MGCDxxAv synchronous binary counter counts down on the rising edge of the clock. This counter is available in all of AMI's supported processes.

The "xx" in the name represents the number of bits in the counter. For example, an 8-bit counter built for minimum delay would be named MGCD08A2.

The counter has three input controls LOAD, CE, and RSTN. Both LOAD and CE must be asserted for the parallel input to be latched in on the next rising clock edge. When LOAD is low and CE is high the counter decrements by one on each rising clock edge. When the count reaches zero the TERM signal is asserted high. The RSTN is asynchronous and asserted low. The counter output (CNT) is the same size as the counter input (D).

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead. These Megacells are produced using parameterized synthesizers that allow the creation of various sizes and speeds. The synthesized Megacell can be optimized for either minimum delay, minimum gate count or can be designed to meet a specified delay. Each implementation is given a different version number. For example, an 8-bit counter that must run on a 20 ns clock cycle would be named MGCD08A20.

MGCDxxAv
Decrement Counter

AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

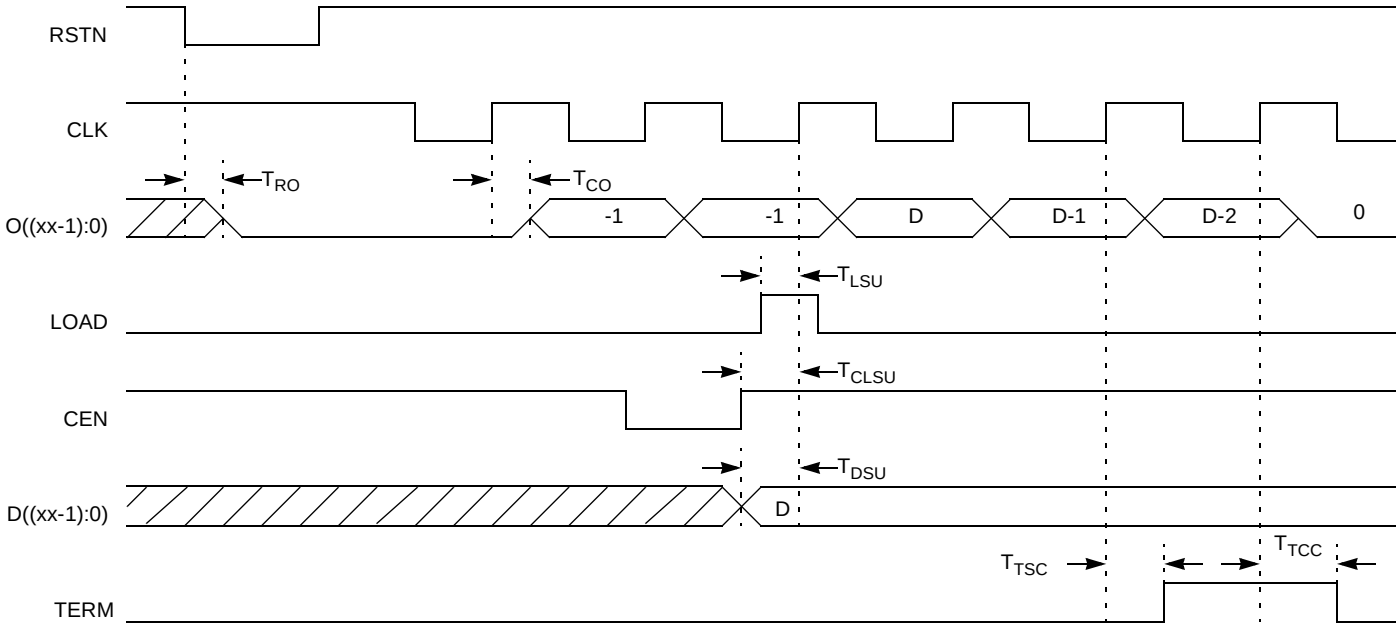
Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
LOAD	Input	Load new count. Data is latched when LOAD and CE are high and the clock transitions from low to high.
CE	Input	Count enable. Next count or input latched when CE is high and the clock transitions from low to high.
RSTN	Input	Reset signal. Asynchronously resets counter to 0 when low.
D((xx-1):0)	Input	Data inputs. Data appearing on these inputs is latched into the count when LOAD and CE are high and the clock transitions from low to high.
TERM	Output	Terminal count. Asserted high when the count is all zeros.
CNT((xx-1):0)	Output	Data outputs. The output is decremented by one when the clock transitions from low to high and the CE is asserted.

Equivalent Gates

CELL NAME	EQ GATES
MGCU08A1	120
MGCU08A2	188
MGCU12A1	179
MGCU12A2	288

Count Timing



Timing Characteristics

SYMBOL	CHARACTERISTIC	REFERENCED TO
T_{RO}	reset to output zero	RSTN falling
T_{CO}	clock to count valid	CLK rising
T_{LSU}	load set-up	CLK rising
T_{CLSU}	count enable load set-up	CLK rising
T_{DSU}	data set-up	CLK rising
T_{TSC}	term set valid	CLK rising
T_{TCC}	term clear valid	CLK rising

MGCUxxAv
Increment Counter

AMERICAN MICROSYSTEMS, INC.

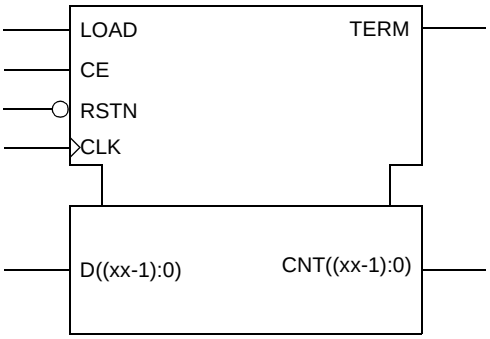
Digital Soft Megacells

Features

- High-performance, HDL-based megacell synthesizer
- Counter size is definable
- Includes terminal count when count is all ones
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGCUxxAv



Description

MGCUxxAv synchronous binary counter counts on the rising edge of the clock. This counter is available in all of AMI's supported processes.

The "xx" in the name represents the number of bits in the counter. For example, an 8-bit counter built for minimum delay would be named MGCU08A2.

The counter has three input controls LOAD, CE, and RSTN. Both LOAD and CE must be asserted for the parallel input to be latched in on the next rising clock edge. When LOAD is low and CE is high the counter increments by one on each rising clock edge. When the count reaches the maximum count the TERM signal is asserted high. The RSTN is asynchronous and asserted low. The counter output (CNT) is the same size as the counter input (D).

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead. These Megacells are produced using parameterized synthesizers that allow the creation of various sizes and speeds. The synthesized Megacell can be optimized for either minimum delay, minimum gate count or can be designed to meet a specified delay. Each implementation is given a different version number. For example, an 8-bit counter that must run on a 20 ns clock cycle would be named MGCU08A20.

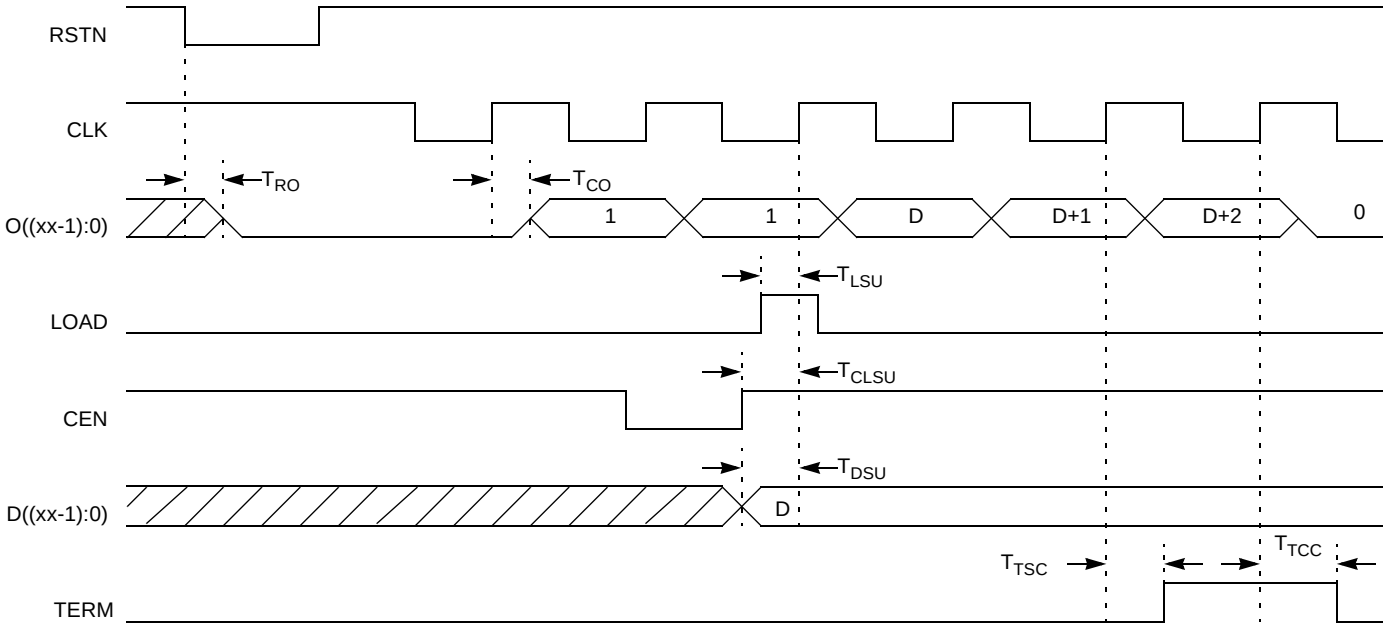
Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
LOAD	Input	Load new count. Data is latched when LOAD and CE are high and the clock transitions from low to high.
CE	Input	Count enable. Next count or input latched when CE is high and the clock transitions from low to high.
RSTN	Input	Reset signal. Asynchronously resets counter to 0 when low.
D((xx-1):0)	Input	Data inputs. Data appearing on these inputs is latched into the count when LOAD and CE are high and the clock transitions from low to high.
TERM	Output	Terminal count. Asserted high when the count is all ones.
CNT((xx-1):0)	Output	Data outputs. The output is incremented by one when the clock transitions from low to high and the CE is asserted.

Equivalent Gates

CELL NAME	EQ GATES
MGCU08A1	119
MGCU08A2	155
MGCU12A1	178
MGCU12A2	261

Count Timing



Timing Characteristics

SYMBOL	CHARACTERISTIC	REFERENCED TO
T_{RO}	reset to output zero	RSTN falling
T_{CO}	clock to count valid	CLK rising
T_{LSU}	load set-up	CLK rising
T_{CLSU}	count enable load set-up	CLK rising
T_{DSU}	data set-up	CLK rising
T_{TSC}	term set valid	CLK rising
T_{TCC}	term clear valid	CLK rising

AMERICAN MICROSYSTEMS, INC.

MGCxxAv
2-Function Comparator

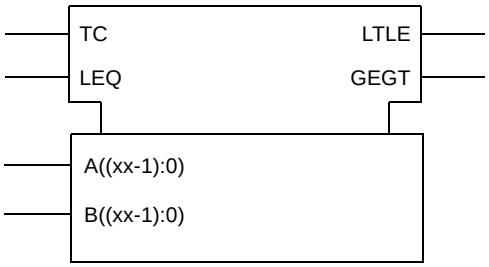
Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Word length for inputs A and B are user definable
- Unsigned and two's complement data comparison
- Two comparison functions available
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGCxxAv



Description

MGCxxAv comparator synthesizer builds xx-bit 2-function comparators. The comparator compares signed or unsigned numbers (A and B) and produces two output conditions (LTLE and GEGT).

The input signal LEQ determines what these two output conditions are (see Functional Description). The input TC determines whether the two inputs are compared as unsigned (TC = 0) or signed (TC = 1).

In the name, "xx" represents the A and B input size and the "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit comparator optimized for minimum delay would be named MGC24A2.

Functional Description

LEQ	Condition	LTLE	GEGT
1	A <= B	1	0
1	A > B	0	1
0	A < B	1	0
0	A => B	0	1

Contact the factory for information on specific speeds and sizes or to have a Comparator built.

MGCxxAv
2-Function Comparator

AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
TC	Input	When 1, signifies A and B inputs are two's complement.	1
LEQ	Input	Determines function of LTLE and GEGT pins.	1
A((xx-1):0)	Input	A Data inputs. A(0) is the LSB.	width > 0
B((xx-1):0)	Input	B Data inputs. B(0) is the LSB.	width > 0
LTLE	Output	'Less than' or 'less than or equal' depending on LEQ.	1
GEGT	Output	'Greater than or equal' or 'greater than' depending on LEQ.	1

Equivalent Gates

CELL NAME	EQ GATES
MGC08A1	39
MGC08A2	92
MGC12A1	53
MGC12A2	100

AMERICAN MICROSYSTEMS, INC.

MGCxxBv
6-Function Comparator

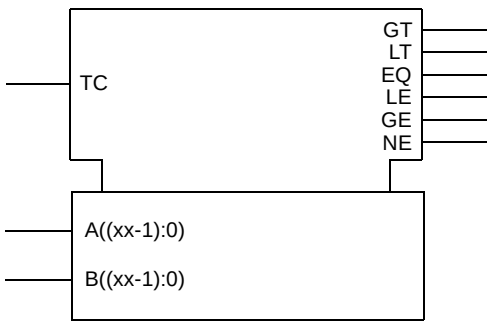
Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Word length for inputs A and B are user definable
- Unsigned and two's complement data comparison
- Six comparison functions available
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGCxxBv



Description

MGCxxBv comparator synthesizer builds xx-bit 6-function comparators. The comparator compares signed or unsigned numbers (A and B) and produces six output conditions (GT, LT, EQ, LE, GE, NE).

The input TC determines whether the two inputs are compared as unsigned (TC=0) or signed (TC=1).

In the name, "xx" represents the A and B input size and the "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit comparator optimized for minimum delay would be named MGC24B2.

Functional Description

Condition	GT	LT	EQ	LE	GE	NE
A > B	1	0	0	0	1	1
A < B	0	1	0	1	0	1
A = B	0	0	1	1	1	0

Contact the factory for information on specific speeds and sizes or to have an 6-function Comparator built.

MGCxxBv
6-Function Comparator

AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
TC	Input	When 1, signifies A and B inputs are two's complement.	1
A((xx-1):0)	Input	A Data inputs. A(0) is the LSB.	width > 0
B((xx-1):0)	Input	B Data inputs. B(0) is the LSB.	width > 0
GT	Output	Asserted when A is greater than B.	1
LT	Output	Asserted when A is less than B.	1
EQ	Output	Asserted when A equals B.	1
LE	Output	Asserted when A is less than or equal to B.	1
GE	Output	Asserted when A is greater than or equal to B.	1
NE	Output	Asserted when A does not equal B.	1

Equivalent Gates

CELL NAME	EQ GATES
MGC08B1	70
MGC08B2	120
MGC12B1	98
MGC12B2	182

AMERICAN MICROSYSTEMS, INC.

MGDxxAv Decrementer

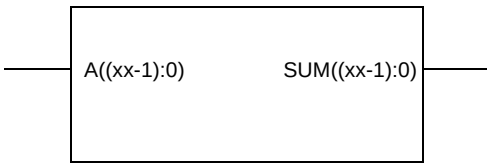
Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Word length for input A is user definable
- Selects multiple architectures for size and speed efficiency
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGDxxAv



Description

MGDxxAv decrementer synthesizer builds xx-bit decrementers. The decrementer subtracts 1 from input A to produce the output SUM.

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead.

The SUM output is the same size as the input A.

In the name, “xx” represents the A input size and the “v” represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit decrementer optimized for minimum delay would be named MGD24A2.

Functional Description

A	SUM
A	A - 1

Contact the factory for information on specific speeds and sizes or to have a Decrementer built.

Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
A((xx-1):0)	Input	A Data inputs. A(0) is the LSB.	width > 0
SUM((xx-1):0)	Output	SUM Data outputs. SUM(0) is the LSB.	width > 0

Equivalent Gates

CELL NAME	EQ GATES
MGD08A1	31
MGD08A2	53
MGD12A1	48
MGD12A2	88

AMERICAN MICROSYSTEMS, INC.

MGIxxAv Incrementer

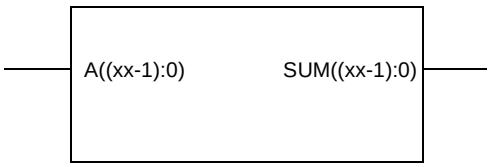
Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Word length for input A is user definable
- Selects multiple architectures for size and speed efficiency
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGIxxAv



Description

MGIxxAv Incrementer synthesizer builds xx-bit Incrementers. The incrementer adds 1 to input A to produce the output SUM.

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead.

In the name, “xx” represents the A and SUM input sizes, and the “v” represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit incrementer optimized for minimum delay would be named MGI24A2.

Functional Description

A	SUM
A	A + 1

Contact the factory for information on specific speeds and sizes or to have an Incrementer built.

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
A((xx-1):0)	Input	A Data inputs. A(0) is the LSB.	width > 0
SUM((xx-1):0)	Output	SUM Data outputs. SUM(0) is the LSB.	width > 0

Equivalent Gates

CELL NAME	EQ GATES
MGI08A1	33
MGI08A2	45
MGI12A1	52
MGI12A2	83

AMERICAN MICROSYSTEMS, INC.

MGIxxBv Incrementer/Decrementer

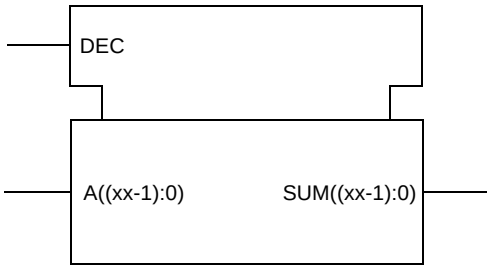
Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Word length for input A is user definable
- Selects multiple architectures for size and speed efficiency
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGIxxBv



Description

MGIxxBv Incrementer/Decrementer synthesizer builds xx-bit Incrementer/Decrementers. When the DEC input is active (DEC=1) the Incrementer/Decrementer subtracts 1 from input A. When DEC is not active (DEC=0) the Incrementer/Decrementer adds 1 to input A.

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead.

In the name, “xx” represents the A and SUM input sizes, and the “v” represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit Incrementer/Decrementer optimized for minimum delay would be named MGI24B2.

Functional Description

A	DEC	SUM
A	0	A + 1
A	1	A - 1

Contact the factory for information on specific speeds and sizes or to have an Incrementer/Decrementer built.

MGIxxBv Incrementer/Decrementer

AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
DEC	Input	Decrement. Megacell decrements when input is high.	1
A((xx-1):0)	Input	A Data inputs. A(0) is the LSB.	width > 0
SUM((xx-1):0)	Output	SUM Data outputs. SUM(0) is the LSB.	width > 0

Equivalent Gates

CELL NAME	EQ GATES
MGI08B1	60
MGI08B2	86
MGI12B1	95
MGI12B2	162

MGMxxyyDv Multiplier

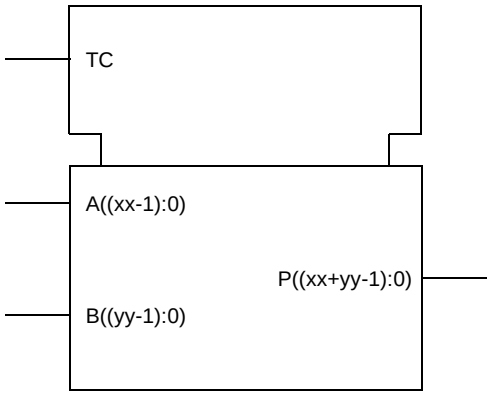
Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Inputs and output sizes are user definable
- Selects multiple architectures for size and speed efficiency
- Two's complement control allows either unsigned or two's complement format
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGMxxyyDv



Description

MGMxxyyDv Multiplier synthesizer builds multipliers of various sizes. The operands A and B are multiplied to produce the product P. The input and output data are interpreted as unsigned when TC=0 or two's complement when TC=1.

The "xxyy" represents a four character sequence assigned to each multiplier configuration where "xx" represents the number of A input bits and "yy" represents the number of B input bits. The number of products bits are equal to "xx" + "yy".

The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 16-bit by 12-bit multiplier optimized for minimum delay would be named MGM1612D2.

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
TC	Input	Determines whether the input and output data are interpreted as unsigned (TC=0) or two's complement (TC=1) numbers.	1
A((xx-1):0)	Input	A input bits. A(0) is the LSB.	width > 0
B((yy-1):0)	Input	B input bits. B(0) is the LSB.	width > 0
P((xx+yy-1):0)	Output	Product bits. P(0) is the LSB.	xx + yy > width > 0

Equivalent Gates

CELL NAME	EQ GATES
MGM0808D1	490
MGM0808D2	696
MGM1212D1	1,060
MGM1212D2	1,357

AMERICAN MICROSYSTEMS, INC.

MGMxxyyEv Multiplier-Accumulator

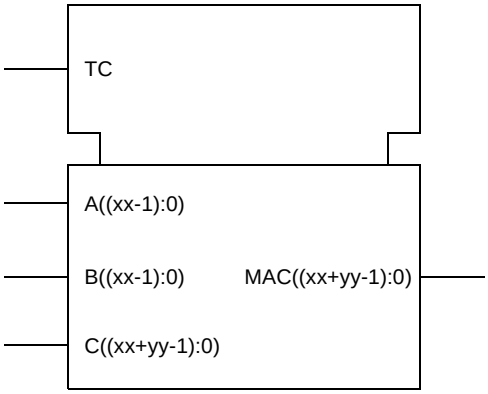
Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Widths for inputs A and B are definable
- Selects multiple architectures for size and speed efficiency
- Two's complement control allows unsigned or two's complement multiplication-accumulation
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGMxxyyEv



Description

MGMxxyyEv multiplier-accumulator synthesizer builds multiplier-accumulators of various sizes. The operands A and B are multiplied and the product is added to C producing the result MAC. The input and output data are interpreted as unsigned when TC=0 or two's complement when TC=1.

The "xxyy" represents a four character sequence assigned to each multiplier-accumulator configuration where "xx" represents the number of A input bits and "yy" represents the number of B input bits. The number of MAC bits are equal to "xx" + "yy".

The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 16-bit by 12-bit multiplier-accumulator optimized for minimum delay would be named MGM1612E2.

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
TC	Input	Determines whether the input and output data are interpreted as unsigned (TC=0) or two's complement (TC=1) numbers.	1
A((xx-1):0)	Input	A input bits. A(0) is the LSB.	width > 0
B((yy-1):0)	Input	B input bits. B(0) is the LSB.	width > 0
C((xx+yy-1):0)	Input	C input bits. C(0) is the LSB.	width = xx + yy
MAC((xx+yy-1):0)	Output	Result bits. MAC(0) is the LSB.	width = xx + yy

Equivalent Gates

CELL NAME	EQ GATES
MGM0808E1	702
MGM0808E2	777
MGM1212E1	1,415
MGM1212E2	1,610

AMERICAN MICROSYSTEMS, INC.

MGSxxyyAv Subtractor

Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Word length for inputs A and B are user definable
- Selects multiple architectures for size and speed efficiency
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGSxxyyAv

Description

MGSxxyyAv subtractor synthesizer builds xx-bit by yy-bit subtractors. Input operands are A and B with an input carry CI to produce the output DIFF with a carry-out CO.

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead.

Inputs A and B and output DIFF can be interpreted to be either in the two's complement or unsigned number format. The DIFF output is the same format as the inputs, and its size is the same as the largest of inputs A or B.

In the name, "xx" represents the A input size and "yy" represents the B input size. The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit by 20-bit subtractor optimized for minimum delay would be named MGS2420A2.

Functional Description

A	B	CI	DIFF	CO
A	B	0	A - B	carry-out
A	B	1	A - B - 1	carry-out

Contact the factory for information on specific speeds and sizes or to have an Subtractor built.

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
CO	Output	Carry out, active high.	1
A((xx-1):0)	Input	A Data inputs. A(0) is the LSB.	width > 0
B((yy-1):0)	Input	B Data inputs. B(0) is the LSB.	width > 0
CI	Input	Carry in, active high.	1
DIFF((ww-1):0)	Output	DIFF Data outputs. DIFF(0) is the LSB.	width > 0

Equivalent Gates

CELL NAME	EQ GATES
MGS0808A1	70
MGS0808A2	163
MGS1212A1	105
MGS1212A2	217

AMERICAN MICROSYSTEMS, INC.

MGFxxyyC1
Latch-based FIFO

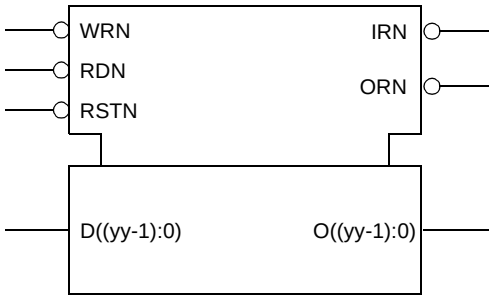
Digital Soft Megacells

Features

- High-performance, schematic-based megacell synthesizer
- Uses latch-array, fall-through architecture
- Array sizes are definable
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGFxxyyC1



Description

MGFxxyyC1 FIFO (First In, First Out) memory synthesizer builds latch based FIFOs of various sizes. FIFOs built with this synthesizer use the fall-through algorithm in which data is written to the top of the register stack and falls through to the bottom of the stack. If the FIFO is not empty the data stops falling through when valid data are encountered. Data fallen through to the bottom of the stack are available at the outputs.

These FIFOs have separate asynchronous read and write clocks. Flags include ORN (output ready not) which determines if the FIFO is empty and IRN (input ready not) which determines if the FIFO is full. Indeterminable results may occur during writes when IRN is active.

The “xxyy” in the name represents a four character sequence assigned to each FIFO configuration where “xx” represents the number of words and “yy” represents the number of bits per word. For example, a 32-word by 8-bit FIFO would be named MGF3208C1.

Contact the factory for information on specific speeds and sizes or to have a FIFO built.

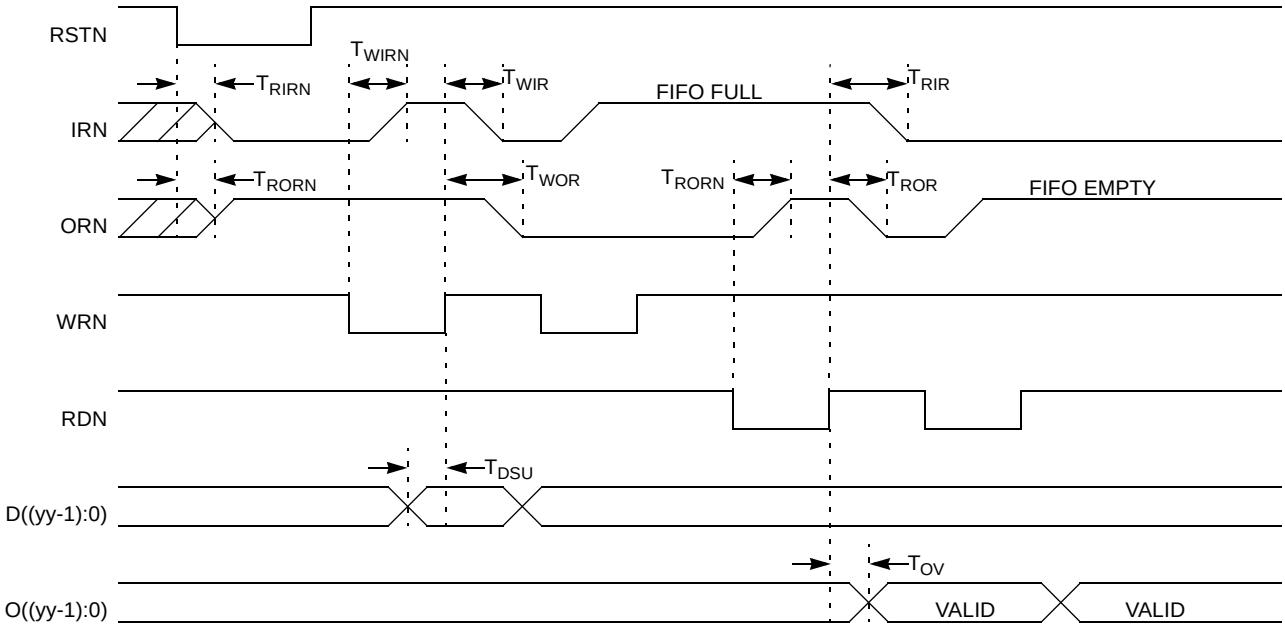
Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
WRN	Input	Write clock. Data is latched when WRN transitions from low to high.
RDN	Input	Read clock. On the low to high transition of RDN data on the bottom of the FIFO is replaced with data from immediately above.
RSTN	Input	Reset signal. Sets FIFO to empty.
D((yy-1):0)	Input	Data inputs. Data appearing on these inputs are written into the FIFO on the low to high transition of WRN. D(0) is the LSB.
IRN	Output	Input Ready Not. A low on this signal indicates the FIFO is either full or busy. Writing when IRN is low will cause data to be lost.
ORN	Output	Output Ready Not. A low on this signal indicates that data appearing on the outputs are valid.
O((yy-1):0)	Output	Data outputs. The data stored on the bottom of the stack are constantly available through these signals and are updated on the rising edge of RDN.

Equivalent Gates

CELL NAME	EQ GATES
MGF0232C1	260
MGF0809C1	290
MGF1616C1	843
MGF1632C1	1,542

Read / Write Timing



Timing Characteristics

SYMBOL	CHARACTERISTIC	REFERENCED TO
T_{RIRN}	reset to input ready set	RSTN falling
T_{RORN}	reset to output ready clear	RSTN falling
T_{WIRN}	write to input ready clear	WRN falling
T_{WOR}	write to output ready set	WRN rising
T_{WIR}	write to input ready set	WRN rising
T_{RIR}	read to input ready set	RDN rising
T_{RORN}	read to output ready clear	RDN falling
T_{ROR}	read to output ready set	RDN rising
T_{DSU}	data setup to write	WRN rising
T_{OV}	read to output valid	RDN rising

MGFxxxxyyD Synchronous FIFO

AMERICAN MICROSYSTEMS, INC.

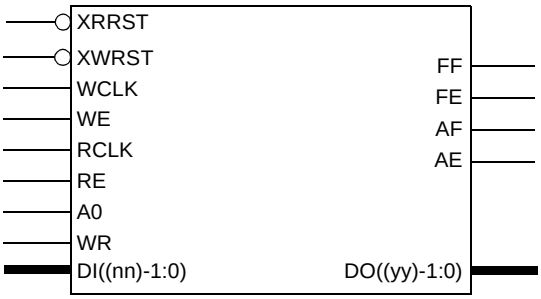
Digital Soft Megacells

Features

- Dual-port RAM architecture for zero fall-through time
- Dynamically programmable almost-full and almost-empty flags.
- Synchronous design
- Word width and depth are user definable
- High-performance, Schematic-based megacell

LOGIC SYMBOL

MGFxxxxyyD



Description

MGFxxxxyyD FIFO (First In, First Out) builds synchronous FIFOs of various sizes. These FIFOs use a Dual-Port Synchronous Static RAM to allow large FIFO depth without any fall-through time.

The “xxxx” in the name represents the number of words in the FIFO, and must be a power of 2 between five and ten (i.e. 32 minimum to 1024 maximum). The “yy” is the number of bits per word and can be from one to any size needed. For example, a 128 word by 16 bit FIFO would be named MGF012816D.

Clock inputs WCLK and RCLK are free-running. Data is written into the FIFO on the falling edge of WCLK when WE is high. WE should only transition when WCLK is low. Data is read on the rising edge of RCLK when RE is high. The output data must be captured by external logic before the next rising edge of RCLK.

Inputs A0 and WR are used to write to the registers which control the AE (almost empty) and AF (almost full) flags. When A0 is low, data on the DI bus is written into the AE register on the rising edge of WR. When A0 is high data is written into the AF register. On reset the AE register defaults to 25% of “xxxx” and AF to 75% of “xxxx”.

The width of the data input (DI) bus is equal to the greater of, the number of bits per word or log2 (number of words in FIFO).

Flags include FE, (FIFO empty) FF, (FIFO full) and the dynamically programmable AE (almost empty) and AF (almost full) flags.

The MGFxxxxyyD features a split reset line to allow implementation of a retransmit function. XRRST and XWRST are synchronous active low resets for the read counter and write counter respectively. Each reset must be held active for at least one rising edge of its respective clock to initialize the FIFO.

To implement a retransmit function the total number of writes since the last general reset must be LESS THAN the number of words in the FIFO. As long as this condition is met the read counter may be reset and all the words written since the general reset may be reread. Notice that if the AE register has been programed to a different value, the read reset will return it to the default.

Contact the factory for information on specific speeds and sizes or to have a FIFO built.

Pin Description

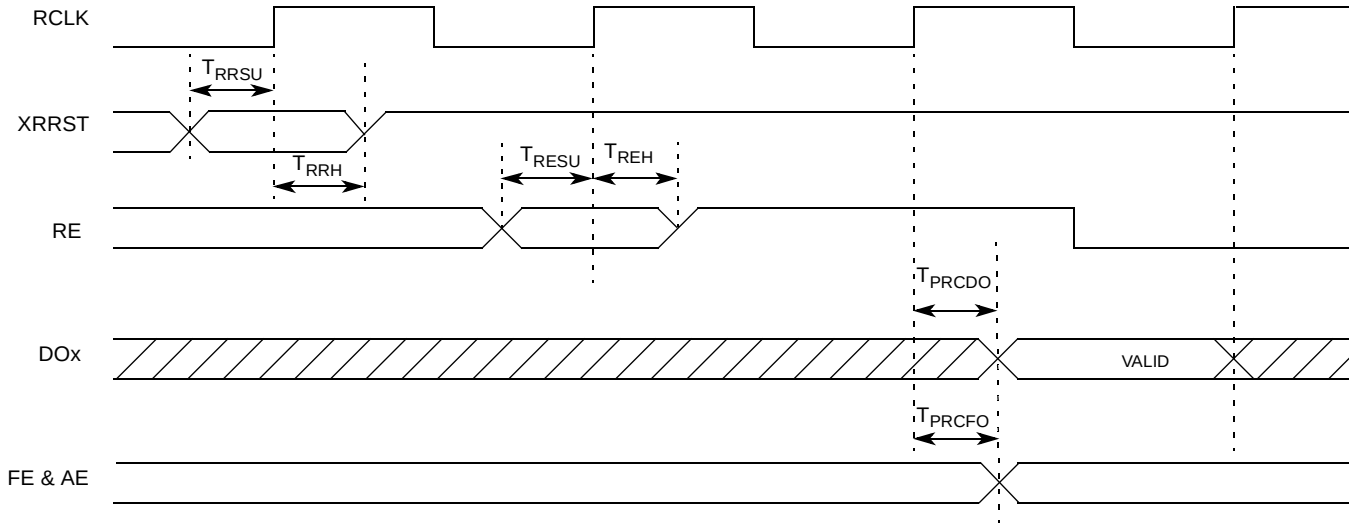
SIGNAL	TYPE	SIGNAL DESCRIPTIONS
XWRST	I	Synchronous write reset. Resets the write portion of the FIFO. Must be held low during a rising edge of WCLK.
WCLK	I	Free-running write clock.
WE	I	Write enable. Data appearing on DIn will be written into the FIFO on the falling edge of WCLK when WE is high. WE should transition only when WCLK is low.
XRRST	I	Synchronous read reset. Resets the read portion of the FIFO. Must be held low during a rising edge of RCLK.
RCLK	I	Free-running read clock.
RE	I	Read enable. Data is read from the FIFO on the rising edge of RCLK when RE is high.
A0	I	Address for determining if the AE or AF flag register is to be written. When A0 = 1 the AF flag register is written.
WR	I	Write control for AE and AF registers. Data appearing on DIn is written into either the AE or AF register on the rising edge of WR.
DI((nn)-1:0)	I	Data into the FIFO and the AE/AF registers.
DO((yy)-1:0)	O	Data out of the FIFO.
FF	O	FIFO full flag, active high. Synchronized to WCLK.
AF	O	FIFO almost full flag, active high. Synchronized to WCLK.
FE	O	FIFO empty flag, active high. Synchronized to RCLK.
AE	O	FIFO almost empty flag, active high. Synchronized to RCLK.

Equivalent Gates[1]

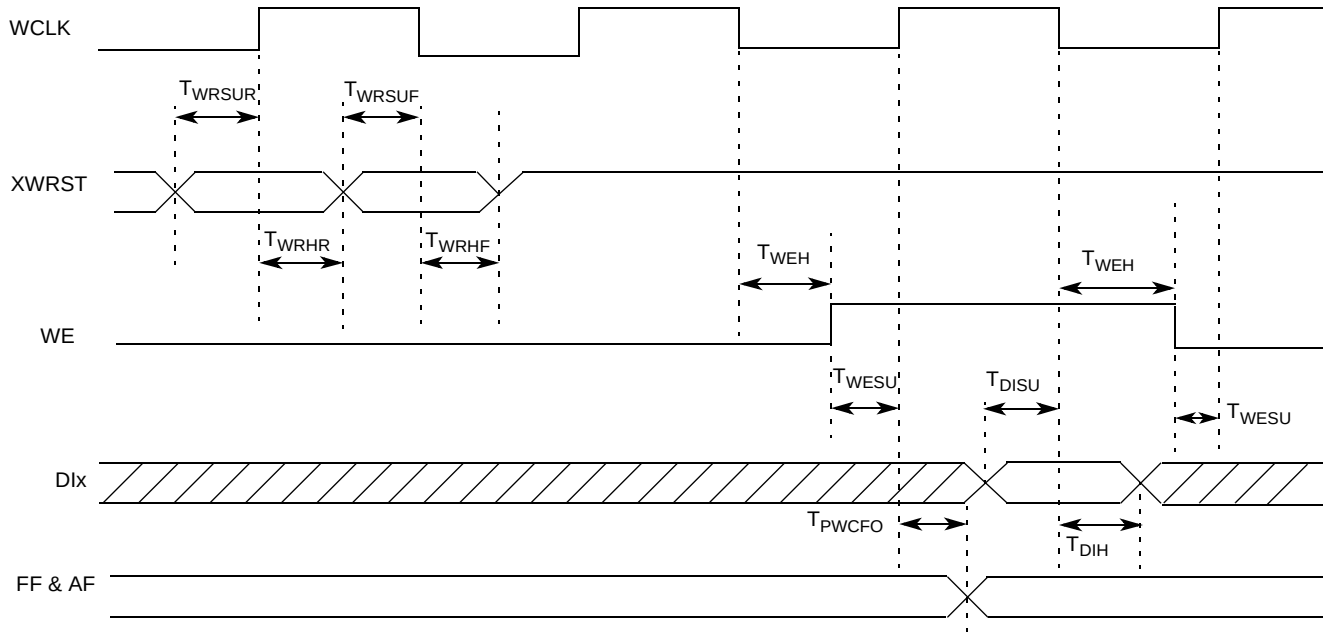
Cell Name	EQ GATEST
MGF0032yyD	470
MGF0064yyD	540
MGF0128yyD	640
MGF0256yyD	740
MGF0512yyD	840
MGF1024yyD	940

Note: 1. Does not include RAM.

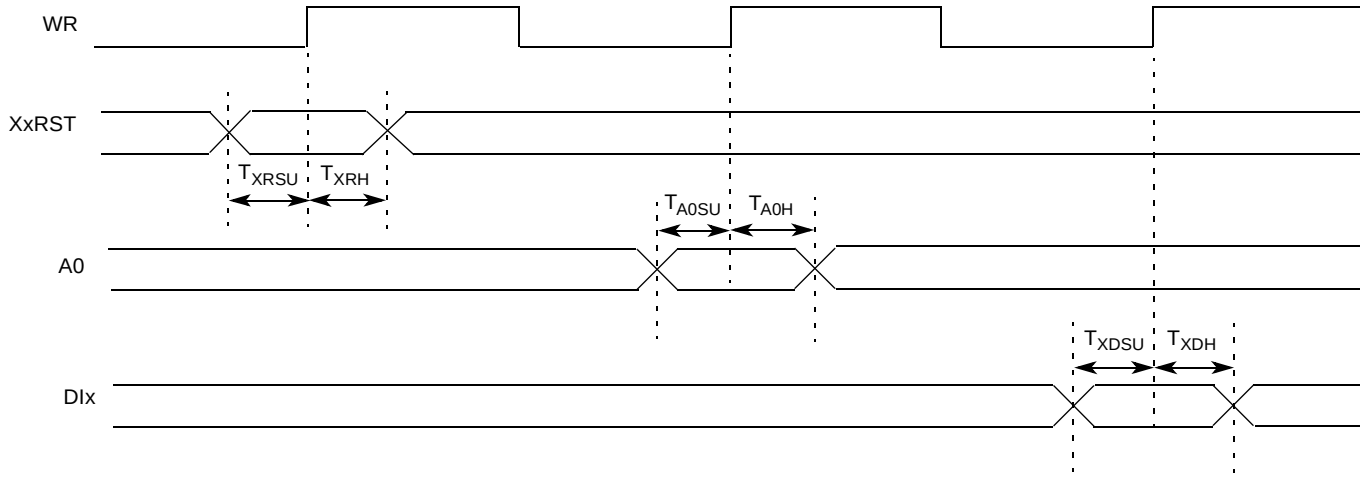
Read Timing



Write Timing



Register Write Timing



Timing Characteristics

Symbol	Characteristic	Referenced to
T_{RRSU}	read reset setup	RCLK rising
T_{RRH}	read reset hold	RCLK rising
T_{RESU}	read enable setup	RCLK rising
T_{REH}	read enable hold	RCLK rising
T_{PRCDO}	read clock to data out valid	RCLK rising
T_{PRCFO}	read clock to flag out valid	RCLK rising
T_{WRSUR}	write reset setup	WCLK rising
T_{WRHR}	write reset hold	WCLK rising
T_{WRSUF}	write reset setup	WCLK falling
T_{WRHF}	write reset hold	WCLK falling
T_{WESU}	write enable setup	WCLK rising
T_{WEH}	write enable hold	WCLK falling
T_{DISU}	data in setup	WCLK falling
T_{DIH}	data in hold	WCLK falling
T_{PWCFO}	write clock to flag out valid	WCLK rising
T_{XRSU}	either reset setup	WR rising
T_{XRH}	either reset hold	WR rising
T_{A0SU}	A0 setup	WR rising
T_{A0H}	A0 hold	WR rising
T_{XDSU}	data in setup	WR rising
T_{XDH}	data in hold	WR rising

MGFxxxxyyE
Asynchronous FIFO

AMERICAN MICROSYSTEMS, INC.

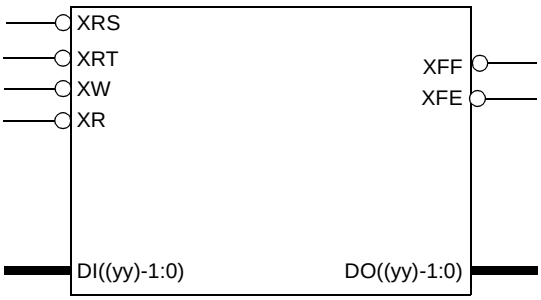
Digital Soft Megacells

Features

- Dual-port RAM architecture for zero fall-through time
- Asynchronous design
- Word width and depth are user definable
- High-performance, Schematic-based megacell

LOGIC SYMBOL

MGFxxxxyyE



Description

MGFxxxxyyE FIFO (First In, First Out) builds asynchronous FIFOs of various sizes. These FIFOs use a Dual-Port Synchronous Static RAM to allow large FIFO depth without any fall-through time.

The “xxxx” in the name represents the number of words in the FIFO, and must be a power of 2 between five and ten (i.e. 32 minimum to 1024 maximum). The “yy” is the number of bits per word and can be from one to any size needed. For example, a 128 word by 16 bit FIFO would be named MGF012816E.

Data is written into the FIFO on the rising edge of XW, and read on the falling edge of XR. Flags are updated on the rising edge of XW and XR. Flags include XFE, (FIFO empty not) and XFF (FIFO full not).

The MGFxxxxyyE has a general reset, XRS pin, and a retransmit function enabled by the XRT pin. Both pins are active low.

To use the retransmit function the total number of writes since the last general reset MUST NOT EXCEED the number of words in the FIFO.

As long as this condition is met, pulling XRT low will reset the read counter and all the words written since the general reset may be read.

Contact the factory for information on specific speeds and sizes or to have a FIFO built.

Pin Description

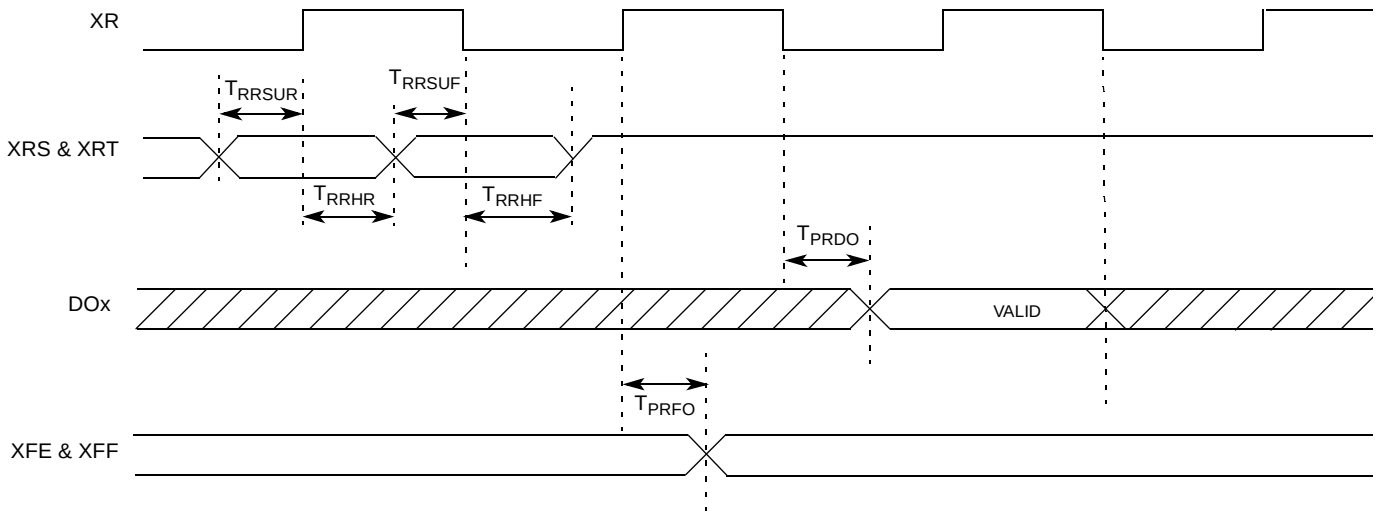
SIGNAL	TYPE	SIGNAL DESCRIPTIONS
XRS	I	Asynchronous reset. Resets FIFO when pulsed low.
XRT	I	Activates retransmit function when pulsed low.
XW	I	Active low write signal. Data appearing on DIn will be written into the FIFO on the rising edge of XW.
XR	I	Active low read signal. Data is read from the FIFO on the falling edge of XR.
DI((yy)-1:0)	I	Data input into the FIFO.
DO((yy)-1:0)	O	Data output from the FIFO.
XFF	O	FIFO full flag, active low.
XFE	O	FIFO empty flag, active low.

Equivalent Gates[1]

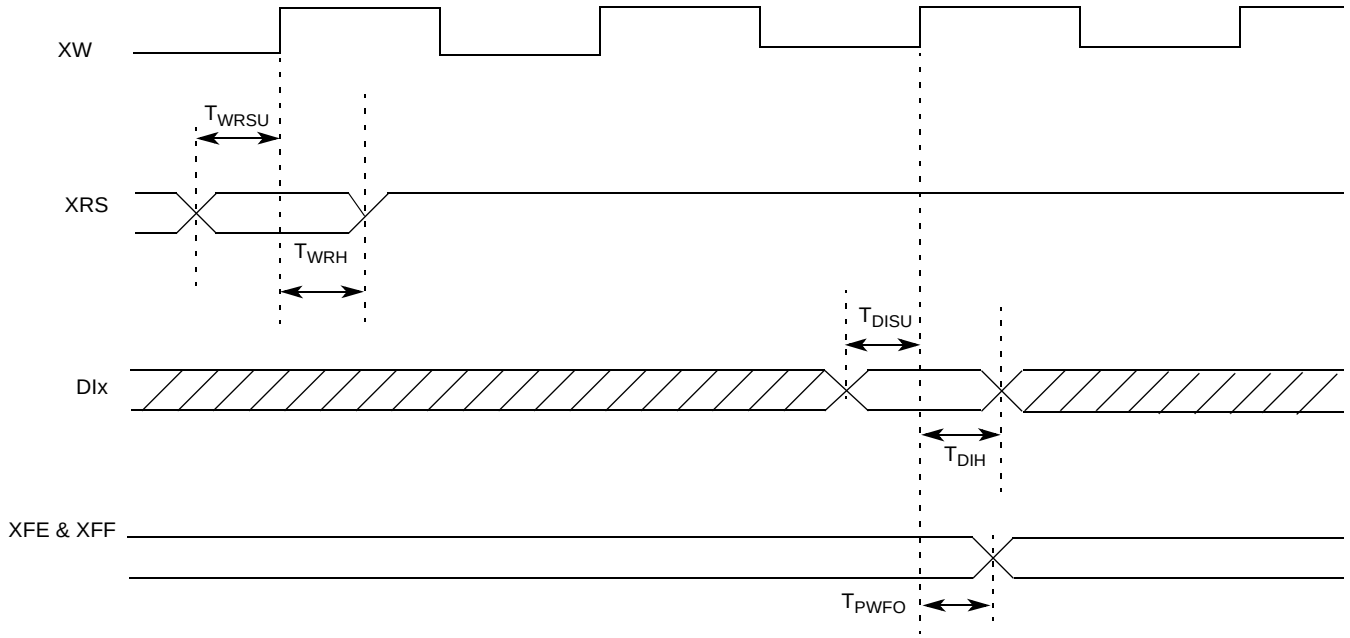
Cell Name	EQ GATES
MGF0032yyE	300
MGF0064yyE	360
MGF0128yyE	430
MGF0256yyE	495
MGF0512yyE	560
MGF1024yyE	630

NOTE: 1. Does not include RAM.

Read Timing



Write Timing



Timing Characteristics

Symbol	Characteristic	Referenced to
T_{RRSUR}	read reset setup	XR rising
T_{RRH}	read reset hold	XR rising
T_{RRSUF}	read reset setup	XR falling
T_{RRHF}	read reset hold	XR falling
T_{PRDO}	read clock to data out valid	XR falling
T_{PRFO}	read clock to flag out valid	XR rising
T_{WRSU}	write reset setup	XW rising
T_{WRH}	write reset hold	XW rising
T_{DISU}	data in setup	XW rising
T_{DIH}	data in hold	XW rising
T_{PWFO}	write clock to flag out valid	XW rising

SECTION 6
MEMORIES

AMERICAN MICROSYSTEMS, INC.

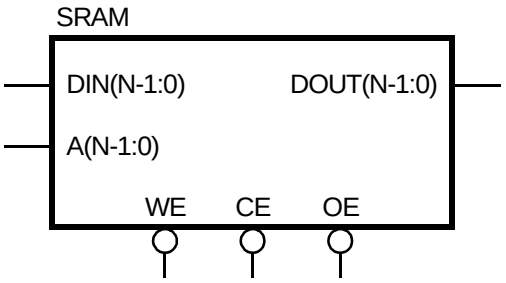
SRAM
High Speed Low-Power Single Port

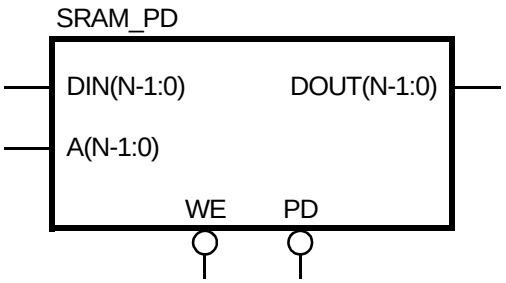
CMOS ASIC Standard Cell Memories

Features

- 6-T memory cell design
- Simple combinational logic decoding
- Small bitline differential in read mode eliminates precharge delay
- Fast ATD circuit turns on wordlines and sense amps only as needed to save power while allowing asynchronous operation

Logic Symbol





SRAM: High Speed Low-Power Single Port Description

AMI's high speed, low power CMOS RAM is available in both single and dual port versions. Column select passgates provide a cascode gain stage, followed by a differential voltage sense amp. The memory array columns may be multiplexed to optimize the aspect ratio. Multiplexing of columns, or column folding, shortens the bitline length (reduces the number of rows in the array) while increasing the width of the memory array. No change in the total memory bit count occurs.

The zero_out option sets all outputs to to 'zero'. This operation is controlled by the PD signal.

The RAM draws current only in response to changing inputs, minimizing power consumption and allowing complete IDDQ testing. In addition to normal CMOS transient current, address changes activate the sense amps and one row of memory cells for a period of time longer than access time. The current drawn by each sense amp is comparable to the read current of each memory cell.þ

SRAM
High Speed Low-Power Single Port

AMERICAN MICROSYSTEMS, INC.

CMOS ASIC Standard Cell Memories

Signal Summary

INPUTS		OUTPUTS	
PORT LABEL	**FUNCTION**	**PORT LABEL**	**FUNCTION**
A	Address	DOUT	Output Data
DIN	Input Data		
CE	Chip Enable, avtive low		
WE	Write Enable, active low		
OE	Output Enable, active low, tristated output control		
PD	Power Down, active high, read and write cycles disabled and output driven to zero (0) when active		

Parameters

NAME	DEFINITION	DATA TYPE	VALUES
N	bits per word	Integer	1 -144
WORDS	number of words	Integer	8 -16384
M	address size	Integer	3 - 14
BPC	bits per column	Integer	2, 4, 8, 16, 32
FLOORPLAN	auto floorplan	Integer	0, 1
BUFFER_SIZE	buffer size	String	1-6
FREQUENCY	frequency in MHz	Integer	1-100
VDROP	voltage drop in millivolts	Integer	1-249

Block height range is 4-512; block width range is 4-288; max total bits is 144K (16K x 9).

Bits Per Column (BPC) Options

BPC VALUE	MINIMUM WORDS	MAXIMUM WORDS	ADDRESS INCREMENT	MINIMUM BITS	MAXIMUM BITS
2	8	1024	4	1	144
4	16	2048	8	1	72
8	32	4096	16	1	36
16	64	8192	32	1	18
32	128	16384	64	1	9

Parts

PART NAME	PINS
sram	A, CE, DIN, OE, WE, DOUT
sram_pd	A, DIN, PD, WE, DOUT

Truth Table

zero-out option false

INPUTS					OUTPUTS	COMMENT
A	CE	OE	DIN	WE	DOUT	
0/1	0	0	X	1	Data	Read
X	0	1	X	1	Z	Output Disabled (standard) - RAM Active
X	1	1	X	X	Z	Output Disabled (standard) - RAM Disabled
X	1	0	X	X	Data	Output Stable, RAM disabled
0/1	0	0	0/1	0	Data	Write with Write-Through
0/1	0	1	0/1	0	Z	Write

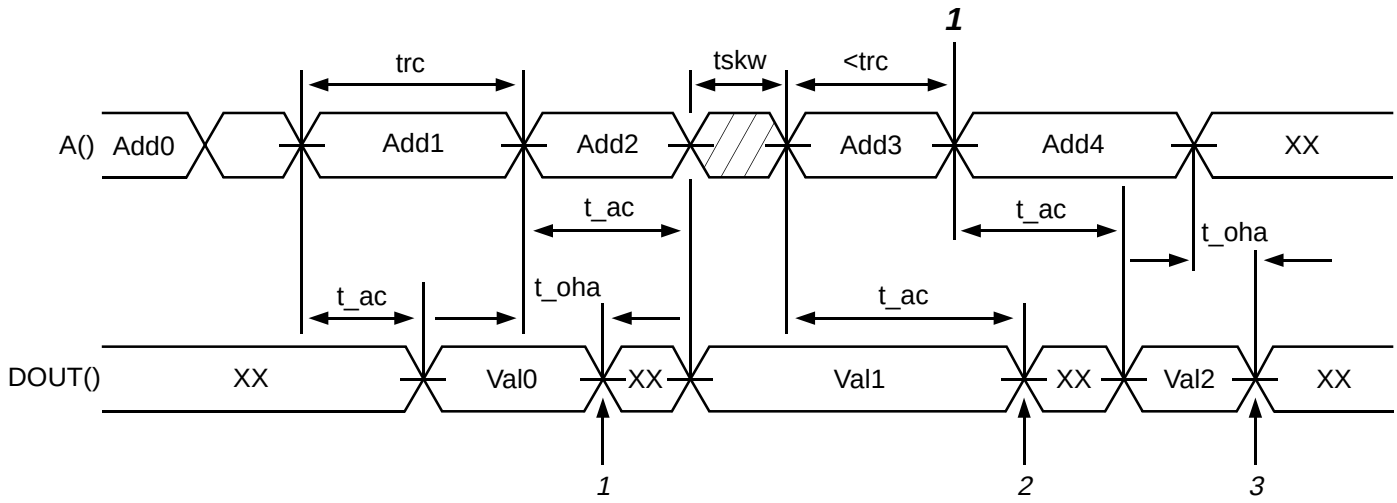
zero-out option true

INPUTS				OUTPUTS	COMMENT
A	PD	DIN	WE	DOUT	
X	1	X	X	0	Output Disabled (zero_out), RAM disabled
0/1	0	X	1	Data	Read
0/1	0	0/1	0	Data	Write with Write-Through

SWITCHING TIME WAVEFORMS

Single Port RAM Read Cycle 1

sram :CE = '0', OE = '0', WE = '1'
sram_pd:PD='0', WE='1'



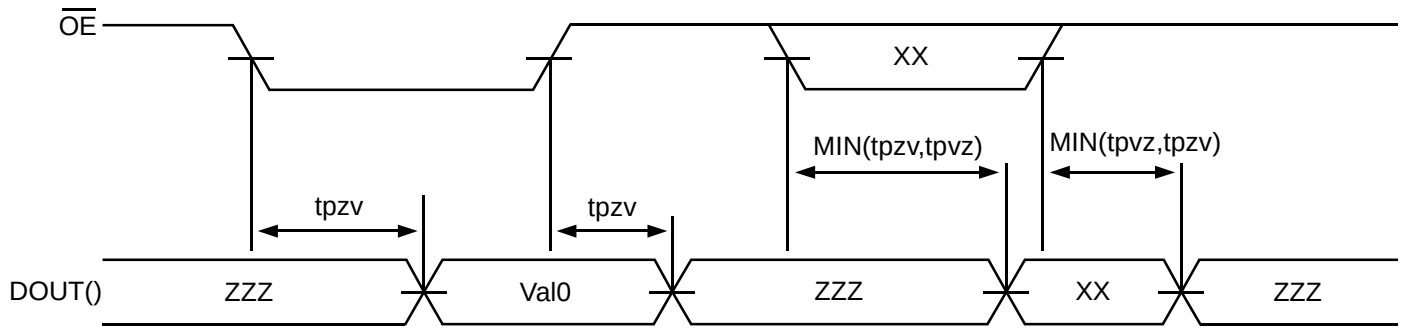
Notes: t_ac : Address Access Time (maximum of Rise/Fall)
trc : Read Cycle Time
t_oha : Output Hold Time from Address Change (minimum of Rise/Fall)
tskw : All addresses must complete transition within this time

1. t_oha delay will only be applied to the last data accessed, otherwise, t_ac will be used for the pin-to-pin delay.
2. trc <= t_ac. If Add3 width is less than trc, DOUT() goes to 'X'.
3. If A() becomes 'X', DOUT() goes 'X' after time t_oha.

***1**. Error: Illegal Address input: Address cycle time is smaller than minimum trc.*

Single Port RAM Read Cycle 2

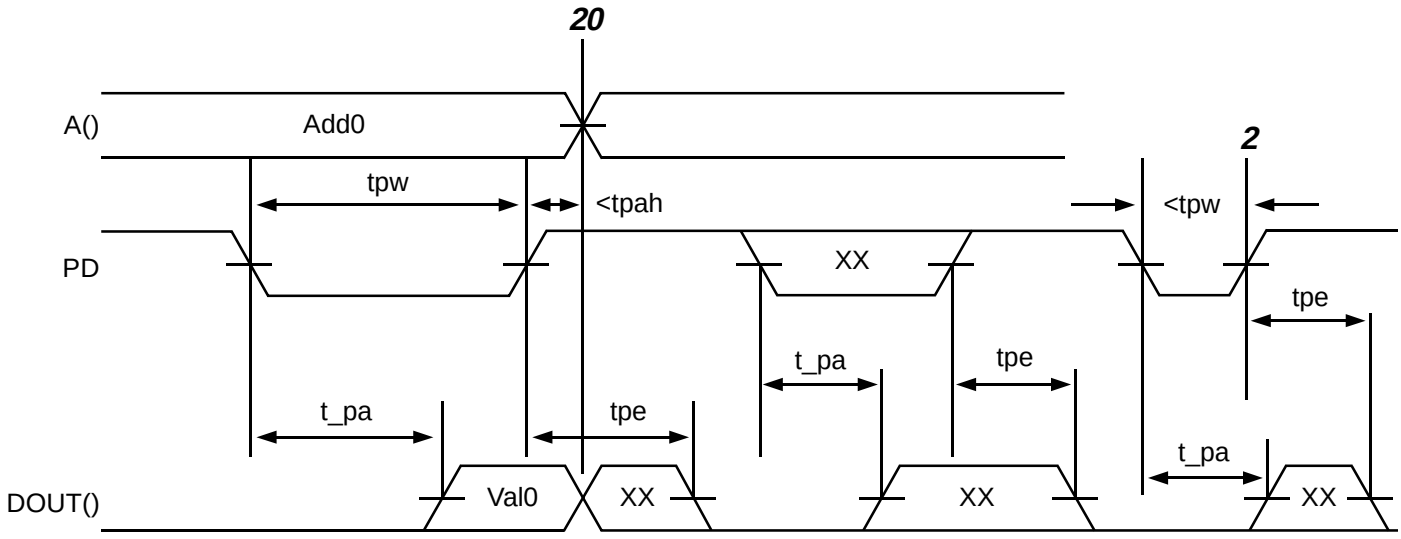
sram: CE = '0', WE = '1'



Notes: tpvz : Delay to propagate valid DOUT() to high impedance
tpzv : Delay to propagate high impedance to valid DOUT()

Single Port RAM Read Cycle 3

sram_pd: WE = '1'

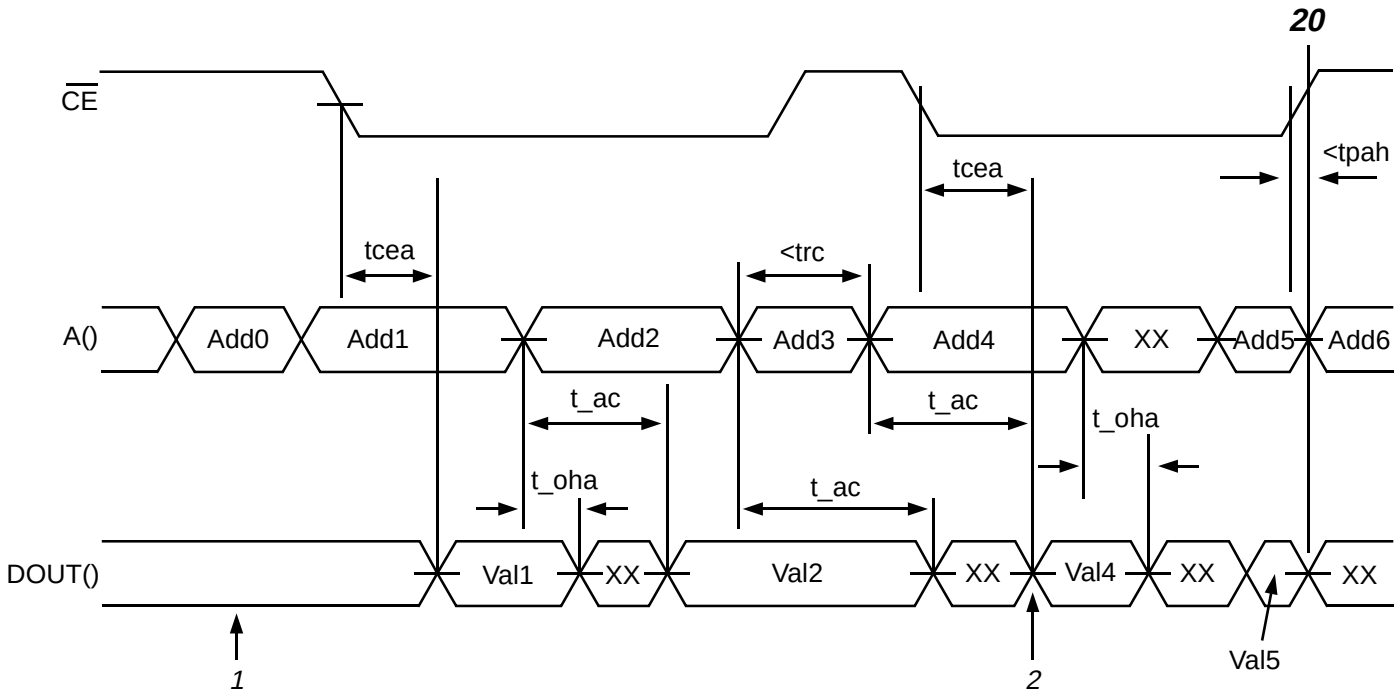


Notes: t_pa : Access time from PD
tpe : PD shutting off to DOUT() Fall
tpw : Minimum pulse width for PD
tpah : Address hold time from PD rising

***2**. Error: Illegal PD input: PD "Low" width time smaller than min. tpw.*
***20**. Error: Illegal address input: hold time to PD is smaller than min. tpah.*

Single Port RAM Read Cycle 4

sram: OE = '0', WE = '1'



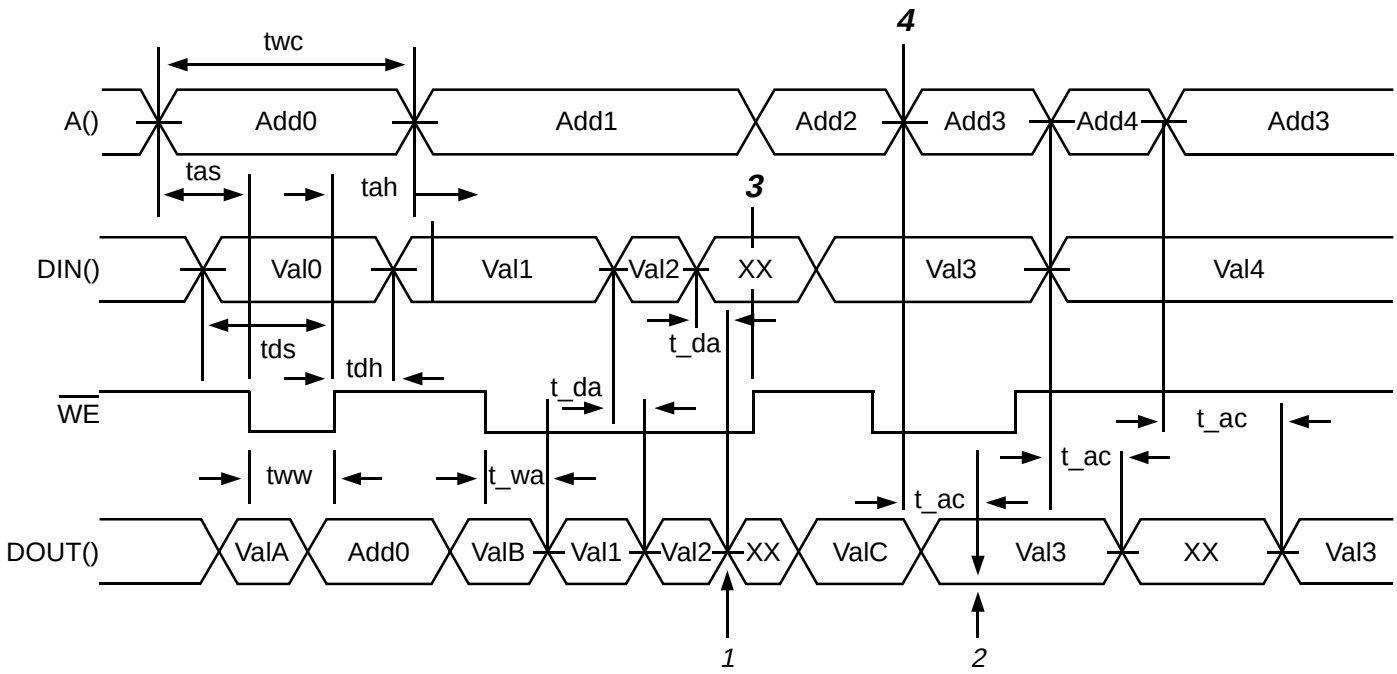
Notes: t_ac : Address access time
tcea : CE Access Time (maximum of Rise/Fall)
tpah : Address hold time from PD or CE rising
trc : Min. ready cycle time
t_oha : Output hold time from address change (minimum of Rise/Fall)

1. Normal DOUT() change due to address change is locked out by 'CE' pin set to '1'.
2. Output becomes valid after the MAX of t_ac or tcea. Note that the 'CE' pin rising does not trigger a RAM access.

***20**. Error: Illegal address input: hold time to CE/PD is smaller than min. tpah.*

Single Port RAM Write Cycle 1

sram : CE = '0', OE = '0'
sram_pd : PD = '0'



Notes:
- t_da : Output delay time from Data (t_da < t_ac) (MAX of Rise/Fall)
- t_wa : Output delay time from WE (MAX of Rise/Fall)
- t_ac : Address access time
- tas : Address setup time
- tah : Address hold time
- tds : Data setup time
- tdh : Data hold time
- tww : Write pulse width low
- twc : Write cycle time

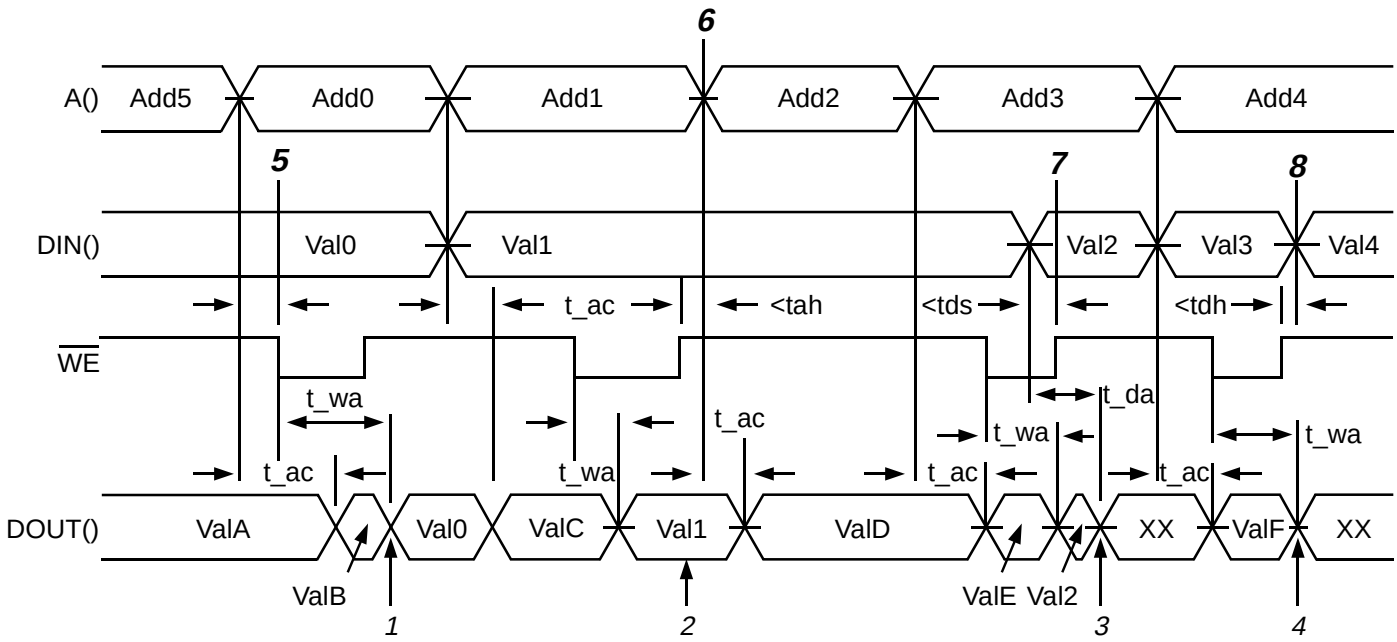
ValA, ValB, and ValC are previously retained in address Add0, Add1, and Add2

1. Data retained in Add1 is overwritten by 'X' at this time.
2. Data retained in all words is overwritten by 'X' at this time. Writing Val3 into Add3 should be successful.

***3**. Error: Illegal Operation: Data "X" is written at rising edge of WE*
***4**. Error: Illegal Operation: Address was changed while WE low*

Single Port RAM Write Cycle 2

sram : CE = '0', OE = '0'
sram_pd : PD = '0'



Notes:
- t_da : Output delay time from Data (t_da < t_ac) (MAX of Rise/Fall)
- t_wa : Output delay time from $\overline{WE}$ (MAX of Rise/Fall)
- t_ac : Address access time
- tah : Address hold time
- tds : Data setup time
- tdh : Data hold time
- tas : Address setup time

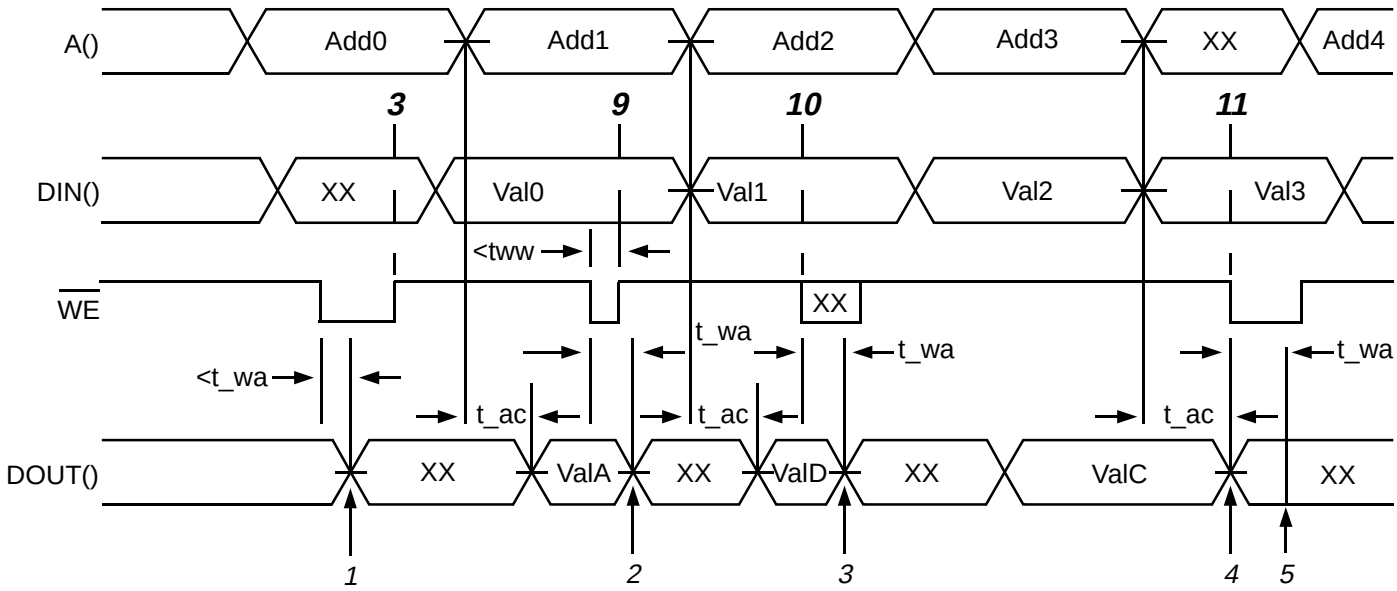
ValA-ValF are previously retained in Add5-Add4.

1. Data retained in all words is overwritten by 'X' at this time. Writing Val0 into Add0 should be successful.
2. Data retained by all words is overwritten by 'X' at this time.
3. Data retained in Add3 is overwritten by 'X' at this time.
4. Data retained in Add4 is overwritten by 'X' at this time.

***5**. Error: Illegal Address Input: Address setup time to $\overline{WE}$ is smaller than Min tas.*
***6**. Error: Illegal Address Input: Address hold time to $\overline{WE}$ is smaller than Min tah.*
***7**. Error: Illegal Data Input: DIN setup time to $\overline{WE}$ is smaller than Min tds.*
***8**. Error: Illegal Data Input: DIN hold time to $\overline{WE}$ is smaller than Min tdh.*

Single Port RAM Write Cycle 3

sram : CE = '0', OE = '0'
sram_pd : PD = '0'

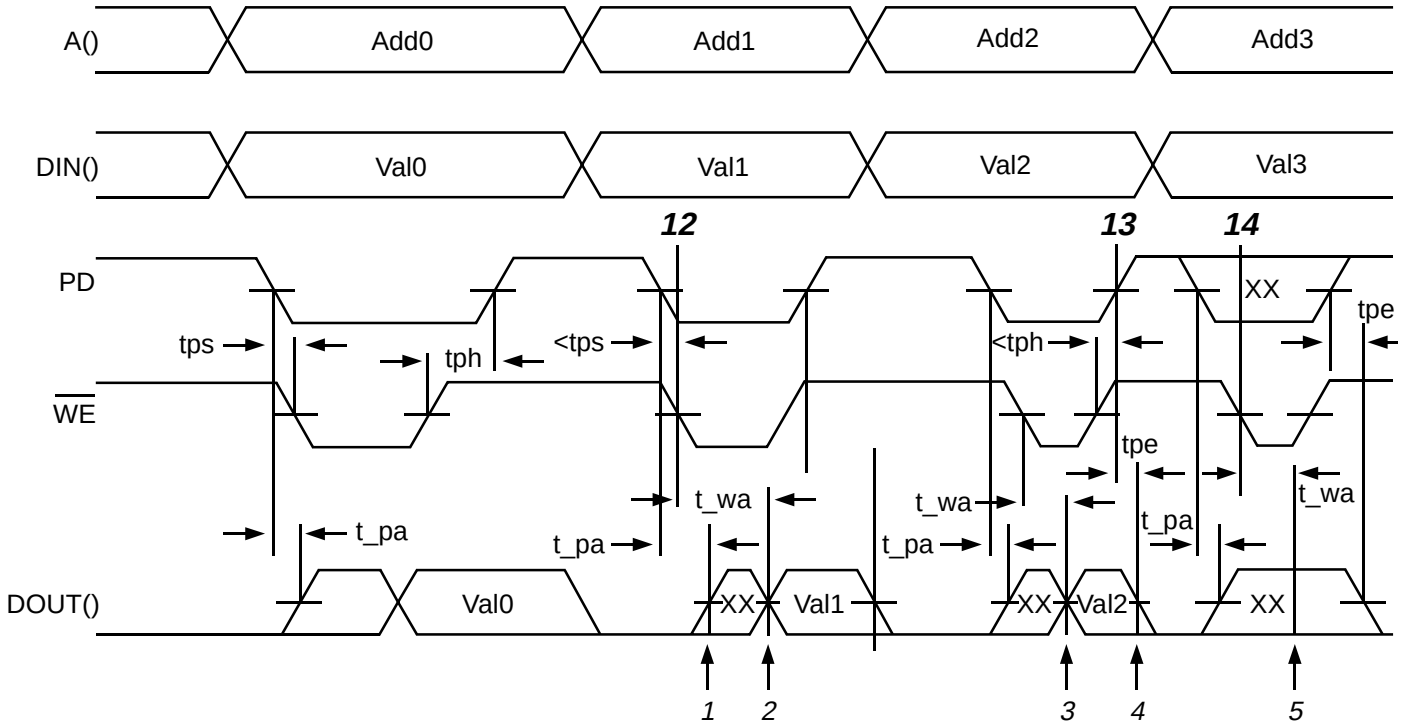


Notes: t_wa : Ouput delay time from $\overline{WE}$ (MAX of Rise/Fall)
t_ac : Address access time
tww : Write pulse width low

1. Data retained in Add0 is overwritten by 'X' at this time.
2. Data retained in Add1 is overwritten by 'X' at this time.
3. Data retained in Add2 is overwritten by 'X' at this time.
4. DOUT() becomes 'X' after t_ac time from leading edge of address 'X'.
5. Data retained in all words is overwritten by 'X' after t_wa time from falling edge of $\overline{WE}$.

***3**. Error: Illegal Operation: Data "X" is written at rising edge of $\overline{WE}$.*
***9**. Error: Illegal $\overline{WE}$ Input: $\overline{WE}$ "Low" width time is smaller than Min tww.*
***10**. Error: Illegal Operation: $\overline{WE}$ input went to "X".*
***11**. Error: Illegal Operation: Address was "X" at the falling edge of $\overline{WE}$.*

Single Port RAM Write Cycle 4 (sram_pd)



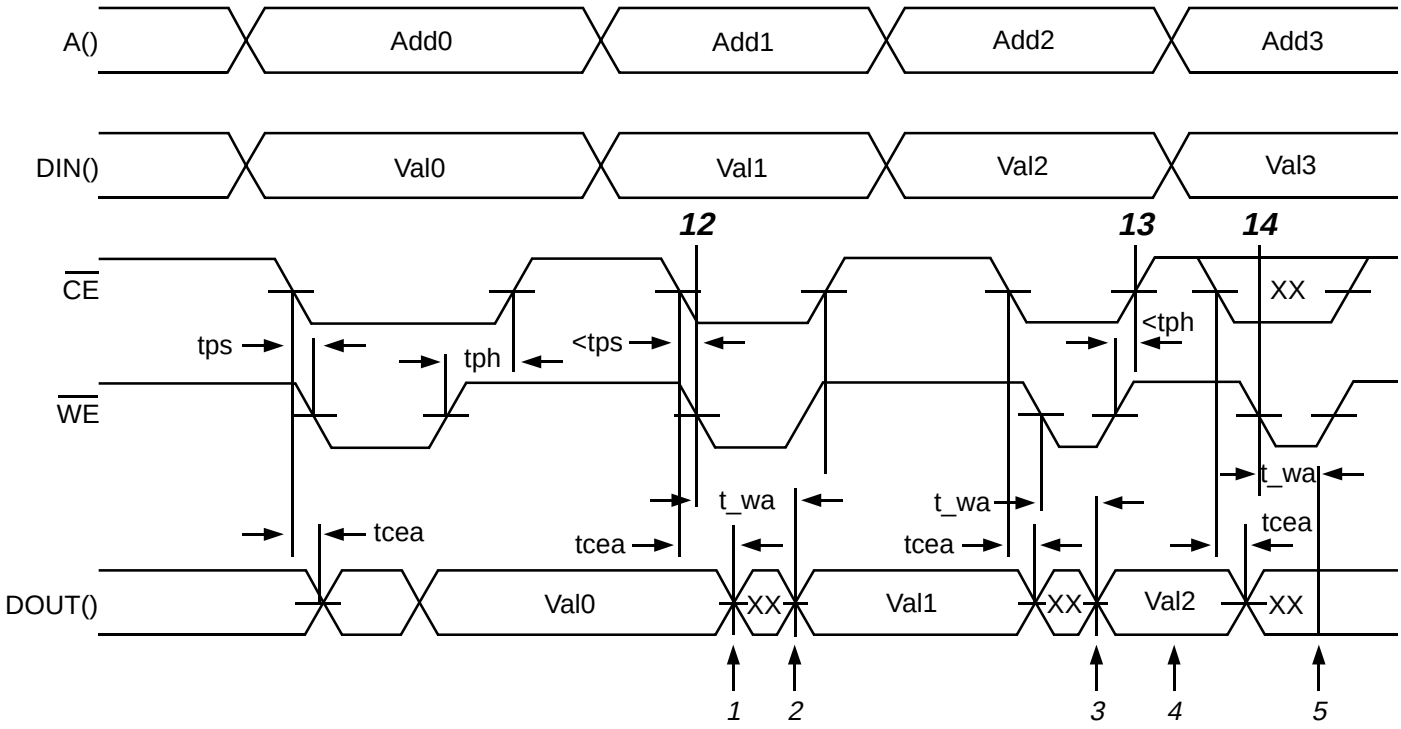
Notes: tps : $\overline{CE}$/PD setup time (PD pin used for zero_out function)
tph : $\overline{CE}$/PD hold time (PD pin used for zero_out function)
t_wa : Output delay time from $\overline{WE}$ (MAX of Rise/Fall)
t_pa : Access time from $\overline{CE}$/PD
tpe : $\overline{CE}$/PD shutting off to DOUT() Fall

1. 4. Data retained in all words is overwritten by 'X' at this time.
2. "X" retained in Add1 is overwritten by Val1 at this time.
3. "X" retained in Add2 is overwritten by Val2 at this time.
5. If Data retained in Add3 is not equal to Val3, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***12**. Error: Illegal $\overline{CE}$/PD Input: $\overline{CE}$/PD setup time to $\overline{WE}$ is smaller than Min tps.*
***13**. Error: Illegal $\overline{CE}$/PD Input: $\overline{CE}$/PD hold time to $\overline{WE}$ is smaller than Min tph.*
***14**. Error: Illegal Operation: $\overline{CE}$/PD was "X" at the falling edge of $\overline{WE}$.*

Single Port RAM Write Cycle 5

sram: OE = '0'

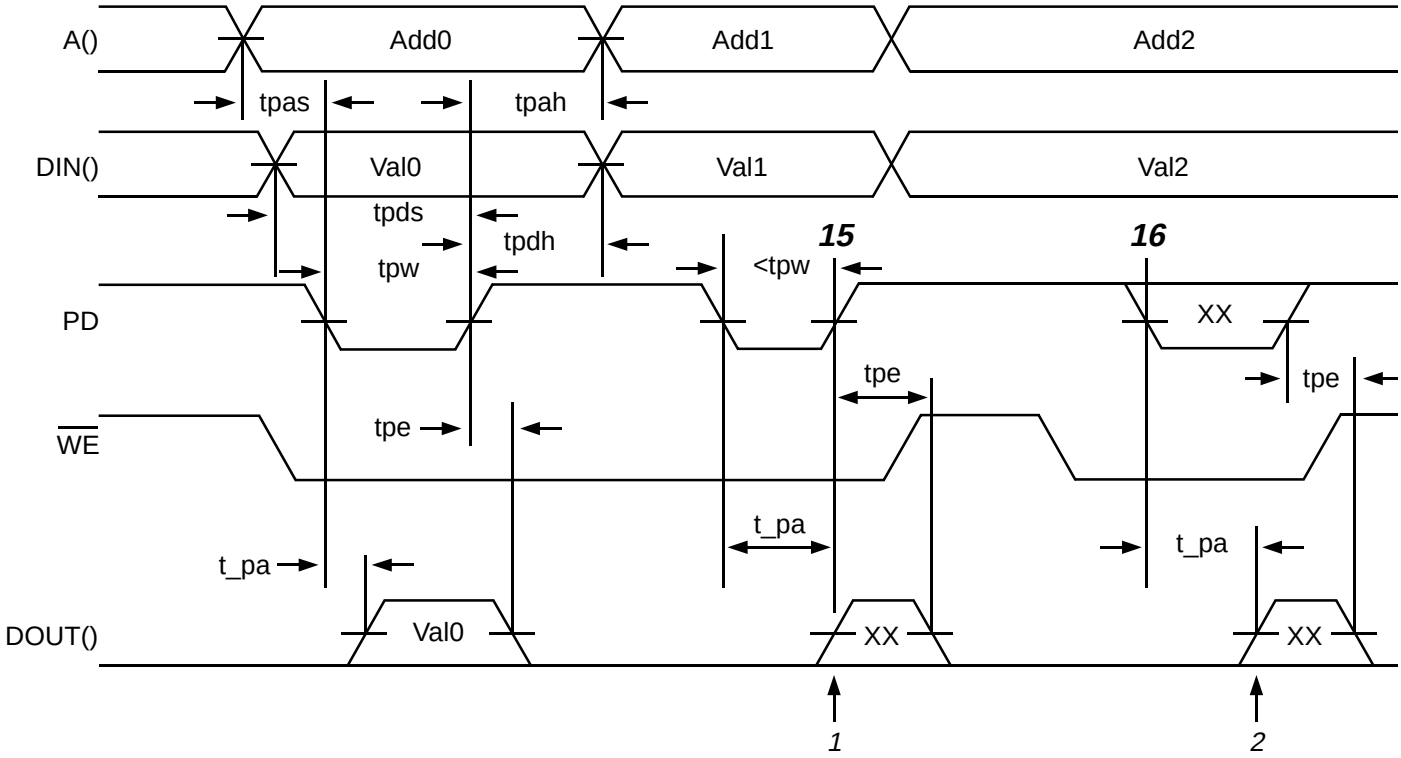


Notes: tps : $\overline{CE}$/PD setup time
tph : $\overline{CE}$/PD hold time
t_wa : Output delay time from $\overline{WE}$ (MAX of Rise/Fall)
tcea : Access time from $\overline{CE}$

1. 4. Data retained in all words is overwritten by 'X' at this time.
2. "X" retained in Add1 is overwritten by Val1 at this time.
3. "X" retained in Add2 is overwritten by Val2 at this time.
5. If Data retained in Add3 is not equal to Val3, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***12**. Error: Illegal $\overline{CE}$/PD Input: $\overline{CE}$/PD setup time to $\overline{WE}$ is smaller than Min tps.*
***13**. Error: Illegal $\overline{CE}$/PD Input: $\overline{CE}$/PD hold time to $\overline{WE}$ is smaller than Min tph.*
***14**. Error: Illegal Operation: $\overline{CE}$/PD was "X" at the falling edge of $\overline{WE}$.*

Single Port RAM Write Cycle 6 (sram_pd)

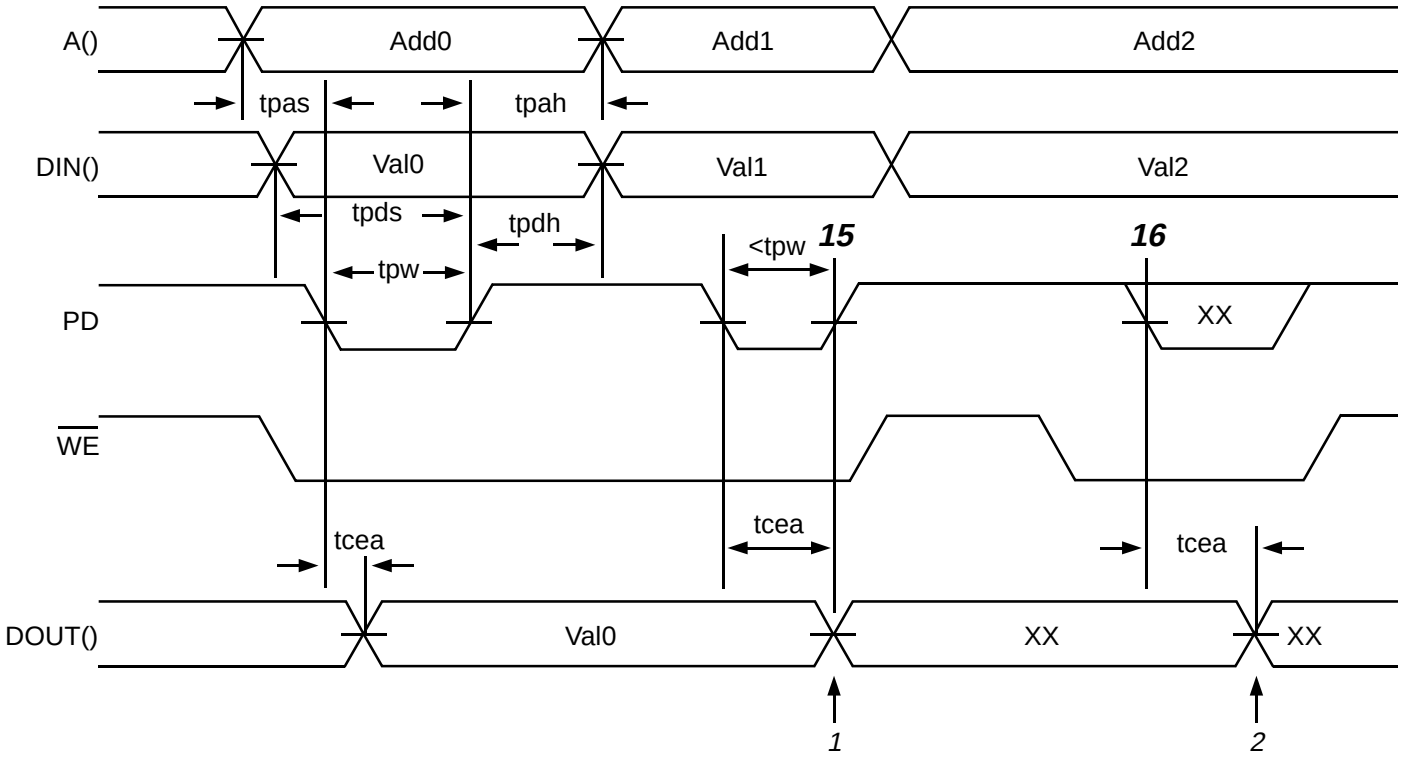


Notes:
- tpas : Address setup time to $\overline{CE}$/PD (PD pin used for zero_out function)
- tpah : Address hold time to $\overline{CE}$/PD (PD pin used for zero_out function)
- tpds : Data setup time to $\overline{CE}$/PD
- tpdh : Data hold time to $\overline{CE}$/PD
- t_pa : Access time from $\overline{CE}$/PD
- tpe : PD shutting off to DOUT() Fall
- tpw : Minimum pulse width for $\overline{CE}$/PD

1. If Data retained in Add1 is not equal to Val1, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.
2. If Data retained in Add2 is not equal to Val2, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***15**. Error: Illegal $\overline{CE}$/PD input: $\overline{CE}$/PD "Low" width time smaller than Min tpw.*
***16**. Error: Illegal Operation: $\overline{CE}$/PD went "X" while $\overline{WE}$ is "Low".*

Single Port RAM Write Cycle 7 (sram)

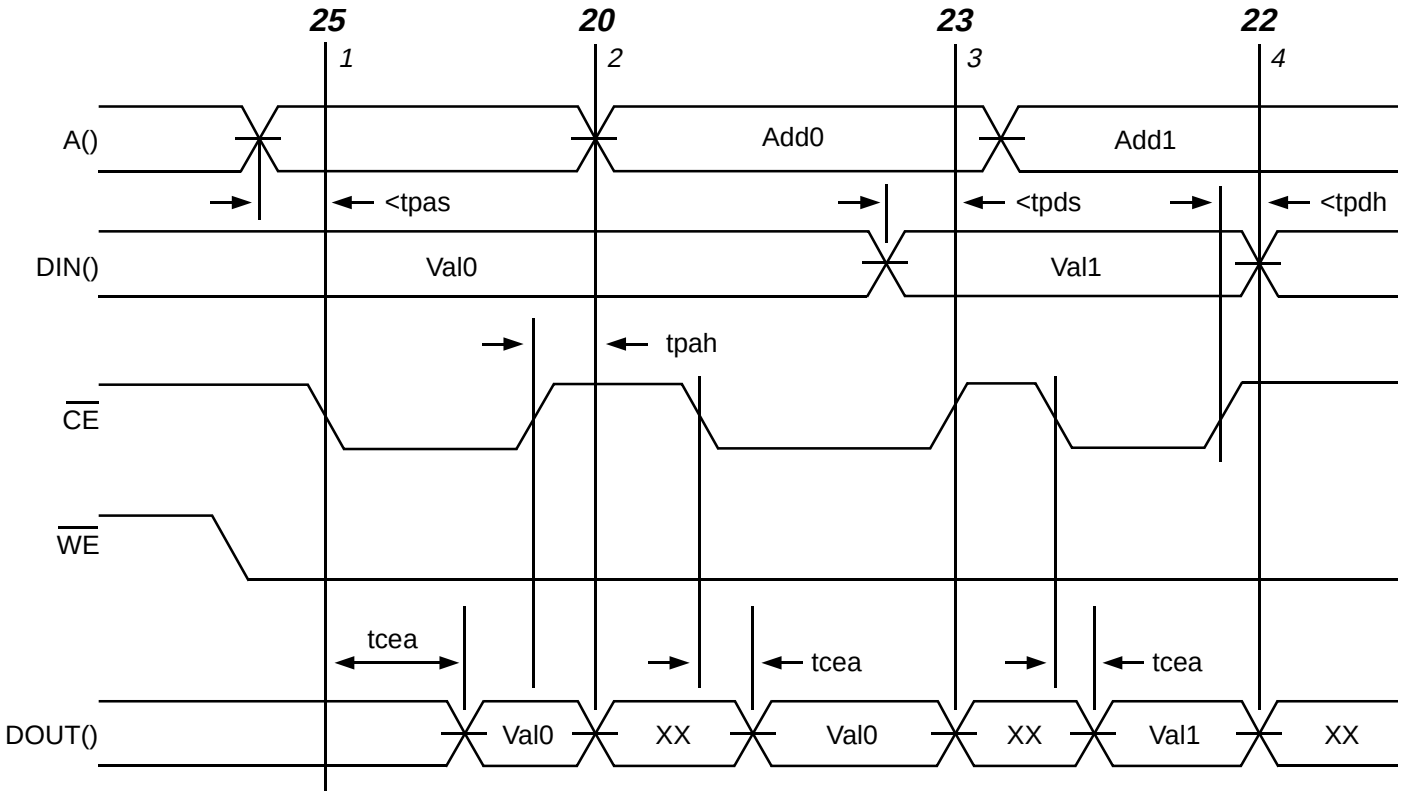


Notes: tpas : Address setup time to $\overline{CE}$/PD
tpah : Address hold time to $\overline{CE}$/PD
tpds : Data setup time to $\overline{CE}$/PD
tpdh : Data hold time to $\overline{CE}$/PD
tcea : Access time from $\overline{CE}$
tpe : PD shutting off to DOUT() Fall
tpw : Minimum pulse width from $\overline{CE}$/PD

1. If Data retained in Add1 is not equal to Val1, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.
2. If Data retained in Add2 is not equal to Val2, retained data is overwritten by "X' at this time. If both are identical, retained data is not overwritten by any value.

***15**. Error: Illegal $\overline{CE}$/PD input: $\overline{CE}$/PD "Low" width time smaller than Min tpw.*
***16**. Error: Illegal Operation: $\overline{CE}$/PD went "X" while $\overline{WE}$ is "Low".*

Single Port RAM Write Cycle 8 (sram)

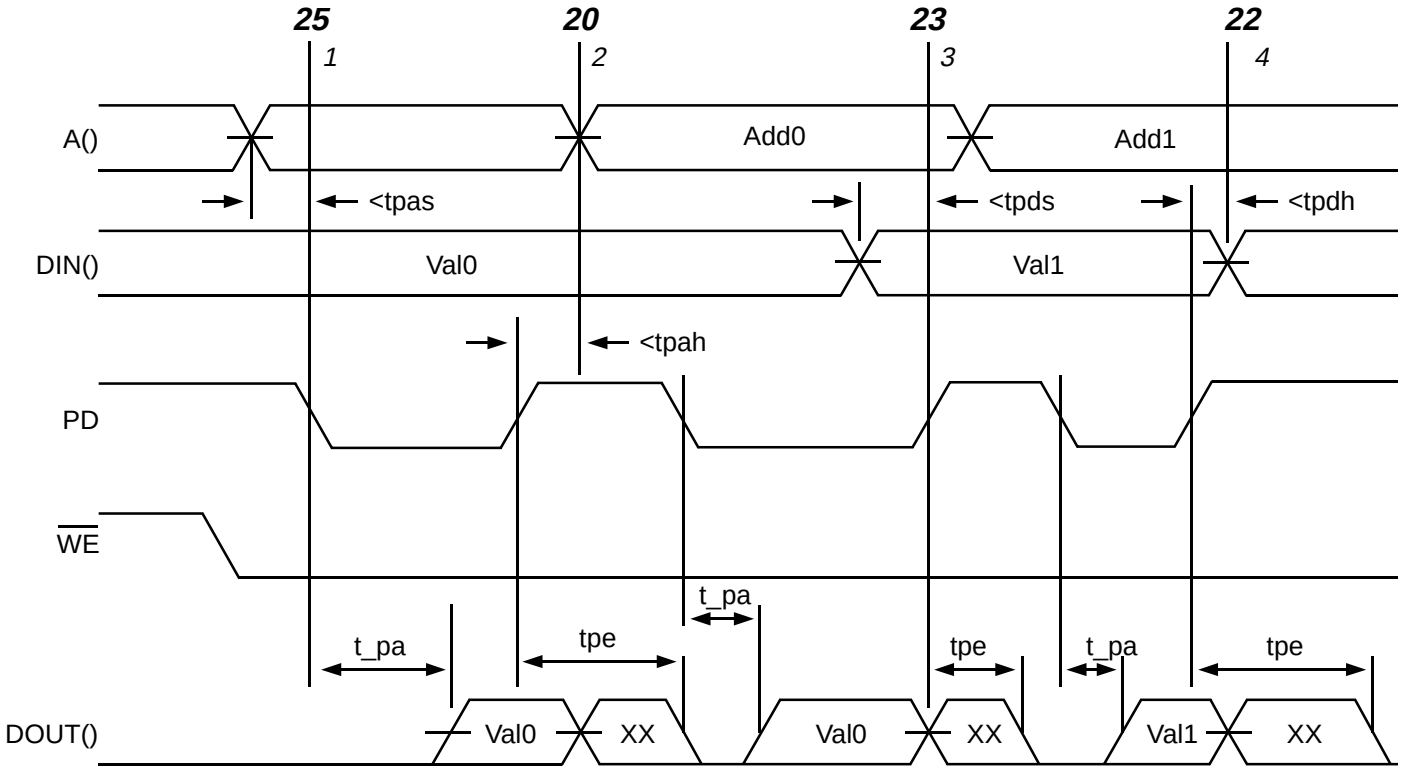


Notes:
- tpas : Address setup time to $\overline{CE}$/PD
- tpah : Address hold time to $\overline{CE}$/PD
- tpds : Data setup time to $\overline{CE}$/PD
- tpdh : Data setup time to $\overline{CE}$/PD
- tcea : Access time from $\overline{CE}$

1. If tpas is violated, data in all addresses is overwritten by "X" at this time.
2. If tpah is violated, data in all addresses is overwritten by "X" at this time.
3. If tpds is violated, data in Add0 is overwritten by "X" at this time.
4. If tpdh is violated, data in Add1 is overwritten by "X" at this time.

20. Error: Illegal address input: hold time to $\overline{CE}$/PD is smaller than min. tpah.
22. Error: Illegal data input: DIN hold time to $\overline{CE}$/PD is smaller than min. tpdh.
23. Error: Illegal data input: DIN setup time to $\overline{CE}$/PD is smaller than min. tpds.
25. Error: Illegal address input: setup time to $\overline{CE}$/PD is smaller than min. tpas.

Single Port RAM Write Cycle 9 (sram_pd)



Notes:
- tpas : Address setup time to $\overline{CE}$/PD
- tpah : Address hold time to $\overline{CE}$/PD
- tpds : Data setup time to $\overline{CE}$/PD
- tpdh : Data hold time to $\overline{CE}$/PD
- t_pa : Access time from PD
- tpe : PD shutting off to DOUT() Fall

1. If tpas is violated, data in all addresses is overwritten by "X" at this time.
2. If tpah is violated, data in all addresses is overwritten by "X" at this time.
3. If tpds is violated, data in Add0 is overwritten by "X" at this time.
4. If tpdh is violated, data in Add1 is overwritten by "X" at this time.

***20**. Error: Illegal address input: hold time to $\overline{CE}$/PD is smaller than min. tpah.*
***22**. Error: Illegal data input: DIN hold time to $\overline{CE}$/PD is smaller than min. tpdh.*
***23**. Error: Illegal data input: DIN setup time to $\overline{CE}$/PD is smaller than min. tpds.*
***25**. Error: Illegal address input: setup time to $\overline{CE}$/PD is smaller than min. tpas.*

DPRAM_1R1W
High Speed Low-Power Dual Port RAM

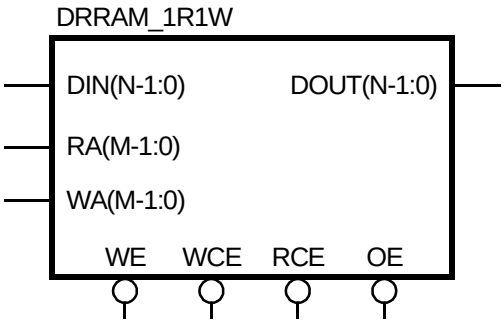
AMERICAN MICROSYSTEMS, INC.

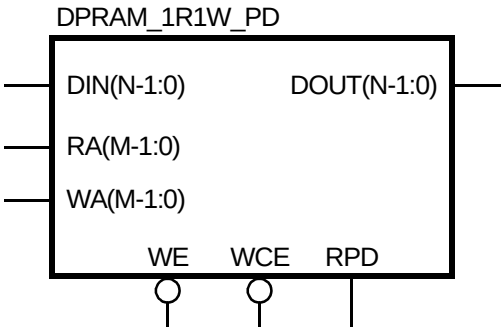
CMOS ASIC Standard Cell Memories

Features

- 8-T memory cell design
- Simple combinational logic decoding
- Small bitline differential in read mode eliminates precharge delay
- Fast ATD circuit turns on wordlines and sense amps only as needed to save power while allowing asynchronous operation

Logic Symbol





DPRAM_1R1W: High Speed Low-Power Dual Port Description

AMI's high speed, low power CMOS RAM is available in both single and dual port versions. Column select passgates provide a cascode gain stage, followed by a differential voltage sense amp. The memory array columns may be multiplexed to optimize the aspect ratio. Multiplexing of columns, or column folding, shortens the bitline length (reduces the number of rows in the array) while increasing the width of the memory array. No change in the total memory bit count occurs.

The zero_out option sends the outputs all to "zero". This operation is controlled by the PD signal.

The RAM draws current only in response to changing inputs, minimizing power consumption and allowing complete IDDQ testing. Address changes activate the sense amps and one row of memory cells for a period of time longer than access time. The current drawn by each sense amp is comparable to the read current of each memory cell.

DPRAM_1R1W High speed Low-Power dual Port RAM.

DPRAM_1R1W
High Speed Low-Power Dual Port RAM

Signal Summary

INPUTS		OUTPUTS	
PORT LABLE	**FUNCTION**	**PORT LABEL**	**FUNCTION**
RA	Read Address	DOUT	Output Data
WA	Write Address		
DIN	Input Data		
RCE	Read Chip Enable, active low		
WCE	Write Chip Enable, active low		
WE	Write Enable, active low		
OE	Output Enable, active low		
RPD	Read Power Down, active high, read cycle disabled and output driven to zero (0) when active		

Parameters

NAME	DEFINITION	DATA TYPE	VALUES
WORDS	number of words	Integer	8-16384
N	bits per word	Integer	1-144
M	address size	Integer	3-14
BPC	bits per column	Integer	2, 4, 8, 16, 32
FLOORPLAN	auto floorplan	Integer	0, 1
BUFFER_SIZE	buffer size	String	1-6
FREQUENCY	frequency in MHz	Integer	1-100
VDROP	voltage drop in millivolts	Integer	1-249

Block height range is 4-512; block width range is 4-288; max total bits is 144K (16K x 9).

BPC Options

BPC VALUE	MINIMUM WORDS	MAXIMUM WORDS	ADDRESS INCREMENT	MINIMUM BITS	MAXIMUM BITS
2	8	1024	4	1	144
4	16	2048	8	1	72
8	32	4096	16	1	36
16	64	8192	32	1	18
32	128	16384	64	1	9

DPRAM_1R1W
High Speed Low-Power Dual Port RAM

AMERICAN MICROSYSTEMS, INC.

CMOS ASIC Standard Cell Memories

Parts

PART NAME	PINS
dpram_1r1w	DIN, OE, RA, RCE, WA, WCE, WE, DOUT
dpram_1r1w_pd	DIN, RA, RPD, WA, WCE, WE, DOUT

Truth Tables

zero-out option false

INPUTS					OUTPUTS	COMMENT
RA, WA	WCE, RCE	OE	DIN	WE	DOUT	
0/1	0	0	X	1	Data	Read
X	0	1	X	1	Z	Output Disabled (standard) - RAM Active
X	1	1	X	X	Z	Output Disabled (standard) - RAM Disabled
X	1	0	X	X	Data	Outputs Stable, RAM Disabled
0/1	0	0	0/1	0	Data	Write with Write-Through
0/1	0	1	0/1	0	Z	Write

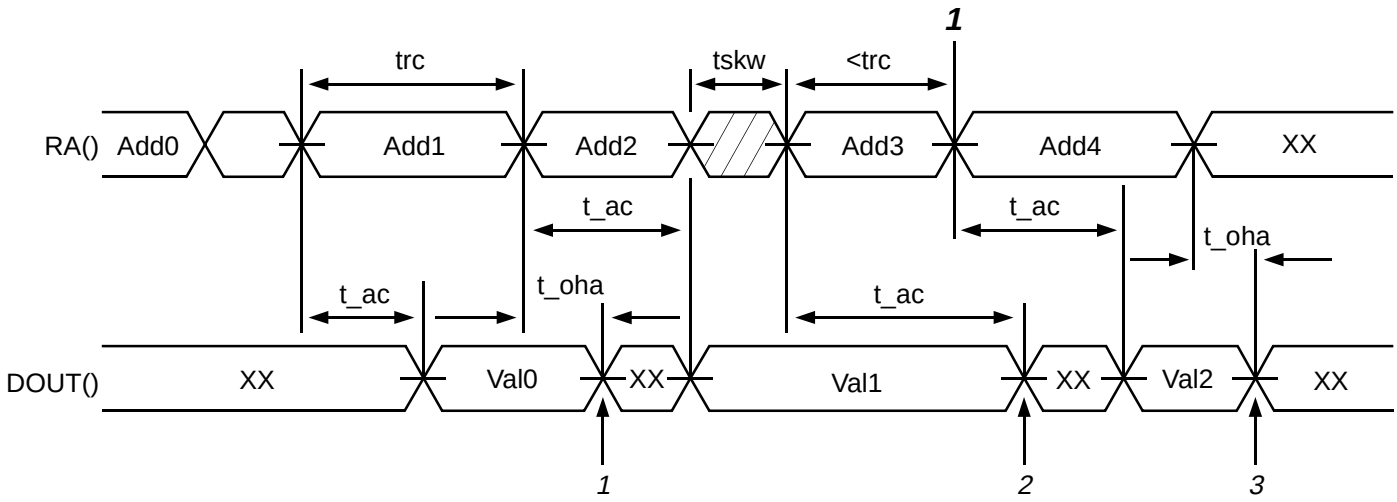
zero-out option true

INPUTS					OUTPUTS	COMMENT
RA, WA	RPD	DIN	WCE	WE	DOUT	
X	1	X	1	X	0	Output Disabled (zero_out), RAM Disabled
0/1	0	X	1	1	Data	Read
0/1	0	0/1	0	0	Data	Write with Write-Through
0/1	1	0/1	0	0	0	Write without Write-Through

SWITCHING TIME WAVEFORMS

Dual Port RAM 1R1W Read Cycle 1

dpram_1r1w : WE = '1', OE = '0', WCE = '0', RCE = '0'
dpram_1r1w_pd : WE = '1', WCE = '0', RPD = '0'



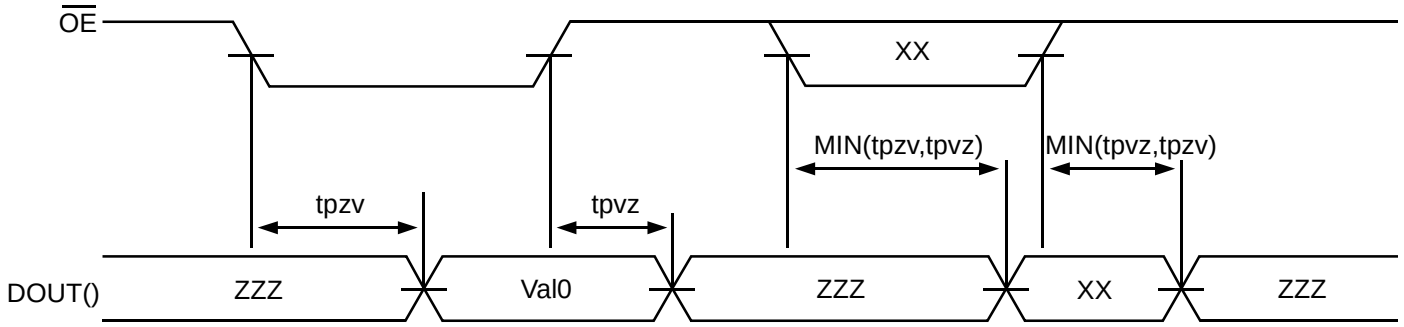
Notes: t_ac : Address Access Time (maximum of Rise/Fall)
trc : Read Cycle Time
t_oha : Output Hold Time from Address Change (minimum of Rise/Fall)
tskw : All addresses must complete transition within this time

1. t_oha delay will only be applied to the last data accessed, otherwise, t_ac will be used for the pin-to-pin delay.
2. trc = t_ac. If Add3 width is less than trc, DOUT() goes to'X'.
3. If A() becomes 'X', DOUT() goes 'X' after time t_oha.

***1**. Error: Illegal Address input: Address cycle time is smaller than minimum trc.*

Dual Port RAM 1R1W Read Cycle 2

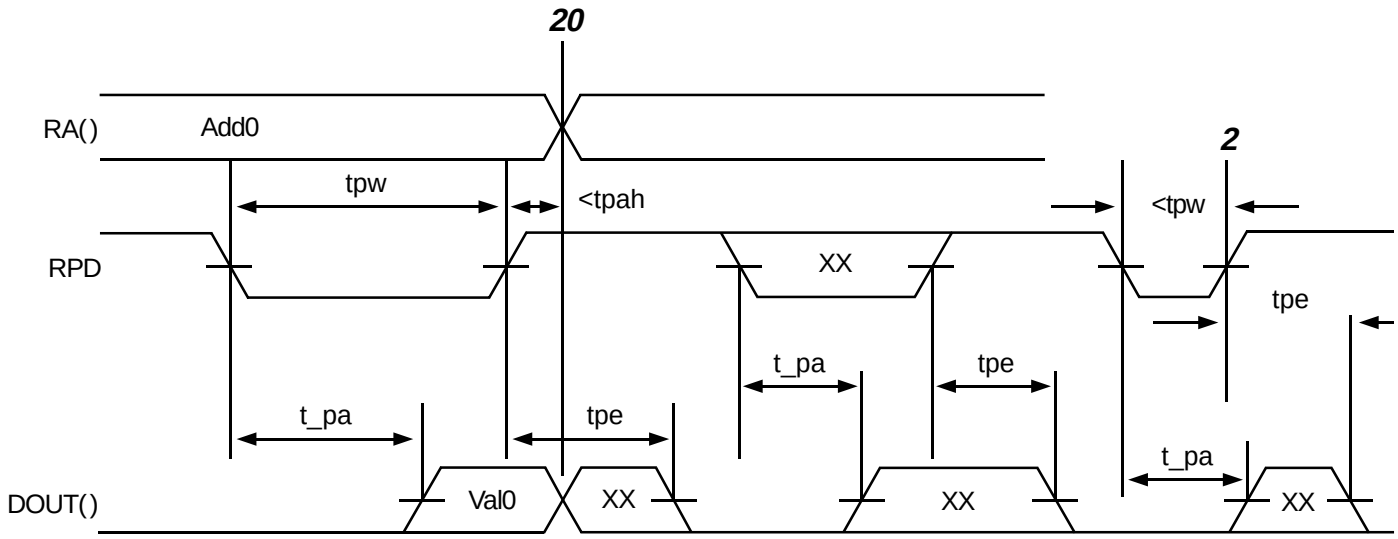
dpram_1r1w: WE = '1', WCE = '0', RCE = '0'



Notes: tpvz : Delay to propagate valid DOUT() to high impedance
tpzv : Delay to propagate high impedance to valid DOUT()

Dual Port RAM 1R1W Read Cycle 3

dpram_1r1w_pd: WE = '1', WCE = '0'

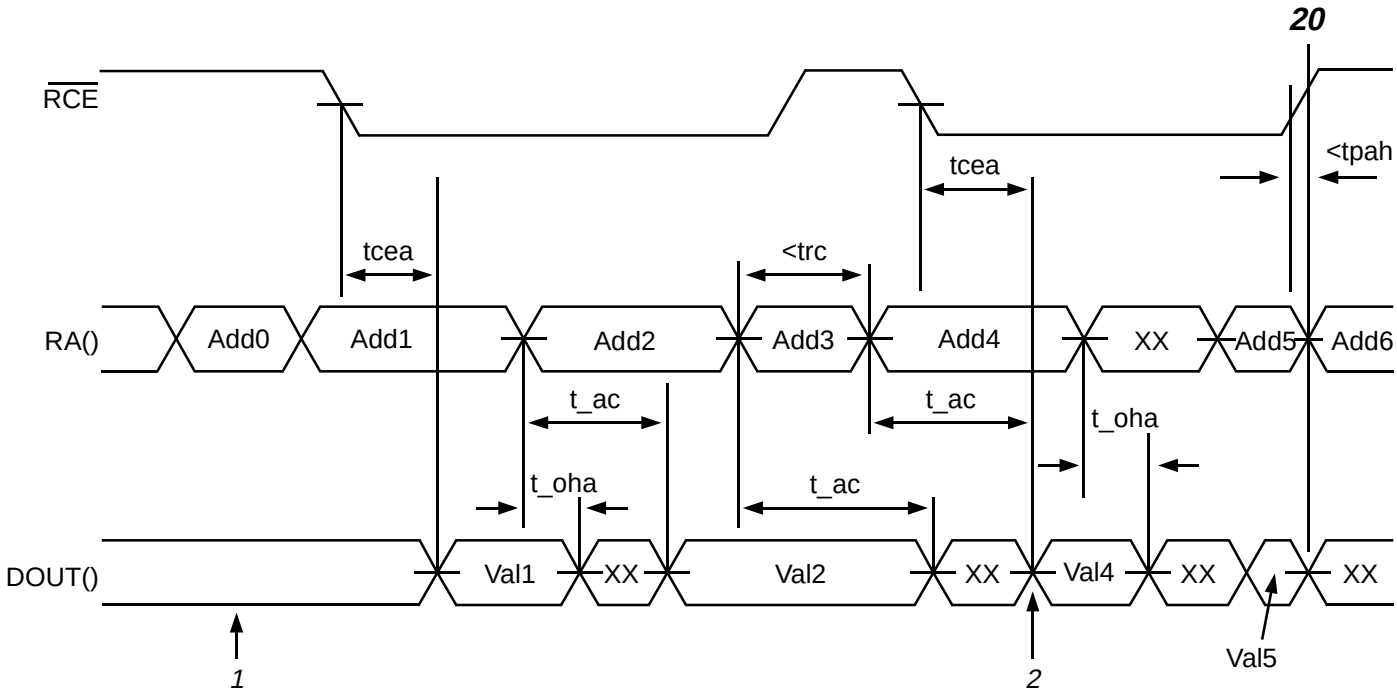


Notes: t_pa : Access time from RPD
tpe : RPD shutting off to DOUT() Fall
tpw : Minimum pulse width for RPD
tpah : Address hold time from RPD rising

***2**. Error: Illegal RPD input: RPD "Low" width time smaller than Min tpw.*
***20**. Error: Illegal address input: hold time to RPD is smaller than min. tpah.*

Dual Port RAM 1R1W Read Cycle 4

dpram_1r1w: WE = '1', WCE = '0', OE = '0'



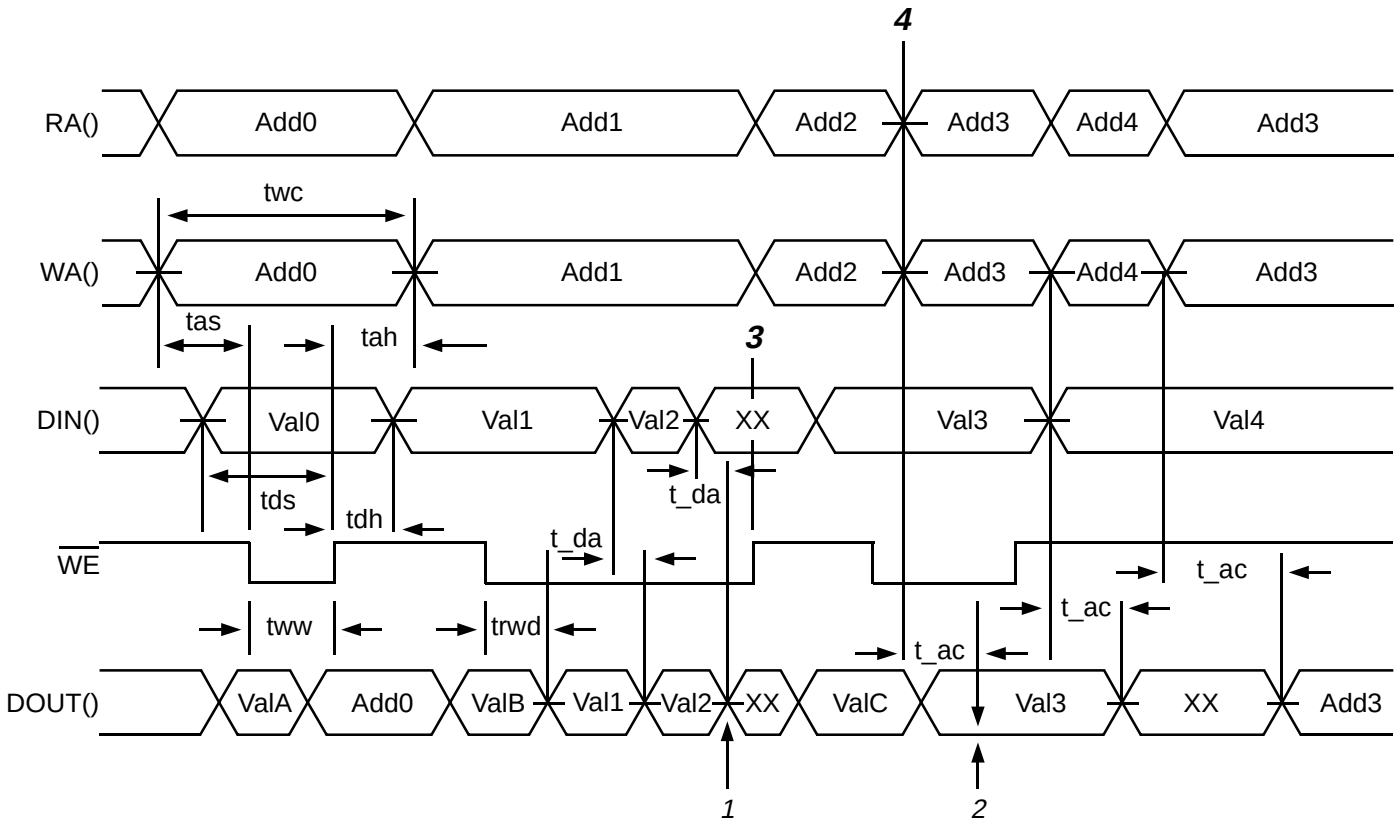
Notes: t_ac : Address access time
tcea : RCE access time (maximum of Rise/Fall)
tpah : Address hold time from RCE rising
trc : Read cycle time
t_oha : Output hold time from address change (minimum of Rise/Fall)

1. Normal DOUT() change due to address change is locked out by RCE pin set to '1'.
2. Output becomes valid after the MAX of t_ac or tcea. Note that the RCE pin rising does not trigger a RAM access.

***20**. Error: Illegal address input: hold time to RCE is smaller than min. tpah.*

Dual Port RAM 1R1W Write Cycle 1

dpram_1r1w : OE = '0', WCE = '0', RCE = '0'
dpram_1r1w_pd : WCE = '0', RPD = '0'



Notes:
- t_da : Output delay time from Data (t_da < t_ac) (MAX of Rise/Fall)
- trdw : Data access for a write-through operation
- t_ac : Address access time
- tas : Address setup time
- tah : Address hold time
- tds : Data setup time
- tdh : Data hold time
- tww : White pulse width low
- twc : Write cycle time

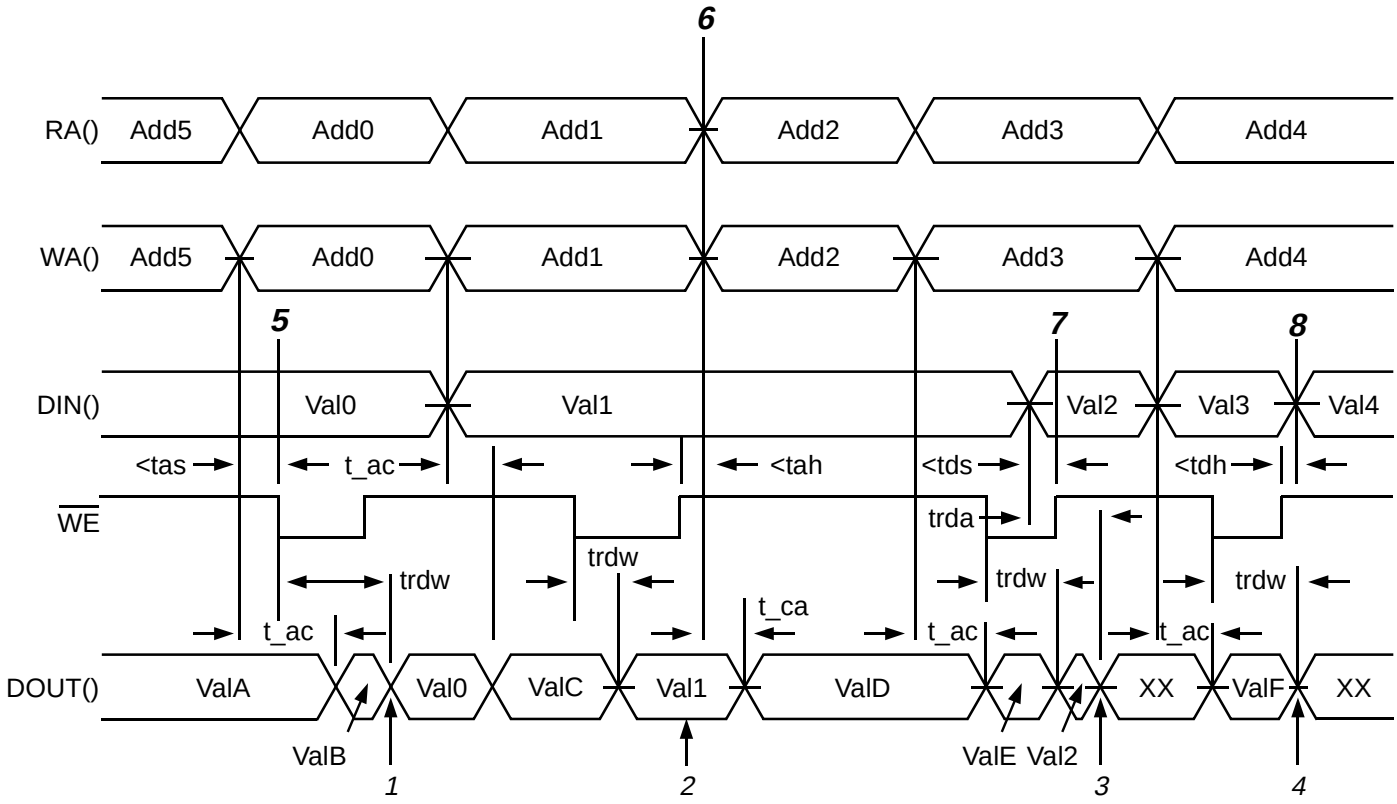
ValA, ValB, and ValC are previously retained in address Add0, Add1, and Add2.

1. Data retained in Add1 is overwritten by 'X' at this time.
2. Data retained in all words is overwritten by 'X' at this time. Writing Val3 into Add3 should be successful.

***3**. Error: Illegal Operation: Data "X" is written at rising edge of $\overline{WE}$.*
***4**. Error: Illegal Operation: Address was changed while $\overline{WE}$ low.*

Dual Port RAM 1R1W Write Cycle 2

dpram_1r1w : OE = '0', WCE = '0', RCE = '0'
dpram_1r1w_pd : WCE = '0', RPD = '0'



Notes: t_ac : Address access time
trda : Output delay time from DIN to DOUT (<t_ac) (MAX of Rise/Fall)
trdw : Data access for a write-through operation
tas : Address setup time
tah : Address hold time
tds : Data setup time
tdh : Data hold time

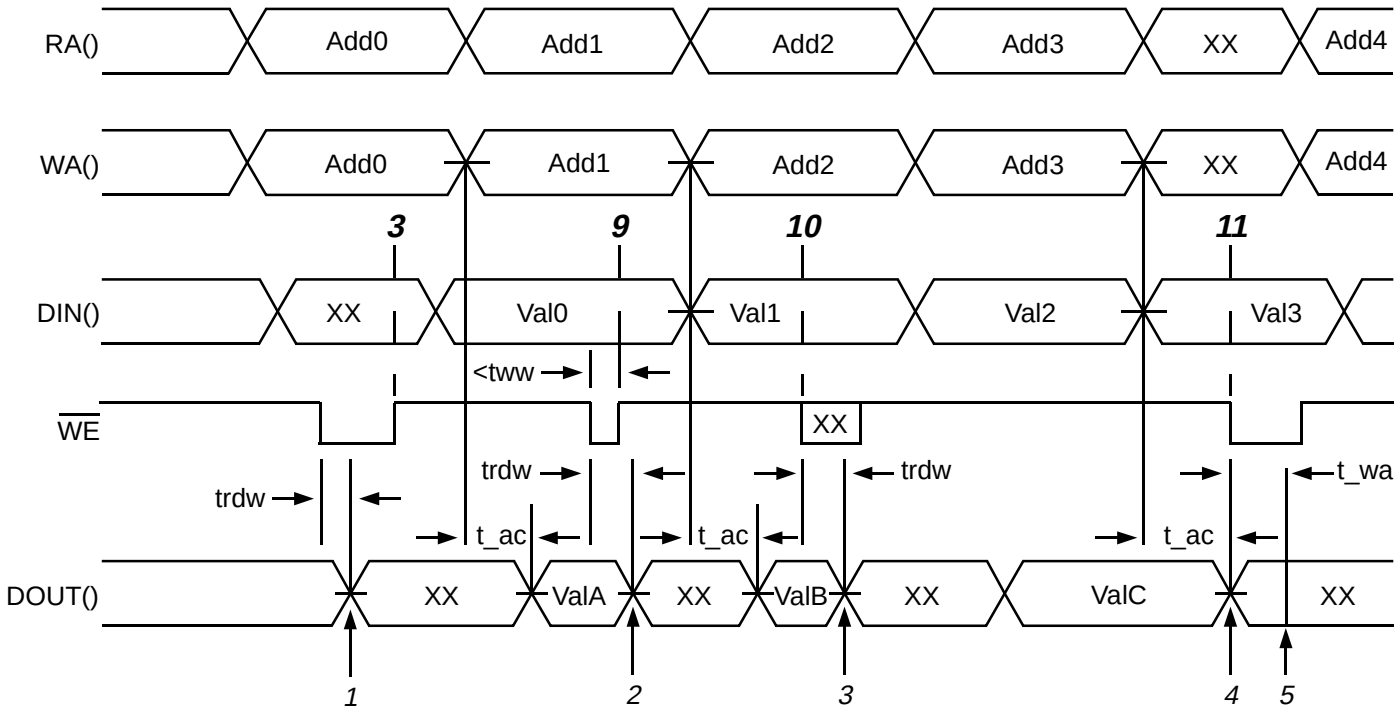
ValA-ValF are previously retained in Add5-Add4.

1. Data retained in all words is overwritten by 'X' at this time. writing Val0 into Add0 should be successful.
2. Data retained by all words is overwritten by 'X' at this time.
3. Data retained in Add3 is overwritten by 'X' at this time.
4. Data retained in Add4 is overwritten by 'X' at this time.

***5**. Error: Illegal Address Input: Address setup time to $\overline{WE}$ is smaller than Min tas.*
***6**. Error: Illegal Address Input: Address hold time to $\overline{WE}$ is smaller than Min tah.*
***7**. Error: Illegal Data Input: DIN setup time to $\overline{WE}$ is smaller than Min tds.*
***8**. Error: Illegal Data Input: DIN hold time to WE is smaller than Min tdh.*

Dual Port RAM 1R1W Write Cycle 3

dpram_1r1w : OE = '0', WCE = '0', RCE = '0'
dpram_1r1w_pd : WCE = '0', RPD = '0'



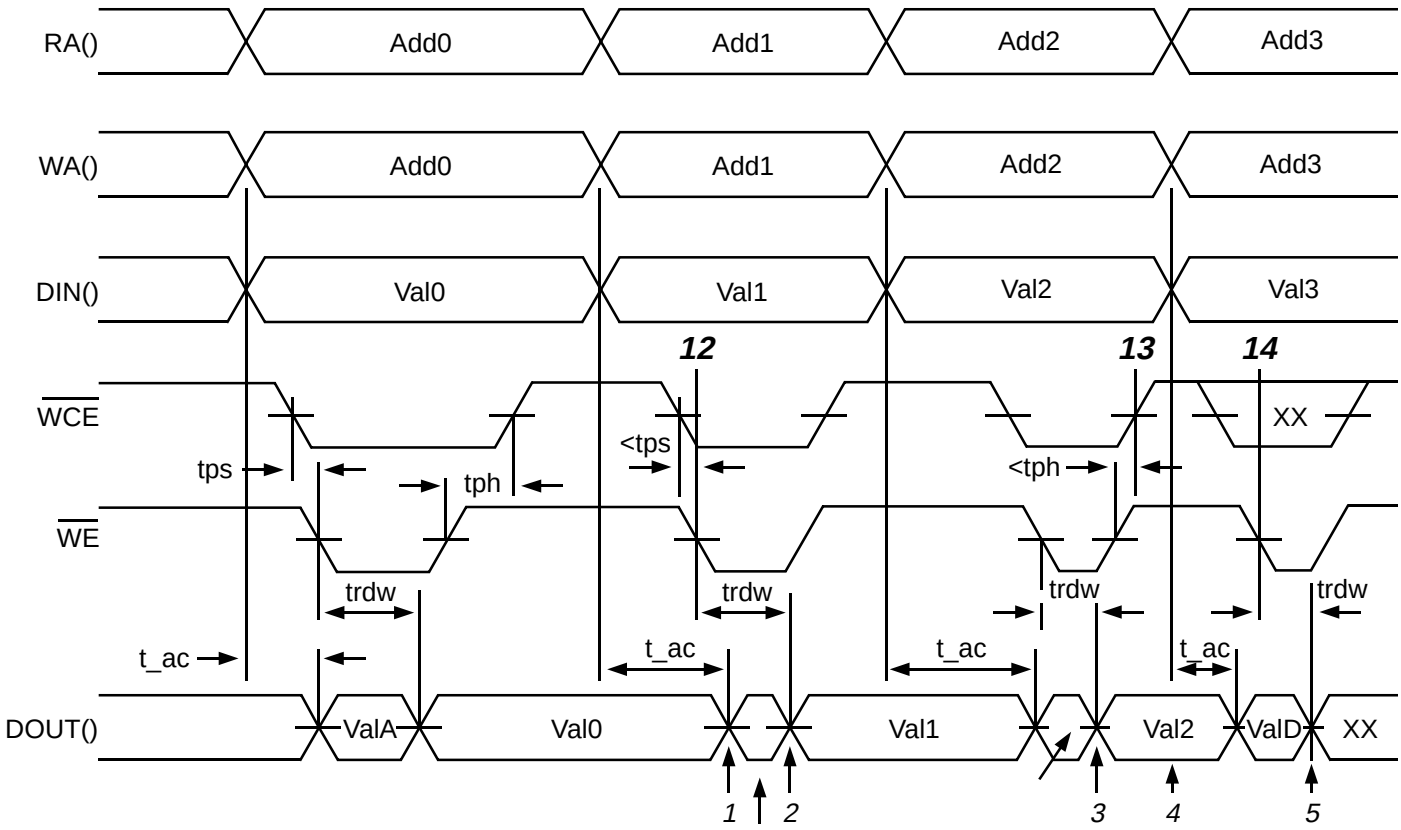
Notes: trdw : Data access for a write-through operation
t_wa : Output delay time from $\overline{WE}$ (Max of Rise/Fall)
t_ac : Address access time
tww : Write pulse width low

1. Data retained in Add0 is overwritten by 'X' at this time.
2. Data retained in Add1 is overwritten by 'X' at this time.
3. Data retained in Add2 is overwritten by 'X' at this time.
4. DOUT() becomes 'X' after t_ac time from leading edge of address 'X'.
5. Data retained in all words is overwritten by 'X' after t_wa time from falling edge of $\overline{WE}$.

***3**. Error: Illegal Operation: Data "X" is written at rising edge of $\overline{WE}$.*
***9**. Error: Illegal WE input: WE "Low" width time is smaller than Min tww.*
***10**. Error: Illegal Operation: $\overline{WE}$ input went to "X".*
***11**. Error: Illegal Operation: Address was "X" at the falling edge of $\overline{WE}$.*

Dual Port RAM 1R1W Write Cycle 4, and Write Cycle 5

dpram_1r1w_pd : RPD = '0'
dpram_1r1w : RCE = '0', OE = '0'



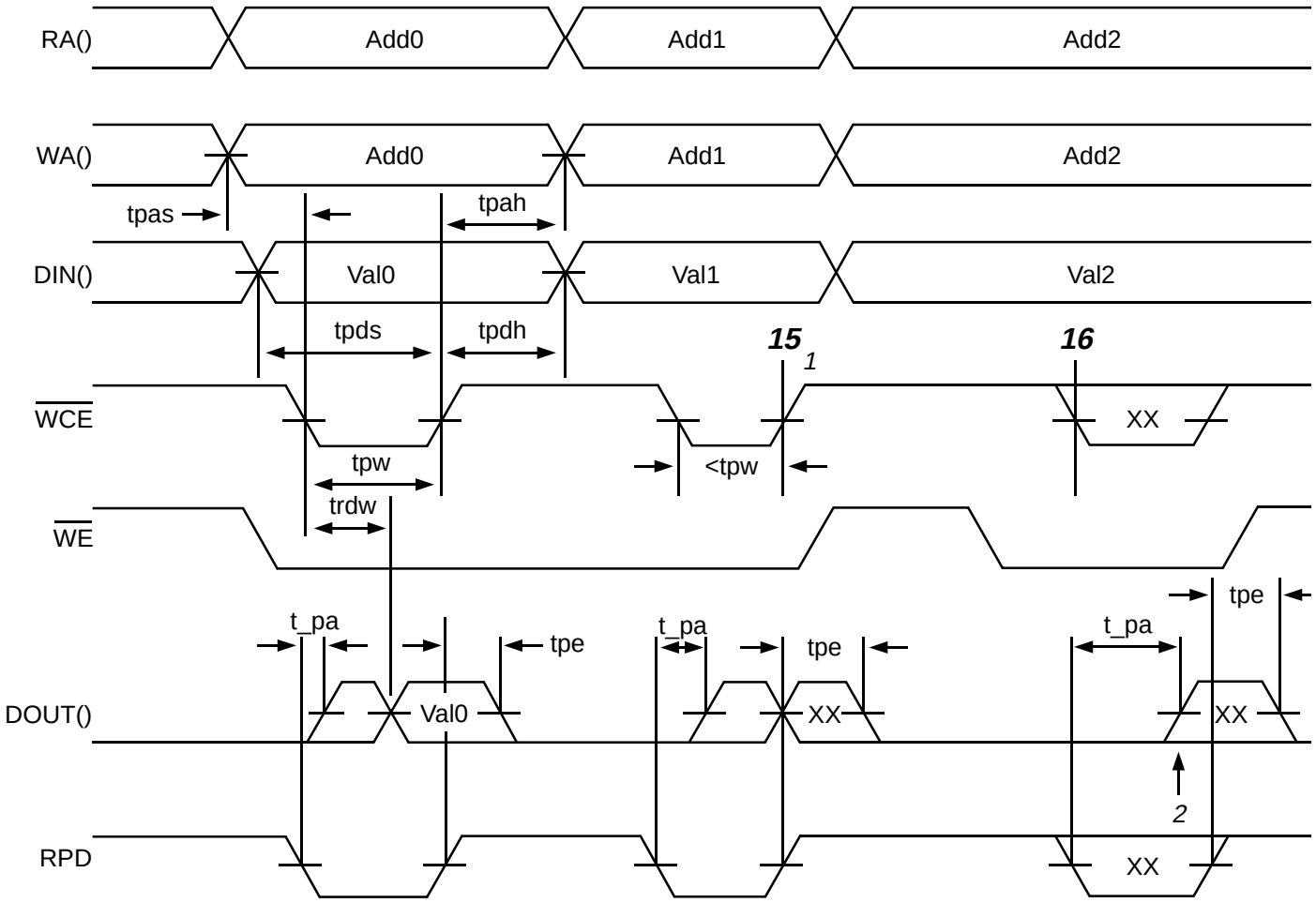
Notes: tps : $\overline{WCE}$/RPD setup time
tph : PD hold time
trdw : Data access for a write-through operation
t_ac : Address access time

ValA-ValD are previously retained in address Add0-Add3.

1. 4. Data retained in all words is overwritten by 'X' at this time.
2. "X" retained in Add1 is overwritten by Val1 at this time.
3. "X" retained in Add2 is overwritten by Val2 at this time.
5. If Data retained in Add3 is not equal to Val3, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***12**. Error: Illegal RPD Input: RPD setup time to $\overline{WE}$ is smaller than Min tps.*
***13**. Error: Illegal RPD Input: RPD hold time to $\overline{WE}$ is smaller than Min tph.*
***14**. Error: Illegal Operation: RPD was "X" at the falling edge of $\overline{WE}$.*

Dual Port RAM 1R1W Write Cycle 6 (dpram_1r1w_pd)

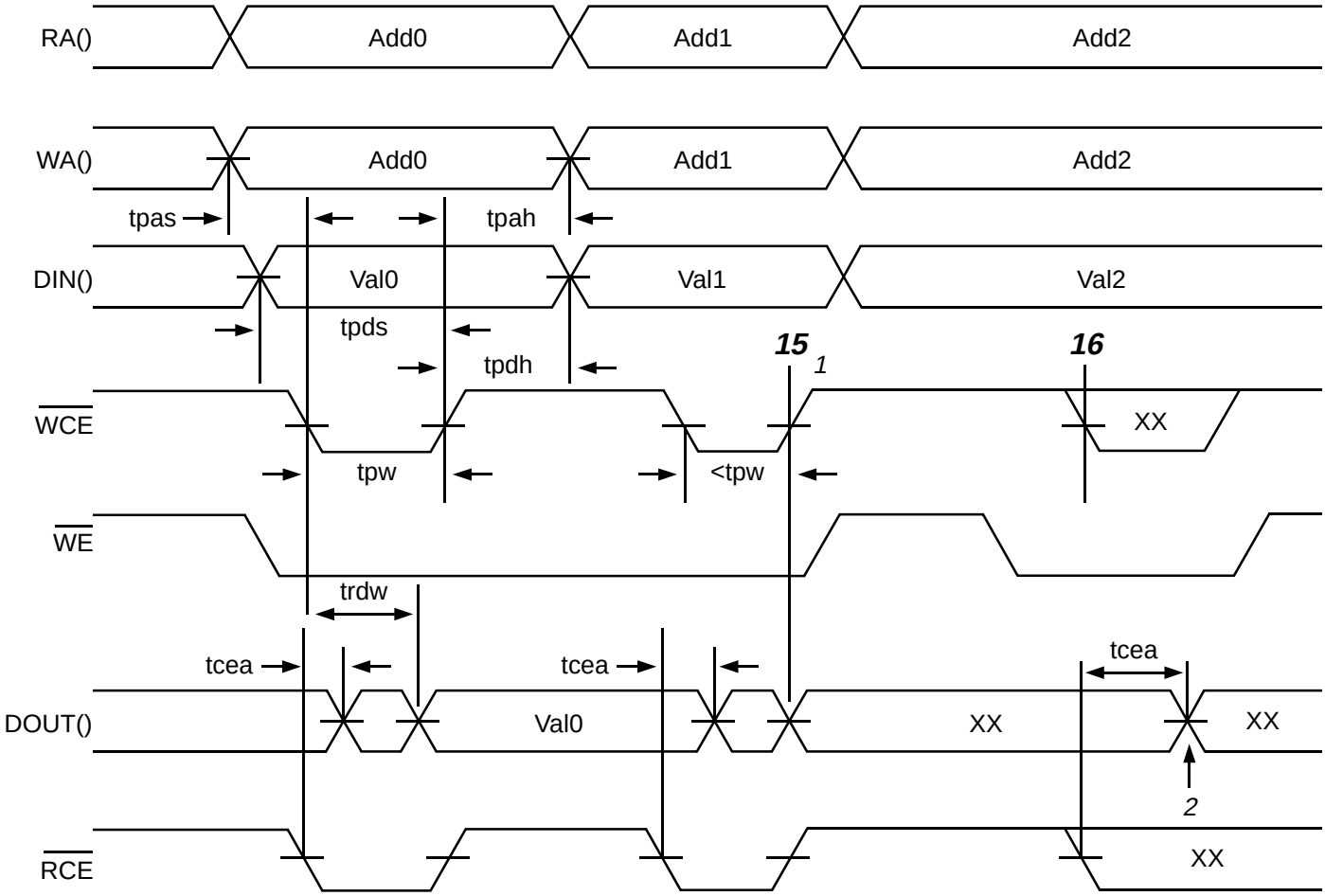


Notes:
- tpas : Address setup time to $\overline{WCE}$
- tpah : Address hold time to $\overline{WCE}$
- tpds : Data setup time to $\overline{WCE}$
- tpdh : Data hold time to $\overline{WCE}$
- t_pa : Access time from RPD
- tpe : RPD shutting off to DOUT() Fall
- tpw : Minimum pulse width for $\overline{WCE}$
- trdw : Data access for a write-through operation

1. If Data retained in Add1 is not equal to Val1, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.
2. If Data retained in Add2 is not equal to Val2, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***15**. Error: Illegal $\overline{WCE}$ input: $\overline{WCE}$ "Low" width time smaller than Min tpw.*
***16**. Error: Illegal Operation: $\overline{WCE}$ went "X" while $\overline{WE}$ is "Low".*

Dual Port RAM 1R1W Write Cycle 7 (dpram_1r1w)



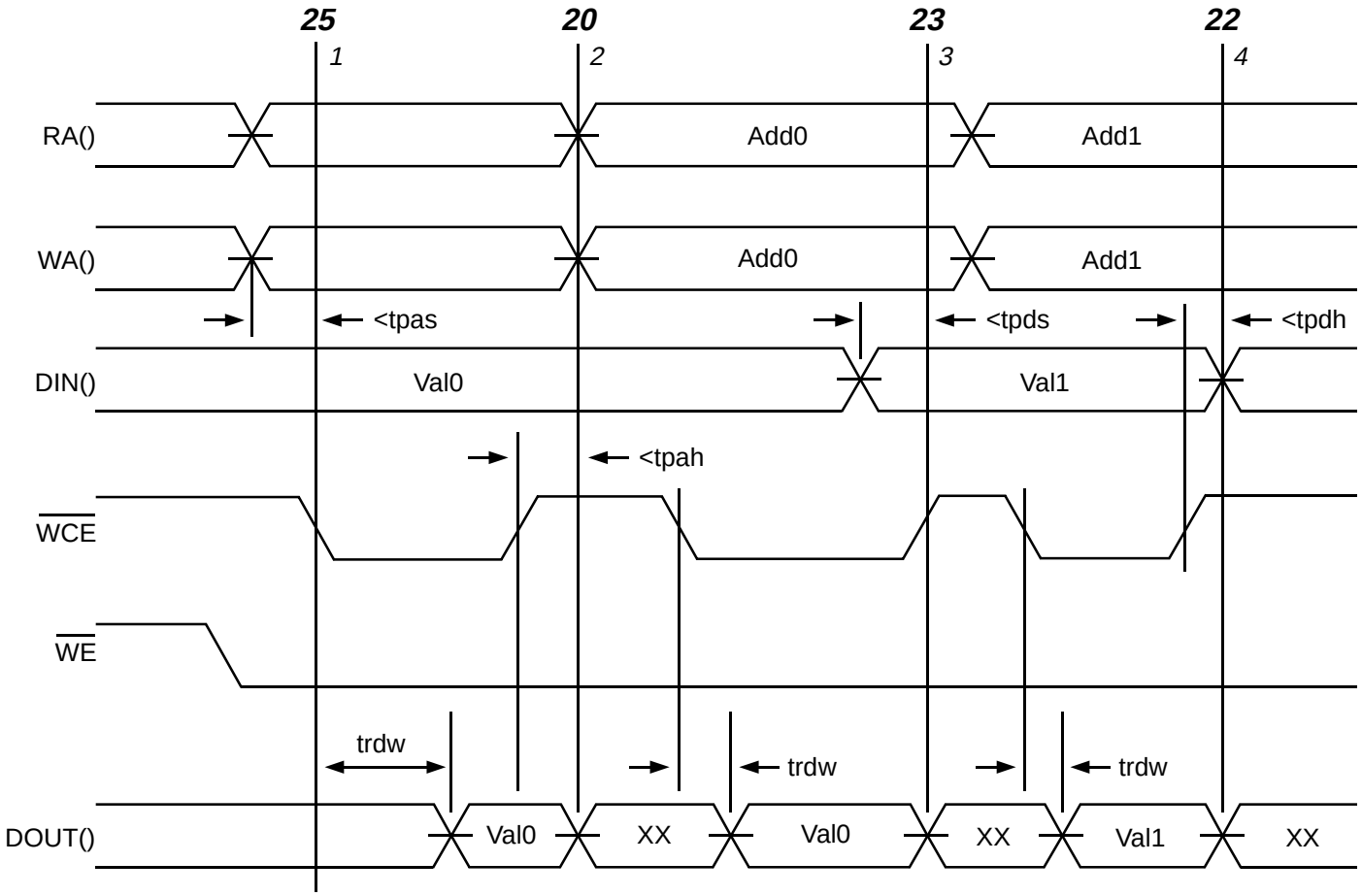
Notes: tpas : Address setup time to $\overline{WCE}$
tpah : Address hold time to $\overline{WCE}$
tpds : Data setup time to $\overline{WCE}$
tpdh : Data hold time to $\overline{WCE}$
tcea : Access time from $\overline{RCE}$
tpw : Minimum pulse width for $\overline{WCE}$
trdw : Data access for a write-through operation

1. If Data retained in Add1 is not equal to Val1, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.
2. If Data retained in Add2 is not equal to Val2, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***15**. Error: Illegal $\overline{WCE}$ input: $\overline{WCE}$ "Low" width time smaller than Min tpw.*
***16**. Error: Illegal Operation: $\overline{WCE}$ went "X" while $\overline{WE}$ is "Low".*

Dual Port RAM 1R1W Write Cycle 8, Write Cycle 9

dpram_1r1w_pd : RPD = '0'
dpram_1r1w : RCE = '0', OE = '0'



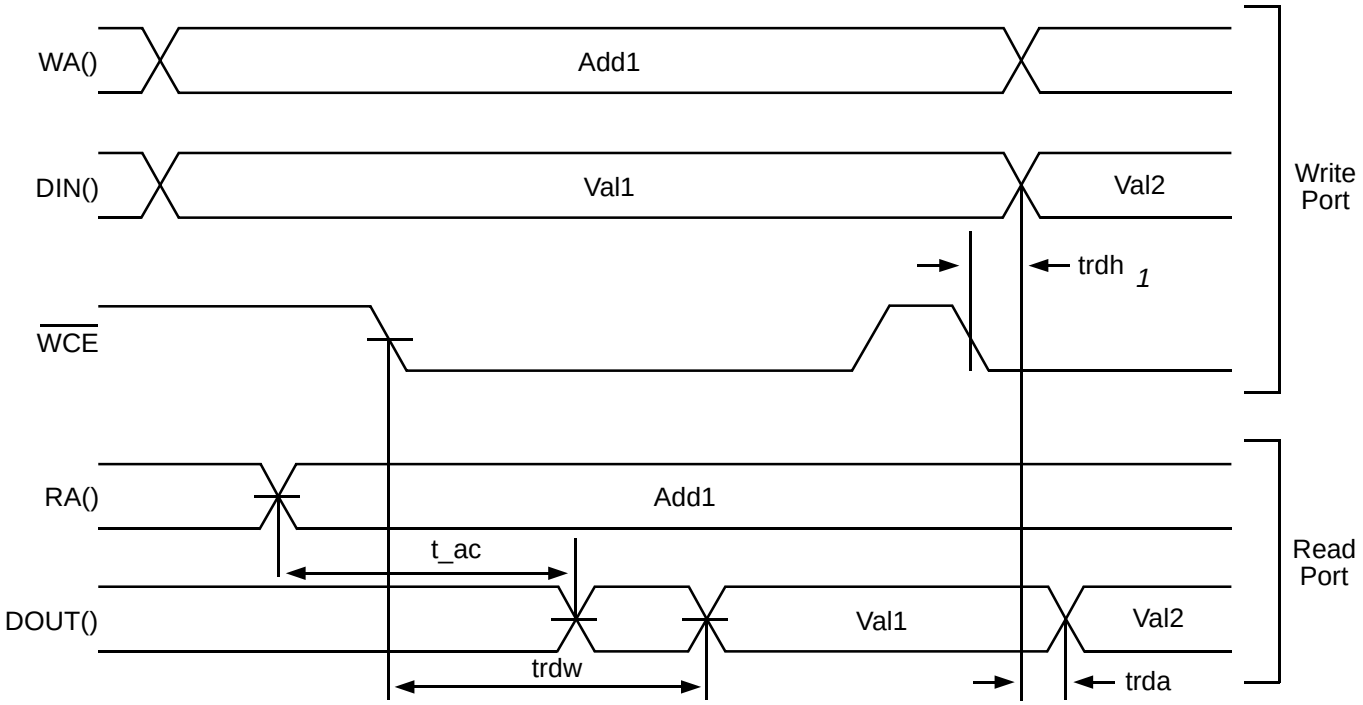
Notes: tpas : Address setup time to $\overline{WCE}$
tpah : Address hold time to $\overline{WCE}$
tpds : Data setup time to $\overline{WCE}$
tpdh : Data hold time to $\overline{WCE}$
trdw : Data access for a write-through operation

1. If tpas is violated, data in all addresses is overwritten by "X" at this time.
2. If tpah is violated, data in all addresses is overwritten by "X" at this time.
3. If tpds is violated, data in Add0 is overwritten by "X" at this time.
4. If tpdh is violated, data in Add1 is overwritten by "X" at this time.

***20**. Error: Illegal address input: hold time to $\overline{WCE}$ is smaller than min. tpah.*
***22**. Error: Illegal data input: DIN hold time to $\overline{WCE}$ is smaller than min. tpdh.*
***23**. Error: Illegal data input: DIN setup time to $\overline{WCE}$ is smaller than min. tpds.*
***25**. Error: Illegal address input: setup time to $\overline{WCE}$ is smaller than min. tpas.*

Dual Port RAM 1R1W Write Through

dpram_1r1w : OE = '0', WCE = '0', RCE = '0'
dpram_1r1w_pd : WCE = '0', RPD = '0'



Notes: t_ac : Address access time
trdw : Data access for a write-through operation from $\overline{WE}$ to data out. This time is always longer than t_wa or t_ac
trdh : Data hold from $\overline{WE}$ rising/falling for write-through
trda : Output delay from DIN

1. If DIN change from $\overline{WE}$ falling edge is greater than trdh, the DIN change will not propagate through to DOUT until the rising edge of $\overline{WE}$.

DPRAM_2RW
High Speed Low-Power Dual Port RAM

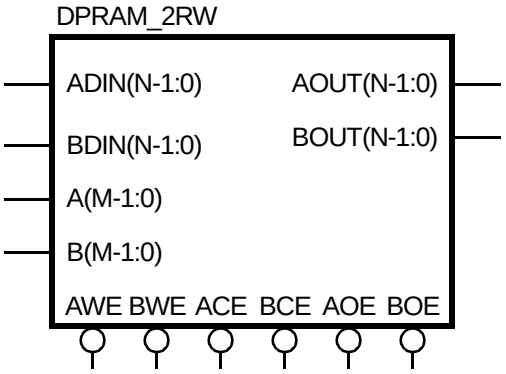
AMERICAN MICROSYSTEMS, INC.

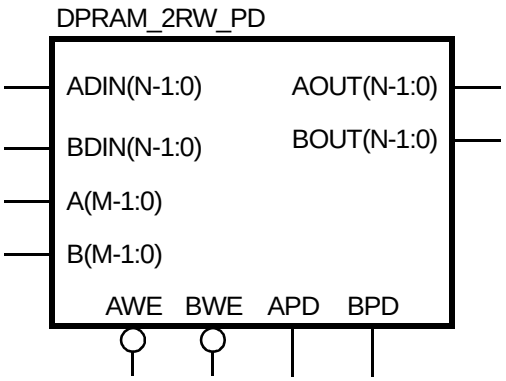
CMOS ASIC Standard Cell Memories

Features

- 8-T memory cell design
- Simple combinational logic decoding
- Small bitline differential in read mode eliminates precharge delay
- Fast ATD circuit turns on wordlines and sense amps only as needed to save power while allowing asynchronous operation

Logic Symbol





DPRAM_2RW: High Speed Low-Power Dual Port Description

AMI's high speed, low power CMOS RAM is available in both single and dual port versions. Column select passgates provide a cascode gain stage, followed by a differential voltage sense amp. The memory array columns may be multiplexed to optimize the aspect ratio. Multiplexing of columns, or column folding, shortens the bitline length (reduces the number of rows in the array) while increasing the width of the memory array. No change in the total memory bit count occurs.

The zero_out option sends the outputs all to "zero". This operation is controlled by the PD signal.

The RAM draws current only in response to changing inputs, minimizing power consumption and allowing complete IDDQ testing. Address changes activate the sense amps and one row of memory cells for a period of time longer than access time. The current drawn by each sense amp is comparable to the read current of each memory cell.

Signal Summary

INPUTS		OUTPUTS	
PORT LABEL	**FUNCTION**	**PORT LABEL**	**FUNCTION**
A, B	Addresses	ADOUT, BDOUT	Output Data
ADIN, BDIN	Input Data		
ACE, BCE	Chip Enable, active low		
AWE, BWE	Write Enable, active low		
AOE, BOE	Output Enable, active low, tristated output control		
APD, BPD	Power Down, active high, read and write cycles disabled and output driven to zero (0) when active		

Parameters

NAME	DEFINITION	DATA TYPE	VALUES
N	bits per word	Integer	1 - 144
WORDS	number of words	Integer	8 - 16384
M	address size	Integer	3-14
BPC	bits per column	Integer	2, 4, 8, 16, 32
FLOORPLAN	auto floorplan	Integer	0, 1
BUFFER_SIZE	buffer size	String	1-6
FREQUENCY	frequency in MHz	Integer	1-100
VDROP	voltage drop in millivolts	Integer	1-249

Core Size

MEASUREMENT	DATA TYPE	VALUE
Block Height	Integer	4 to 512
Block Width	Integer	4 to 288
Maximum Total Bits	Integer	144K (16K by 9)

DPRAM_2RW
High Speed Low-Power Dual Port RAM

AMERICAN MICROSYSTEMS, INC.

CMOS ASIC Standard Cell Memories

Bits Per Column (BPC) Options

BPC VALUE	MINIMUM WORDS	MAXIMUM WORDS	ADDRESS INCREMENT	MINIMUM BITS	MAXIMUM BITS
2	8	1024	4	1	144
4	16	2048	8	1	72
8	32	4096	16	1	36
16	64	8192	32	1	18
32	128	16384	64	1	9

Parts

PART NAME	PINS
dpram_2rw	A, ACE, ADIN, AOE, AWE, B, BCE, BDIN, BOE, BWE, ADOUT, BDOUT
dpram_2rw_pd	A, ADIN, APD, AWE, B, BDIN, BPD, BWE, ADOUT, BDOUT

Truth Tables

zero-out option false

INPUTS					OUTPUTS	COMMENT
A, B	ACE, BCE	AOE, BOE	ADIN, BDIN	AWE, BWE	ADOUT, BDOUT	
0/1	0	0	X	1	Data	Read
X	0	1	X	1	Z	Output Disabled (standard) - RAM Active
X	1	1	X	X	Z	Output Disabled (standard) - RAM Disabled
X	1	0	X	X	Data	Outputs Stable, RAM disabled
0/1	0	0	0/1	0	Data	Write with Write-Through
0/1	0	1	0/1	0	Z	Write

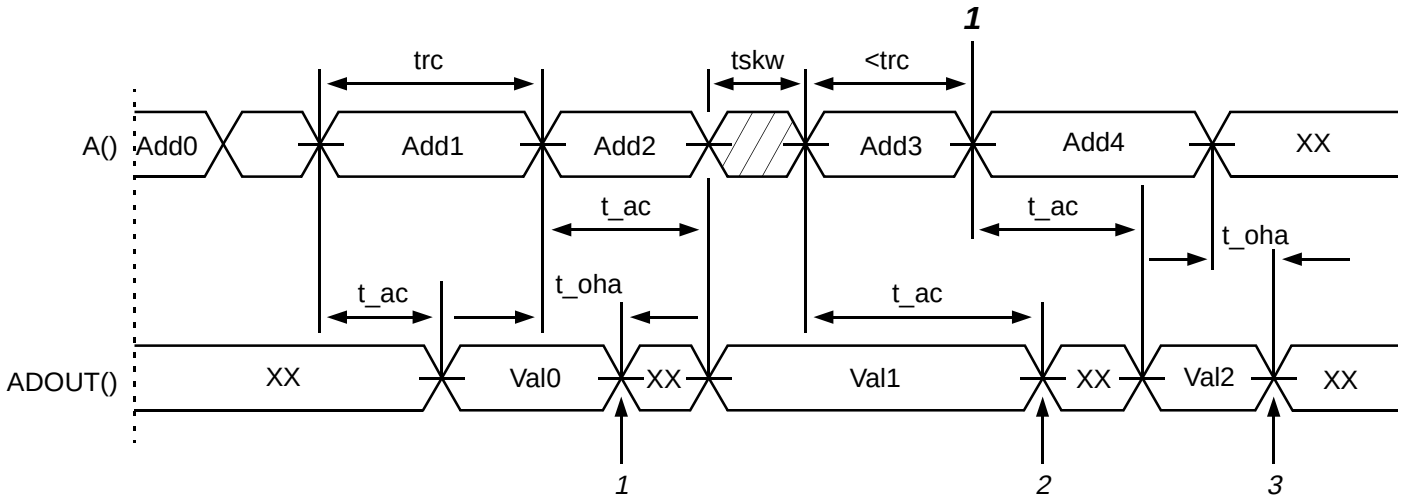
zero-out option true

INPUTS				OUTPUTS	COMMENT
A, B	APD, BPD	ADIN, BDIN	AWE, BWE	ADOUT, BDOUT	
X	1	X	X	0	Output Disabled (zero_out), RAM disabled
0/1	0	X	1	Data	Read
0/1	0	0/1	0	Data	Write with Write-Through

SWITCHING TIME WAVEFORMS

Dual Port RAM 2RW Read Cycle 1

dpram_2rw :AWE = '1', BWE = '1', AOE = '0', BOE = '0', ACE = '0', BCE = '0'
dpram_2rw_pd :AWE = '1', BWE = '1', APD = '0', BPD = '0'

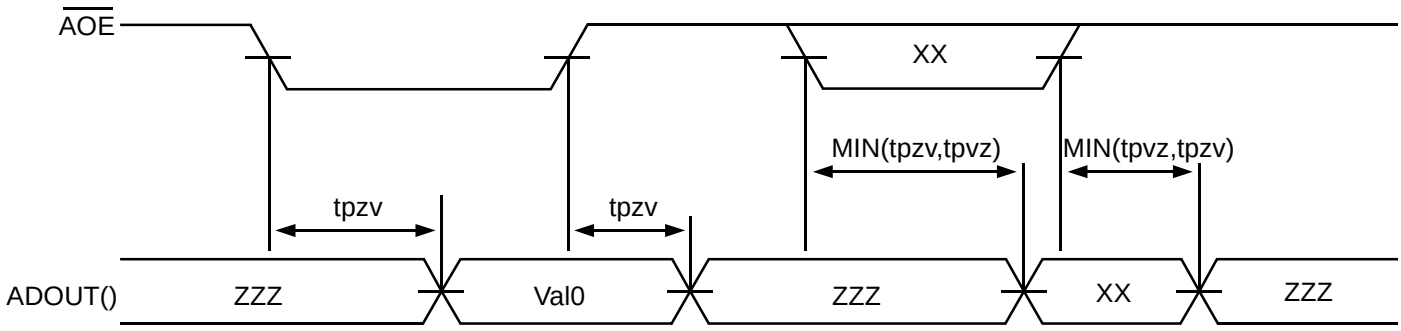


Notes: t_ac : Address Access Time (maximum of Rise/Fall)
trc : Read Cycle Time
t_oha : Output Hold Time from Address Change (minimum of Rise/Fall)
tskw : All addresses must complete transition within this time

1. t_oha delay will only be applied to the last data accessed, otherwise, t_ac will be used for the pin-to-pin delay.
2. trc = t_ac. If Add3 width is less than trc, DOUT() goes to 'X'.
3. If A() becomes 'X', DOUT() goes 'X' after time t_oha.
***1**. Error: Illegal Address input: Address cycle time is smaller than minimum trc.*

Dual Port RAM 2RW Read Cycle 2

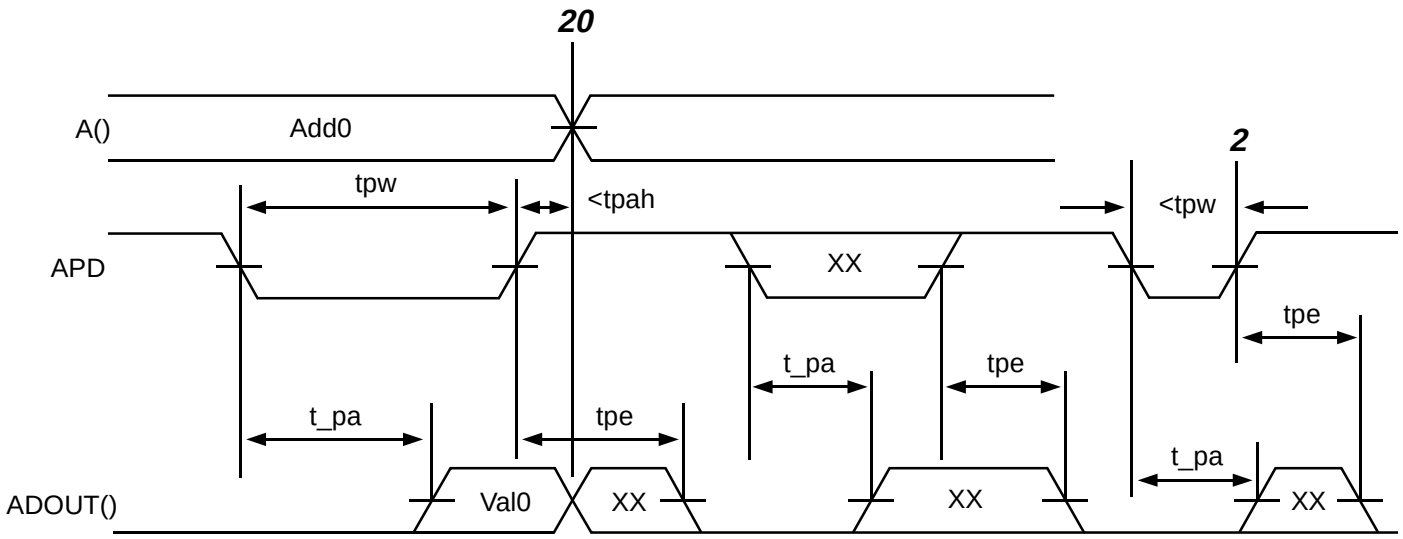
dpram_2rw: AWE = '1', BWE = '1', ACE = '0', BCE = '0'



Notes: tpvz : Delay to propagate valid DOUT() to high impedance.
tpzv : Delay to propagate high impedance to valid DOUT().

Dual Port RAM 2RW Read Cycle 3

dpram_2rw_pd: AWE = '1', BWE = '1'

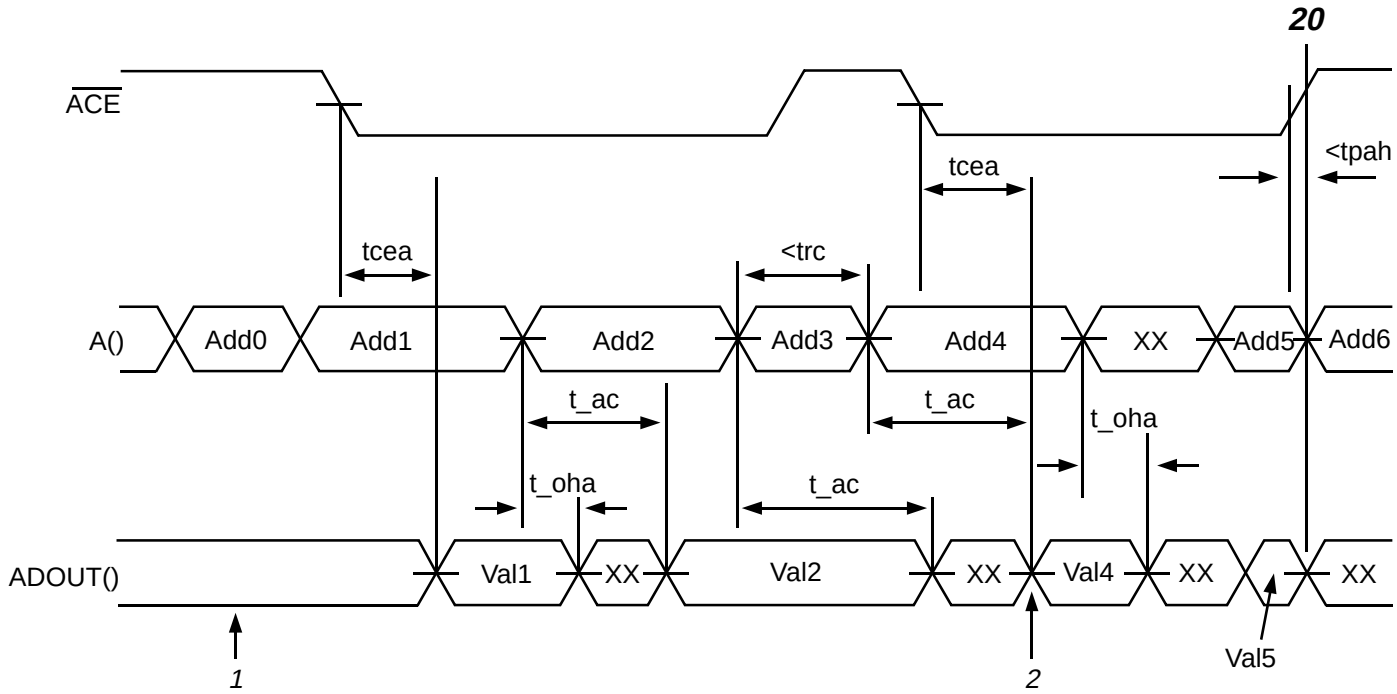


Notes: t_pa : Access time from PD
tpe : PD shutting off to DOUT() Fall
tpw : Minimum pulse width for PD
tpah : Address hold time from APD rising

***2**. Error: Illegal ADP input: ADP "Low" width time smaller than min. tpw.*
***20**. Error: Illegal address input: hold time to ADP is smaller than min. tpah.*

Dual Port RAM 2RW Read Cycle 4

dpram_2rw: AWE = '1', BWE = '1', AOE = '0', BOE = '0'



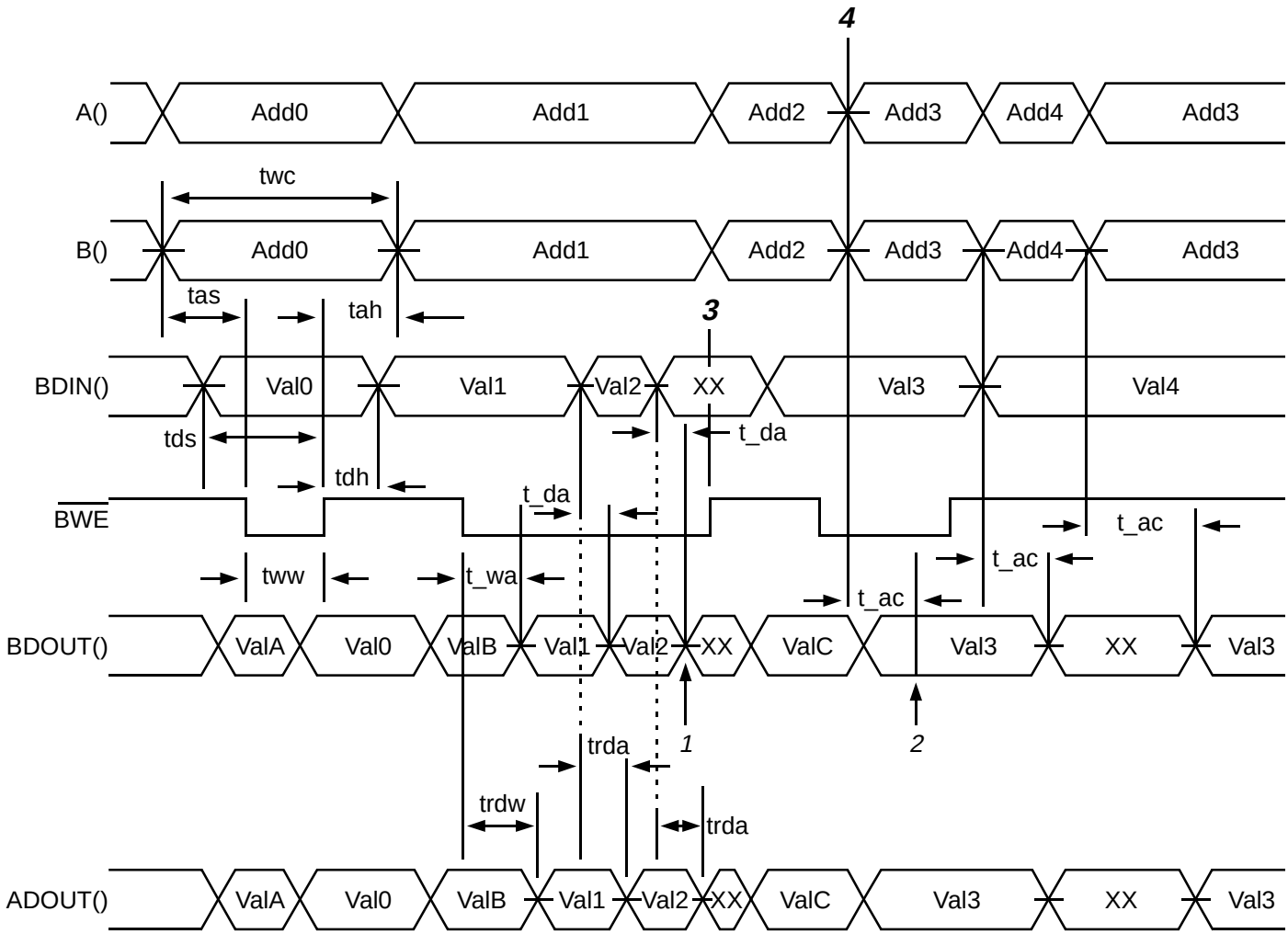
Notes: t_ac : Address access time
tcea : ACE Access Time (maximum Rise/Fall)
tpah : Address hold time from ACE rising
trc : Read Cycle Time
t_oha : Output hold time from address change (minimum of Rise/Fall)

1. Normal DOUT() change due to address change is locked out by 'ACE' pin set to '1'.
2. Output becomes valid after the MAX of t_ac or tcea.
Note that the 'ACE' pin rising does not trigger a RAM access.

***20**. Error: Illegal address input: hold time to ACE is smaller than min. tpah.*

Dual Port RAM 2RW Write Cycle 1

dpram_2rw : AWE = '1', AOE = '0', BOE = '0', ACE = '0', BCE = '0'
dpram_2rw_pd: AWE = '1', APD = '0', BPD = '0'



Notes:
- t_da : Output delay time from Data (t_da<t_ac) (MAX of Rise/Fall)
- t_wa : Output delay time from $\overline{BWE}$ (MAX of Rise/Fall)
- t_ac : Address Access Time (maximum of Rise/Fall)
- trdw : Data access for write-through operation from $\overline{BWE}$ to ADOUT. This time is always longer than t_wa or t_ac
- trda : Output delay from BDIN
- tas : Access setup time
- tah : Address hold time
- tds : Data setup time
- tdh : Data hold time
- tww : Write pulse width low

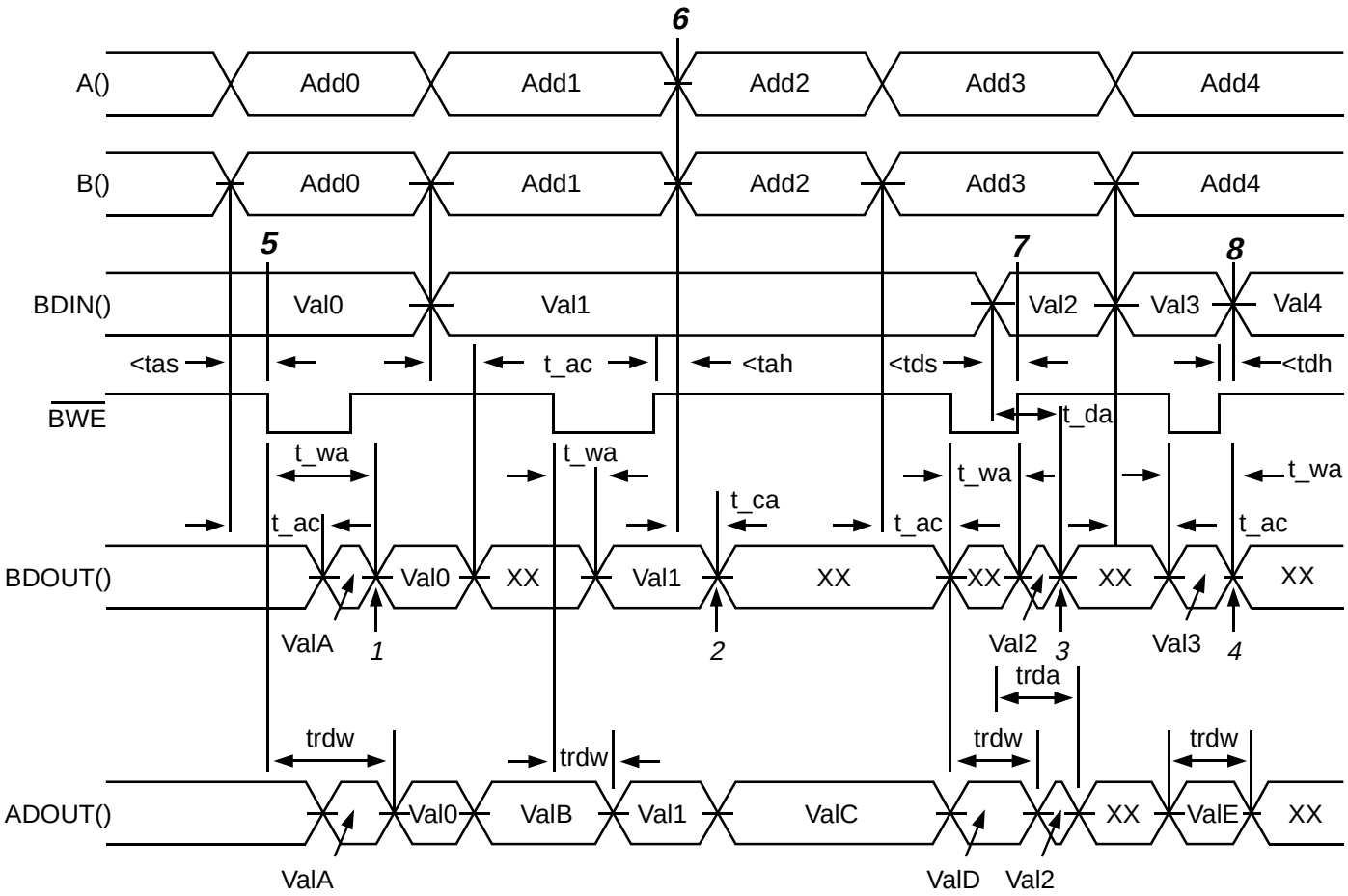
ValA, ValB, and ValC are previously retained in address Add0, Add1, and Add2.

1. Data retained in Add1 is overwritten by 'X' at this time.
2. Data retained in all words is overwritten by 'X' at this time. Writing Val3 into Add3 should be successful.

***3**. Error: Illegal Operation: Data "X" is written at rising edge of $\overline{BWE}$.*
***4**. Error: Illegal Operation: Address was changed while $\overline{BWE}$ low.*

Dual Port RAM 2RW Write Cycle 2

dpram_2rw : AWE = '1', AOE = '0', BOE = '0', ACE = '0', BCE = '0'
dpram_2rw_pd: AWE = '1', APD = '0', BPD = '0'



Notes:
- t_da : Output delay time from Data (t_da<t_ac) (MAX of Rise/Fall)
- t_wa : Output delay time from BWE (MAX of Rise/Fall)
- t_ac : Address Access Time (maximum of Rise/Fall)
- trdw : Data access for write-through operation from BWE to ADOUT. This time is always longer than t_wa or t_ac
- trda : Output delay from BDIN to ADOUT
- tas : Access setup time
- tah : Address hold time
- tds : Data setup time
- tdh : Data hold time

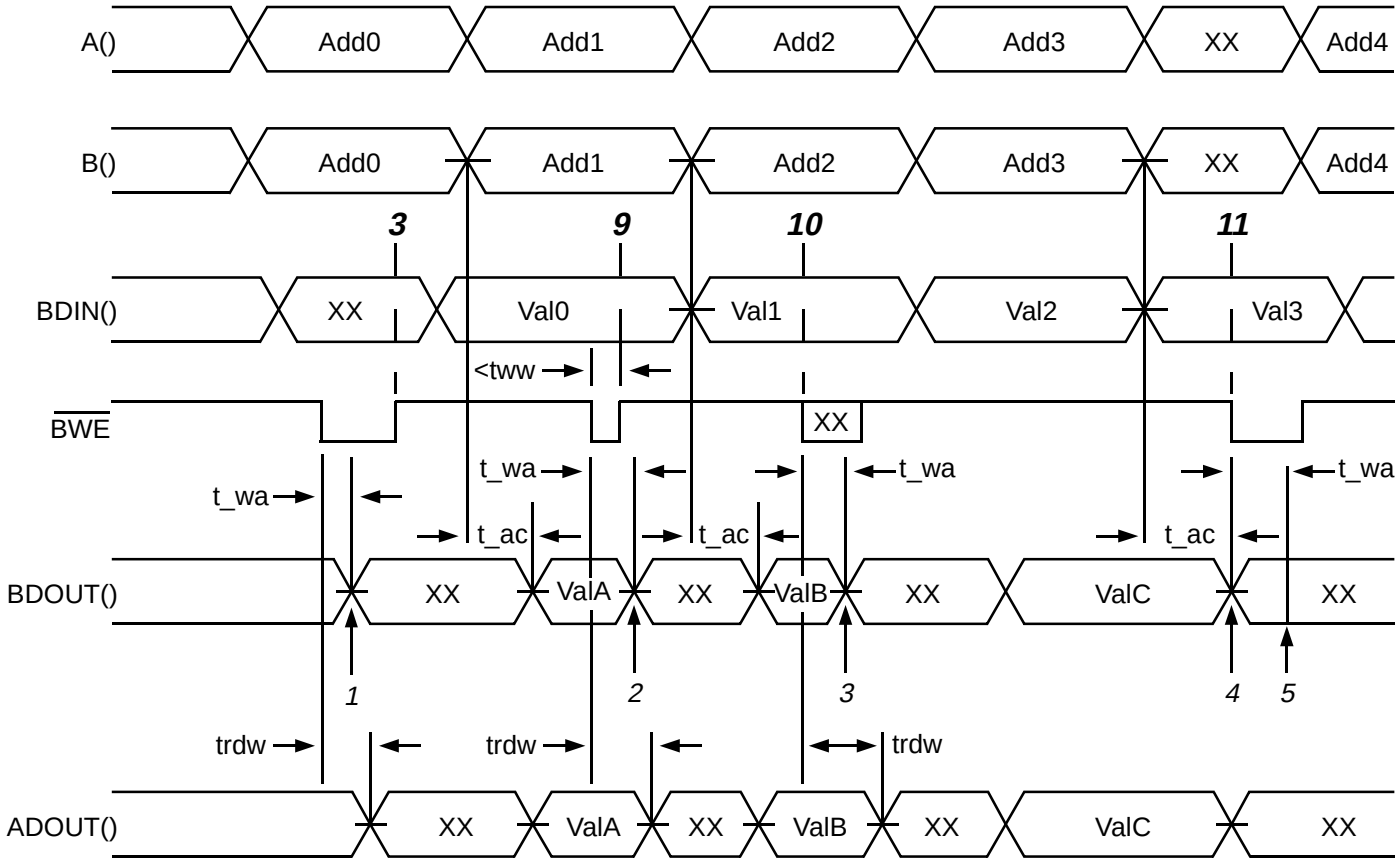
ValA - ValE are previously retained in Add0 - Add4.

1. Data retained in all words is overwritten by 'X' at this time. Writing Val0 into Add0 should be successful.
2. Data retained by all words is overwritten by 'X' at this time.
3. Data retained in Add3 is overwritten by 'X' at this time.
4. Data retained in Add4 is overwritten by 'X' at this time.

***5**. Error: Illegal Address Input: Address Setup time to BWE is smaller than Min tas.*
***6**. Error: Illegal Address Input: Address hold time to BWE is smaller than Min tah.*
***7**. Error: Illegal Data Input: DIN setup time to BWE is smaller than Min tds.*
***8**. Error: Illegal Data Input: DIN hold time to BWE is smaller than Min tdh.*

Dual Port RAM 2RW Write Cycle 3

dpram_2rw : AWE = '1', AOE = '0', BOE = '0', ACE = '0', BCE = '0'
dpram_2rw_pd: AWE = '1', APD = '0', BPD = '0'



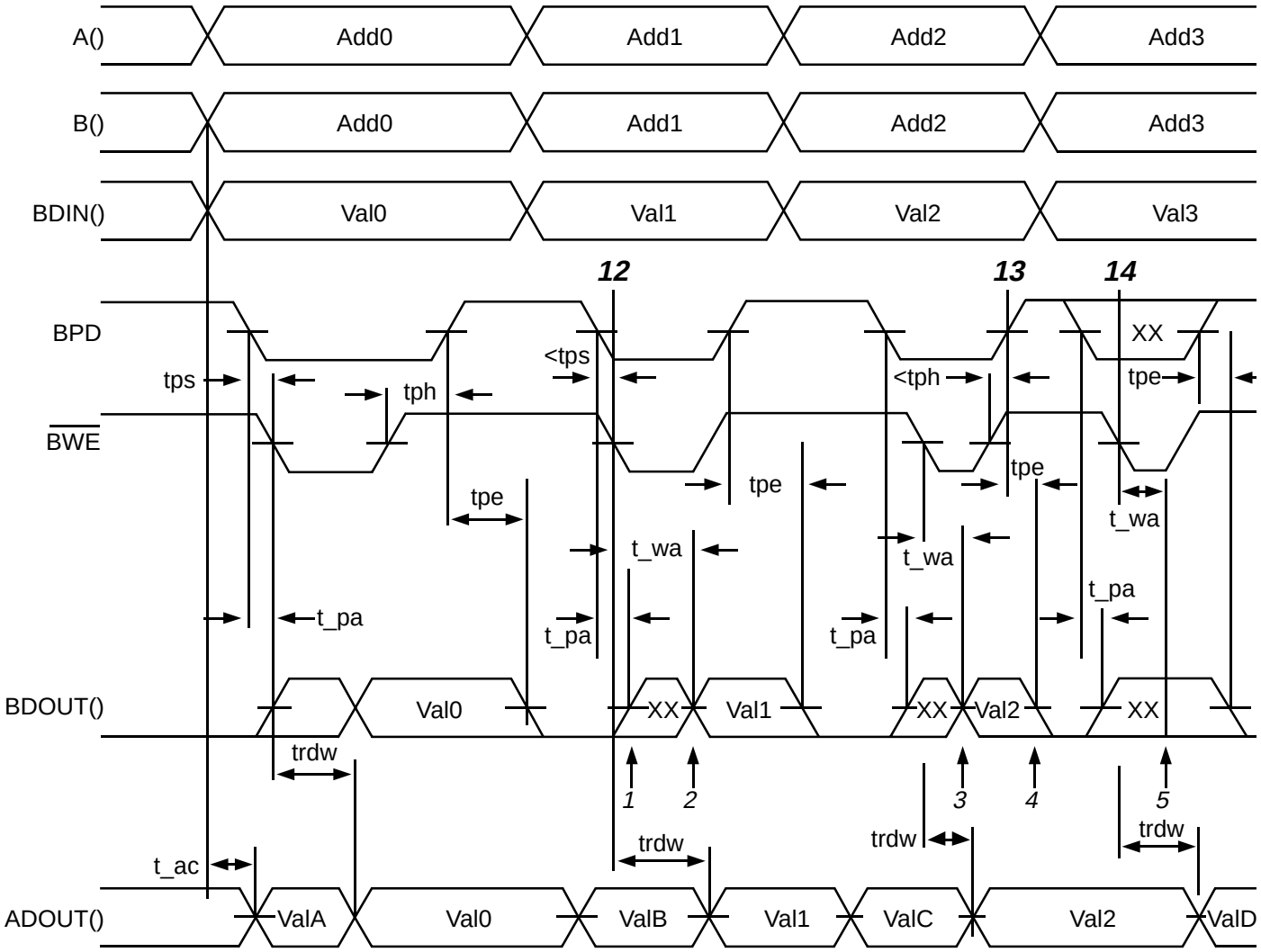
Notes: t_wa: Output delay time from $\overline{WE}$ (MAX of Rise/Fall)
t_ac: Address Access Time (maximum of Rise/Fall)
trdw: Data access for write-through operation from $\overline{BWE}$ to ADOUT. This time is always longer than t_wa or t_ac
tww: Write pulse width low

1. Data retained in Add0 is overwritten by 'X' at this time.
2. Data retained in Add1 is overwritten by 'X' at this time.
3. Data retained in Add2 is overwritten by 'X' at this time.
4. BDOUT() becomes 'X' after t_ac time from leading edge of address 'X'.
5. Data retained in all words is overwritten by 'X' after t_wa time from falling edge of $\overline{BWE}$.

***3**. Error: Illegal Operation: Data "X" is written at rising edge of $\overline{BWE}$.*
***9**. Error: Illegal BWE Input: $\overline{BWE}$ "Low" width time is smaller than Min. tww.*
***10**. Error: Illegal Operation: $\overline{BWE}$ input went to "X".*
***11**. Error: Illegal Operation: Address was "X" at the falling edge of $\overline{BWE}$.*

Dual Port RAM 2RW Write Cycle 4

dpram_2rw_pd: AWE = '1', APD = '0'



Notes: t_ac : Address Access Time (maximum of Rise/Fall)
tps : BCE/BPD setup time (BPD pin used for zero_out function)
tph : BCE/BPD hold time (BPD pin used for zero_out function)
t_wa : Output delay time from WE (MAX of Rise/Fall)
trdw : Data access for write-through operation from BWE to ADOUT. This time is always longer than t_wa or t_ac
t_pa : Access time from BPD
tpe : BPD shutting off to BDOUT() Fall

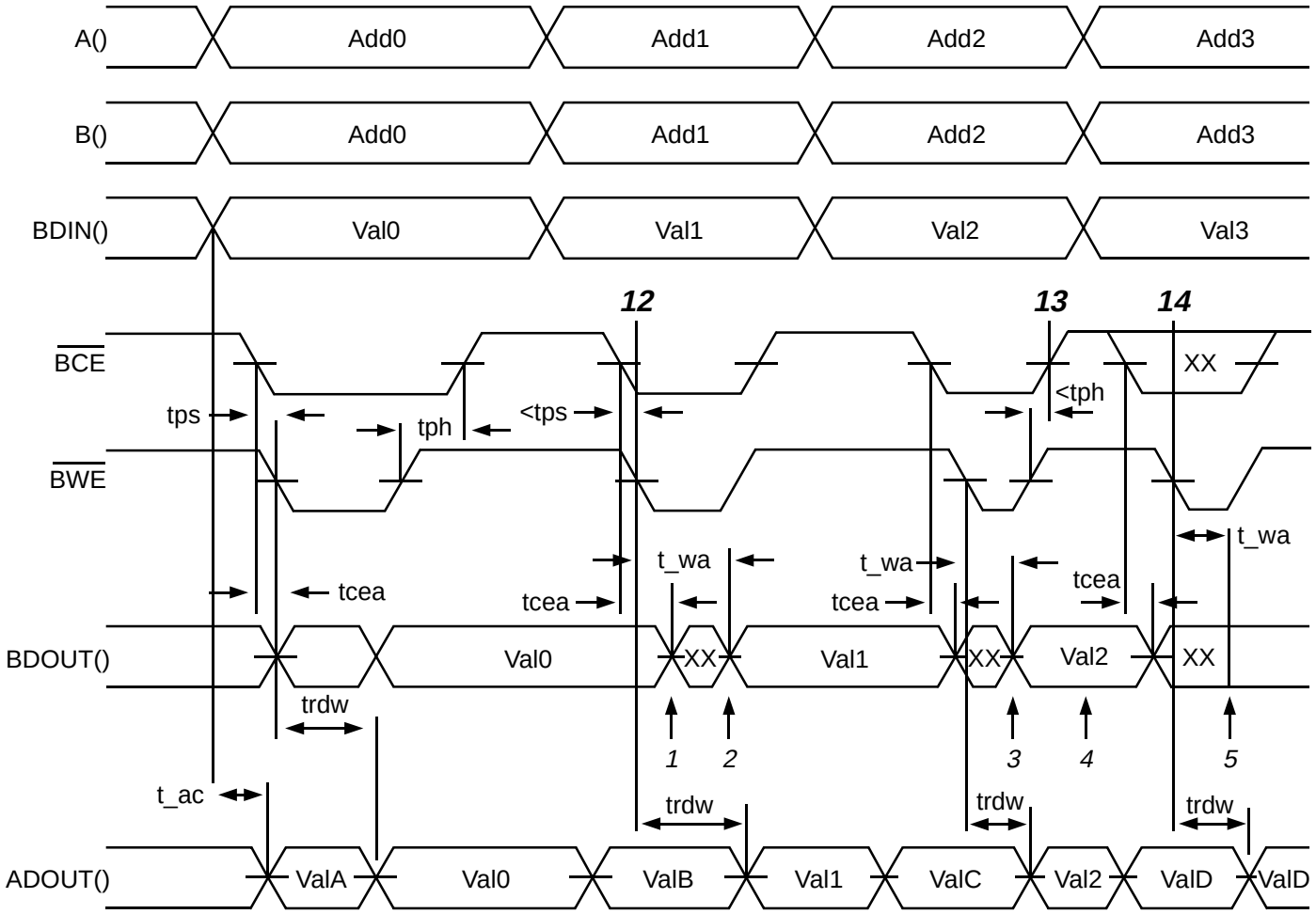
ValA - ValD are previously retained in Add0 - Add3.

1. 4. Data retained in all words is overwritten by 'X' at this time.
2. "X" retained in Add1 is overwritten by Val1 at this time.
3. "X" retained in Add2 is overwritten by Val2 at this time.
5. If data retained in Add3 is not equal to Val3, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***12**. Error: Illegal BCE/BPD Input: BCE/BPD Setup time to BWE is smaller than Min. tps*
***13**. Error: Illegal BCE/BPD Input: BCE/BPD hold time to BWE is smaller than Min. tph.*
***14**. Error: Illegal Operation: BCE/BPD was "X" at the falling edge of BWE.*

Dual Port RAM 2RW Write Cycle 5

dpram_2rw: AWE = '1', ACE = '0', AOE = '0', BOE = '0'



Notes: t_ac : Address access time (maximum of Rise/Fall)
tps : BCE/BPD setup time
tph : BCE/BPD hold time
t_wa : Output delay time from WE (MAX of Rise/Fall)
trdw : Data access for a write-through operation from BWE to ADOUT. This time is always longer than t_wa or t_ac
tcea : Access time from BCE

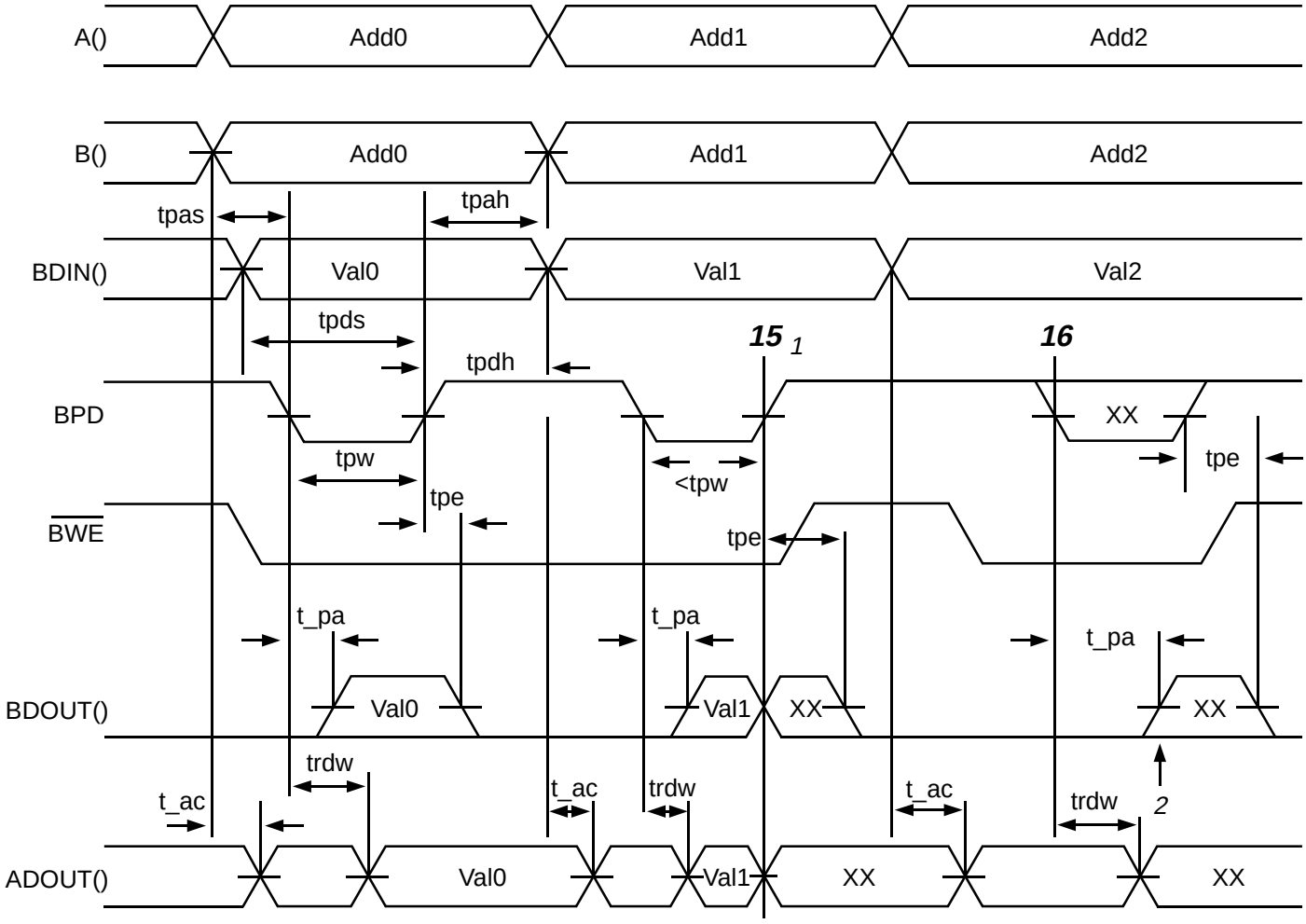
ValA - ValD are previously retained in Add0 - Add3.

1., 4. Data retained in all words is overwritten by 'X' at this time.
2. "X" retained in Add1 is overwritten by Val1 at this time.
3. "X" retained in Add2 is overwritten By Val2 at this time.
5. If data retained in Add3 is not equal to Val3, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***12**. Error: Illegal BCE/BPD Input: BCE/BPD setup time to BWE is smaller than Min. tps.*
***13**. Error: Illegal BCE/BPD Input: BCE/BPD hold time to BWE is smaller than Min. tph.*
***14**. Error: Illegal Operation: BCE/BPD was "X" at the falling edge of BWE.*

Dual Port RAM 2RW Write Cycle 6

dpram_2rw_pd: AWE = '1', APD = '0'



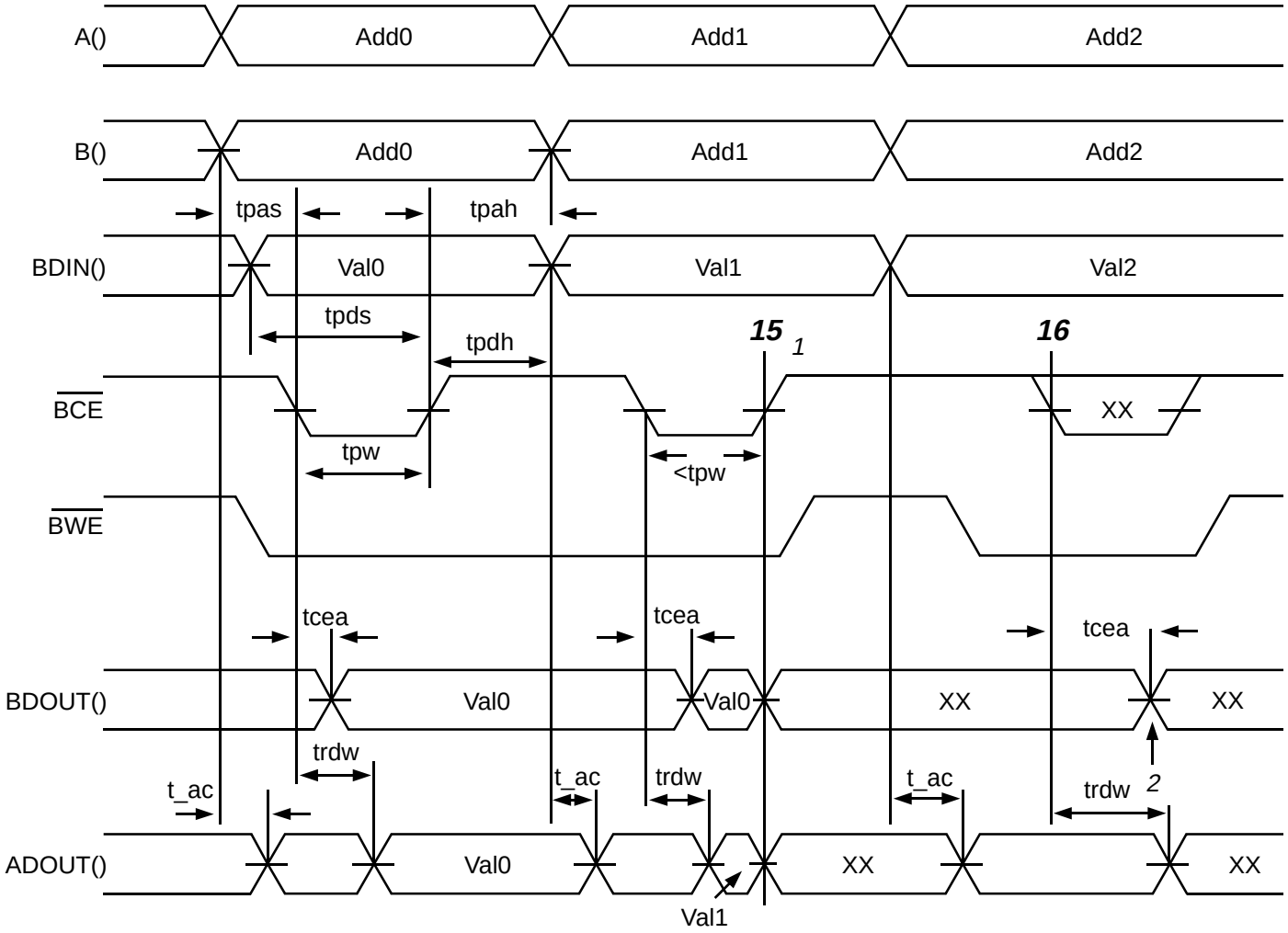
Notes:
- tpas : Address setup time to BPD (BPD pin used for zero_out function)
- tpah : Address hold time to BPD (BPD pin used for zero_out function)
- tpds : Data setup time to BPD
- tpdh : Data hold time to BPD
- t_ac : Address access time
- t_pa : Access time from BPD
- trdw : Data access for write-through operation from $\overline{BWE}$ to ADOUT. This time is always longer than t_ac
- tpw : Minimum pulse width for BPD
- tpe : PD shutting off to BDOUT() Fall

1. If data retained in Add1 is not equal to Val1, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.
2. If data retained in Add2 is not equal to Val2, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***15**. Error: Illegal BPD Input: BPD "Low" width time smaller than Min. tpw.*
***16**. Error: Illegal Operation: BPD went "X" while $\overline{WE}$ is "Low".*

Dual Port RAM 2RW Write Cycle 7

dpram_2rw: AWE = '1', ACE = '0', AOE = '0', BOE = '0'



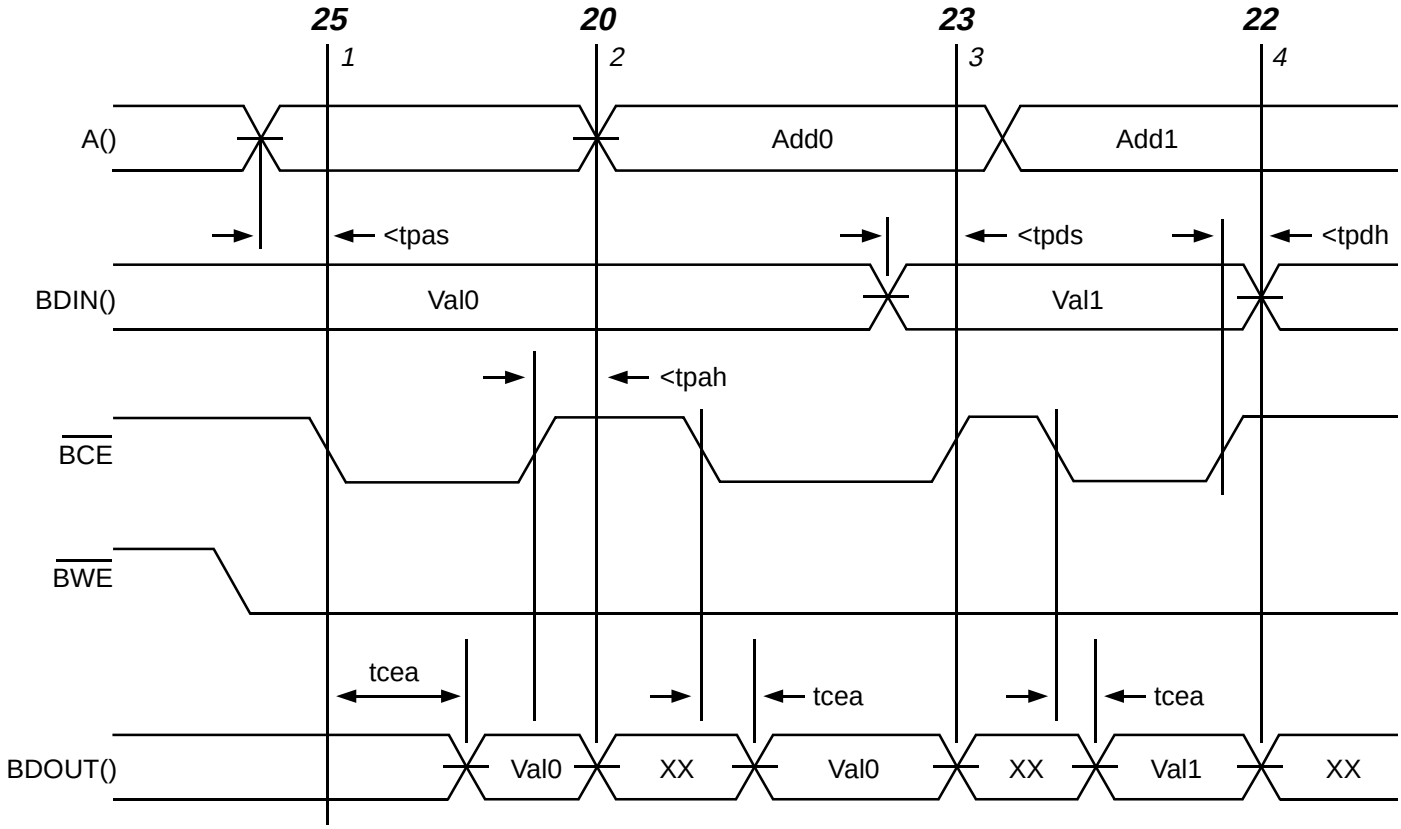
Notes:
- tpas : Address setup time to $\overline{BCE}$
- tpah : Address hold time to $\overline{BCE}$
- tpds : Data setup time to $\overline{BCE}$
- tpdh : Data hold time to $\overline{BCE}$
- t_ac : Address access time
- tcea : Address time from $\overline{BCE}$
- trdw : Data access for write-through operation from $\overline{BWE}$ to ADOUT. This time is always longer than t_ac
- tpw : Minimum pulse width for $\overline{BCE}$

1. If data retained in Add1 is not equal to Val1, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.
2. If data retained in Add2 is not equal to Val2, retained data is overwritten by "X" at this time. If both are identical, retained data is not overwritten by any value.

***15**. Error: Illegal $\overline{BCE}$ Input: $\overline{BCE}$ "Low" width time smaller than Min. tpw.*
***16**. Error: Illegal Operation: $\overline{BCE}$ went "X" while $\overline{WE}$ is "Low".*

Dual Port RAM 2RW Write Cycle 8

dpram_2rw: ACE = '0', AOE = '0', BOE = '0', AWE = '1'



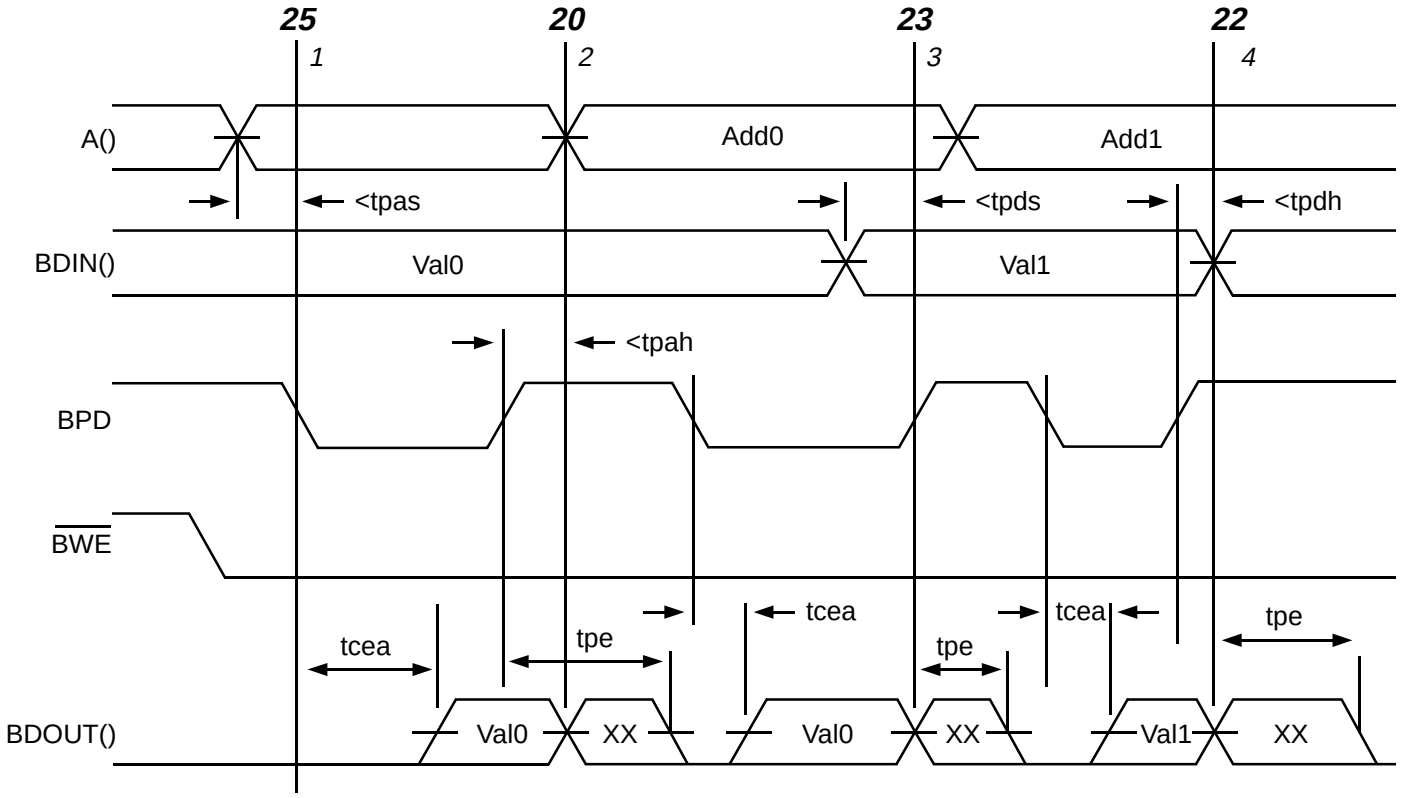
Notes: tpas : Address setup time to $\overline{BCE}$
tpah : Address hold time to $\overline{BCE}$
tpds : Data setup time to $\overline{BCE}$
tcea : BCE access time

1. If tpas is violated, data in all addresses is overwritten by "X" at this time.
2. If tpah is violated, data in all addresses is overwritten by "X" at this time.
3. If tpds is violated, data in Add0 is overwritten by "X" at this time.
4. If tpdh is violated, data in Add1 is overwritten by "X" at this time.

***20**. Error: Illegal address input: hold time to $\overline{BCE}$ is smaller than Min. tpah.*
***22**. Error: Illegal data input: DIN hold time to $\overline{BCE}$ is smaller than Min. tpdh.*
***23**. Error: Illegal data input: DIN setup time to $\overline{BCE}$ is smaller than Min. tpds.*
***25**. Error: Illegal address input: setup time to BCE is smaller than MIn. tpas.*

Dual Port RAM 2RW Write Cycle 9

dpram_2rw_pd: APD = '0', AWE = '1'



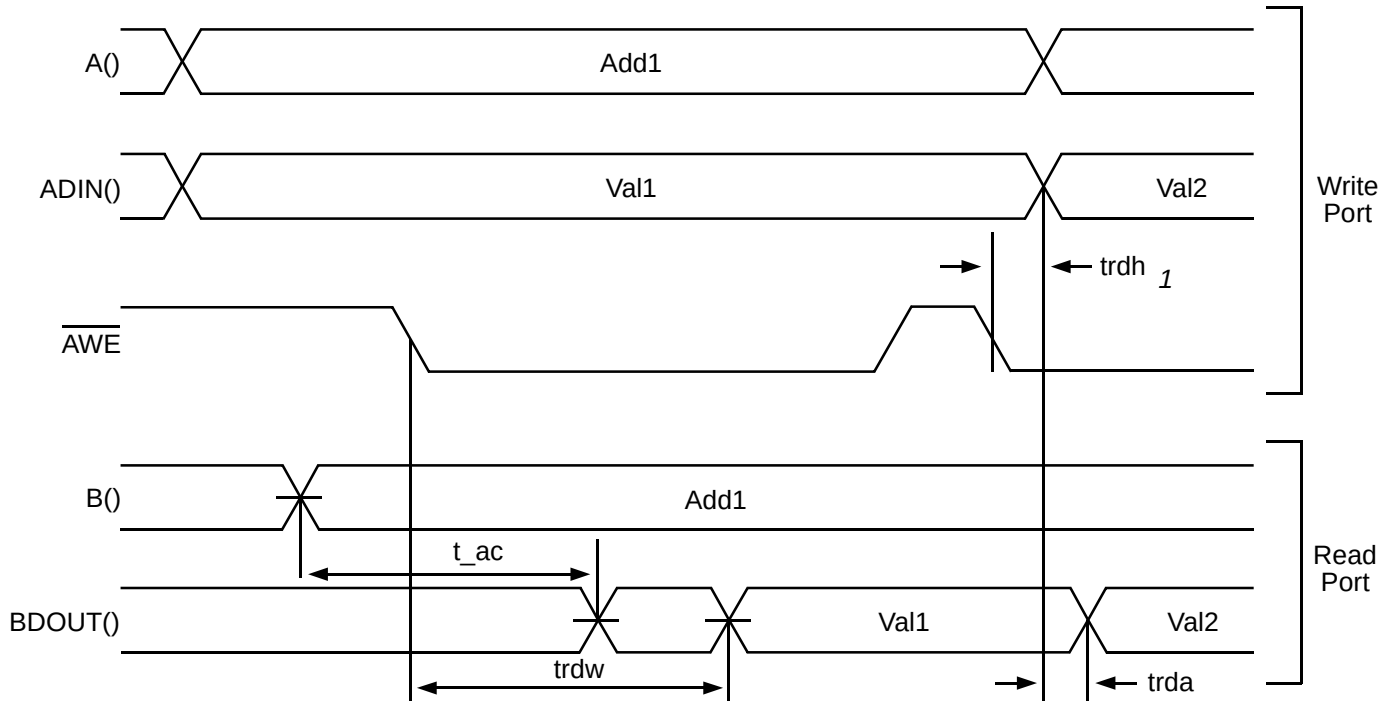
Notes:
- tpe : BPD shutting off to BDOUT() Fall
- tpas : Address setup time to BPD
- tpah : Address hold time to BPD
- tpds : Data setup time to BPD
- tcea : BPD access time

1. If tpas is violated, data in all addresses is overwritten by "X" at this time.
2. If tpah is violated, data in all addresses is overwritten by "X" at this time.
3. If tpds is violated, data in Add0 is overwritten by "X" at this time.
4. If tpdh is violated, data in Add1 is overwritten by "X" at this time.

***20**. Error: Illegal address input: hold time to BPD is smaller than Min. tpah.*
***22**. Error: Illegal data input: BDIN hold time to BPD is smaller than Min. tpdh.*
***23**. Error: Illegal data input: BDIN setup time to BPD is smaller than Min. tpds.*
***25**. Error: Illegal address input: setup time to BPD is smaller than MIn. tpas.*

Dual Port RAM 2RW Write Through

dpram_2rw : BWE = '1', AOE = '0', BOE = '0', ACE = '0', BCE = '0'
dpram_2rw_pd: BWE = '1', APD = '0', BPD = '0'



Notes: t_ac : Address access time
trdw : Data access for a write-through operation from $\overline{AWE}$ to data out. This time is always longer than t_ac
trdh : Data hold from $\overline{AWE}$ rising/falling for write-through
trda : Output delay from ADIN

1. If ADIN change from $\overline{AWE}$ falling edge is greater than trdh, the ADIN change will not propagate through to BDOUT until the rising edge of $\overline{AWE}$.

High Speed ROM

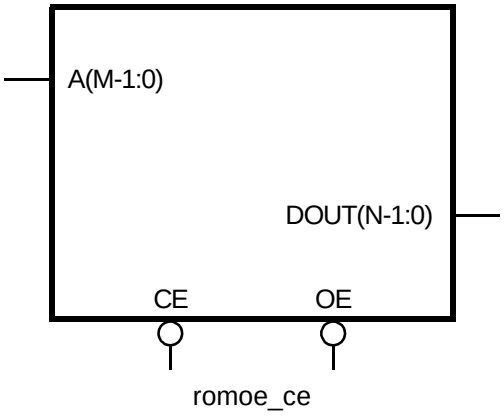
AMERICAN MICROSYSTEMS, INC.

CMOS ASIC Standard Cell Memories

Features

- Maximum of 32K words; 2 MBits
- Word length selectable from 2 to 64 bits per word
- Setup and hold timing constraints on address lines eliminated using combinational address decoding
- Powerdown option minimizes power consumption

Logic Symbol



N = Number of bits per memory word
M = Number of address lines

ROM: High Speed ROM Description

AMI's high speed ROM is built to customer specified parameters including number of bits per word, number of address lines, number of words per module, number of bits per column, tristate output, and power down.

The powerdown option adds a chip enable input (CE), that allows the output to be disabled, minimizing power consumption. CE is independent of output enable (OE). While the ROM is disabled with CE, outputs either go to 1, or are tristated with the optional OE pin.

AMI's ROM has an output enable port when tristate output is selected. When output enable is held high, the output is tristated.

Bits Per Column Options

BITS PER COLUMN	MINIMUM WORDS	MAXIMUM WORDS	ADDRESS INCREMENT
4	64	4096	32
8	64	8192	64
16	512	16384	128
32	512	32768	256

Signal Summary

PORT LABEL	FUNCTION
A(i)	Address input, bit i
OE	Output enable (tristate output buffer)
CE	Chip enable (powerdown)
DOUT(i)	Data output, bit i

Parameters

NAME	DEFINITION	DATA TYPE	VALUES
N	Bits per word	Integer	2-64
WORDS	Number of words	Integer	64-32768
M	Number of address lines	Integer	6-15
CODEFILE	Name of codefile	String	<codefile_name>
BUFFER_SIZE	Buffer size	String	1-4
FREQUENCY	Frequency in MHz	Integer	1-100
VDROP	Voltage drop in millivolts	Integer	1-249

Parts

PART NAME	PINS	OPTIONS	
		TRISTATE	PWR_DOWN
rom	A, DOUT		
romce	A, CE, DOUT		X
romoe	A, OE, DOUT	X	
romoe_ce	A, CE, OE, DOUT	X	X

Truth Tables

With Tristate

A	OE	MODE	DOUT
Addr	0	Read	Data[a]
X	1	High impedance	z

With Powerdown

A	CE	MODE	DOUT
Addr	0	Read	Data[a]
X	1	Pwerdown	All 1’s

With Tristate and Powerdown

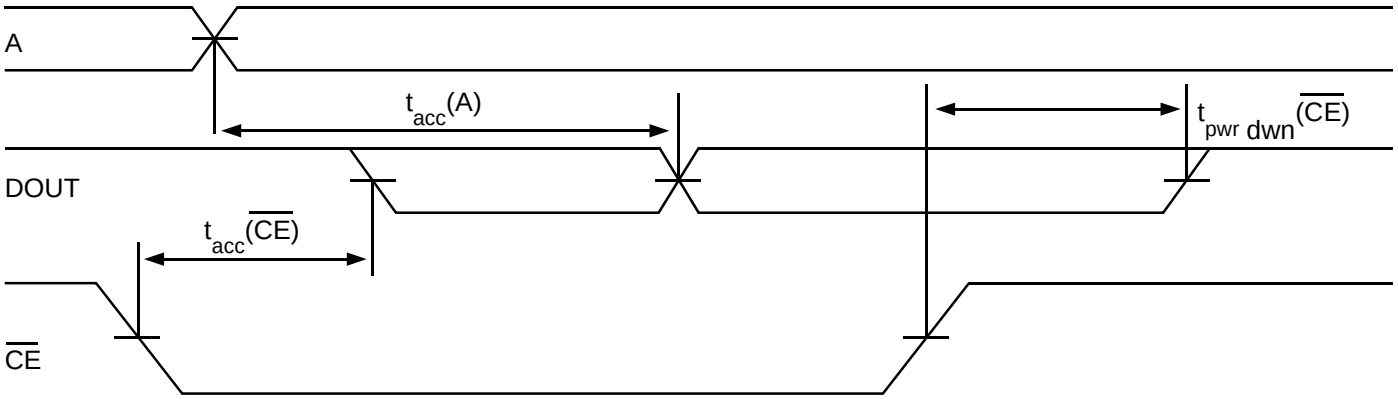
A	CE	OE	DOUT
X	1	1	z
X	1	0	1
X	0	1	z
Addr	0	0	Data[a]

a. Data = stored data

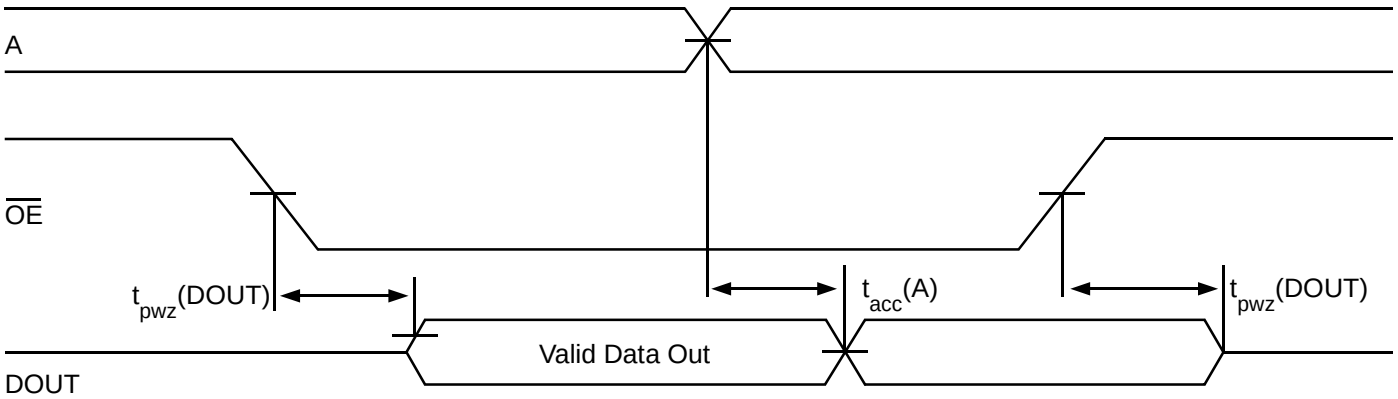
The truth table for the ROM is user-specified.

Figure 1: High Speed ROM Switching Time Waveforms

With Powerdown, Without Tristate



With Tristate, Without Powerdown



Parameters:

t acc (A)	=	Access time
t acc (CE)	=	Power up time
t pwrdwn (CE)	=	Powerdown time
t pzv (DOUT)	=	Transition time for DOUT bus from high impedance to valid data following OE falling edge
t pvz (DOUT)	=	Transition time for DOUT bus from valid data to high impedance following OE rising edge

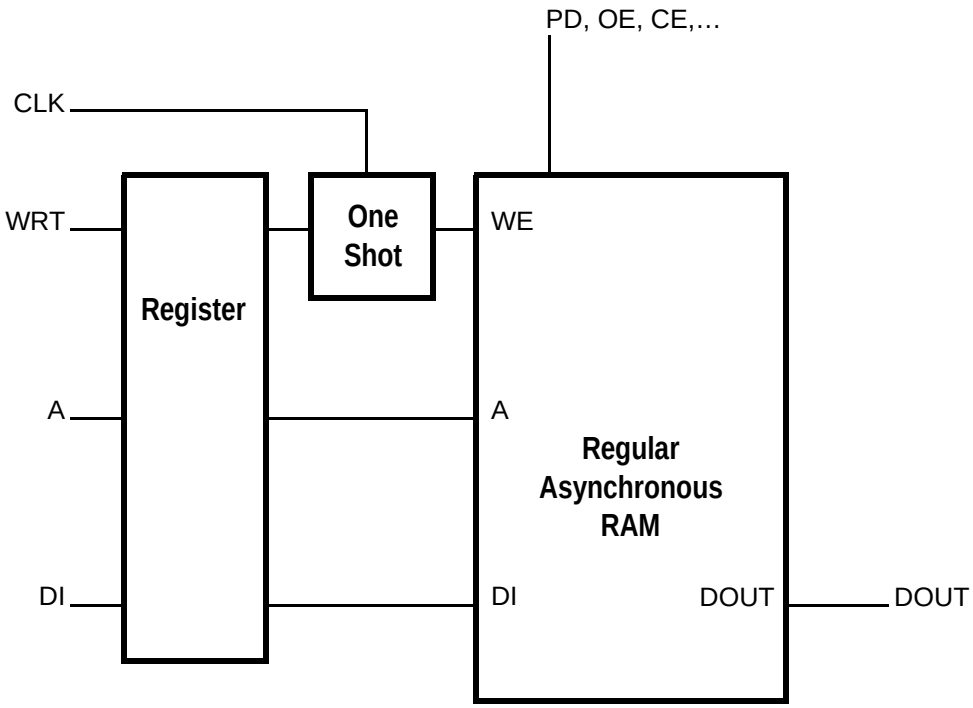
Features

- Makes any AMI asynchronous memory function like a synchronous memory
- Automated process
- Approximate number of equivalent gates per wrap is 50 to 100:
  # of eq. gates = ((# of address and data bits)*3.9) + 17.5

Sync-Wrap Description

A Sync-Wrap (think “shrink-wrap’) is a netlist that instantiates the regular asynchronous memory with extra logic (see Figure below). The memory is ultimately still asynchronous, and all timing requirements to that asynchronous memory still apply. The Sync-Wrap design uses regular logic cells to clock the address inputs, and re-create the “write” pulse on the RAM cells. A CLK signal is used to clock the address lines, and to synchronize the WRT signal. Other control signals (such as PD, CE, etc.) on the asynchronous RAM are pinned out. Carefully use these control signals with regard to the clocked inputs. Use waveform data from original asynchronous RAM, and then consider separately the synchronized inputs.

Sync-Wrap Block Diagram



AMERICAN MICROSYSTEMS, INC.

CMOS ASIC Standard Cell Memories

BIST (Built-In Self Test) Features

- Available for all of AMI's embedded memories
- 100% fault coverage available
- Simplifies test methodologies
- Enables “at speed” testing of memories
- SMarch Test Algorithm
- Adds only a single mux delay
- Configurable for optimal test time
- Requires no external test patterns
- Minimal cost in silicon area
- Shares test hardware when multiple memories on a chip are tested

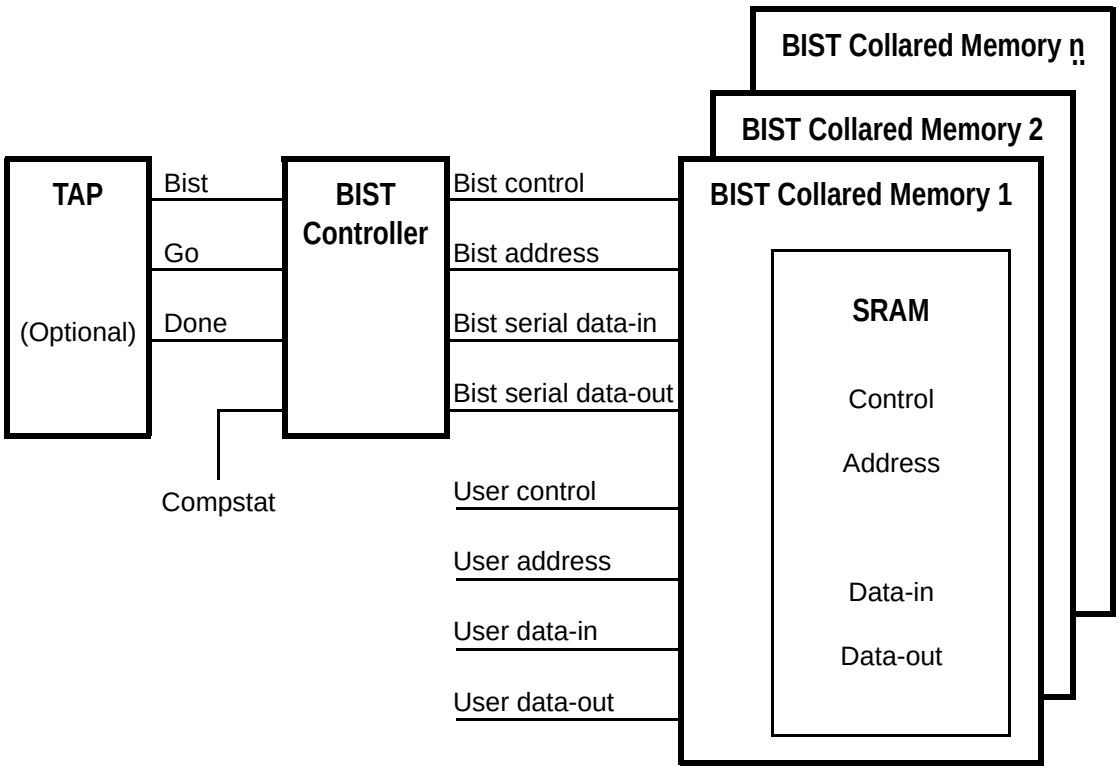
Memory Bist Description

Any of AMI's embedded ASIC memories, including Single and Dual-Port RAM and ROM, can be ordered with BIST (Built-In Self Test). AMI’s BIST data is proprietary and can only be manufactured or used in silicon by AMI. BIST typically uses less than 1500 gates, even when several memories of different sizes are tested. User's can achieve 100% fault coverage in many categories.

The BIST circuitry is a “firm core” (a netlist) of cells from AMI’s library. The customer receives a “testbench” in Verilog or VHDL, with the BIST surrounding the AMI memory models. BIST can also be inserted into a complete design (Verilog or VHDL) which includes AMI memory models.

With memory BIST, stimulus is applied and outputs are evaluated completely within hardware. Following is a block diagram of the memory BIST functionality:

Figure 1: Memory BIST Functionality



BIST Implementation

Files to connect BIST with the memory cells are provided for each system:

- “bist_assembly.vb” file for Verilog.
- “bist_assembly.vhd” file for VHDL.
- “bist_assembly” schematic for some other systems.

This file can be instantiated directly in the design. The BIST controller, the collars, and the memories are included in “bist_assembly” file, with all of the ports needed to access the BIST and the memories. The memory ports in “bist_assembly” are usually listed as “MEM#_portname”, for example MEM0_A15. Different memories are usually listed as MEM0, MEM1, MEM2, etc. A review of the port list will indicate how to hook up the memory signals.

To use BIST, first enable the BIST and supply a BIST_CLK clock signal (See Table) The BIST runs until the “DONE” signal goes high. The “GO” signal indicates if the test passed or failed. (See Figure 2, "BIST Timing", on page 52) MBIST_GO remains high during test mode as long as the memory is functioning properly. When MBIST_DONE goes high, the test is complete, and if MBIST_GO stays high, then the memory or memories have passed the test. If more than one memory is being tested under BIST, MBIST_GO_ID identifies which memory is currently undergoing test. MBIST_GO_ID is usually a bus, and wouldn’t need to be pinned out if there are only a few memories being tested. A “COMP_STAT” signal determines exactly where in the memory a failure occurs. The MBIST_RST_MEM input is used to leave the memory in a “zeroed out” state when the BIST operation is done. If this is not needed, then this pin can be tied low, and does not need to be pinned out. In most cases, BIST_TM and MBIST_EN are tied together. (See Table) If “scan test mode” (logic BIST) is not used, then BIST_TM and MBIST_EN can be tied together.

When BIST is not enabled, the memory is available for regular use. The only performance penalty is a single mux delay on the inputs of the memory.

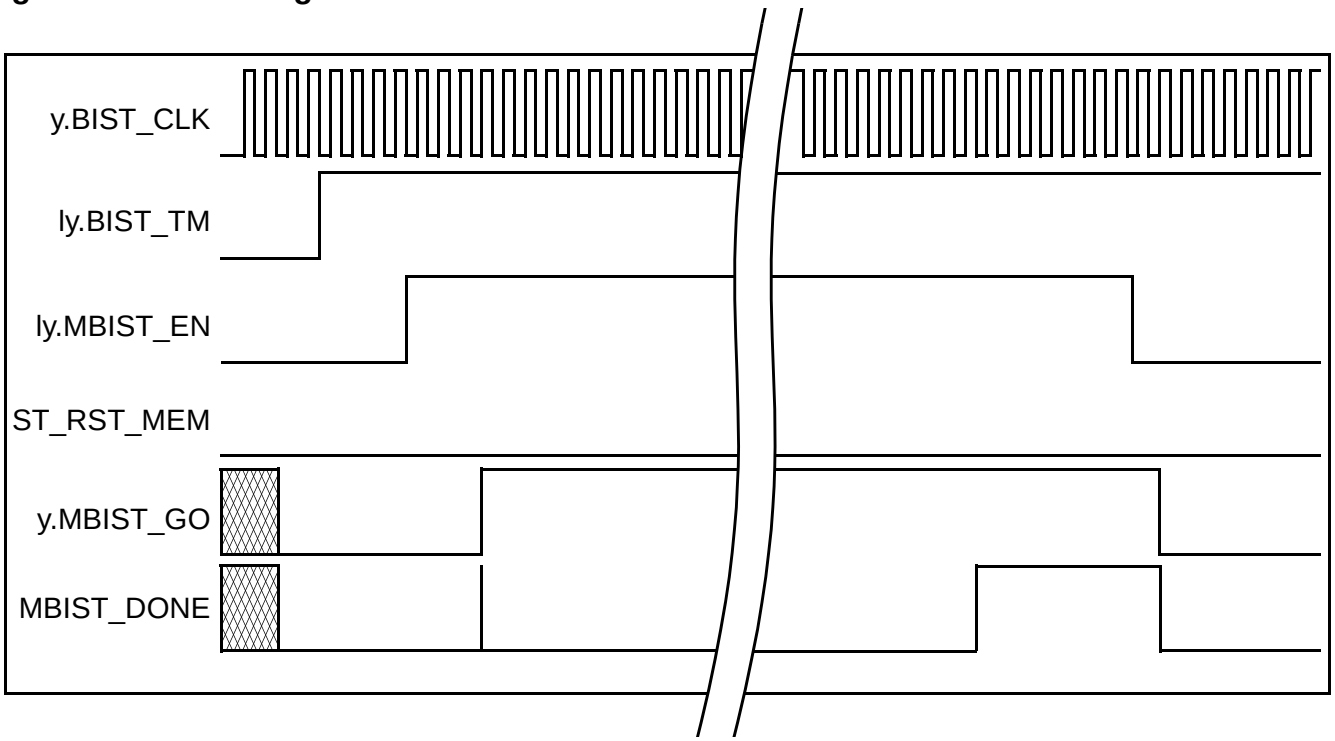
BIST Signals

SIGNAL NAME	TYPE	DESCRIPTION
BIST_CLK	Input	The BIST clock signal
BIST_TM	Input	Test mode, active high
MBIST_EN	Input	Enables the BIST, active high
MBIST_RST_MEM	Input	Resets the memories, active high (option tie low)
MBIST_ON	Output	Goes high when BIST starts (optional)
MBIST_GO	Output	Test result signal
MBIST_GO_ID	Output	Identifies which memory is under test (optional)
MBIST_DONE	Output	Done signal, goes high when BIST is done

BIST Truth Table

BIST_TM	MBIST_EN	MODE
0	0	Regular non-test mode
0	1	Not used
1	0	Scan test mode
1	1	BIST mode

Figure 2: BIST Timing



SMarch Fault Coverage

Using the SMarch algorithm with Memory BIST, the following fault coverage can be achieved:

	FAULT MODEL	BEHAVIOR	SMARCH COVERAGE
SAF	Stuck-At Fault	Cell value always 0 or always 1	100%
SOF	Stuck-Open Fault	Cell inaccessible due to open word line	100%
AF	Address Decoder Faults	Multiple cells accessed from address, multiple addresses access cell	100%
TF	Transition Faults	Cells fail to make 0 to 1 or 1 to 0 transition	100%
CFin	Inversion Coupling Faults	Transition on cell A causes fixed value on cell B	100%
CFid	Idempotent Coupling Faults	Transition on cell A causes fixed value on cell B	100%
CFst	State Coupling Faults	State of cell A forces cell B to a fixed value	100%
DRF	Data Retention Fault	Cell fails to retain value after a period of time	100%
	Write Recovery	Write followed by a read at different locations accesses wrong cell due to timing faults in address decoder	100%
	Multi-Port Faults	Word-line and bit-line shorts between ports	100%
	Destructive Reads	Read access to cell corrupts data	100%

SECTION 7
SALES INFORMATION

AMERICAN MICROSYSTEMS, INC.

Terms Of Sale

1. ACCEPTANCE:

THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold or sold hereunder. Prices for the items called for hereby are not subject to audit.

2. PAYMENT:

(a) Unless otherwise agreed, all invoices are due and payable thirty (30) days from date of invoice. No discounts are authorized. Shipments, deliveries, and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and conditions or security satisfactory to such department.

(b) If, in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.

(c) Each shipment shall be considered a separate and independent transaction, and payment therefore shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer.

3. TAXES:

Unless otherwise provided herein, the amount of any present or future sales, revenue, excise or other taxes, fees, or other charges of any nature, imposed by any public authority (national, state, local or other) applicable to the products covered by this order, or the manufacture or sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof, the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authority.

4. F.O.B. POINT:

All sales are made F.O.B. point of shipment. Seller's title passes to Buyer, and Seller's liability as to delivery ceases upon making delivery of material purchased hereunder to carrier at shipping point, the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Shipments will normally be made by Parcel Post, United Parcel Service (UPS), Air Express, or Air Freight. Unless specific instructions from Buyer specify which of the foregoing methods of shipment is to be used, the Seller will exercise his own discretion.

5. DELIVERY:

Shipping dates are approximate and are based upon prompt receipt from Buyer of all necessary information. In no event will Seller be liable for any re-procurement costs, nor for delay or non-delivery, due to causes beyond its reasonable control including, but not limited to, acts of God, acts of civil or military authority, priorities, fires, strikes, lockouts, slow-downs, shortages, factory or labor conditions, yield problems, and inability due to causes beyond the Seller's reasonable control to obtain necessary labor, materials, or manufacturing facilities. In the event of any such delay, the date of delivery shall, at the request of the Seller, be deferred for a period equal to the time lost by reason of the delay. In the event Seller's production is curtailed for any of the above reasons so that Seller cannot deliver the full amount released hereunder, Seller may allocate production deliveries among its various customers then under contract for similar goods. The allocation will be made in a commercially fair and reasonable manner. When allocation has been made, Buyer will be notified of the estimated quota made available.

6. PATENTS:

The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents, trademarks, or unfair competition arising from compliance with Buyer's designs, specifications, or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements.

Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer, so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information, and assistance (at the Seller's expense) for defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is, in such suit, held to constitute infringement of patent, and the use of said product is enjoined, the Seller shall, at its own expense, either procure for the Buyer the right to continue using said product or part, replace same with non-infringing product, modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. In no event shall Seller's total liability to the Buyer under or as a result of compliance with the provisions of this paragraph exceed the aggregate sum paid by the Buyer for the allegedly infringing product. The foregoing states the entire liability of the Seller for patent infringement by the said products or any part thereof. THIS PROVISION IS STATED IN LIEU OF ANY OTHER EXPRESSED, IMPLIED, OR STATUTORY WARRANTY AGAINST INFRINGEMENT AND SHALL BE THE SOLE AND EXCLUSIVE REMEDY FOR PATENT INFRINGEMENT OF ANY KIND.

7. INSPECTION:

Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at the place of manufacture, such inspection shall be so conducted as to not interfere unreasonably with Seller's operations, and consequent approval or rejection shall be made before shipment of the material. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent. Seller's Return Material Authorization form must accompany such returned material.

8. LIMITED WARRANTY:

The Seller warrants that the products to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES, EXPRESS, STATUTORY, OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, accident, or improper storage. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller.

It is understood that if this order calls for the delivery of semiconductor devices which are not finished and fully encapsulated, then no warranty, statutory, express

or implied, including the implied warranty of merchantability and fitness for a particular purpose, shall apply. All such devices are sold as is where is.

9. PRODUCTS NOT WARRANTED BY SELLER:

The second paragraph of Paragraph 6, Patents, and Paragraph 8, Limited Warranty, above apply only to integrated circuits of Seller's own manufacture. IN THE CASE OF PRODUCTS OTHER THAN INTEGRATED CIRCUITS OF SELLER'S OWN MANUFACTURE, SELLER MAKES NO WARRANTIES, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY, FREEDOM FROM PATENT INFRINGEMENT AND FITNESS FOR A PARTICULAR PURPOSE. Such products may be warranted by the original manufacturer of such products. For further information regarding the possible warranty of such products, contact Seller.

10. PRICE ADJUSTMENTS:

Seller's unit prices are based on certain material costs. These materials include, among other things, gold, packages and silicon. Adjustments shall be as follows:

(a) Gold. The price at the time of shipment shall be adjusted for increases in the cost of gold in accordance with Seller's current Gold Price Adjustment List. This adjustment will be shown as a separate line item on each invoice.

(b) Other Materials. In the event of significant increases in the cost of other materials, Seller reserves the right to renegotiate the unit prices. If the parties cannot agree on such increase, then neither party shall have any further obligations with regard to the delivery or purchase of any units not then scheduled for production.

11. VARIATION IN QUANTITY:

If this order calls for a product not listed in Seller's current catalog, or for a product which is specially programmed for Buyer, it is agreed that Seller may ship a quantity which is five percent (5%) more or less than the ordered quantity and that such quantity shipped will be accepted and paid for in full satisfaction of each party's obligation hereunder for the quantity order.

12. CONSEQUENTIAL DAMAGES:

In no event shall Seller be liable for special, incidental or consequential damages.

13. GENERAL:

(a) The validity, performance and construction of these terms and all sales hereunder shall be governed by the laws of the State of California.

(b) The Seller represents that with respect to the production of articles and/or performance of the services covered by this order it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended, Williams-Steiger Occupational Safety and Health Act of 1970, Section 202 of Executive Order 11246, as amended and where applicable, and other affirmative action requirements made applicable to this order by federal statute, rule or regulation.

(c) The Buyer may not unilaterally make changes in the drawings, designs or specifications for the items to be furnished hereunder without Seller's prior consent.

(d) Except to the extent provided in Paragraph 14, below, this order is not subject to cancellation or termination for convenience.

(e) If Buyer is in breach of its obligations under this order, Buyer shall remain liable for all unpaid charges and sums due to Seller and will reimburse Seller for all damages suffered or incurred by Seller as a result of Buyer's breach. The remedies provided herein shall be in addition to all other legal means and remedies available to Seller.

(f) Buyer acknowledges that all or part of the products purchased hereunder may be manufactured and/or assembled at any of Seller's facilities domestic or foreign.

(g) Unless otherwise agreed in a writing signed by both Buyer and Seller, Seller shall retain title to and possession of all tooling of any kind (including but not limited to masks and pattern generator tapes) used in the production of products furnished hereunder.

(h) Buyer, by accepting these products, certifies that he will not export or re-export the products furnished hereunder unless he complies fully with all laws and regulations of the United States relating to such export or re-export, including but not limited to the Export Administration Act of 1979 and the Export Administration Regulations of the U.S. Department of Commerce.

(i) Seller shall own all copyrights in or relating to each product developed by Seller whether or not such product is developed under contract with a third party.

(j) The design, development or manufacture by Seller of product for a specific customer shall not be deemed to produce a work made for hire and shall not give to the customer any copyright interest in the product or any interest in all or any portion of the mask works relating to the product. In addition, all such rights shall remain the property of Seller. Seller shall retain all rights in mask work on any circuit designed using Seller's standard cell library and Seller shall retain all rights in mask work to the non-personalized portion of any gate array developed for Buyer.

(k) Engineering work performed by Seller of any kind, including but not limited to, development of test programs, shall only be on a best efforts basis.

14. GOVERNMENT CONTRACT PROVISIONS:

If Buyer's original purchase order indicates by contract number that it is placed under a government contract, only the following provisions of the current Federal Acquisition Regulations are applicable, in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be – i.e., "Contracting Officer" shall mean "Buyer," "Contractor" shall mean "Seller," and the term "Contract" shall mean this order:

52.202-1 Definitions; 52.232-11 Extras; 52.212-9 Variation in Quantity; 52.232-23 Assignment of Claims; 52.228-2 Additional Bond Security; 52.224-11 Certain Communist Areas; 52.222-4 Contract Work Hours and Safety Standards Act-Overtime Compensation; 52.222-20 Walsh-Healey Public Contracts Act, if this Order exceeds $10,000; 52.222-26 Equal Opportunity; 52.203-1 Officials Not to Benefit; 52.203-5 Covenant Against Contingent Fees; 52.249-1 Termination for Convenience of the Government if this Order does not exceed $500,000 (only to the extent that Buyer's contract is terminated for the convenience of the government); 52.246-1 Contractor Inspection Requirements; 52.247-1 Commercial Bills of Lading; 52.222-35 Affirmative Action Viet Nam Veterans if this Order exceeds $10,000; 52.222-36 Affirmative Action Handicapped Workers, if this Order exceeds $2,500; 52.222-1 Notice to the Government of Labor Disputes; 52.215-1 Examination of Records by Comptroller General; 52.220-3 Utilization of Labor Surplus Area Subcontracting Concerns.

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