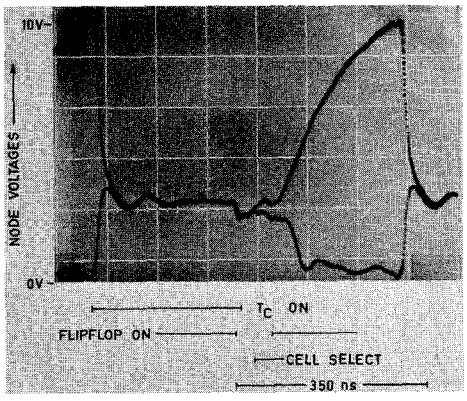

Fig. 12. Node voltages of a flip-flop realized in n-silicon-gate technology during a READ/REWRITE cycle [cf. Fig. 10(a)].

area of 1450 μm^2 could be operated in the same way. This confirms the value of the stet V_{tr} of the undefined region of the sense/refresh amplifier, estimated to be 0.6 V in this circuit. To get a more representative and reliable value of V_{tr}, yield and stability investigations need to be done.

Conclusion

It has been shown that the use of a gated flip-flop as a sense/refresh amplifier and memory cells with inversion-layer storage capacitors in standard silicon-gate technology eliminates the major disadvantages of single-transistor memory cells.

Realizing a 4096-bit chip with the present 1600-μm^2 cells would require a chip size of the order of 4 × 4.5 mm. For this chip an access time of about 250 ns and a cycle time of 350 ns are estimated. The cycle time includes the precharge of the digit lines and dummy cells, which is done simultaneously, as well as the sensing and rewriting.

Further development towards finer structures will yield smaller cell areas down to 625 μm^2 (1 mil^2) for structures characterized by 5-μm aluminum line width and line separation. With the storage density achieved thereby the 1-kbyte RAM chip seems feasible.

Acknowledgment

The authors would like to express their appreciation to M. Leitmeir and G. Lindert for their assistance in the design and the electrical measurements and to H. Friedrich for the n-silicon-gate processing.

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Merged-Transistor Logic (MTL)—A Low-Cost Bipolar Logic Concept

HORST H. BERGER AND SIEGFRIED K. WIEDMANN

***Abstract*—This paper describes a novel bipolar logic featuring a direct injection of minority carriers into the switching transistor. Since this concept utilizes merged complementary transistors, it has been named merged-transistor logic (MTL). The fabrication process is as simple as that of single transistors, requiring only four mask steps through metalization. MTL is based on inverters having decoupled multicollector outputs for the logical combinations. The devices are self-isolated and no ohmic load resistors are required. This is a key to monolithic logic chips of very high functional density and low power dissipation. On experimental chips an excellent power-delay product of 0.35 pJ has been measured. These experiments show that a density of 100 gates/mm^2 can be achieved with present manufacturing tolerances (minimum dimensions: 0.3-mil metal line width, 0.15-mil spacing, 0.2 × 0.2-mil^2 contact holes). Level compatibility with transistor-transistor logic (T^2L) logic, good driving capability, and high noise immunity are further advantages over present FET approaches.**

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I. Introduction

IN ORDER to exploit the bipolar potential for low-cost logic, new concepts are needed that allow higher functional densities but require fewer process steps [1], [2] than presently used. This paper describes a novel bipolar logic featuring a direct injection of minority carriers into the switching transistor. Since this concept utilizes merged complementary transistors, it has been named merged-transistor logic (MTL).

With MTL, the device isolation problem is totally eliminated. The process becomes as simple as that of single transistors, requiring only four mask steps through metalization. The device's self-isolation and the complete omission of ohmic resistors are the key for the high functional density. From our experimental chips we can project a density of about 100 gates/mm^2 with present manufacturing tolerances. Despite the simple technology, an excellent power-delay product of 0.35 pJ has been measured.

After explaining the basic logic structure and operation some pertinent device parameters are discussed based on theoretical investigations and measured data. Experimental results obtained from small logic blocks are presented to verify the improvements in power × delay product, density, and process simplicity.

II. Basic MTL Structure and Operation

MTL can be plainly derived from the principal circuit schematic shown in Fig. 1. It shows an implementation of the logic NOR function which, as is well known, can be used for realizing any kind of complex logic. This circuit resembles dc-transistor logic (DCTL) or resistor-transistor logic (RTL) [3], but fundamentally differs in the current supply mode. Each switching transistor in Fig. 1 is provided with an individual current supply at the base terminal, whereas in a DCTL gate the supply element is associated with the collectors. As in DCTL, the gate consists of inverter transistors that are dotted at their outputs to logically combine the input signals A and B. The output delivering the function $\overline{A + B}$ is connected to several succeeding inverter inputs. The logic levels are about the same as in DCTL.

Since the emitters of all n-p-n transistors are tied to a common reference potential (which is normally ground), they should be implemented in a common n plane to achieve a high density. In terms of a standard bipolar structure, it means to employ common-collector n-p-n transistors and to operate them upside down, so that the former collector region becomes the emitter. This has been done in MTL and, therefore, we shall refer to this operation mode as the normal mode here.

The current source I_B in Fig. 1 provides the drive current for the transistor switch and the charge current for the circuit capacitances. An obvious but not attractive realization of the current source would be an ohmic resistor tied to a positive voltage supply. However, the required current supply to the base of the n-p-n transistor can also be attained through a collection of excess minority carriers generated in the vicinity of the emitter–base junction as illustrated in Fig. 2. These excess minority carriers can be generated, e.g., by a hole injection from a p emitter in the common n-emitter region [4], [5].

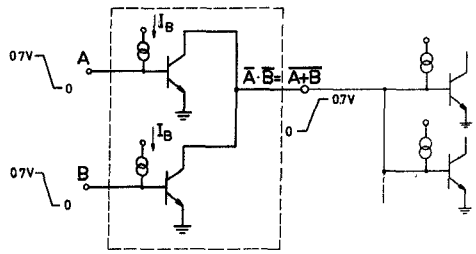


Fig. 1. NOR circuit.

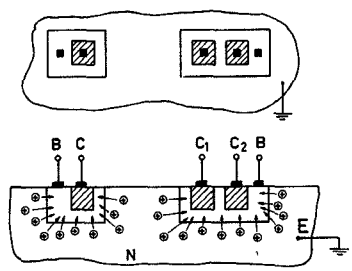
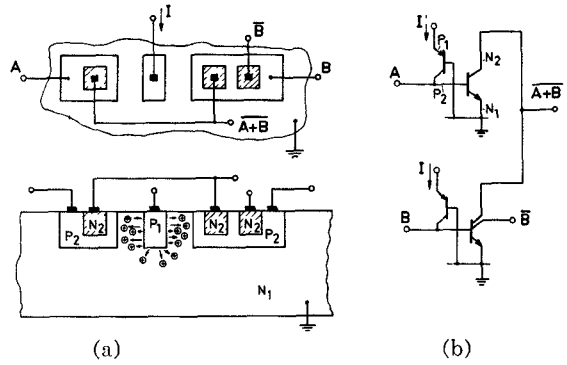


Fig. 2. Base current by minority carrier collection.

A practical solution in a readily available technology is shown in Fig. 3, together with the equivalent circuit. The p_1 emitter provides the minority carrier injection into the n_1 region, where most of them are collected by the adjacent p_2 regions. Hence, the p_1-n_1-p_2 structure forms a lateral grounded-base p-n-p transistor, which is here represented in the equivalent circuit. Instead of the lateral p-n-p configuration, a vertical structure may be used as well, for instance by choosing a p substrate for the carrier injection. The p-n_1-p transistor has now replaced the current source in the equivalent circuit of Fig. 1. The n-p-n transistor with emitter n_1, base p_2, and collector n_2 is operated upside down as explained earlier. Since the n_1 and p_2 regions are commonly used by both transistors, we end up with a merged transistor structure having very few metal interconnections. This is a key for the high functional density of MTL.

Because of the excellent tracking of the emitter–base voltages on a chip,[1] the p-emitter regions p_1 are fed in parallel. As shown in Fig. 4(a), the p emitters may be connected directly to a chip pad and supplied by an external current source I_0, resulting in a chip voltage of about 0.8 V. However, a common series resistor R_V con-

[1] First measurements on parallel p-n-p transistors on the same chip have shown a collector current variation of less than ±15 percent.



(a) (b)

Fig. 3. (a) Principal MTL structure. (b) Equivalent circuit.

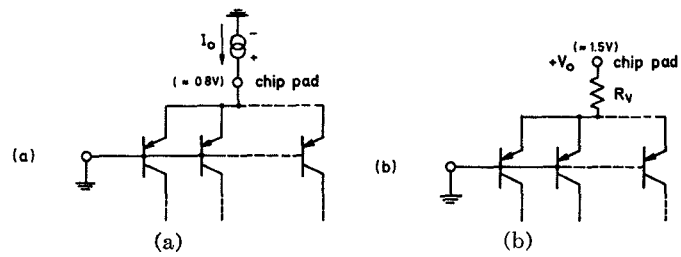


Fig. 4. Principal methods of supplying power to MTL chip. (a) External current supply. (b) External voltage supply.

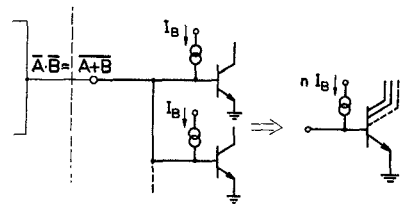


Fig. 5. MTL multicollector inverter as logic element.

nected to an external voltage supply V_0 can be used as well [cf. Fig. 4(b)]. This resistor can be implemented by the n-diffusion used for the n-p-n collectors. The currents of the MTL gates can be adjusted by the sizes of the p-n-p and n-p-n transistors in order to obtain different delay times or driving capabilities on the same chip.

After having discussed the MTL principle more from a circuit and device point of view, we will briefly characterize MTL from a logic systems aspect. This may better illustrate the differences to presently known logic.

Looking back to Fig. 1, one recognizes that an MTL gate output, the bases of the succeeding inverters are tied together. This leads to a multicollector structure as shown in Fig. 5. Thus, MTL basically consists of inverters with one input (base terminal) and several outputs (multicollectors). Of course, two or more inverters can be connected in parallel if the number of collectors is not sufficient. By dotting the collector outputs of different inverters, the NOR function is realized. Compared to standard NOR logic, the number of collectors of one dot corresponds to fan-in and the number of collector outputs of one inverter to fan-out. Hence, the logic flexibility of MTL is comparable with that of other bipolar logic circuits.

In addition, it should be pointed out that MTL fits well into an economical array layout scheme as proposed by Weinberger [6]. Fig. 6(a) shows as an example the principal layout of a three-address decoder. A similar layout configuration would result for an MTL read-only memory. If necessary, the series resistance of long p stripes can be effectively reduced by shunting low-ohmic n^+ stripes as illustrated in Fig. 6(b).

III. Interfacing

So far, the advantages of MTL have been shown for realizing logic systems on chip level. But MTL can also cope economically with the system environment as shall be discussed below.

Main problems are noise at the input and driving capabilities at the outputs having loads by orders of magnitude larger than the circuits inside the chip.

The noise immunity of a logic circuit is not only determined by the voltage thresholds but also by the energy necessary for switching the gate. This energy is rather high, since all nodes are at low impedance level. The more noise-endangered input stages can be operated at a higher power level in order to further increase their energy threshold. As already mentioned previously, this can be achieved by properly adjusting the MTL device size for a higher injection current and thus making it noise insensitive.

The problem of driving heavy output loads can be solved the same way; if necessary, two or more stages may be put in series for scaling up the power in steps. Furthermore, the output voltage swings can be made larger than the swing of about 0.7 V inside the chip by choosing a proper load supply. In this context, MTL has similar characteristics as T^2L since both circuits use a grounded-emitter output transistor having good driving capability, the swing can be adjusted by choosing the appropriate output voltage supply and load resistors. From these common features with T^2L it also becomes evident that the MTL logic levels are compatible with those of T^2L-type logic circuits being widely used in present low-cost systems. Thus usually no level converters would be required.

IV. Pertinent MTL Device Characteristics

In the foregoing section the basic structure and operation of MTL have been discussed without going into details on the device characteristics. Concluding from experience with conventional monolithic logic circuits, three basic questions would arise with MTL.

1) What factors determine the current gain in an n-p-n transistor operated upside down?

2) What is the influence of the "partially saturated" grounded-base p-n-p transistors on the supply current distribution?

3) Are there current hogging effects [7] in the parallel

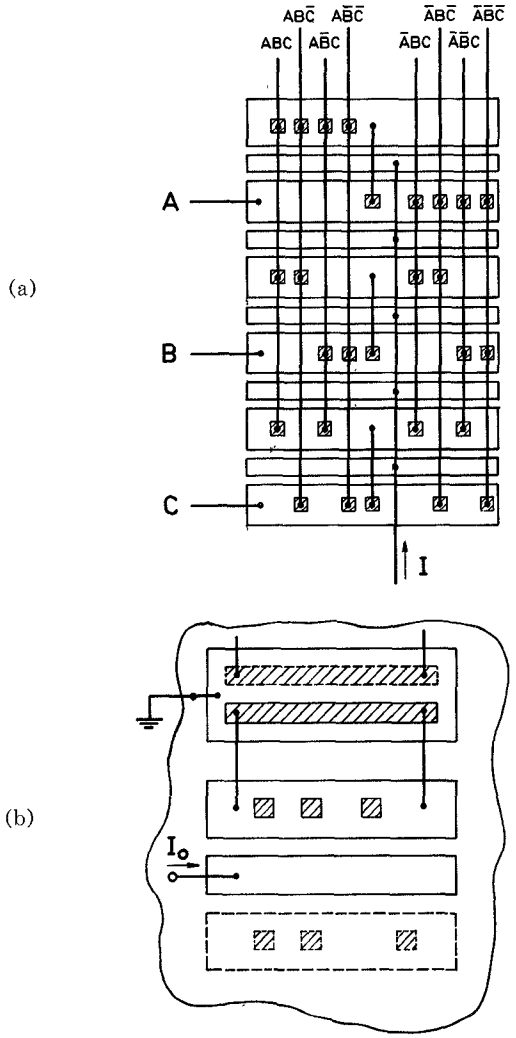


Fig. 6. (a) Schematic MTL array layout showing 3-bit decoder. (b) Example of low-ohmic bypass resistor.

grounded-emitter n-p-n transistors (equivalent to multicollector transistors) owing to saturation?

In the discussion on the n-p-n transistor current gain β_n, it will be shown that the question of the supply current sharing in partially saturated p-n-p transistors becomes irrelevant owing to a suitable definition of β_n. The current hogging of the parallel n-p-n transistors will be demonstrated to be insignificant because of the inherently high inverse current gain of the upside-down-operated transistors.

When the emitter–base junction n_1-p_2 of the n-p-n transistor in the MTL device [Fig. 7(a)] is forward biased, electrons are injected into the p_2 region, holes into the n_1 region. These injections may be portioned and then be represented by adequate diodes as indicated in Fig. 7(b). Specifically, the electron injection into section 1–1 has been symbolized by the emitter–base diode of an ideal n-p-n transistor T_1, assuming a total collection of the electrons by region n_2. Similarly the hole injection into section 2–2 has been represented by an ideal p-n-p transistor T_2.

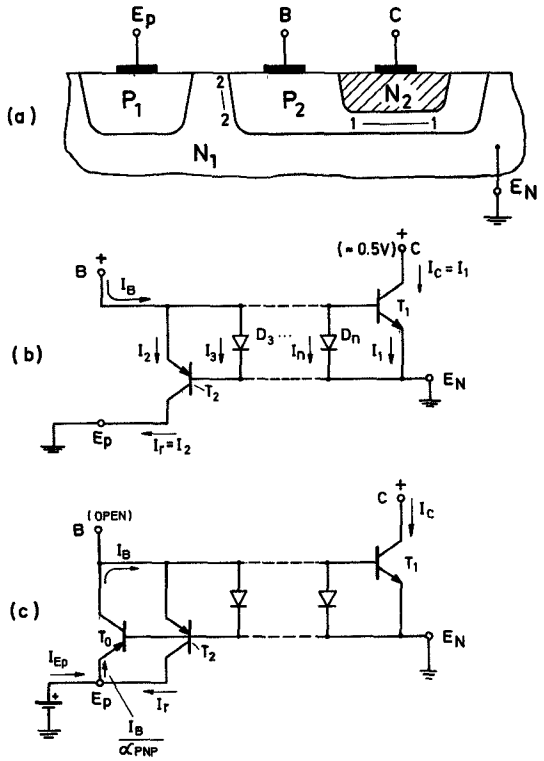


Fig. 7. (a) Cross section showing injection regions for equivalent circuit. (b) Equivalent circuit of n-p-n transistor operated upside down. (c) Equivalent circuit of MTL device.

The current gain $\beta_n = I_c/I_B$ of the extrinsic n-p-n transistor (terminals E_N, B, C) shall be measured with E_p grounded. Obviously, to obtain a large current gain β_n, the parasitic diode currents $I_2 \cdots I_n$ must be kept small compared to current I_1 of the intrinsic transistor T_1. This ratio

$$\beta_n = I_1 \Big/ \sum_{\nu=2}^{n} I_\nu \tag{1}$$

not only depends on the individual doping and area ratios (which are usually adverse for such a structure), but on the ratio of effective diffusion lengths of the minority carriers as well. This explains why even with the standard buried layer structure, current gains $\beta > 10$ are observed. Furthermore, it should be mentioned that an n^+ collar around the base helps to reduce the parasitic diode current.

Defining the current gain β as above with E_p grounded [Fig. 7(b)], the problem of current sharing in the p-n-p transistors supplied in parallel becomes more transparent for circuit calculation. One may assume that on an MTL chip having many gates, the number of ON and OFF n-p-n transistors is always about equal. Therefore, the common emitter–base voltage V_{EB} is constant for a given supply current. Fig. 7(c) illustrates this condition of constant V_{EB} on a single MTL device. The lateral p-n-p transistor is represented by the superposition of an active forward-

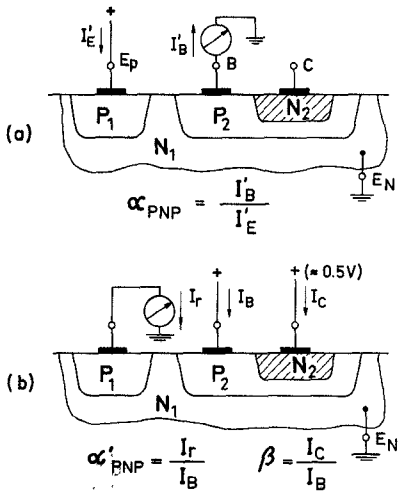


Fig. 8. (a) Definition and measurement of common-base current gain $\alpha_{p\text{-}n\text{-}p}$ of p-n-p current source transistor. (b) Definition and measurement of common-emitter current gain β_n of n-p-n transistor and of recollection factor $\alpha'_{p\text{-}n\text{-}p}$.

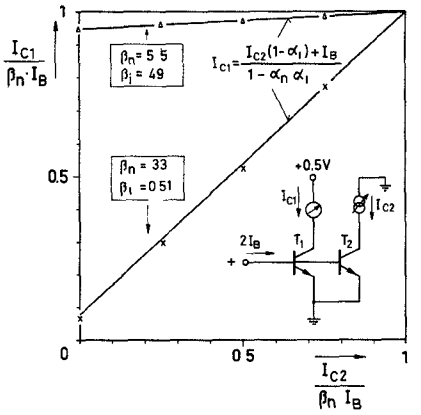


Fig. 9. Influence of inverse current gain β_i on current hogging.

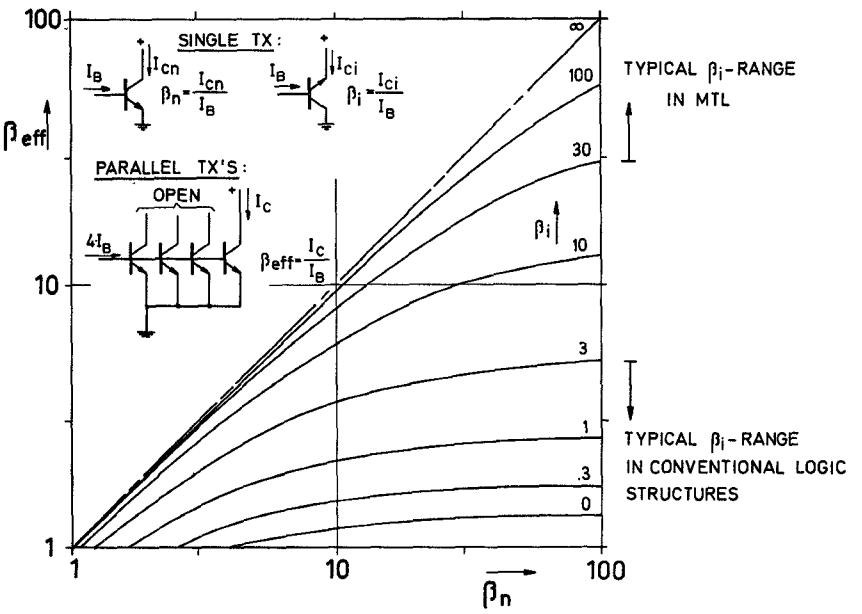


Fig. 10. Maximum current hogging for various current gains.

operated transistor T_0 and the active inversely operated transistor T_2 of Fig. 7(b).[2]

Thus, the external emitter current I_{EP} of one p-n-p transistor is

$$I_{EP} = I_B[(1/\alpha_{p\text{-}n\text{-}p}) - \alpha'_{p\text{-}n\text{-}p}] \quad (2)$$

when the corresponding n-p-n transistor is ON and

$$I_{EP} = I_B \cdot (1/\alpha_{p\text{-}n\text{-}p})$$

when this transistor is OFF. $\alpha_{p\text{-}n\text{-}p}$ and $\alpha'_{p\text{-}n\text{-}p}$ have been defined in Fig. 8. Hence, for the total supply current I_0 of n parallel p-n-p transistors on the logic chip one obtains

$$I_0 = (n \cdot I_B/\alpha_{p\text{-}n\text{-}p})(1 - \tfrac{1}{2}\alpha'_{p\text{-}n\text{-}p} \cdot \alpha_{p\text{-}n\text{-}p}). \quad (3)$$

All considerations may be applied to multicollector p-n-p or multicollector n-p-n structures as well by dividing them into single transistors connected in parallel.

The influence of the inverse current gain β_i on the current hogging of parallel-connected grounded emitter transistors is illustrated by the interdependence of collector currents measured on different matched transistor pairs and theoretically verified (Fig. 9). In case of the large inverse current gain of $\beta_i \approx 50$, which is typical for MTL, the collector current of the nonsaturated transistor T_1 is almost independent to the degree of saturation in transistor T_2. However, in the case of $\beta_i \approx 0, 5$, which is

[2] This representation is justified by the Ebers–Moll equations.

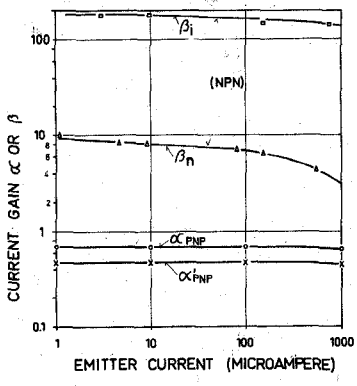
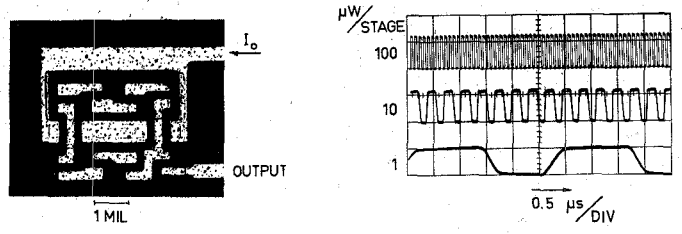


Fig. 11. Common base current gain α_{p-n-p} and recollection factor α'_{p-n-p} of current source p-n-p transistor, common-emitter gains β_n and β_i of n-p-n transistor versus emitter current.



(a) (b)

Fig. 12. (a) Chip photomicrograph and (b) output signal oscillograms of seven-stage closed-loop MTL inverter chain.

typical for conventional gold-doped structures, both currents are closely coupled. This indicates a strong base-current hogging by the saturated transistor.

In practice, one would calculate the effective current gain of one active transistor in parallel with $(m - 1)$ saturated transistors being supplied by m times I_B, when the saturated transistors carry no collector current at all (worst case). This effective current gain is

$$\beta_{eff} = \frac{\alpha_n}{1 - \alpha_n\left[\frac{1 + (m-1)\alpha_i}{m}\right]} \tag{4}$$

For $m = 1$ (single transistor) one gets $\beta_{eff} = \beta_n$ as expected, whereas for $m \gg 1$, (4) yields

$$\beta_{eff} = \alpha_n/(1 - \alpha_n \cdot \alpha_i). \tag{5}$$

In Fig. 10 a typical example ($m = 4$) again confirms that with MTL the current hogging is insignificant in contrast to conventional structures.

V. Experimental Results

Test chips have been fabricated containing single devices and small logic blocks using the simplest structure according to Fig. 3. That is, two diffusions into a blanket n wafer (0.1 Ω cm, no epitaxy). All devices have a n^+ collar implemented with the n^+ collector diffusion. Fig. 11 shows the grounded base current gain α_{p-n-p} and the recollection factor α'_{p-n-p} of the lateral p-n-p transistor according to Fig. 8. This diagram says that even at very low currents a satisfactory power efficiency is achieved.

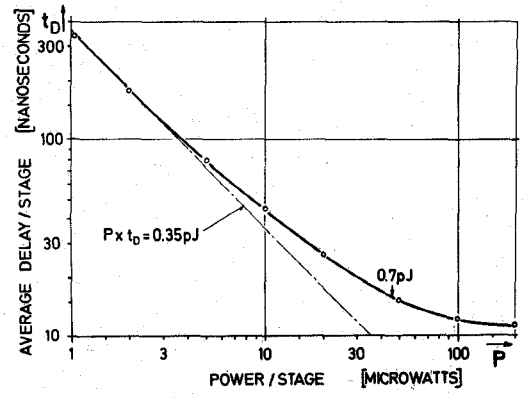
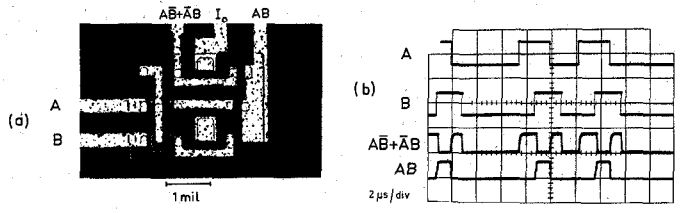


Fig. 13. Propagation delay versus power dissipation of seven-stage closed-loop MTL inverter chain.



(a) (b)

Fig. 14 (a) Chip photomicrograph (11 mils²). (b) Input and output signals of MTL half-adder.

The common emitter gain of the n-p-n transistor in the normal and inverse operation modes have also been plotted in Fig. 11 as a function of the emitter current. Despite the simple structure, reasonable forward current gain values have been obtained allowing a fan-out of five which is usually adequate for the logic design. The inverse current gain β_i is sufficiently large to make current hogging negligible.

To test the propagation delay of MTL, a seven-stage closed-loop inverter chain has been built. Fig. 12 shows the chip microphotograph of this circuit and its output signal for three power levels differing by factors of 10. This oscillogram demonstrates an outstanding feature of MTL, namely that the same MTL logic chip can be operated at hugely different power levels to select the performance suitable for a given application. In Fig. 13 the measured delay has been plotted versus power dissipation over several orders of magnitude. The minimum delay time of ≈10 ns corresponds to a common base switching time constant $\tau \approx 3$ ns for the n-p-n transistor. At low power, where this switching time constant has a negligible effect compared to the charging times of the depletion layer capacitances, a constant power-delay product results as low as 0.35 pJ.

The high functional density of MTL is illustrated by the photomicrograph [Fig. 14(a)] of a half-adder, implemented on an area of only 11 mils², with 0.3-mil-wide metal lines and 0.15-mil spacing. The oscillogram Fig. 14(b), shows the input and output signals of this circuit.

VI. Summary and Conclusions

MTL as a novel bipolar logic concept has been discussed and experimentally verified. It is based on inverters having decoupled multicollector outputs for the logical combinations. These inverters are powered by a direct injection of minority carriers into their common n-emitter plane. MTL is a self-isolated structure requiring no ohmic load resistors. This simple structure offers considerable advantages of which the most significant ones are

1) high noise immunity and good driving capabilities (TTL compatible);
2) fabrication substantially simplified (only four mask steps through metalization);
3) extremely high functional density (about 1000 gates on 130 × 130-mils^2 chip with present manufacturing tolerances, such as 0.3-mil metal lines, 0.15-mil spacing, and 0.2 × 0.2-mil contact holes);
4) excellent power-delay product (0.35 pJ above 100-ns delay, 0.7 pJ in the 15–20-ns range, and power speed externally alterable).

These results have been obtained on a very simple structure implemented by using readily available processing facilities. By taking advantage of modern technological accomplishments, improvements can be expected without increasing the processing complexity.

VII. Acknowledgment

The authors are indebted to D. Young[3] and his department for the test chip artwork and to H. Rupprecht[3] and his department for test chip fabrication. Special thanks are due to C. S. Chang[3] for valuable contributions.

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Integrated Injection Logic: A New Approach to LSI

KEES HART AND ARIE SLOB

Abstract—**Logic gates suitable for large-scale integration (LSI) should satisfy three important requirements. Processing has to be simple and under good control to obtain an acceptable yield of reliable IC's containing about 1000 gates. The basic gate must be as simple and compact as possible to avoid extreme chip dimensions. Finally, the power-delay time product must be so high that operation at a resonable speed does not cause excessive chip dissipation.**

Multicollector transistors fed by carrier injection proved to be a novel and attractive solution. A simplified (five masks) standard bipolar process is used resulting in a packing density of 400 gates/mm^2 with interconnection widths and spacings of 5 μm. The power-delay time product is 0.4 pJ per gate. An additional advantage is a very low supply voltage (less than 1 V). This, combined with the possibility of choosing the current level within several decades enables use in very low-power applications. With a normal seven-mask technology, analog circuitry has been combined with integrated injection logic (I^{2}L).

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Introduction

LOGIC gates suitable for large-scale integration (LSI) must satisfy three important requirements.

1) The processing has to be simple and under good control in order to obtain an acceptable yield of reliable IC's containing about 1000 gates.

2) The basic gate must be as simple and compact as possible to avoid extreme chip dimensions.

3) The power-delay time product must be such that operation at a reasonable speed does not cause excessive dissipation on the chip.

Multicollector transistors fed by carrier injection proved to be a novel and attractive solution that fulfills the previous three requirements [1]–[3]. Two ways of injection will be discussed, viz., injection by light and injection with a p-n diode. A number of realized LSI circuits will be mentioned.