An Experimental 512-bit Nonvolatile Memory with Ferroelectric Storage Cell

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Abstract —An experimental 512-bit random access memory based on ferroelectric-capacitor storage cells has been successfully fabricated and tested. The device was designed solely for use in process development and electrical characterization and includes on-board test circuitry for that purpose. The internal timing of the memory is controlled externally to allow experimentation with timing algorithms, hence the name 512 externally controlled device, or 512 ECD. This paper will discuss the properties of the ferroelectric ceramics used in integrated circuit memories, the operation of a destructively read ferroelectric memory cell, and the organization of the 512 ECD die, including its on-board test circuitry. The paper will close with a discussion of the retention and wear-out properties of ferroelectric capacitors as they relate to design requirements.

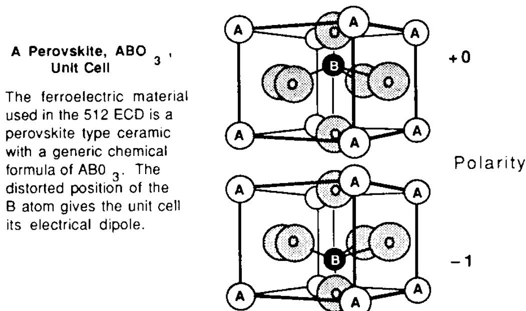

Fig. 1. A unit cell of the 512 ECD ferroelectric material.

I. Ferroelectric Properties

A FERROELECTRIC capacitor has a highly nonlinear dielectric with permanent charge retention after application of a voltage by an external circuit. The permanent charge originates from a net ionic displacement in unit cells of the material resulting from the external voltage application (see Fig. 1). The individual unit cells interact constructively with their neighbors to produce domains within the material. As the voltage is removed, the majority of the domains will remain poled in the direction of the applied electric field, requiring compensating charge to remain on the plates of the capacitor. This compensating charge causes a hysteresis in the standard charge versus voltage plot of the capacitor as it is cycled through positive and negative voltage applications (see Fig. 2). A measured hysteresis is shown in Fig. 3. From a digital point of view, if a voltage is applied to a ferroelectric capacitor in a direction opposite of the previously applied voltage, remanent domains will switch, requiring compensating charge to flow onto the capacitor plates. If the field is applied in the direction of the remanent domains, no remanent switching takes place, no change occurs in the compensating charge, and a reduced amount of charge will flow into the capacitor. This property can be used by a properly designed external circuit to sense the last state of the capacitor or write a desired state into the capacitor. Note that the remanent charge does not generate a detectable voltage on the capacitor after the removal of the applied field. In fact, unlike a DRAM capacitor, the plates of the ferroelectric capacitor can be shorted without affecting the remanent charge internally and the charge requires no refresh. More complete descriptions of the properties and applications of ferroelectric materials are given in works listed in the reference section of this paper [1]–[4].

The thin ferroelectric film capacitor is a rugged, highly reliable device which can withstand a wide range of extremes in temperature and radiation. The ferroelectric ceramic used in the 512 externally controlled device (ECD) has a Curie temperature in excess of 300°C with a diffuse phase transition allowing for excellent data retention and storage over the full military temperature range from −55 to 125°C. The Curie temperature is the point at which the unit structural cell loses its distortion and the ferroelectric properties, as well as any stored data, disappear. There is a nondestructive change in the amount of remanent charge in the capacitor generated as a function of temperature. The 512 ECD ferroelectric capacitors have a dynamic signal range of two over the military temperature range. The designer must ensure that his sensing techniques operate over that dynamic range. A conservative technique used on the 512 ECD is the double-ended sense architecture where two ferroelectric cells are matched for each bit. Single-ended sense techniques are certainly possible with the technology if a temperature-compensated reference or dummy cell is generated by the designer.

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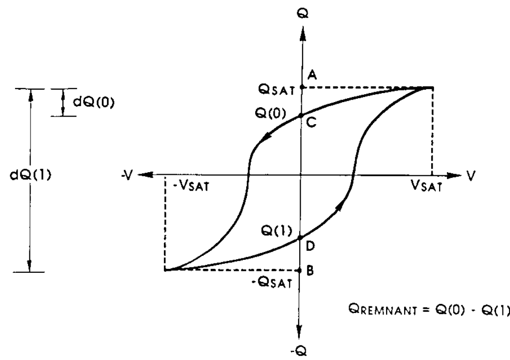

Fig. 2. Hysteresis of ferroelectric capacitor.

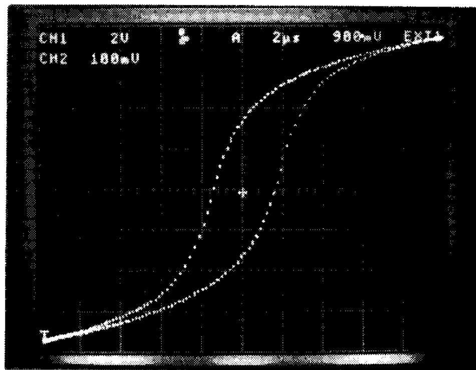

Fig. 3. Measured hysteresis of $100 \times 100\text{-}\mu m^2$ ferroelectric capacitor. Y scale/div $=10\ \mu C/cm^2$; X scale/div $= 2$ V.

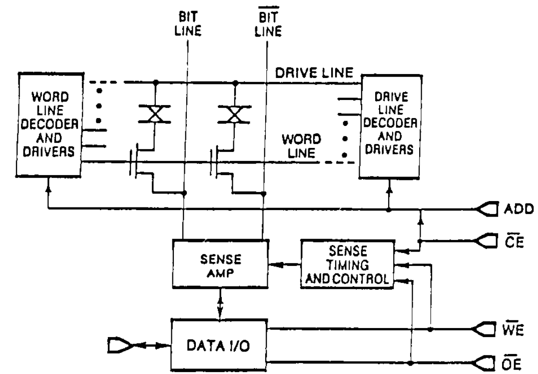

Fig. 4. 512 ECD block diagram.

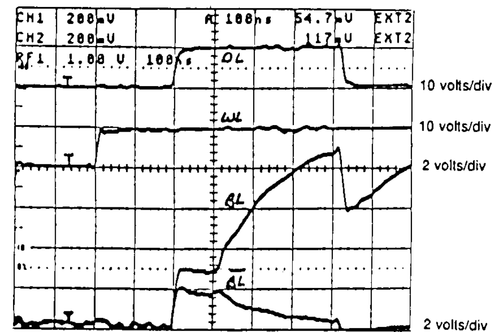

Fig. 5. 512 ECD bit-line voltages during READ.

The very nature of the charge storage mechanism in the ferroelectric material, i.e., ionic displacement, makes the capacitor naturally radiation hard. High-energy particles, gamma radiation, or neutrons must physically move ions in the lattice to erase the stored polarization state and this requires extremely high doses. Radiation tests conducted by the Naval Surface Warfare Center, Sandia National Laboratories, and Raytheon Corporation confirm this model. The radiation hardness of a ferroelectric-based memory will ultimately depend on the hardness of the underlying control circuitry. There are several reports available to the public concerning radiation hardness and test results of ferroelectric capacitors [5], [6].

Unlike a linear capacitor, the switching speed of a ferroelectric capacitor is limited by the domain switching speed. This is much slower than the electronic displacement common in linear capacitors. The modified lead titanate materials used in the 512 ECD can switch at speeds tested above 50 MHz. The limit may be in the gigahertz range. However, we have not been able to determine the maximum switching speed of the ferroelectric material used in the 512 ECD. In a useful CMOS circuit, the response of the ferroelectric material is such that the speed of the circuit will be determined by the circuit's intrinsic ability to deliver charge, not by the speed of the ferroelectric capacitor.

II. Ferroelectric Memory Operation

The memory cell utilized in the 512 ECD consists of a pass-transistor/ferroelectric-capacitor combination. Two cells are used in a double-ended sense scheme to create a self-referencing signal differential across a regenerative sense amp. A block diagram is shown in Fig. 4. The data bit consists of a word line (WL) controlling two pass transistors, a bit line (BL) and bit-bar line (BLb) to collect charge from the capacitors, and a common drive line (DL) to actively drive the capacitors. A sense amp resides between BL and BLb. For a WRITE, the sense amp is set to the desired state driving BL and BLb to the opposite voltage values of V_{drive} and ground. The drive line is then pulsed such that the high drive line against the grounded bit line writes the $Q(0)$ state into that capacitor. When the drive line drops to ground after the pulse, the other capacitor has a $Q(1)$ written in it by its high bit-line voltage. V_{drive} is derived directly from V_{cc2}. The state written into the capacitor on BL represents the polarity of the stored datum.

The READ operation is best understood by examining the photograph of the 512 ECD bit-line signals in Fig. 5. A voltage step is applied to the drive line with the bit lines floating and the sense amp OFF. Since the capacitors are in opposite states, BL and BLb will collect different amounts of charge and produce a voltage differential of a polarity determined by the stored data. The capacitor that is flipped

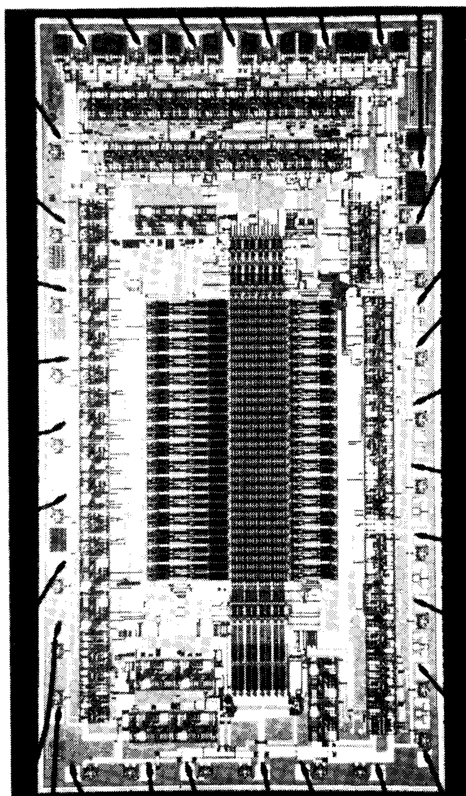

Fig. 6. Die photograph of 512 ECD.

TABLE I
CRITICAL STATISTICS

Technology	N-well CMOS
Critical Feature Size	3 micron
Die size	3.2mm x 6mm
Vcc1	5 volts
Vcc2	5 volts -> 10 volts
Active Power	30mW
Bit Area	1300 μ^2
Capacitor Size	5 μ x 9 μ
Read/Write Access Speed	550ns
Tested Read Accesses per byte (50°C)	10^{12}
Tested Write Accesses per byte (50°C)	10^{11}

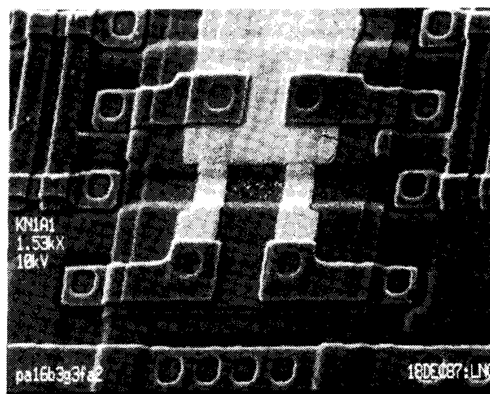

Fig. 7. SEM photograph of 512 ECD capacitors.

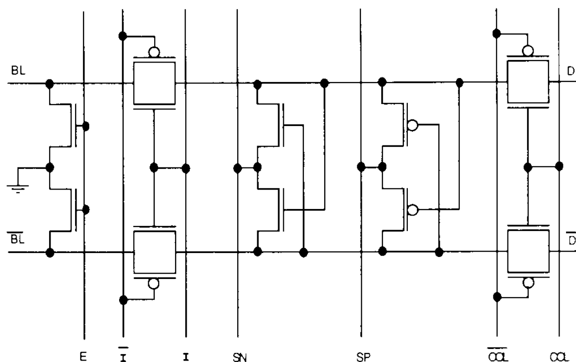

Fig. 8. Circuit of 512 ECD sense amplifier.

during the READ will generate the higher bit-line voltage. When the sense amplifier turns on, it will drive that particular bit line to the high rail while the other bit line will be driven to ground. This situation recreates the original WRITE condition and restores both capacitors to their original states. The restore is invisible to the user and occurs in parallel with the output gating of the READ data to the I/O ports. Note the 1-V differential generated on the bit lines in Fig. 5 by the two capacitor states.

III. 512 ECD ORGANIZATION

Fig. 6 is a die photograph of the 512 ECD and its internal organization. Table I reflects its critical statistics. The device is arranged as a 64×8 memory. The memory array consists of 64 rows of 8 bits apiece with no column decode. One row consists of 16 capacitors sharing a common WL and DL and arranged as eight double-ended memory bits. The capacitors are approximately 5×9 μm^2, less than 1 μm thick, and have a nominal capacitance of 1 pF apiece. The upper half of the photograph in Fig. 7 shows the two matched capacitors of a single bit. As noted in Table I, a single bit occupies approximately 1300 μm^2, a very large area. The part was never intended for production, so large tolerances were provided for in the layout rules to ensure operable parts on first silicon. The 3-μm technology and double-ended architecture also contributed to the memory cell area.

The DL drivers and WL drivers are located on either side of the memory array. Eight regenerative feedback amplifiers similar to those in DRAM's constitute the sense amps. A circuit diagram of one of the sense amps, including equalization, isolation, and output gate controls, is shown in Fig. 8. The device has standard three-state I/O functions. The die size is 3.2×6 mm^2.

The WL, DL, sense amp, and equalization functions are controlled from buffered inputs. In combination with the I/O controls, the 512 ECD requires seven timing inputs to actively control the device in normal operation. The indi-

vidual control lines allow separate switching of:

1) word lines,
2) drive lines,
3) sense amplifiers,
4) equalization of the bit lines,
5) output ports of the sense amplifiers,
6) output enable, and
7) WRITE enable.

Additionally, the isolation between the memory array and the sense amplifiers can be controlled externally. The part has two separate internal power grids with a common ground. V_{cc1} supplies standard voltages to the control circuitry. V_{cc2} supplies the second power grid consisting of the memory array, sense amplifiers, word-line drivers, and drive-line drivers. Voltage translation circuits convert the control signals, data, and addresses between the two voltages. The flexibility of the separate control lines allows examination of various timing algorithms on the ferroelectric-capacitor performance. The dual power system provides the same flexibility in examining the effects of various drive voltages across the capacitors in the memory array. The memory has operated with V_{cc2} as low as 5 V and as high as 10 V. The seven control lines are unique to the 512 ECD. Products based on this technology may be designed with standard SRAM three-line control using a synchronous chip enable to compensate for the destructive READ mechanism.

The performance of 512 ECD is severely limited by the use of buffered control signals to drive the internal operation. Also, its primary mission is to study the ferroelectric capacitors under realistic conditions. Consequently, no attempt to formally characterize the speed performance of the device has been made. The various test programs used on the part have operated as fast as 550-ns access time and 1-μs cycle time to as slow as 1700-ns access time and 2.4-μs cycle time. The part has operated as high as 125°C using these timing algorithms.

The top 20 percent of the die is occupied by special analog test circuitry consisting of source followers connected to the bit lines. A circuit diagram of a source-follower pair connected to one bit-line pair is shown in Fig. 9. There is a source-follower pair for each bit-line pair in the 512 ECD and all 1024 capacitors of the part can be measured individually. Note that one source follower serves both the bit and bit bar of a single column and that the output of the source follower is routed to the associated output pad. The user can select either bit or bit bar for measurement via the TAP control line. The TEST control line disconnects the source followers from the memory array for normal digital operation. A pull-up resistor to an external reference voltage is connected to each I/O pad. In the TEST mode with a voltage on the bit line under observation, the source follower produces a voltage at the I/O pad related to the bit-line voltage. Circuitry is included which allows calibration of the I/O pad voltage relative to the bit-line voltage generating it before starting the test. External computer-controlled analog-to-digital converters are used to measure the bit-line signals generated by the ferroelectric capacitors in the array.

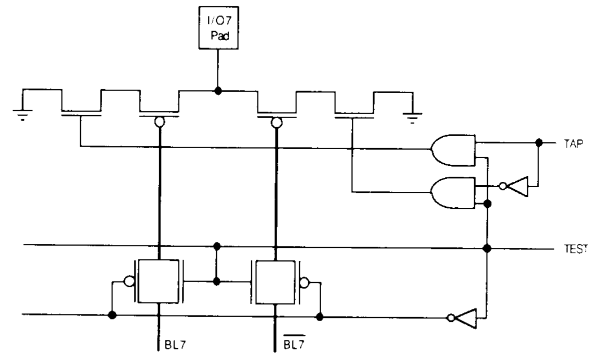

Fig. 9. 512 ECD source-follower circuit.

Using the analog test system, capacitor uniformity after production can be examined. The part can then be subjected to different types of operations under varying environmental conditions to examine the long-term effects on capacitor performance. This is probably the most important feature of the 512 ECD. Wear-out and retention characteristics of the ferroelectric capacitors in an actual digital memory can be objectively quantified over a wide range of operating conditions. It is necessary to measure these characteristics since they must be compensated for in design to produce the longest lifetime and widest temperature margins for a product. Without this information, it is presently impossible to design a product with long-term reliability.

IV. Retention

Ferroelectric capacitors poled into a specified state will depolarize over time. The rate of depolarization is a function of temperature, intrinsic stress, WRITE voltage, and ferroelectric material composition. The sense-amp design used in the 512 ECD has a minimum limit below which the internal threshold imbalances of the sense amp will overcome the READ signal and an error may occur. The time required for the signal level generated by the capacitor to be reduced through the effects of natural depolarization represents the retention capability of the device under the stated conditions of temperature, WRITE voltage, and previous history. The minimum signal level targeted by the designer to ensure a correct READ operation is determined by the product specification and must take into account the radiation and noise environment the part is intended to operate in as well as the level of sense-amp bias resulting from design and process rule variations.

Projections based on analog measurement of retained signals in the 512 ECD at room temperature indicate more than 30 years retention after 10^8 WRITE/READ/invert accesses. The retention capability drops off with temperature and number of accesses.

V. Wear-Out

Thin ferroelectric film capacitors do wear out from being accessed. The access lifetime of the device is determined by the retention period desired by the user. At the beginning of that retention period, the capacitor must retain enough charge to equal the minimum signal required at the end of the retention period to overcome the sense-amp bias in the specified noise environment plus the expected signal loss over the stated retention period. The number of accesses allowed on the capacitor prior to the last desired retention period must not exceed a number that will wear out the capacitor signal below that required to successfully complete the retention period as noted above.

The design of the 512 ECD is such that access limits apply per byte and not to the memory as a whole. Due to the experimental nature of the device, its actual specifications have not been determined. However, the experience gained from extensive testing has been used to determine design rules for follow-on products. The goal for the Krysalis 16K products are for ten years retention after 10^{12} WRITE/READ/invert accesses over the industrial temperature range. This constitutes a 3-kHz access rate per byte constantly for ten years followed by ten years retention.

VI. Conclusion

The 512 ECD represents the first completely integrated CMOS-based ferroelectric memory. It was designed to be used as a test bed for measuring ferroelectric-capacitor performance in realistic conditions and it has proven valuable for that purpose. The results of testing the 512 ECD have significantly improved the chance of success for developing future products using ferroelectric-based memory cells.

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He is a co-founder of Krysalis Corporation in Albuquerque, NM, and responsible for the original ferroelectric-based memory concept at Krysalis. He has three years experience in computer and optical system design at the Air Force Weapons Laboratory, Albuquerque, NM, and three years experience in ferroelectric memories at Krysalis. At Krysalis, he managed the design and product engineering aspects of the 512 ECD and designed the test system presently in use for the 512 ECD and 16K UniRAM. He is now at Radiant Technologies in Albuquerque, NM. He is a co-holder of one patent and has four more in application.

Richard Womack (M'80) received both the B.S.E.E. degree and the B.S. degree in physics from Texas A&M University, College Station, in 1978. He received the M.S.E.E. degree from Southern Methodist University, Dallas, TX, in 1983.

He has ten years of semiconductor design experience, eight of which were at Texas Instruments Incorporated. At Texas Instruments, he designed several products using a wide array of semiconductor technologies and was a major contributor to the 4-Mbit DRAM design team. He is now the lead designer at Krysalis Corporation, Albuquerque, NM, and is responsible for the first ferroelectric UniRAM. He has authored 12 publications and is co-holder of three patents with four patents pending.