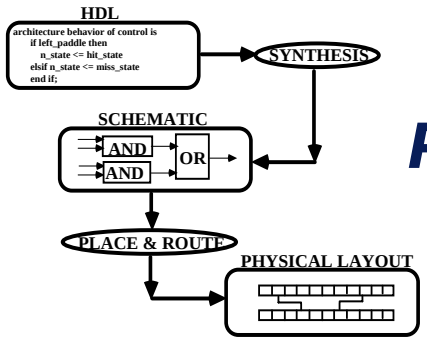
DESIGNING FPGAS & ASICS

FPGAs



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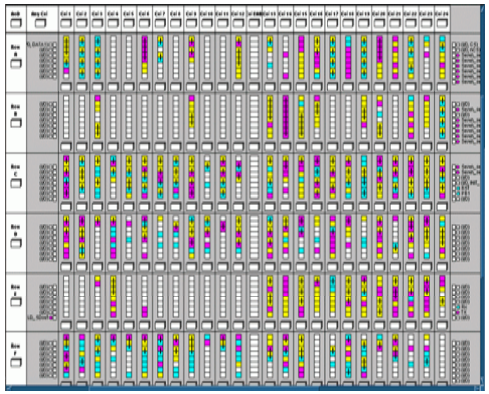
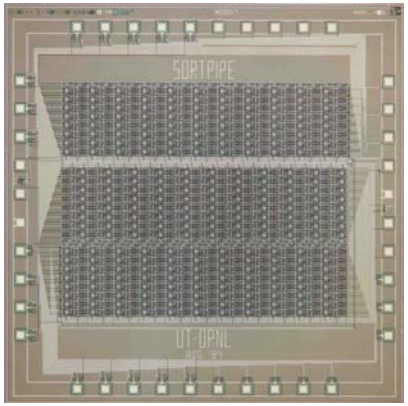
dbouldin@tennessee.edu



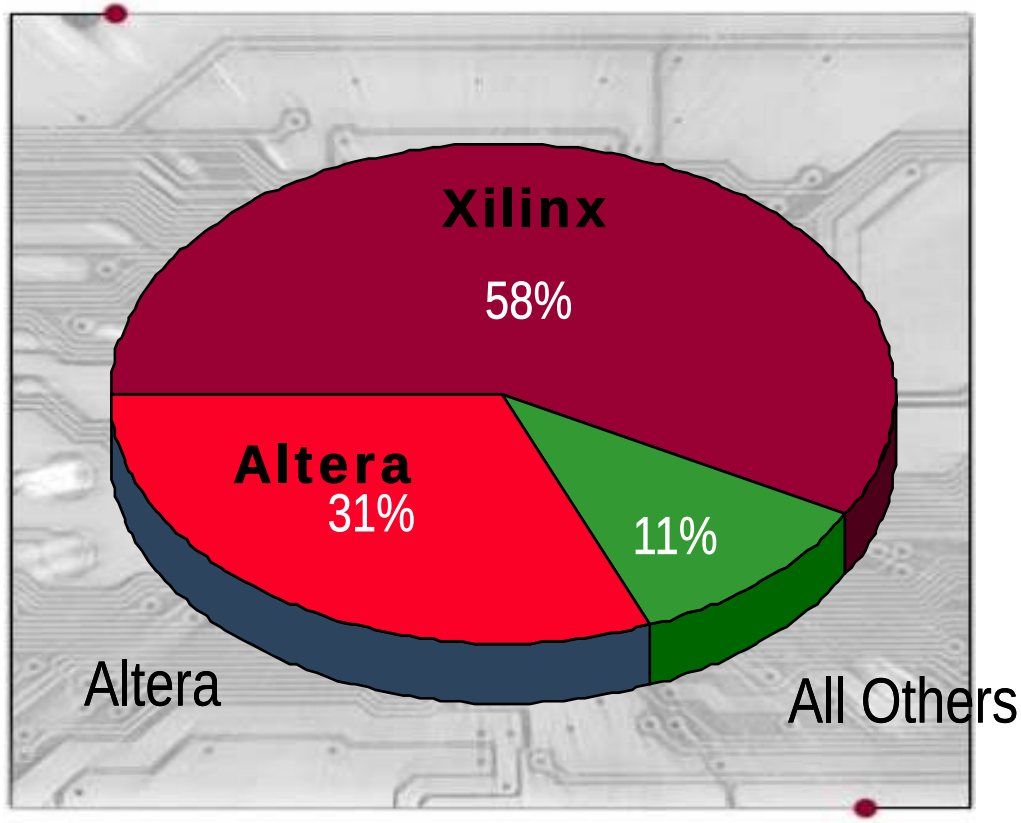


MAJOR FPGA VENDORS

- SRAM-based FPGAs
  - Xilinx – www.xilinx.com
  - Altera – www.altera.com
  - Atmel – www.atmel.com
  - Lattice Semiconductor – www.latticesemi.com
- Antifuse and flash-based FPGAs
  - Actel – www.actel.com
  - QuickLogic– www.quicklogic.com

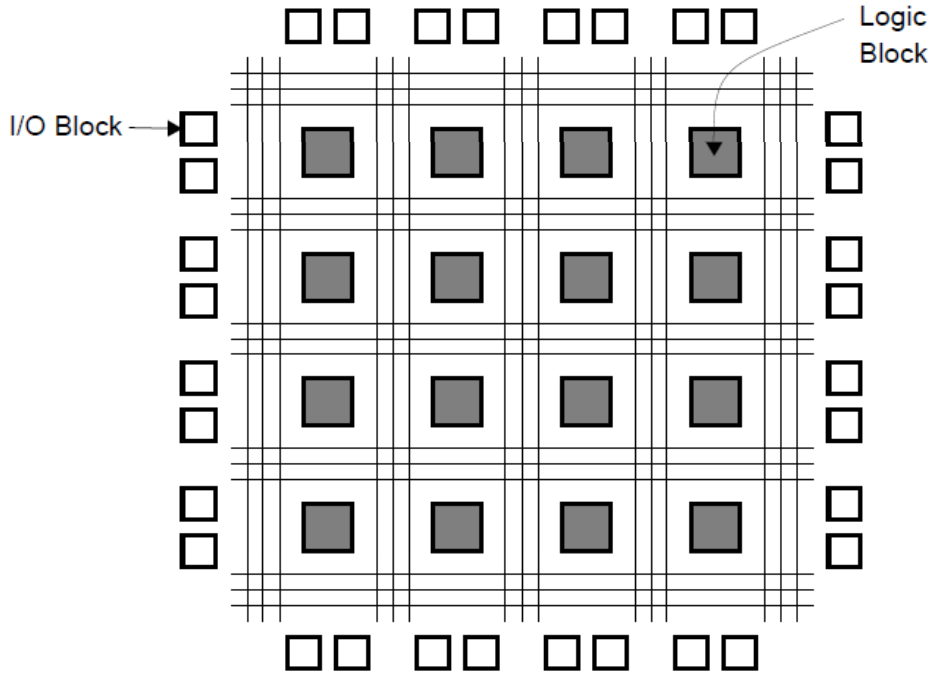
FPGA MARKET SHARE

- **Xilinx + Altera = 89% of the market**



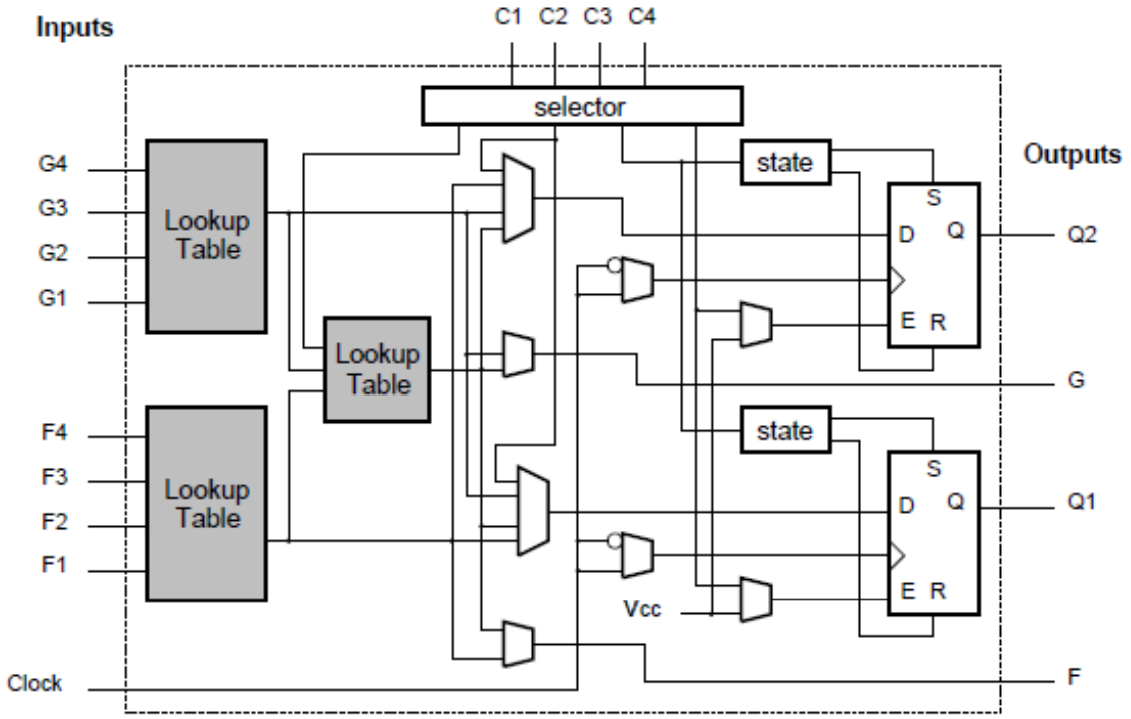
XILINX FPGA ARCHITECTURE

- **FPGA floorplans consist of tiles of programmable logic elements arrayed in two dimensions with interconnect tracks that use programmable switches. Vendors differ in the area devoted to logic and interconnect.**



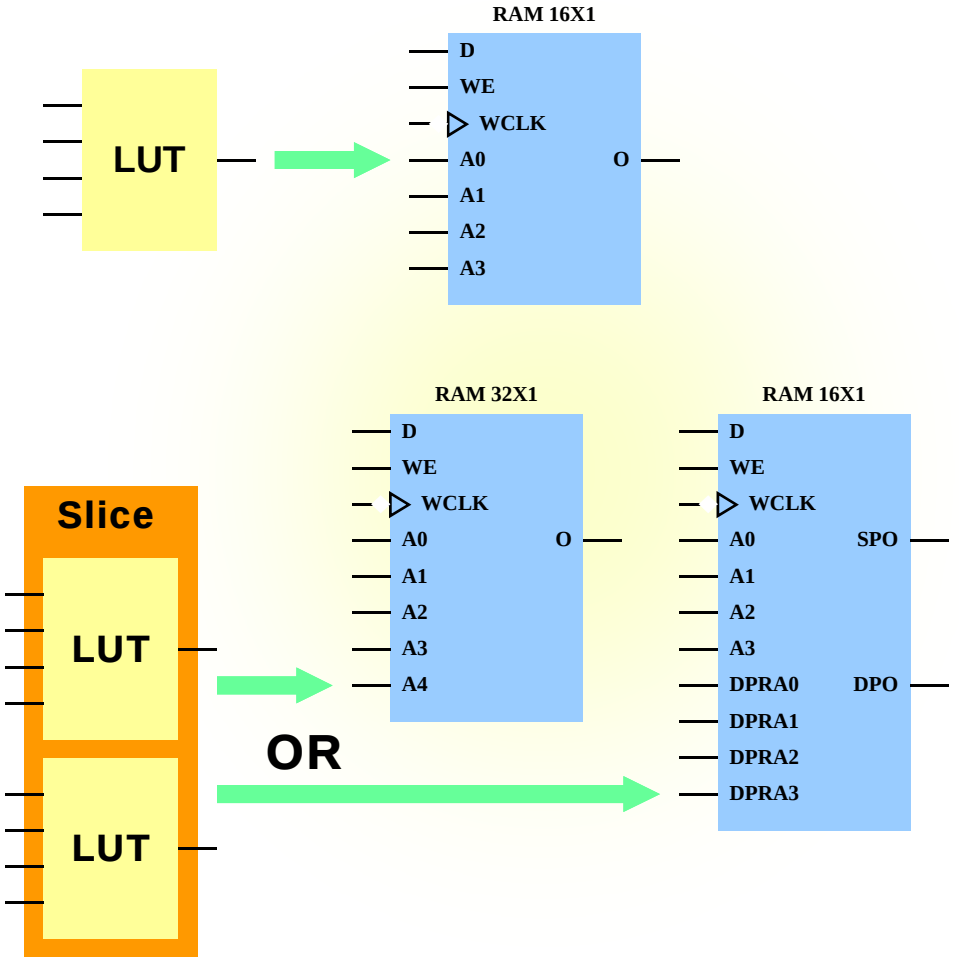
FPGA LOGIC

- **Programmable logic elements consist of LUTs with MUXs and D flip-flops. Newer FPGAS replace these 4-input LUTs with higher capacity 6-input LUTs.**



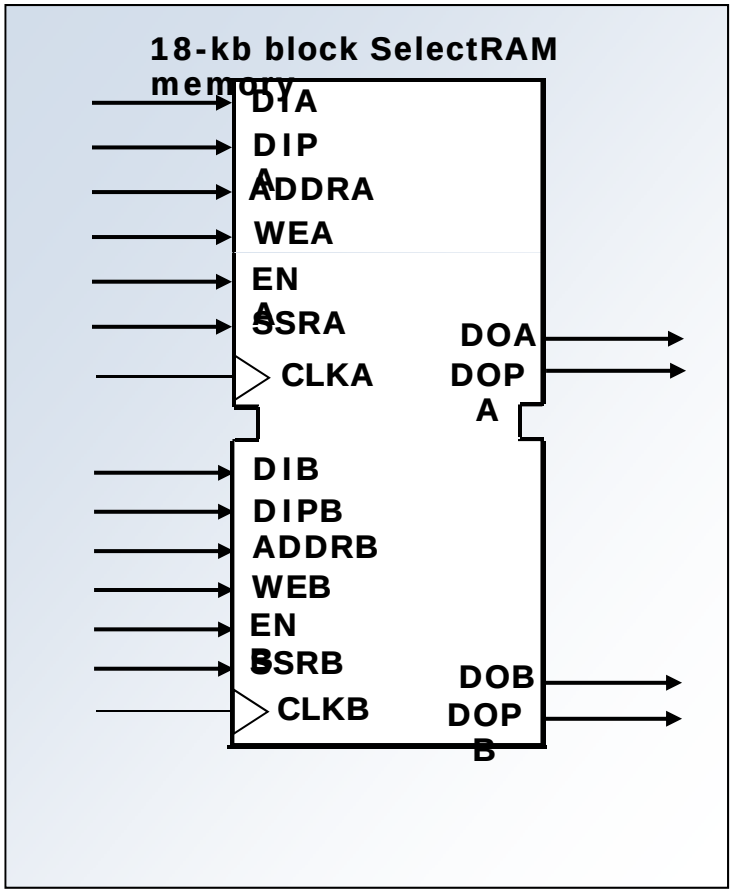
LUTS CAN BE USED FOR LOGIC OR AS DISTRIBUTED RAM

- 1 LUT = 16 RAM bits
- RAM and ROM are initialized during configuration
  - Data can be written to RAM after configuration
- Emulated dual-port RAM
  - One read/write port



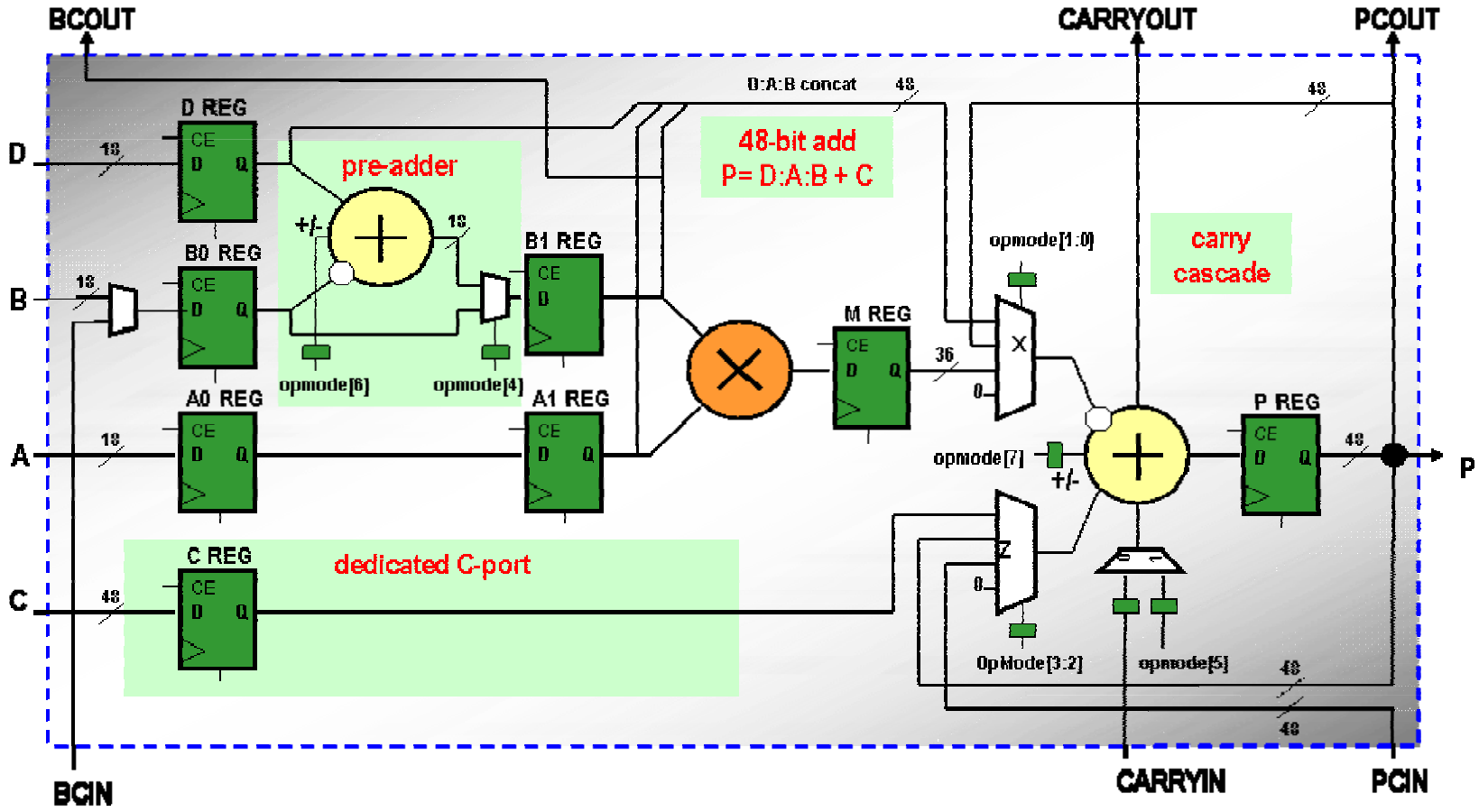
FPGAS ALSO CONTAIN EMBEDDED BLOCKS OF RAM

- **Multiple 18-kb blocks of RAM can be grouped together as needed for fast internal access**
  - **Synchronous read and write**
- **True dual-port memory**
  - **Each port has synchronous read and write capability**
  - **Different clocks for each port**



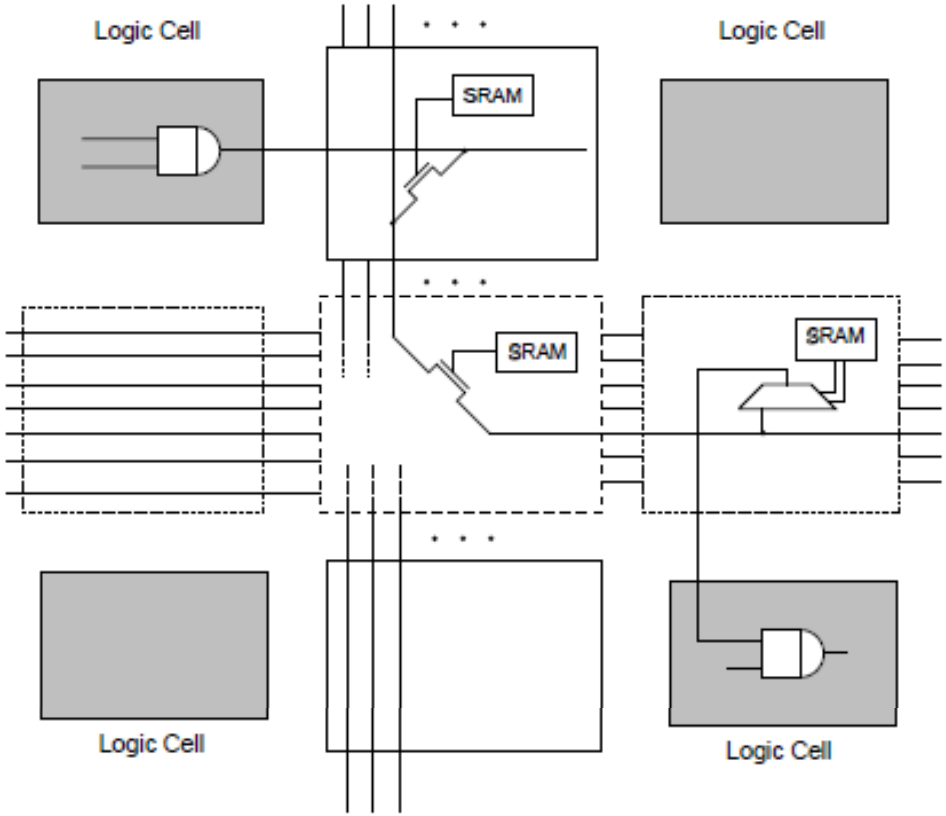
SOME FPGAS NOW INCLUDE EMBEDDED MULTIPLIERS

Xilinx XtremeDSP DSP48A Slice



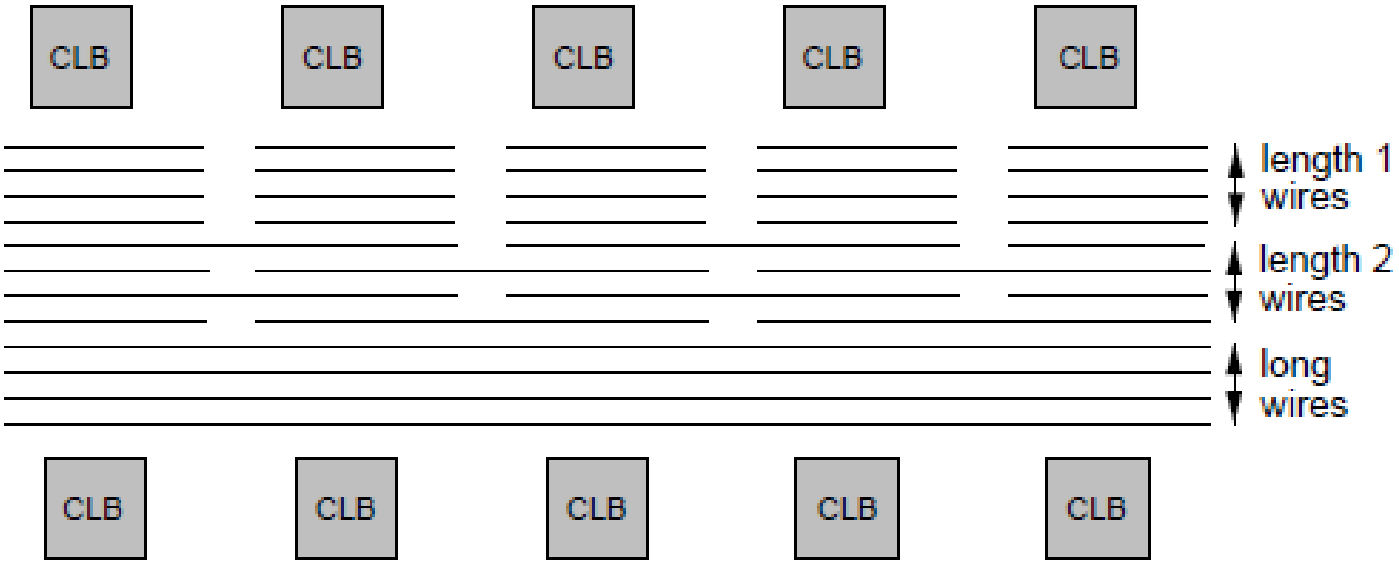
FPGA INTERCONNECT USING SRAM

- **Interconnect tracks can be connected by programming SRAM cells at their junctions.**



FPGA INTERCONNECT TRACKS

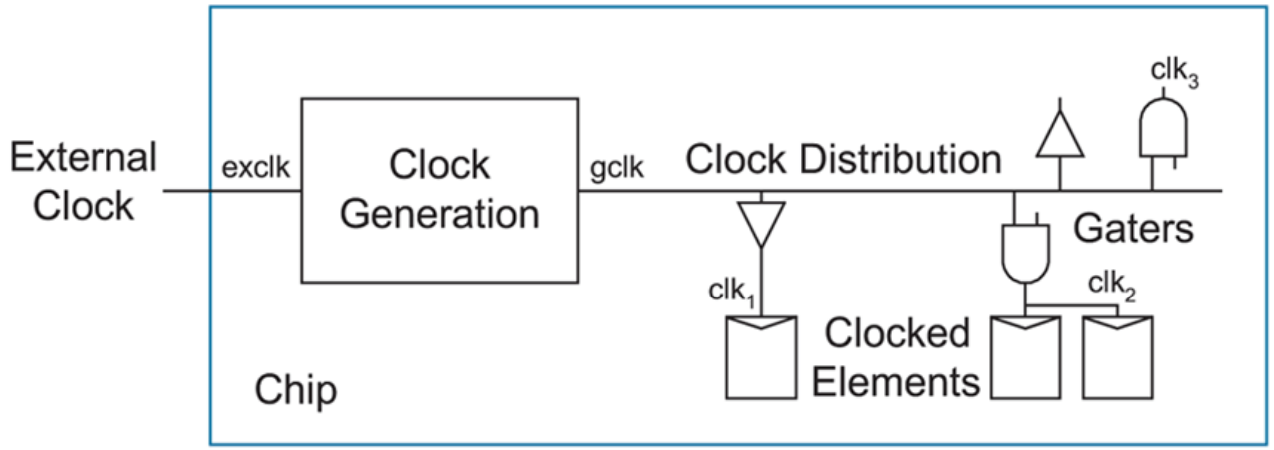
- **Tracks may be short, medium or long**



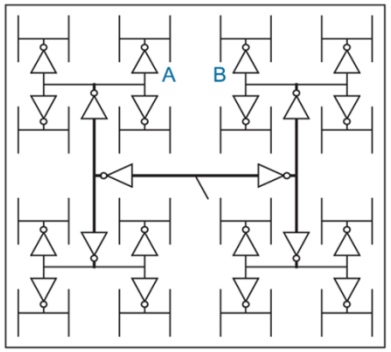
- **Wiring delays differ 30%-50% depending on which combination of tracks and "puddles" are used for interconnect.**

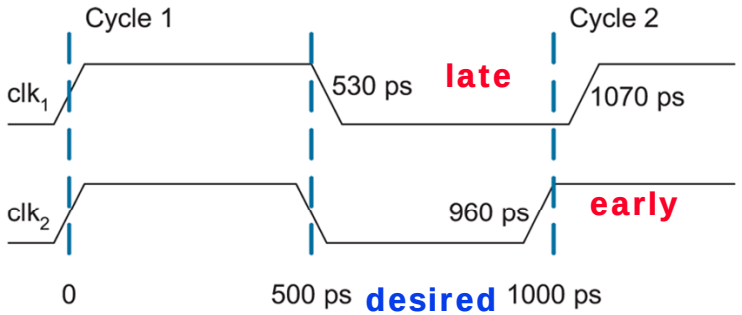
CLOCK DISTRIBUTION

Clock signals must be distributed to all of the flip-flops with a minimum of skew.



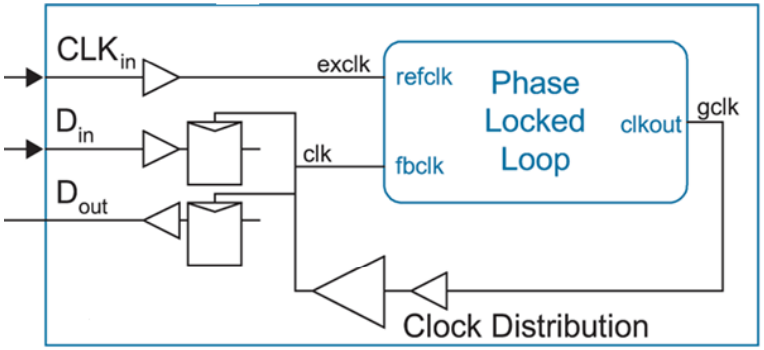
H-Tree

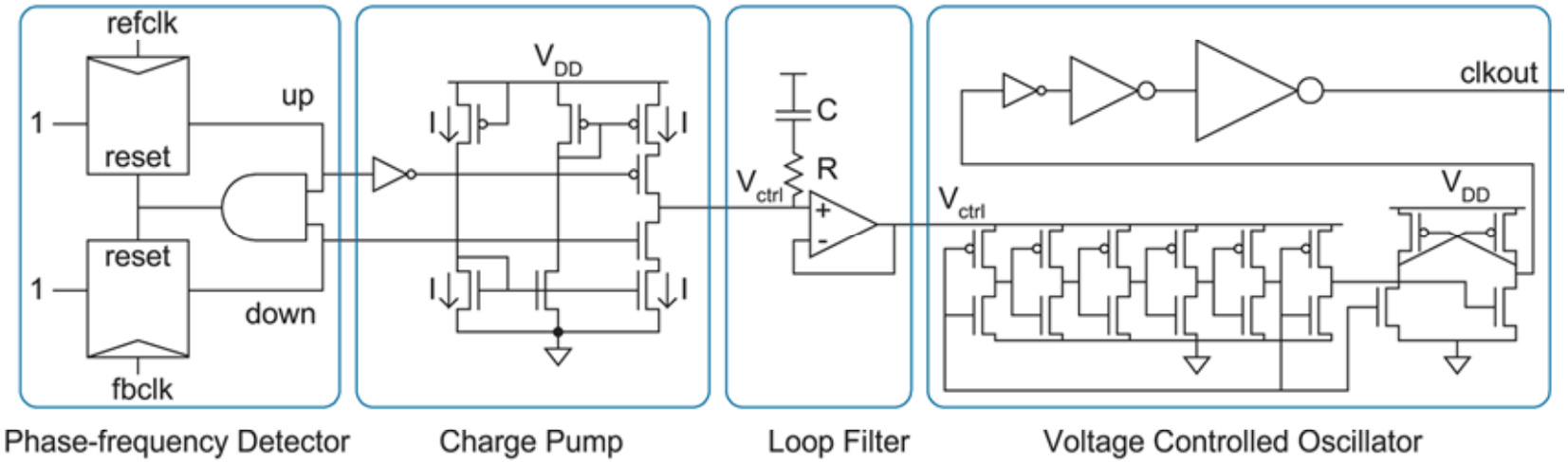




CLOCK MANAGEMENT

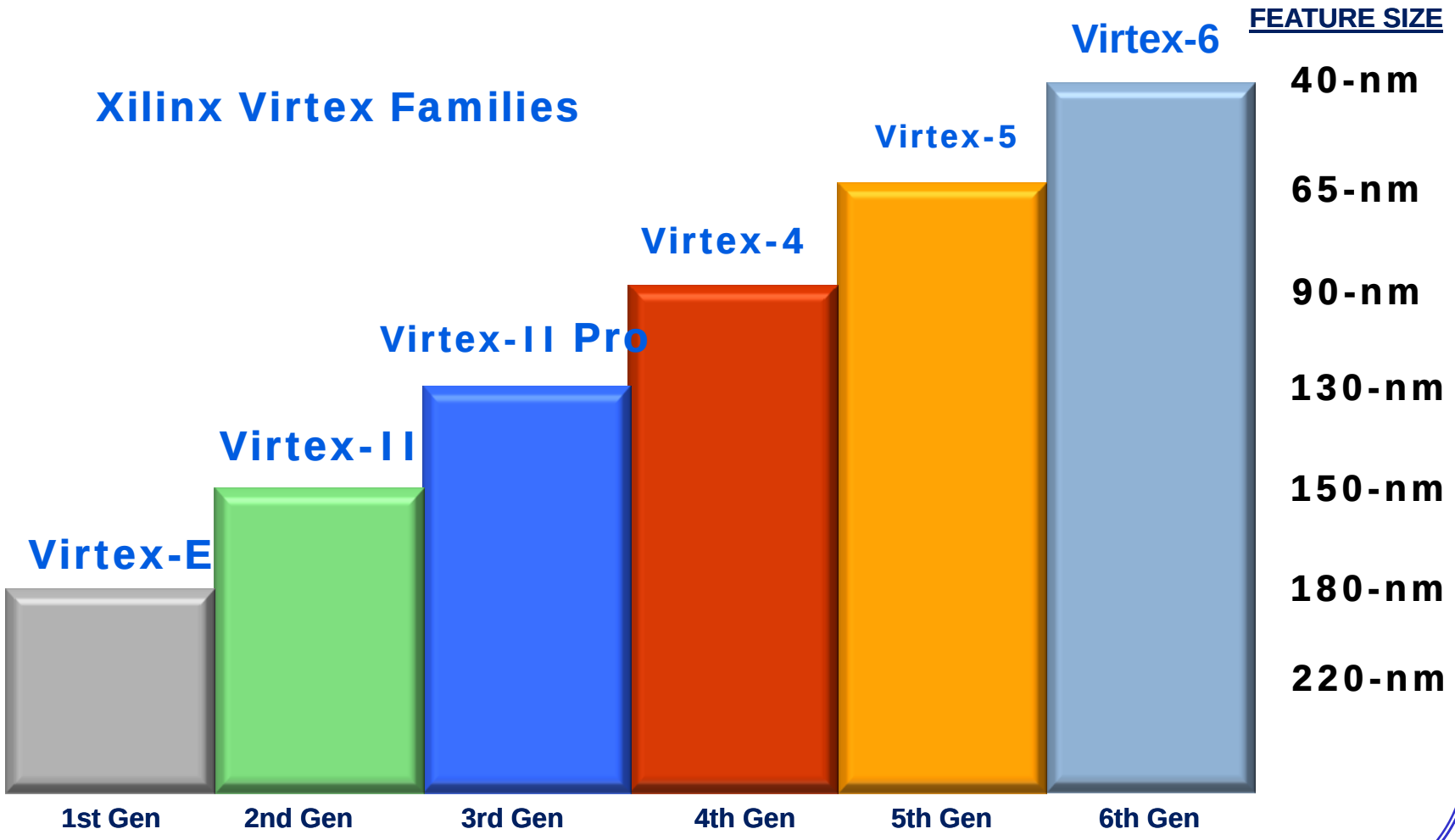
FPGAs include multiple DCMs (digital clock managers) with PLL (phase-locked loop) circuits to achieve low skew.





Phase-Locked Loop

FPGA CAPACITY HAS INCREASED WITH IMPROVEMENTS IN FABRICATION

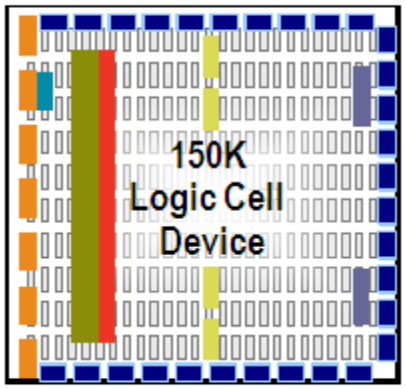


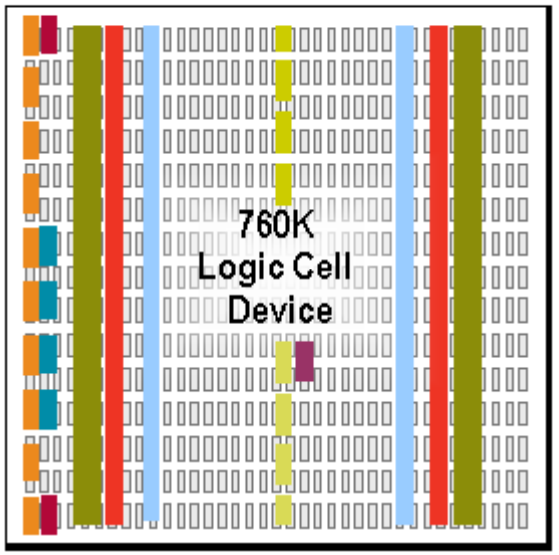
XILINX FPGA FAMILIES

High performance

High capacity

Low Cost





Spartan-3/6

Virtex-4/5/6

www.xilinx.com

XILINX VIRTEX-6 FAMILY

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices[2]	Block RAM Blocks			MMCMs[4]	Interface Blocks for PCI Express	Ethernet MACs[5]	Maximum Transceivers		Total I/O Banks[6]	Max User I/O[7]
		Slices[1]	Max Distributed RAM (Kb)	DSP	18 Kb[3]	36 Kb	Max (Kb)				GTX	GTH		
XC6VLX75T	74,496	11,640	1,045	288	312	156	5,616	6	1	4	12	0	9	360
XC6VLX130T	128,000	20,000	1,740	480	528	264	9,504	10	2	4	20	0	15	600
XC6VLX195T	199,680	31,200	3,040	640	688	344	12,384	10	2	4	20	0	15	600
XC6VLX240T	241,152	37,680	3,650	768	832	416	14,976	12	2	4	24	0	18	720
XC6VLX365T	364,032	56,880	4,130	576	832	416	14,976	12	2	4	24	0	18	720
XC6VLX550T	549,888	85,920	6,200	864	1,264	632	22,752	18	2	4	36	0	30	1200
XC6VLX760	758,784	118,560	8,280	864	1,440	720	25,920	18	0	0	0	0	30	1200
XC6VSX315T	314,880	49,200	5,090	1,344	1,408	704	25,344	12	2	4	24	0	18	720
XC6VSX475T	476,160	74,400	7,640	2,016	2,128	1,064	38,304	18	2	4	36	0	21	840
XC6VHX250T	251,904	39,360	3,040	576	1,008	504	18,144	12	4	4	48	0	8	320
XC6VHX255T	253,440	39,600	3,050	576	1,032	516	18,576	12	2	4	24	24	12	480
XC6VHX380T	382,464	59,760	4,570	864	1,536	768	27,648	18	4	4	48	24	18	720
XC6VHX565T	566,784	58,560	6,370	864	1,824	912	32,832	18	4	4	48	24	18	720

Notes:

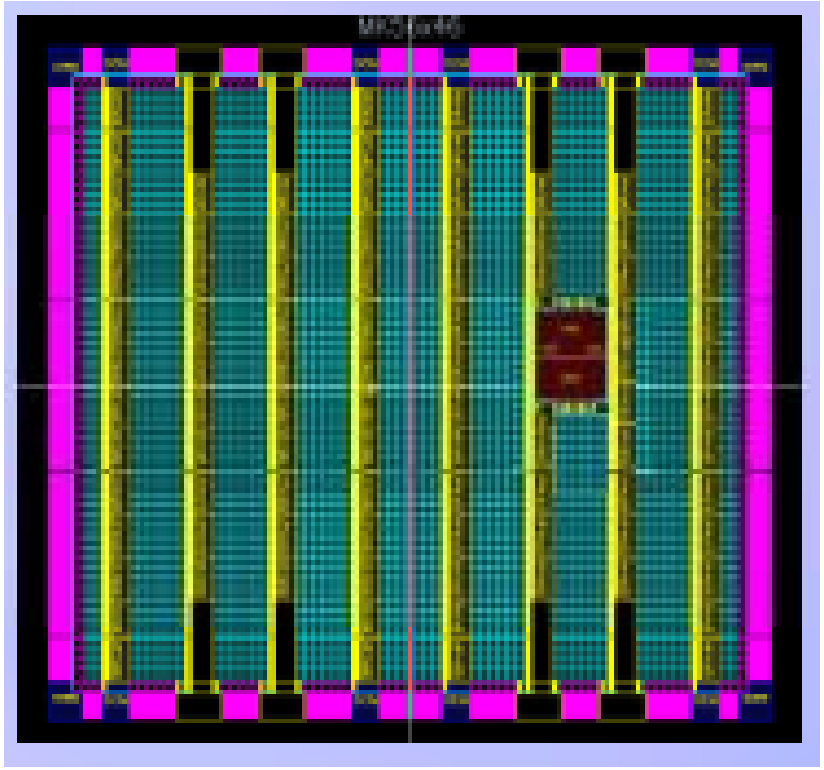
1. Each Virtex-6 FPGA slice contains four LUTs and eight flip-flops, only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP48E1 slice contains a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kbits in size. Each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains two mixed-mode clock managers (MMCM).
5. This table lists individual Ethernet MACs per device.
6. Does not include configuration Bank 0.
7. This number does not include GTX or GTH transceivers.

HIGH PERFORMANCE

http://www.xilinx.com/support/documentation/virtex-6.htm

FPGAS CAN INCLUDE CPUS

- CPU (hard or soft) can be integrated inside the FPGA
  - Replaces board with separate CPU and FPGA packages
  - Higher bandwidth and lower latency
  - CPU performs control functions
  - CPU may lack floating-point capability
  - Programmable System-on-Chip (SoC) Platform
  - Can prototype ASIC SoC or an embedded system



http://www.xilinx.com

XILINX SPARTAN-6 FAMILY

Device	Logic Cells[1]	Configurable Logic Blocks (CLBs)			DSP48A1 Slices[3]	Block RAM Blocks		CMTs[5]	Memory Controller Blocks	Endpoint Blocks for PCI Express	Maximum GTP Transceivers	Total I/O Banks	Max User I/O
		Slices[2]	Flip-Flops	Max Distributed RAM (Kb)		18 Kb[4]	Max (Kb)						
XC6SLX4	3,840	600	4,800	75	8	12	216	2	0	0	0	4	120
XC6SLX9	9,152	1,430	11,440	90	16	32	576	2	2	0	0	4	200
XC6SLX16	14,579	2,278	18,224	136	32	32	576	2	2	0	0	4	232
XC6SLX25	24,051	3,750	30,064	229	38	52	936	2	2	0	0	4	266
XC6SLX45	43,661	6,822	54,576	401	58	116	2,088	4	2	0	0	4	358
XC6SLX75	74,637	11,662	93,296	692	132	172	3,096	6	4	0	0	6	400
XC6SLX100	101,261	15,822	126,576	976	180	268	4,824	6	4	0	0	6	480
XC6SLX150	147,443	23,038	184,304	1,355	180	268	4,824	6	4	0	0	6	570
XC6SLX25T	24,051	3,750	30,064	229	38	52	936	2	2	1	2	4	250
XC6SLX45T	43,661	6,822	54,576	401	58	116	2,088	4	2	1	4	4	296
XC6SLX75T	74,637	11,662	93,296	692	132	172	3,096	6	4	1	8	6	320
XC6SLX100T	101,261	15,822	126,576	976	180	268	4,824	6	4	1	8	6	490
XC6SLX150T	147,443	23,038	184,304	1,355	180	268	4,824	6	4	1	8	6	530

Notes:

1. Spartan-6 FPGA logic cell ratings reflect the increased logic cell capability offered by the new 6-input LUT architecture.
2. Each Spartan-6 FPGA slice contains four LUTs and eight flip-flops.
3. Each DSP48A1 slice contains an 18 x 18 multiplier, an adder, and an accumulator.
4. Block RAMs are fundamentally 18 Kb in size. Each block can also be used as two independent 9 Kb blocks.
5. Each CMT contains two DCMs and one PLL.

LOW COST

http://www.xilinx.com/support/documentation/spartan-6.htm

XILINX SPARTAN-3 FAMILY

Device	System Gates	Equivalent Logic Cells[1]	CLB Array (One CLB = Four Slices)			Distributed RAM Bits (K=1024)	Block RAM Bits (K=1024)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs						
XC3S50[2]	50K	1,728	16	12	192	12K	72K	4	2	124	56
XC3S200[2]	200K	4,320	24	20	480	30K	216K	12	4	173	76
XC3S400[2]	400K	8,064	32	28	896	56K	288K	16	4	264	116
XC3S1000[2]	1M	17,280	48	40	1,920	120K	432K	24	4	391	175
XC3S1500	1.5M	29,952	64	52	3,328	208K	576K	32	4	487	221
XC3S2000	2M	46,080	80	64	5,120	320K	720K	40	4	565	270
XC3S4000	4M	62,208	96	72	6,912	432K	1,728K	96	4	633	300
XC3S5000	5M	74,880	104	80	8,320	520K	1,872K	104	4	633	300

Notes:

1. Logic Cell = 4-input Look-Up Table (LUT) plus a 'D' flip-flop. "Equivalent Logic Cells" equals "Total CLBs" x 8 Logic Cells/CLB x 1.125 effectiveness.
2. These devices are available in Xilinx Automotive versions as described in DS314: Spartan-3 Automotive XA FPGA Family.

LOW COST

XC3S50 costs $8.14 each

http://www.xilinx.com/support/documentation/spartan-3.htm

FPGA DATA SHEETS

- **Details describing the electrical specifications of a FPGA device can be found in the data sheets for the family.**
  - **Absolute Maximum Ratings for Vdd, GND, etc.**
  - **Recommended Operating Conditions**
  - **Typical Quiescent Supply Currents**
  - **Power Supply Ramp Time**
  - **Input and Output Voltage and Current Levels**
  - **Switching Characteristics for I/O, etc.**

XILINX®

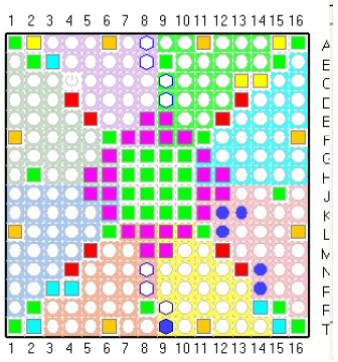
Spartan-6 FPGA Data Sheet:
DC and Switching Characteristics

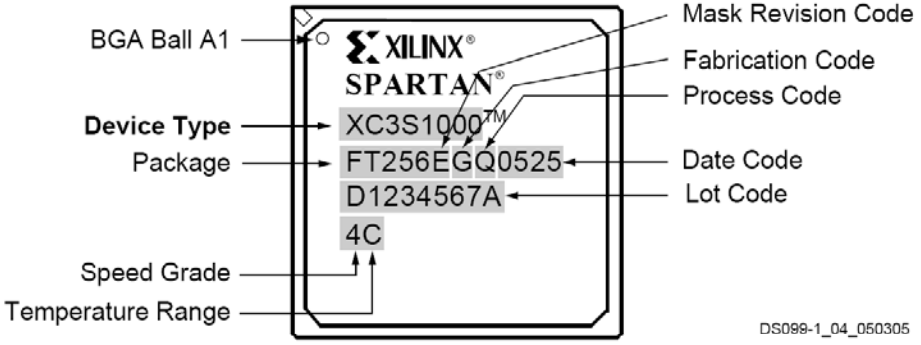
DS162 (v1.1) August 26, 2009 — Advance Product Specification

http://www.xilinx.com/support/documentation/data_sheets/ds162.pdf

MORE FPGA DOCUMENTATION

- **FPGA documentation is available for the following:**
  - **Device Reliability**
  - **Packaging and Pinouts**
  - **I/O Resources**
  - **Clocking Resources**
  - **Logic Resources**
  - **Block RAM Resource**
  - **PCB Design Guide**





http://www.xilinx.com/support/documentation/spartan-6.htm

ALTERA CPLD / FPGA FAMILIES

Low-Cost FPGAs

- Built from the ground up for low cost
- 60% faster than competing FPGAs
- Low power consumption

Cyclone® III Cyclone II Cyclone

High-End FPGAs

- High-density, high-end FPGAs
- Integrated GX transceivers variant
- Design entire systems-on-a-chip

Stratix® IV Stratix III Stratix II

Low-Cost Transceiver-Based FPGAs

- Midrange FPGAs with transceivers
- Optimized for mainstream protocols up to 3.125 Gbps
- Flip-chip packaging and fourth-generation transceivers for excellent signal integrity

Arria® II GX Arria GX

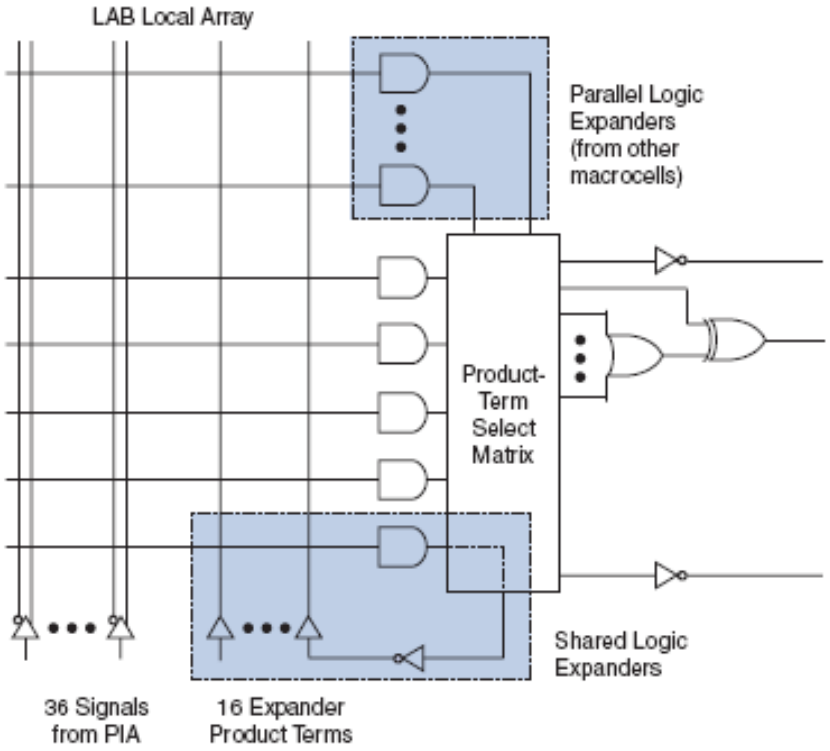
Low-Cost CPLDs

- Lowest cost CPLD ever
- Lowest power for portable apps
- Instant-on single chip solution

MAX® II MAX

www.altera.com

PLD ARCHITECTURE



LAB = Logic Array Block contains a macrocell with AND-OR logic plus local wiring.

PLD global routing increases exponentially with the number of LABs, resulting in a die dominated by routing that is cost-effective only for designs less than 8K gates.

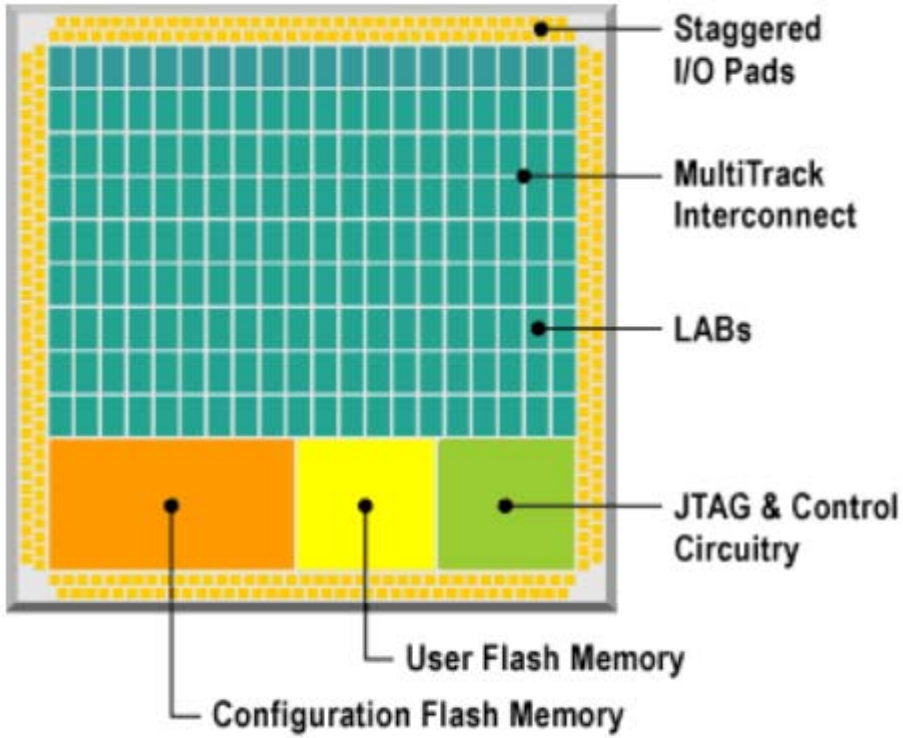
http://www.altera.com/literature/wp/wp_maxii_le.pdf

CPLD ARCHITECTURE

CPLD routing between rows and columns of LABs increases linearly with the number of LABs, resulting in an efficient die size for designs greater than 8K gates.

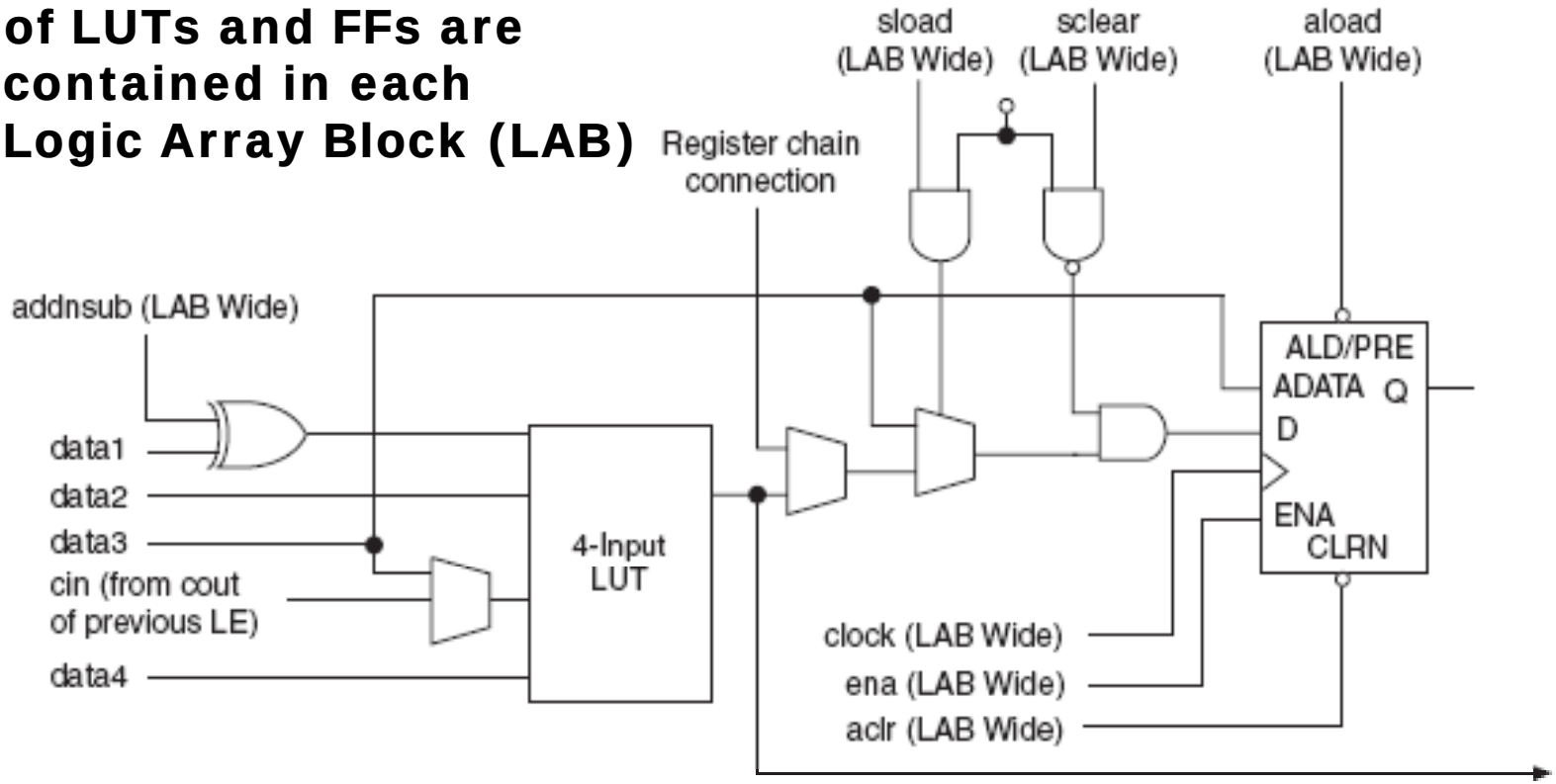
ALTERA MAX-II

www.altera.com



CPLD LOGIC ELEMENT

Ten Logic Elements (LEs) of LUTs and FFs are contained in each Logic Array Block (LAB)



1.3 LEs in a CPLD corresponds to 1 macrocell in a PLD

www.altera.com

MAX-II CPLD FAMILY

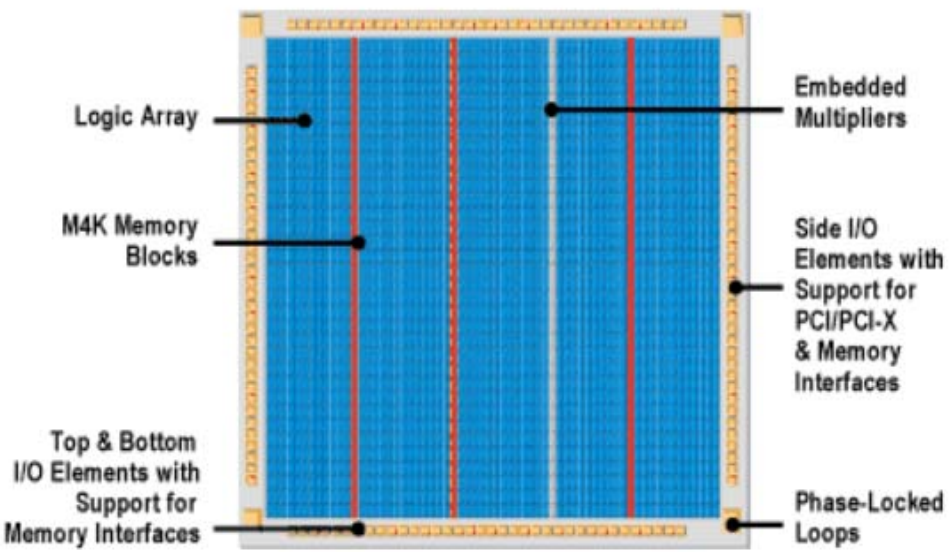
Feature	EPM240 EPM240G	EPM570 EPM570G	EPM1270 EPM1270G	EPM2210 EPM2210G	EPM240Z	EPM570Z
LEs	240	570	1,270	2,210	240	570
Typical Equivalent Macrocells	192	440	980	1,700	192	440
Equivalent Macrocell Range	128 to 240	240 to 570	570 to 1,270	1,270 to 2,210	128 to 240	240 to 570
UFM Size (bits)	8,192	8,192	8,192	8,192	8,192	8,192
Maximum User I/O pins	80	160	212	272	80	160
t_{PD1} (ns) *(1)*	4.7	5.4	6.2	7.0	7.5	9.0
f_{CNT} (MHz) *(2)*	304	304	304	304	152	152
t_{SU} (ns)	1.7	1.2	1.2	1.2	2.3	2.2
t_{CO} (ns)	4.3	4.5	4.6	4.6	6.5	6.7

http://www.altera.com/literature/hb/max2/max2_mii5v1_01.pdf

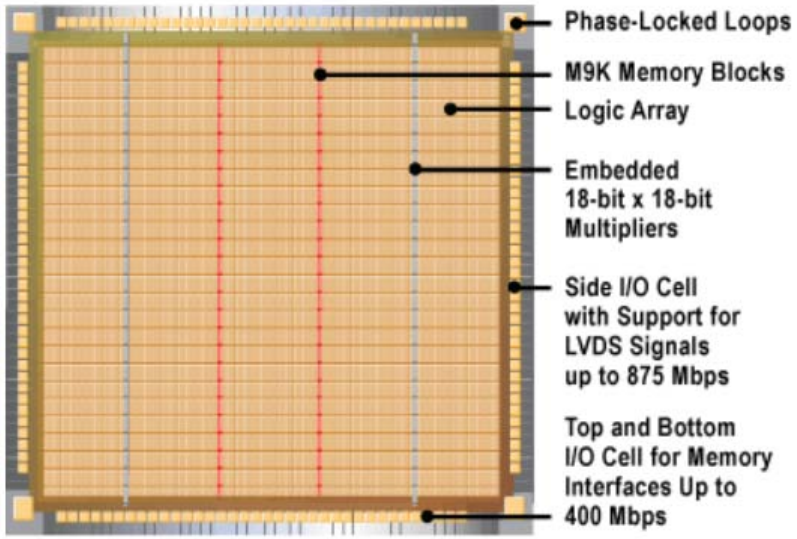
FLASH-based EPM240 costs $6.60 each

CYCLONE FPGA ARCHITECTURES

- Cyclone-II devices are made using a 90-nm process.
- Cyclone-III devices are made using a 65-nm process.
- These are SRAM-based.



CYCLONE-II

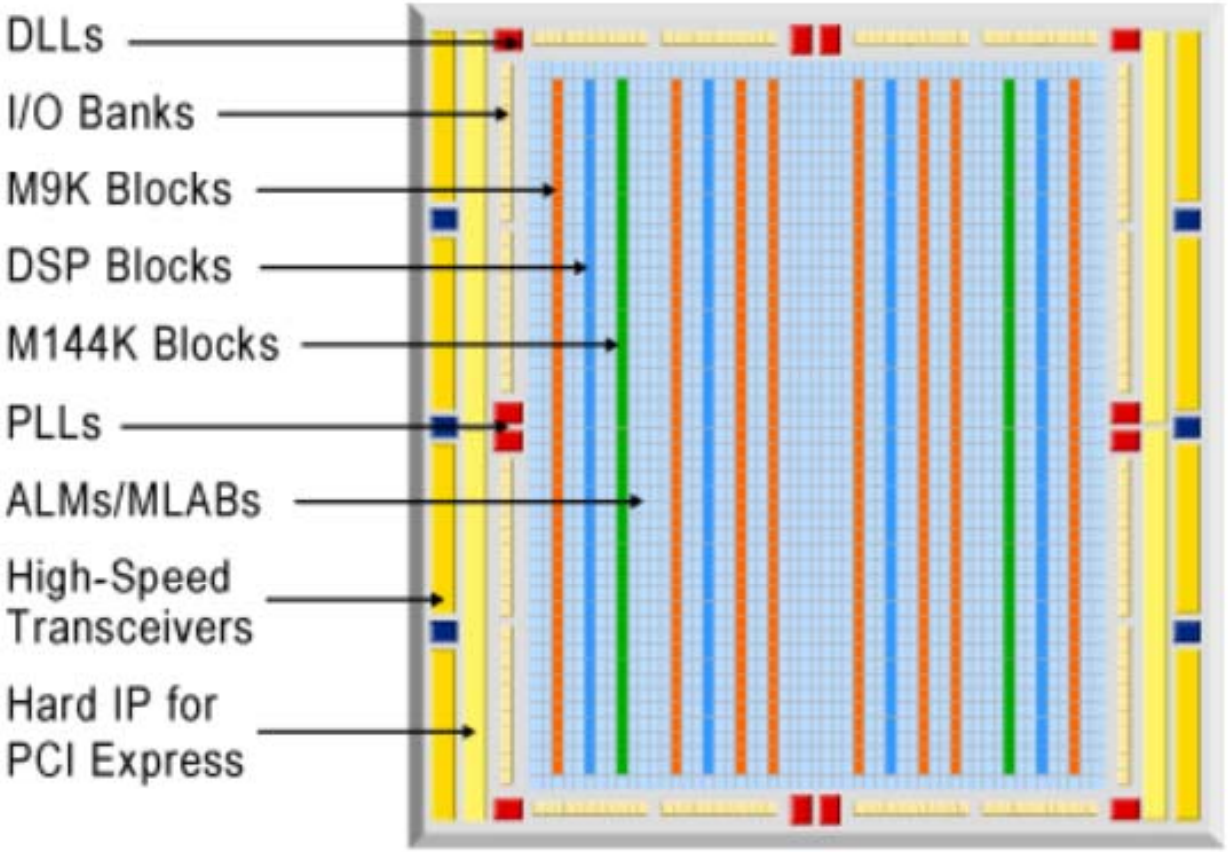


CYCLONE-III

www.altera.com

STRATIX-IV FPGA ARCHITECTURE

- **Stratix-IV devices are made using a 40-nm process.**



STRATIX-IV FPGA FAMILY

- **High performance, high capacity devices**

Stratix IV GT Variants						
Features	EP4S40G2	EP4S40G5	EP4S100G2	EP4S100G3	EP4S100G4	EP4S100G5
Equivalent LEs	228,000	531,200	228,000	291,200	353,600	531,200
Adaptive Logic Modules (ALMs)	91,200	212,480	91,200	116,480	141,440	212,480
Registers	182,400	424,960	182,400	232,960	282,880	424,960
M9K Memory Blocks	1,235	1,280	1,235	936	1,248	1,280
M144K Memory Blocks	22	64	22	36	48	64
Embedded Memory (Kbits)	14,283	20,736	14,283	13,608	18,144	20,736
MLAB (Kbits)	2,850	6,640	2,850	3,640	4,420	6,640
18 x 18 Multipliers (1)	1,288	1,024	1,288	832	1,024	1,024
PCI Express Hard IP Blocks	0	0	0	1	1	1

EP4S with 530K logic elements costs $9,660

ACTEL FPGA FAMILIES

Low-Power FPGAs

IGLOO® FPGAs

- Industry's lowest-power FPGAs
- With Flash*Freeze technology
- Available with Cortex™-M1-enabled processor core

» IGLOO Series Overview » IGLOO » IGLOO nano » IGLOO PLUS

ProASIC®3 FPGAs

- Low-power FPGAs
- Available with Flash*Freeze technology
- Offered with ARM-enabled processor cores

» ProASIC3 Series Overview » ProASIC3 » ProASIC3 nano
» ProASIC3L

Mixed-Signal FPGAs

Actel Fusion® Mixed-Signal FPGA

- Mixed-signal FPGA based on proven ProASIC3 fabric with flash RAM
- Support for soft core ARM® Cortex™-M1 and ARM7
- Embedded A/D converters and analog I/Os

» Fusion

Radiation-Tolerant Devices

RTAX FPGAs

- High-reliability, radiation-tolerant, antifuse-based FPGAs
- Designed for space applications with greater than 350 MHz system performance
- Available with embedded multiply-accumulate blocks for DSP applications

» RTAX-S/SL » RTAX-DSP

RT ProASIC3 FPGAs

- Reprogrammable, nonvolatile, radiation-tolerant, flash-based FPGAs
- For low-power space applications, requiring up to 350 MHz operation
- MIL-STD-883 Class B compliant

» RT ProASIC3

RTSX-SU FPGAs

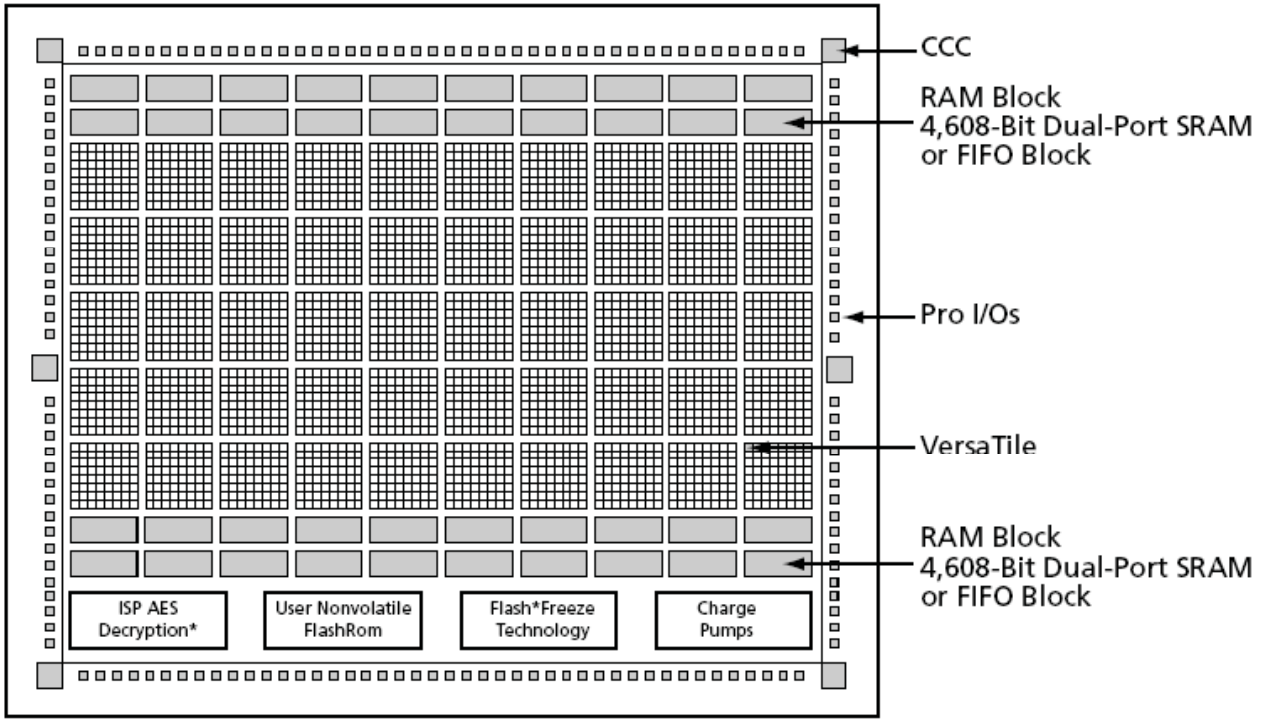
- High-reliability, radiation-tolerant antifuse-based FPGAs
- 250 MHz system performance
- Flight heritage established on many programs

» RTSX-SU

www.actel.com

ACTEL FPGA ARCHITECTURE

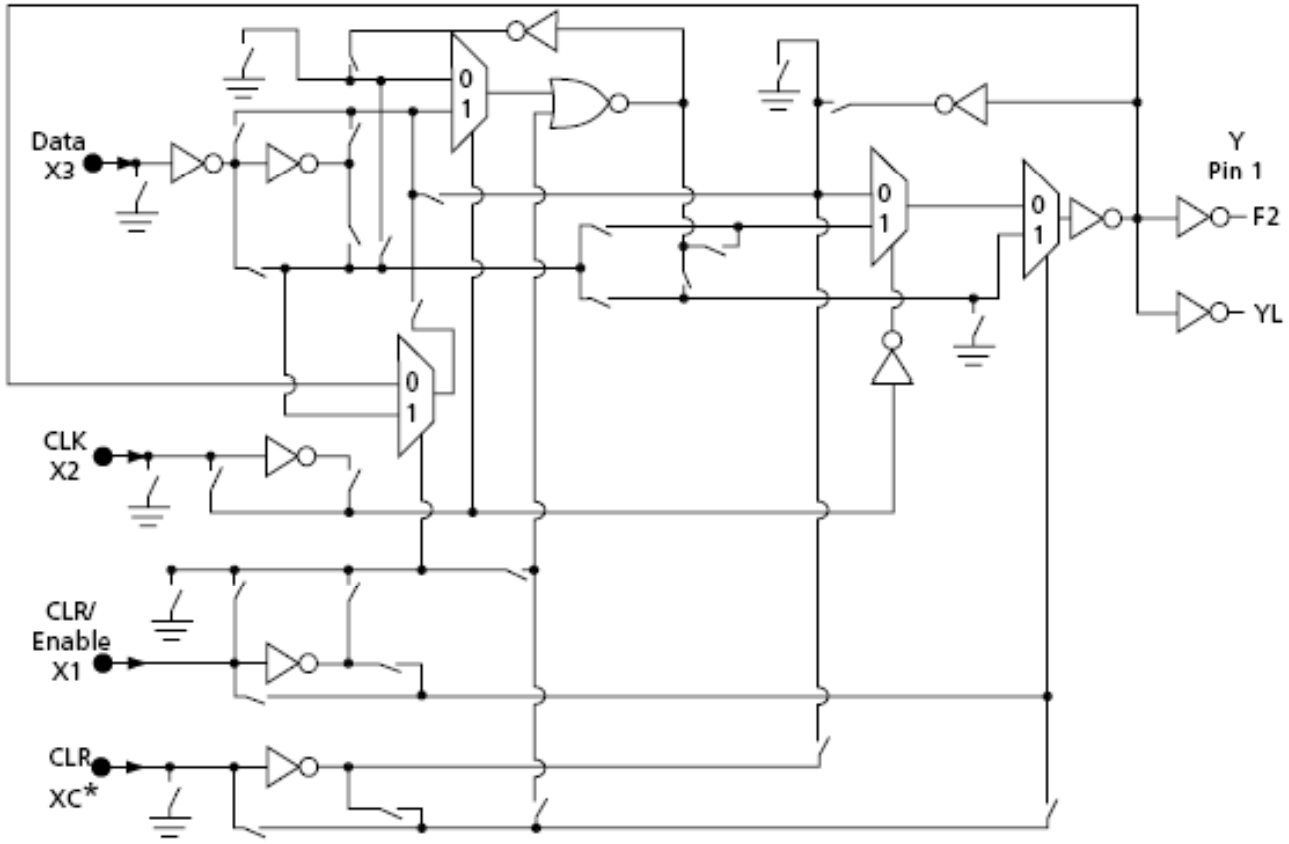
- **Actel's floorplan consists of VersaTiles of programmable logic elements (MUXs) plus Flip-Flops arrayed in two dimensions with interconnect tracks.**



RT-ProASIC3

ACTEL VersaTile LOGIC

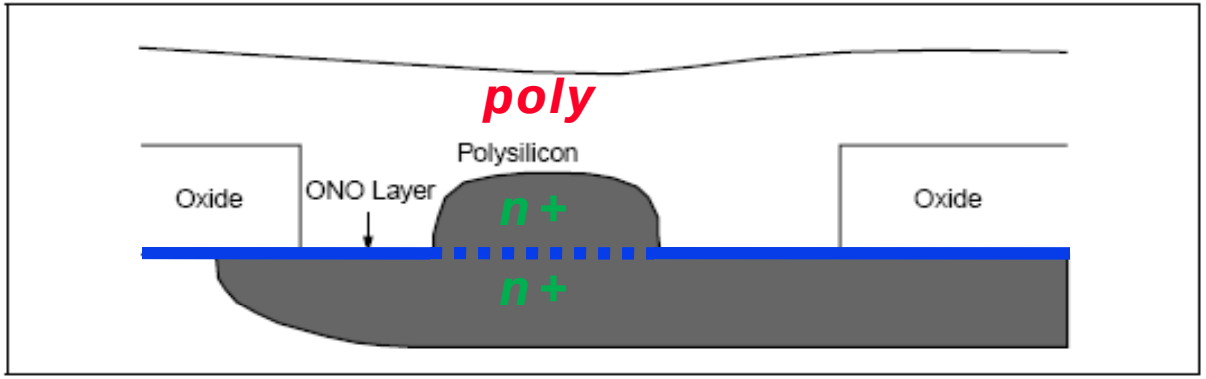
- **Actel's VersaTile logic consists of a collection of MUXs.**



http://www.actel.com/documents/RTPA3_HB.pdf

ACTEL INTERCONNECT ELEMENTS

- Actel uses a one-time programmable anti-fuse or PLICE (programmable logic interconnect element).
- Applying a current to the PLICE makes a permanent connection with less RC delay than a SRAM connection.
- Actel also offers FLASH-based devices.

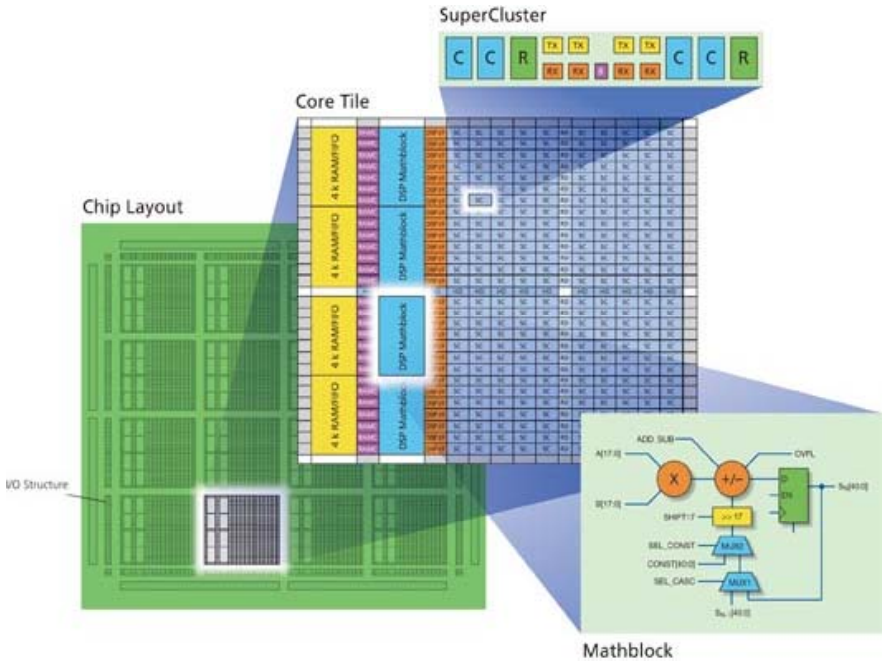


When the programming voltage is applied, the thin sandwich of ONO (oxide-nitride-oxide) melts and the base wafer grows an epitaxial "bump" into the polysilicon, allowing diffusion of the substrate n+ into the polysilicon to form a low-resistance path.

http://www.actel.com/documents/RelGuide.pdf

ACTEL RADIATION-TOLERANT FPGAS

- **Actel's RTAX family of FPGAs includes flip-flops hardened for protection against heavy ion radiation which can cause SEUs (single event upsets).**
- **RTAX-DSP also includes radiation-tolerant multiply-accumulate blocks for digital signal processing.**
- **Actel FPGAs can be one-time programmable (PLICE) or FLASH-based.**



http://www.actel.com/documents/RTAX_DSP-PB.pdf

FPGA ARCHITECTURES AND DETAILS

- A wide variety of FPGA architectures are available which can be configured using SRAM, FLASH or PLICE.
- Configuration bit files can be located inside the FPGA and/or another IC.
- Extra capacity can be used for redundancy or diagnostics.
- FPGA vendors provide synthesis and simulation tools with databases describing the internal architectures and details of each device.
- Portable HDL can retarget to multiple vendors to select the best device.
- Vendor-specific HDL can target almost any device that vendor offers.