High-Frequency CMOS Continuous-Time Filters

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Abstract — **Fully-integrated, high-frequency continuous-time filters can be realized in MOS technology using a frequency-locking approach to stabilize the time constants. A simple fully-differential integrator, optimized for phase-error cancellation, forms the basic element; a complete filter consists of intercoupled integrators. The center frequency of the filter is locked to an external reference frequency by a phase-locked loop. A prototype sixth-order bandpass filter with a center frequency of 500 kHz dissipates 55 mW and occupies 4 mm^2 in a 6 μm CMOS technology.**

I. Introduction

HIGH-PRECISION, high-order monolithic filters in the frequency range of 100 kHz to 10 MHz have many applications in communication receivers such as AM and FM IF filtering and video processing in TV circuits. Additional applications include data communications and local area networks.

Monolithic filters have previously been successfully applied to voice band applications both by utilizing the switched-capacitor technique and the continuous-time filtering method [1], [2]. However, the extension of both techniques to higher frequencies has been delayed due to many problems.

One promising approach for the implementation of high-frequency filters is the switched-capacitor technique. Recently a switched-capacitor bandpass filter at the center frequency of 260 kHz has been designed which has shown excellent performance [3]. Another switched-capacitor filter with low-pass characteristics was reported at a roll-off frequency of 2.8 MHz [4]. One major drawback to this approach is the requirement of continuous-time prefilters to band limit the input spectrum to reduce the aliasing effects. Another problem peculiar to the implementation of high-frequency switched-capacitor filters is that due to settling time limitations in state-of-the-art operational amplifiers, the extension of this technique to higher frequencies requires the lowering of the ratio of clock rate to the center frequency of the filter which brings about the necessity of higher selectivity of the antialiasing prefilters.

Another alternative is to use continuous-time filtering techniques which do not have the aliasing problem of sampled-data systems. However, due to the dependence of the center frequency of the filter on the absolute values of monolithic components such as capacitors and transistor transconductances, which are both process and temperature dependent, some extra circuitry is required to control the center frequency of this type of filters.

This paper describes a high-frequency CMOS continuous-time bandpass filtering technique which utilizes a modified version of the phase-locked loop scheme introduced by Tan [1] to precisely control the center frequency of the filter [5].

In Section II, Tan's approach is reviewed and the problems involved in the direct extension of this technique to higher frequencies are discussed. Solutions to the problems hindering the filter design are proposed in Section III, where a very simple fully differential integrator is described and a sixth-order bandpass filter is implemented. In Section IV, the center frequency control circuit is discussed. The experimental results are presented in Section V, and in the final section the capability of this technique in scaled technology is explored.

II. Extension of Low-Frequency Frequency-Locked Filtering Techniques to Higher Frequencies

The frequency-locked continuous-time filtering technique was first introduced in 1977 [1]. A low-pass voice-band filter was designed and a phase-locked loop scheme was utilized to control the roll-off frequency of the filter. Fig. 1 shows the block diagram of the system. The principle building block of the filter is an integrator. The time constant of the integrators are controlled through V_c. A voltage-controlled oscillator (VO), in conjunction with a phase-comparator, functions as a phase-locked loop. By choosing the same type of integrator for both the filter and the VCO, the bandwidth of the filter tracks the frequency of the oscillator. Thus, while the PLL is in lock, the roll-off frequency of the filter is exactly proportional to the external reference frequency.

The extension of this approach to higher frequencies involves several problems. The main problem is that the behavior of high-frequency filters is highly sensitive to analog integrator nonidealities, particularly the phase shift at the unity-gain frequency. The second problem is the

Manuscript received ; revised . This work was supported in part by the National Science Foundation under Grant ENG-442427 and also by the MOSTEK Corporation.

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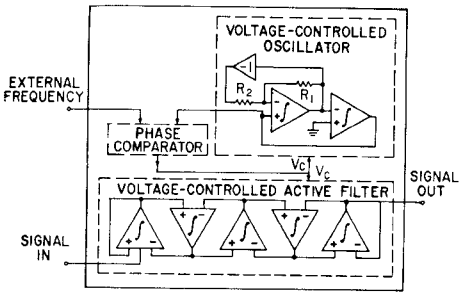


Fig. 1. Block diagram of Tan's approach to the design of low-frequency low-pass continuous time filter.

realization of a CMOS VCO with stable and repeatable center frequency in the MHz range. Because the desired filters are often highly selective (high Q), the power supply rejection (PSRR) is a critical problem. Finally, the feedthrough of the reference signal to the output of the filter can result in the degradation of the dynamic range.

The solution to the first problem will be discussed in detail in Section III. To overcome the second problem, an alternative scheme is discussed in Section IV which utilizes a voltage-controlled filter VCF instead of the conventional VCO. The last two problems are minimized by using fully differential architecture for the circuit design.

III. High-Frequency Bandpass Filter Design

This section deals with the problems associated with the filter design. In Section III-A effect of the phase-shift error in analog integrators on the performance of high-frequency filters is analyzed. In Section III-B a simple integrator is designed and an optimum channel length is derived for which the phase error terms cancel. In Section III-C resonator design considerations are covered followed by the implementation of a sixth-order bandpass filter. In Sections III-E and F the filter dynamic range considerations are discussed.

A. Effect of Integrator Nonidealities on Filter Behavior

As mentioned earlier, the main building block for ladder type active filters is an integrator. In this section the frequency response of an integrator and its effect on the filter behavior is studied.

In Fig. 2 the amplitude and phase response of an ideal integrator is illustrated. It has a pole at the origin and exactly a 90° phase shift at the unity-gain frequency. Using the definition of quality factor, the Q of the ideal integrator is found to be

$$Q_{\text{intg}}^{\text{ideal}} = \infty. \tag{1}$$

For a real integrator with finite dc gain of a, the dominant pole is pushed from the origin to a frequency equal to ω_0/a, where ω_0 is the unity-gain frequency of the integrator. Also, it may have one or more high-frequency nondominant poles. The finite dc gain causes phase lead at the unity-gain frequency and the nondominant poles

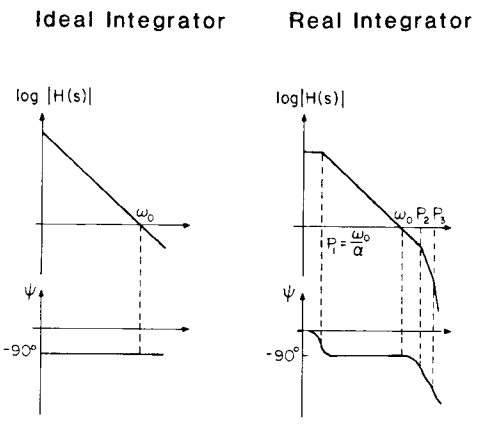


Fig. 2. Amplitude and phase response of an ideal integrator and a nonideal integrator.

result in excess phase shift. The quality factor of the real integrator Q_{intg}, assuming that all the nondominant poles p_i are at much higher frequency than the integrator unity-gain frequency, is found to be

$$\frac{1}{Q_{\text{intg}}} \approx \frac{1}{a} - \omega_0 \sum_{i=2}^{i=\infty} \frac{1}{p_i}. \tag{2}$$

The first term is equal to the phase lead at the unity-gain frequency in radian and the second-term corresponds to the excess phase. Note that as ω_0 is increased, the excess phase term becomes larger.

Fig. 3 demonstrates the effect of these two phase error components on the filter behavior. The bold curve in all three figures shows the frequency response of a sixth-order bandpass filter constructed with ideal integrators. The broken line in Fig. 3(a) shows the frequency response of the same filter made with integrators which have about 0.5° phase lead at their unity-gain frequency. This corresponds to a dc gain of 100 for the integrators. The Q is degraded in this case. In Fig. 3(b) the effect of 0.5° excess phase in integrators, which corresponds to a nondominant pole 100 times larger than the unity-gain frequency, is shown. In this case, the Q is enhanced and as mentioned earlier, as ω_0 is increased the excess phase becomes larger and may result in oscillation. Note that the error in the passband of the filter is directly proportional to $Q_{\text{filter}}/Q_{\text{intg}}$, where Q_{filter} is the quality factor of the filter. Fig. 3(c) shows the effect of exactly equal amounts of phase lead and excess phase at the unity gain frequency of the integrators, which results in phase error cancellation at this frequency. The frequency response of the filter in this case is very close to the ideal case.

These considerations suggest that it is very desirable to design the integrator in such a way that the two phase error components cancel each other right at the unity-gain frequency. However, the dependence of the two phase error components on temperature and process variations limits the accuracy of such phase error cancellation in high-frequency filtering applications and thus, in conjunction with the maximum allowable error in the passband, dic-

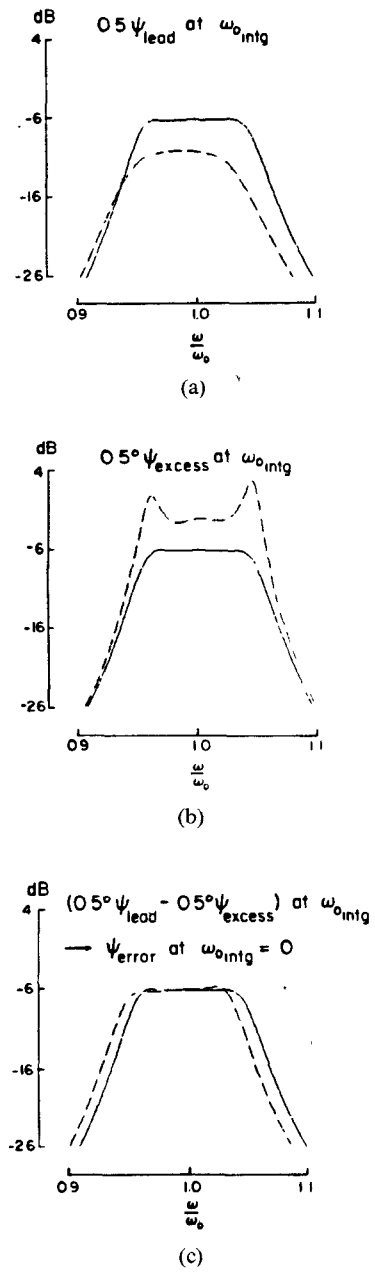


Fig. 3. Effect of integrator nonidealities on the filter behavior.

tates an upper limit for the maximum Q of the filter. This will further be explored in Section VI.

B. Integrator Design

An RC integrator is typically constructed of a multistage operational amplifier connected in the feedback configuration, as shown in Fig. 4. In the previous section, it was shown that the frequency response of high-frequency filters is very sensitive to extra phase-shift in the integrator. The high-frequency poles of the multistage operational amplifier tend to contribute large amounts of excess phase causing large error in the filter response. An important objective, then, is to design an integrator with preferably no nondominant poles.

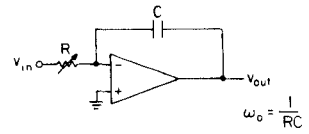


Fig. 4. Typical integrator configuration.

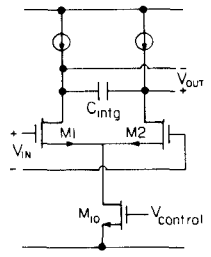


Fig. 5. Simple differential pair integrator.

To achieve this goal, a one-stage source-coupled differential pair configuration was chosen to minimize Q enhancement effects, as shown in Fig. 5. The unity-gain frequency ω_0 of this integrator is given by

$$\omega_0 = \frac{g_{m_{(M1,2)}}}{2C_{\text{intg}}} \tag{3}$$

where $g_{m_{(M1,2)}}$ is the transconductance of the input transistors and C_{intg} corresponds to the integrating capacitor. It is evident that ω_0 is process dependent and can be controlled through $g_{m_{(M1,2)}}$ by varying the drain current of the input transistors through V_{control}.

The quality factor of this integrator Q_{intg}, is found by using (2). The first term is derived by finding the dc gain of the integrator. The second term is estimated by finding an effective nondominant pole $p_{2_{\text{effective}}}$ for the integrator. The dc gain is found to be

$$a = \frac{g_{m_{(M1,2)}}}{g_{0_{(M1,2)}} + g_{0_{\text{load}}}} \tag{4}$$

where $g_{0_{(M1,2)}}$ and $g_{0_{\text{load}}}$ are the small signal output conductance of the input transistors and the load transistors. Assuming that the output resistance of the load transistors is much larger than the output resistance of the input transistors, and by substituting for $g_{m_{(M1,2)}}$ and $g_{0_{(M1,2)}}$, the gain is found to be

$$a = \frac{2}{\lambda(V_{GS} - V_{th})_{(M1,2)}} \tag{5}$$

where λ is the channel-length modulation coefficient. In practice λ is estimated from experimental data and is inversely proportional to the channel length. Here, for simplicity, a new parameter θ is introduced

$$\lambda = \frac{\theta}{L} \tag{6}$$

where θ is in the order of 0.1 $[\mu/V]$. Substituting for λ gives

$$a = \frac{2L}{\theta(V_{GS} - V_{th})_{(M1,2)}}. \tag{7}$$

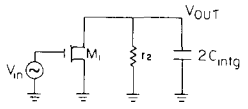


Fig. 6. Small-signal equivalent differential mode half-circuit of the integrator.

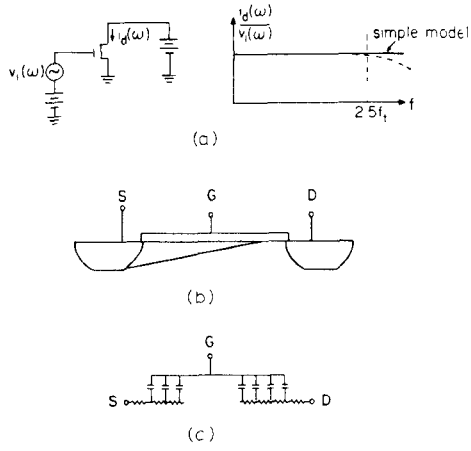


Fig. 7. The high-frequency behavior of an MOS transistor. (a) Drain current as a function of frequency. (b) Cross-sectional view of an MOS transistor in saturation. (c) The distributed channel resistance and gate capacitance.

Fig. 6 shows the small-signal equivalent differential mode half-circuit of the integrator. The circuit has only two nodes, an input node and an output node. The simple IGFET model predicts no nondominant poles for this integrator, in other words, for a transistor biased in the saturation region, a constant drain current as a function of frequency is predicted when the gate is driven by a voltage source [Fig. 7(a)]. However, a more detailed consideration of the distributed nature of the channel resistance and gate capacitance, as illustrated in Fig. 7(b) and (c), shows that the frequency response of the transconductance falls off at high frequencies. It can be shown that this phenomenon gives rise to an infinite number of high-frequency poles and an effective nondominant pole can be approximated by [6]

$$p_{2_{\text{effective}}} \approx \frac{1}{\sum_{i=2}^{i=\infty} \frac{1}{p_i}} = 2.5\omega_{t_{(M1,2)}} \tag{8}$$

where

$$\omega_{t_{(M1,2)}} = \frac{3}{2}\frac{\mu(V_{GS}-V_{th})_{(M1,2)}}{L^2}. \tag{9}$$

Note that the integrator effective nondominant pole is at a much higher frequency than for a typical operational amplifier type integrator.

Substituting from (7), (8), and (9) in (2)

$$\frac{1}{Q_{\text{intg}}} \approx \frac{\theta(V_{GS}-V_{th})_{(M1,2)}}{2L} - \frac{4}{15}\frac{\omega_0 L^2}{\mu(V_{GS}-V_{th})_{(M1,2)}}. \tag{10}$$

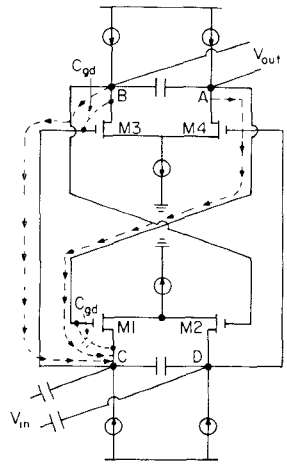


Fig. 8. Resonator implementation.

Here it is assumed that the Q of the integrating capacitor is much larger than the other components quality factor and can be neglected, which is usually the case. The above equation shows that the excess phase shift due to this phenomena is proportional to $L^2_{(M1,2)}$, whereas the phase lead due to the finite dc gain is proportional to $1/L_{(M1,2)}$. From this, the conclusion can be drawn that, for a well-characterized well-controlled process, an optimum input transistor channel length can be chosen for first-order phase error cancellation at a given frequency, which makes the realization of high-Q filters possible. The optimum input channel length will be derived in the next section.

Inspecting the differential mode half circuit, it can be seen that there is a feed-forward path between the input and the output through the C_{gd} of the input transistors (a right-half plane zero). In the next section, it will be shown that connecting the integrators in a resonator configuration results in the disappearance of the right-half plane zero.

C. Resonator Design Considerations

In Fig. 8, a resonator is implemented by connecting two integrators back to back. Note that all parasitic capacitance at the output of each integrator, as well as the gate–source capacitance of the next integrator, adds up to the integrating capacitance of the previous stage. For the resonator quality factor Q_{res}, the effect of the gate–source capacitance quality factor $Q_{C_{gs}}$, which is connected in parallel with the integrating capacitor, must be taken into account. It can be shown that for an MOS transistor operating in the saturation region, due to the distributed channel resistance and gate capacitance, the input impedance behaves as a lossy capacitance with a quality factor of [7]

$$Q_{C_{gs}} \approx \frac{5\omega_t}{\omega}. \tag{11}$$

The resonator quality factor Q_{res} is given by

$$\frac{1}{Q_{\text{res}}} = \frac{2}{Q_{\text{intg}}} + \frac{2}{Q_{C_{gs}}} \tag{12}$$

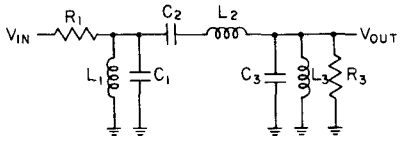


Fig. 9. Sixth-order LC ladder filter.

substituting from (10) and (11) in (12), the resonator quality factor is found to be

$$\frac{1}{Q_{\text{res}}} \approx \frac{\theta(V_{GS}-V_{th})_{(M1,2)}}{L} - \frac{4}{15}\frac{\omega_0 L^2}{\mu(V_{GS}-V_{th})_{(M1,2)}}. \tag{13}$$

It is interesting to note that the phase lag term is cut by exactly half due to the loss in the gate–source capacitances. From the equation above, by equating the two terms, an optimum channel length for the input transistor is found for which the phase error is cancelled

$$L_{\text{opt}} \approx \left[\frac{15}{4}\frac{\theta\mu(V_{GS}-V_{th})^2_{(M1,2)}}{\omega_0}\right]^{1/3}. \tag{14}$$

One interesting aspect of this resonator circuit configuration is that the right-half plane zero due to the gate–drain capacitances of the input transistors cancel out. This can be more clearly understood by inspecting Fig. 8. Lets consider node C, there are two signal feed-through paths to this node. One is from node A through the gate–drain capacitance of M_1; the other path runs from node B through the C_{gd} of M_3. As the circuit is fully balanced, the signals at nodes A and B are equal and of opposite signs, resulting in signal cancellation at node C.

D. Filter Design

The classical doubly-terminated LC ladder structure was used in the experimental chip described in Section V due to its low sensitivity to component variations (Fig. 9) [8]. The corresponding flowgraph is made of intercoupled resonators which in turn are constructed of integrators. All integrators are chosen to have the same time constant for optimum sensitivity [3].

Using the above integrator to implement the filter requires some extra buffers for both the Q-implementation and the unilateral coupling paths. To avoid the necessity of buffering and its inherent extra phase shift, the narrow-band approximation [9] is utilized to transform the unilateral coupling paths to bilateral ones. This scheme exhibits reasonable passband shape for Q greater than about 4. The realization of a sixth-order bandpass filter using the integrator described above is shown in Fig. 10. The coupling is implemented through C_k and the Q is set by adding termination devices, which will be discussed latter. The center frequency of the filter is controlled by V_{control} through varying the transconductance of all input transistors which makes the matching of these transistors critical.

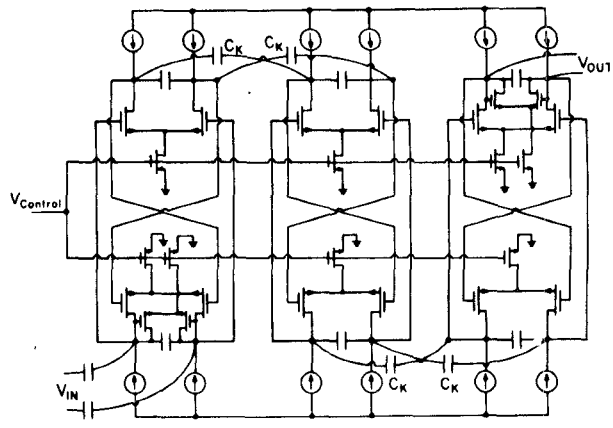


Fig. 10. Active implementation of the sixth-order ladder filter.

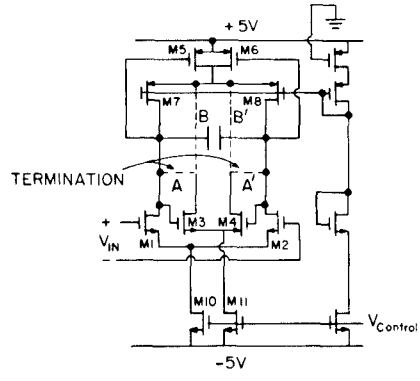


Fig. 11. Complete schematic of the integrator.

The complete schematic of the integrator is shown in Fig. 11. The common-mode output voltage is stabilized by M_5, M_6, which operate in the triode region. M_3, M_4 are the termination devices and are connected in the $(A-A')$ configuration for terminated integrators; $(B-B')$ connection is made for unterminated integrators. The quality factor of a terminated integrator $Q_{\text{intg}}^{\text{term}}$ is given by

$$Q_{\text{intg}}^{\text{term}} = \frac{g_{m_{(M1,2)}}}{g_{m_{(M3,4)}}}. \tag{15}$$

By chosing equal channel lengths for $M_{1,2}$, $M_{3,4}$, and M_{10}, M_{11}, the Q can be implemented by scaling the channel widths of these transistors. To achieve high accuracy for the Q implementation, the termination transistor is chosen as a unit transistor and the input transistors are constructed of an array of Q unit transistors connected in parallel.

E. Maximum Voltage Swing Limitations

In this section the maximum voltage swing of the integrator with acceptable performance is discussed.

The source-coupled pair configuration used for the integrator design displays nonlinear behavior as the input voltage exceeds a certain value [11]. This nonlinearity, which is a function of the gate overdrive voltage $(V_{GS}-V_{th})$ of the input transistors, gives rise to two problems.

The first problem is that as the signal level is increased the transfer function becomes more nonlinear and in the presence of unwanted signals within the passband of the filter may result in spurious signals being generated within the filter itself. For a bandpass filter, the only distortion component which may fall within the passband of the filter is the third-order intermodulation distortion, $IM3$, and for the integrator is found to be

$$IM3 \approx \frac{3}{32}\left[\frac{\hat{v}_i}{(V_{GS}-V_{th})}\right]^2 \tag{16}$$

were $\hat{v}_i$ is the peak input voltage. As an example for a maximum allowable distortion $IM3 = 1$ percent and $(V_{GS} - V_{th})$ of 1.5 V the maximum peak input voltage is computed to be 490 mV.

The second problem is due to the fact that, as the equation below suggests, the input transistor transconductance G_m decreases as the input signal level is increased:

$$G_m \approx g_m\left[1-\frac{3}{8}\left(\frac{\hat{v}_i}{(V_{GS}-V_{th})}\right)^2\right] \tag{17}$$

where g_m is the small signal transconductance. This in turn decreases the unity-gain frequency of the integrator and lowers the center frequency of the filter. The above consideration is of particular importance for the design of high-Q filters.

By simple circuit techniques, such as adding a cross-coupled pair to the input circuit, both problems can be improved. It can be shown that an increase of about 5 to 15 dB in the maximum input signal with acceptable performance can be achieved by properly scaling the W/L ratios of the source-coupled pair and the cross-coupled pair [7].

F. Filter Noise Performance

Assuming that for the frequency range of interest, the $1/f$ noise of the integrator transistors is negligible, and accounting for the thermal noise of both the input transistors and the load transistors, the input referred noise spectral density of the integrator is found to be

$$S_i(f)_{\text{intg}} = 8kT\frac{1}{g_{m_{(M1,2)}}} \tag{18}$$

for

$$\frac{g_{m_{(M1,2)}}}{g_{m_{(M7,8)}}} = 2.$$

The total output noise power of a typical doubly-terminated sixth-order ladder bandpass filter implemented with identical integrators is found to be [7]

$$\overline{v_{\text{out}}^2} = S_i(f)_{\text{intg}} \times \frac{3\pi}{2} \times Q \times f_0 \tag{19}$$

where $S_i(f)_{\text{intg}}$ is assumed to be frequency independent, f_0 corresponds to the center frequency of the filter, and Q is the quality factor of the terminated resonators which,

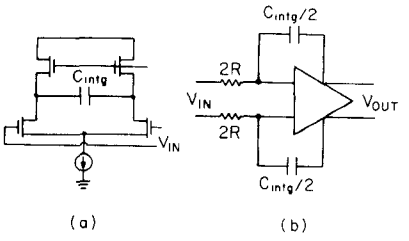


Fig. 12. (a) The simple differential pair integrator. (b) An operational amplifier type fully differential integrator.

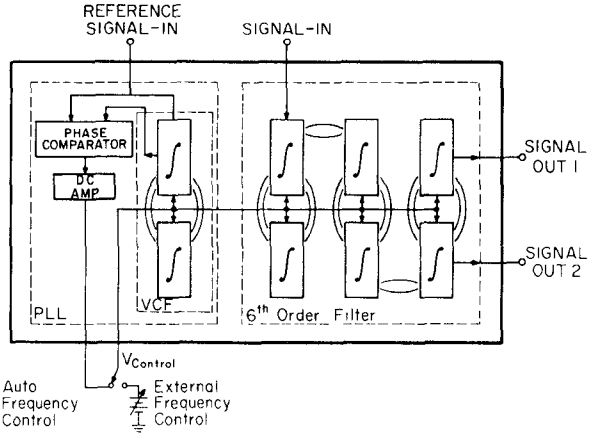


Fig. 13. Block diagram of the filter and the center frequency control circuit.

depending upon the desired shape of the filter frequency characteristics, ranges from one to two times the overall Q of the filter. Substituting for $S_i(f)$ and f_0, the total output noise power is found to be

$$\overline{v_{\text{out}}^2} = 3\frac{kT}{C_{\text{intg}}}Q. \tag{20}$$

It can be demonstrated that the same filter implemented with operational amplifier type fully differential integrators of Fig. 12(b) would exhibit four times more output noise power for equal total integration capacitance. This occurs because of the bridge connection of the integrating capacitance as illustrated in Fig. 12(a).

Since in recursive bandpass filters the output noise power is inversely proportional to the integrating capacitor value, for the above integrator the noise can be drastically reduced by choosing higher values for the integrating capacitors and paying a price in terms of higher power consumption and die area. Whereas in switched-capacitor technique the dependence of the operational amplifier settling time on the integrating capacitance limits the integrating capacitance to relatively small value for high-frequency filters. This in turn makes the achievement of low values of output noise easier in this techniques than in switched-capacitor filters.

IV. Center Frequency Control Circuitry

The block diagram of the filter and the center frequency control circuitry is shown in Fig. 13. The center frequency of the filter can either be controlled externally, or an

on-chip PLL locks the center frequency of the filter to an external reference frequency.

The PLL uses an exact replica of the main filter's second-order section instead of the conventional VCO. The phase detector compares the phase difference ϕ between the input and output of the filter and generates an error voltage v_{error} proportional to this phase difference

$$v_{\text{error}} \approx K v_{\text{in}} v_{\text{out}}^{\text{filt}} \cos\phi \tag{21}$$

where K is the phase detector conversion factor and v_{in} and $v_{\text{out}}^{\text{filt}}$ are the rms values of the input voltage and the second-order filter output voltage. This voltage is then amplified and used to change the center frequency of the filter in a direction which reduces the difference between the two frequencies.

The second-order filter has two outputs. The bandpass output has a 180° phase shift at the center frequency with respect to the input signal. The other output has a high-pass characteristic with a peaking at the center frequency and 90° phase shift at this frequency. The fact that the output of the phase detector is proportional to $\cos\phi$, makes the high-pass output suitable to be used to generate the error voltage. Fig. 14(a) shows the amplitude and phase response of the second order filter output. In Fig. 14(b) the corresponding open loop error voltage is shown. The error voltage is zero for $f = f_0$ and is at its maximum for $f = f_0(1 \pm 1/2Q)$. Once the loop is closed, this voltage changes the center frequency of the filter and reduces the difference between the two frequencies.

The loop gain of the PLL is a function of the second-order filter Q, amplitude of the reference signal, phase detector conversion factor, and the dc amplifier gain. It can be shown that there exists an error between the locked center frequency f_0^{locked} and the reference frequency f_{ref} which tends to increase as the difference between the unlocked center frequency f_0^{unlocked} and the reference signal is increased.

$$f_0^{\text{locked}} = f_{\text{ref}} + \frac{f_0^{\text{unlocked}} - f_{\text{ref}}}{A_{\text{PLL}}} \tag{22}$$

where A_{PLL} corresponds to the phase-locked loop dc gain and is in the order of few hundreds. This error is usually negligible; as an example for a capture range of 30 percent and loop gain of 150 the maximum error is only 0.1 percent.

For the PLL circuit design a CMOS version of the Gilbert type phase-detector is used. The schematic of the dc amplifier and the voltage to current converter is shown in Fig. 15. C_{c1}, C_{c2}, and MA_8, MA_9 perform as a lag-lead type loop filter [10] which generate a pair of left-hand plane pole and zero. The compensation capacitor is Miller multiplied and the frequency response of the loop benefits from the pole-splitting effect of this configuration [11]. The pole location of the loop filter controls the bandwidth and thus, the capture range of the PLL. The zero location can be varied by changing the voltage on the gates of MA_8 and MA_9, and is utilized to increase the loop phase margin.

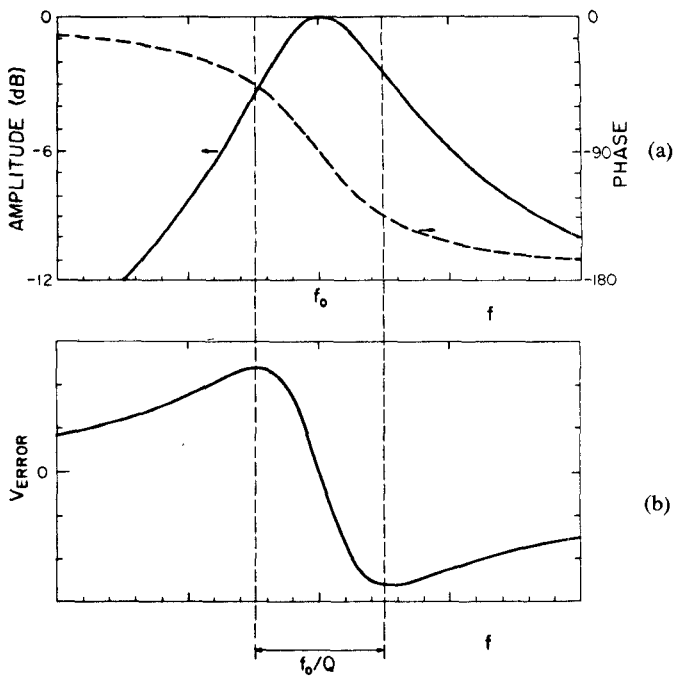


Fig. 14. (a) Amplitude and phase response of the filter output. (b) Open-loop error voltage.

Note that a significant source of extra phase shift, which can result in instability, is that V_{control} has to drive a relatively high capacitance (in this case, eight current source transistor gates). To overcome this problem, $g_{m_{MI3}}$ must be chosen to be sufficiently high.

The fully differential architecture ensures low reference signal feed-through to the output of the filter.

V. Experimental Results

An experimental prototype sixth-order bandpass filter with a center frequency of 500 kHz was designed and fabricated. Fig. 16 shows the microphotograph of the experimental chip. A 6 μm single-poly n-well CMOS technology was used and the die area is about 4 mm^2.

In Fig. 17(a) the overall frequency response of the filter is shown. The detailed passband of the two different outputs of the filter is seen in Fig. 17(b). The frequency response of the filter is very close to the designed shape and a ± 10 percent variation in the power supply voltage produced no significant change in the filter frequency response.

The functionality of the PLL is shown in Fig. 18; note that the markers are added externally to indicate the reference frequency. First, a reference frequency at 450 kHz is applied, the filter frequency response locks to this frequency. Then the reference frequency is changed to 500 kHz, the filter follows this change. The last curve is for a reference frequency at 550 kHz. This corresponds to a 20 percent lock range for the phase-locked loop.

In Table I the results for the sixth-order bandpass filter for 10 V supply voltage is summarized. The total in-band noise is found from Fig. 19 to be about 30 μV rms for a

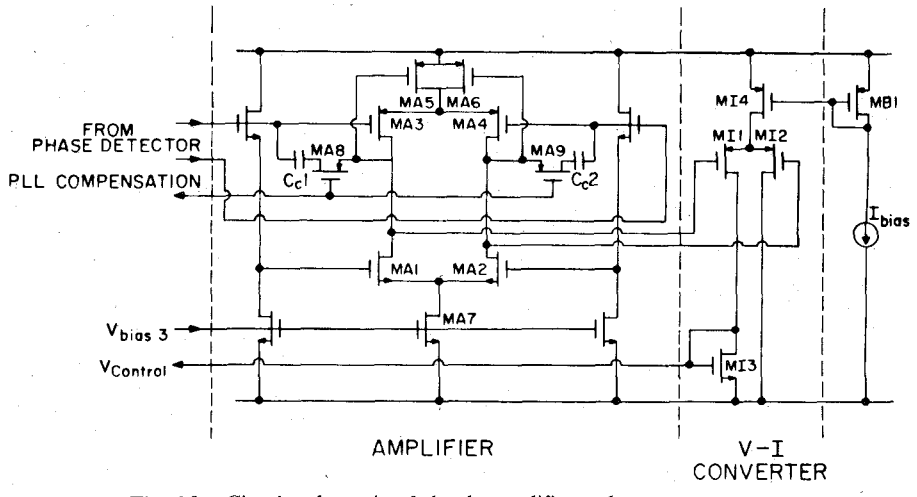


Fig. 15. Circuit schematic of the dc amplifier, voltage to current converter, and loop filter.

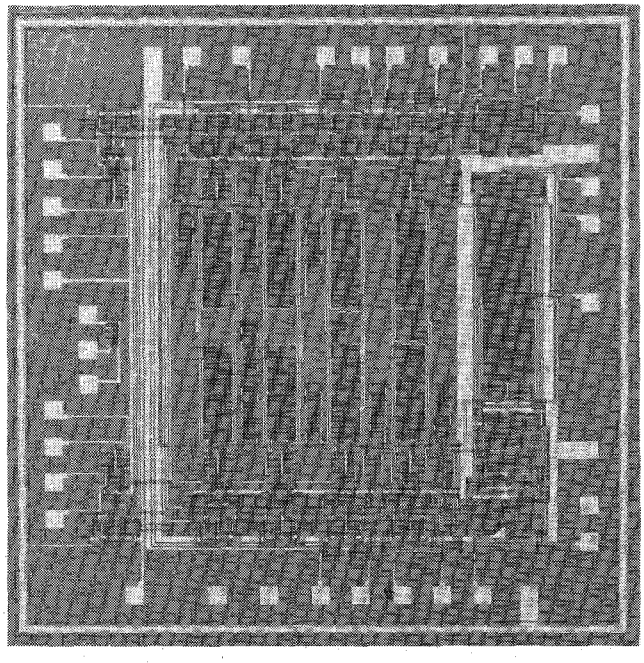
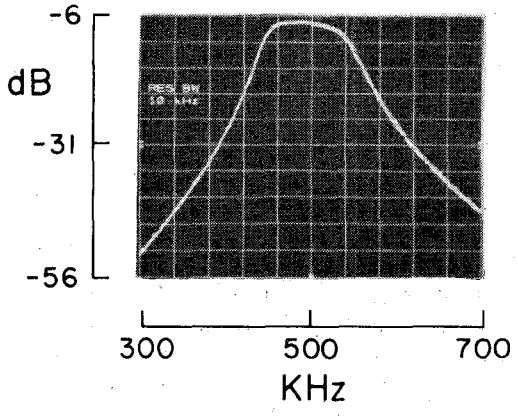
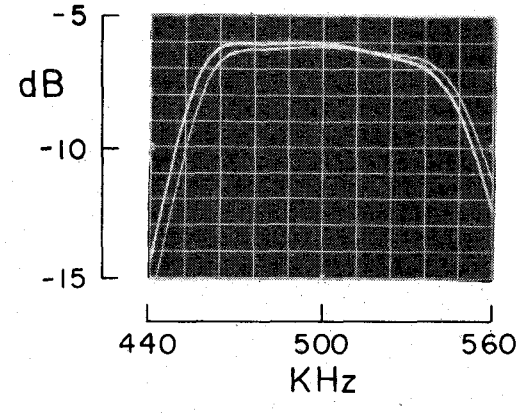


Fig. 16. Microphotograph of the experimental chip.



(a)



(b)

Fig. 17. (a) Overall frequency response of the prototype. (b) Detailed passband of two outputs of the filter.

bandwidth of 96 kHz. In order to compare the experimental noise to the theoretical noise, the prototype values of $C_{\text{intg}} = 38$ pF and $Q_{\text{res}} = 8$ is substituted in (20), which gives a total output noise of 50 μV rms. This is reasonably consistent with the experimental result as most of the noise power falls within the passband of the filter. The center frequency of the filter was controlled externally for the noise measurement. In Table I, the reference signal feedthrough at the output of the filter is given to be 100 μV rms which exceeds the output noise and degrades the dynamic range by 10 dB. The relatively high reference signal feedthrough is partly due to the fact that for debugging purposes some extra nodes were connected to bonding pads which increased the parasitic couplings. Another reason for this is due to some asymmetry in the filter layout. The power supply rejection for both supplies is measured from Fig. 20(a) and Fig. 20(b) and is better than 35 dB. It is believed that a perfectly symmetrical layout and better component matching should improve both the power supply rejection and the reference signal feed-through.

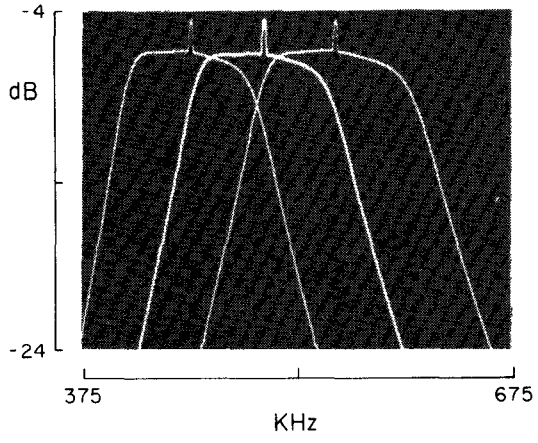


Fig. 18. PLL functionality test.

Center frequency	500KHz
-3dB bandwidth	96KHz
Total in-band noise	30μVrms
Reference signal feed-thru	100μVrms
Dynamic Range 1% intermodulation	60dB
Minimum PSRR ($+V_{DD}$)	-35dB
Minimum PSRR ($-V_{SS}$)	-38dB
Power dissipation	55mW

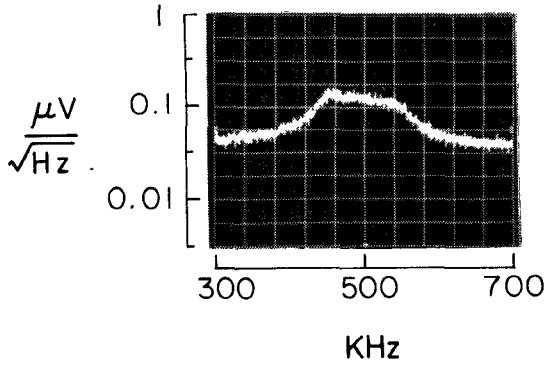


Fig. 19. Measured noise response of the filter.

VI. Conclusion

To conclude, the capability of this technique in a scaled technology is projected. As was mentioned earlier, the Q of the integrator, due to phase error components, is process dependent and the error in the filter passband is proportional to $Q_{\text{filter}}/Q_{\text{intg}}$. A worst-case value for Q_{intg} for different center frequencies was found under the following conditions:

± 15 percent tolerance in process parameters (μ, λ)

1 μm uncertainty in polysilicon width.

Assuming 1 dB maximum error in filter passband and using the worst-case values of Q_{intg}, a maximum value for Q_{filter} as a function of center frequency is derived and sketched in Fig. 21. This figure shows a maximum Q of about 50 at the center frequency of 100 kHz and the maximum Q drops down to about 2.5 for 100 MHz. With the progress of processing technology (e.g., more accurate

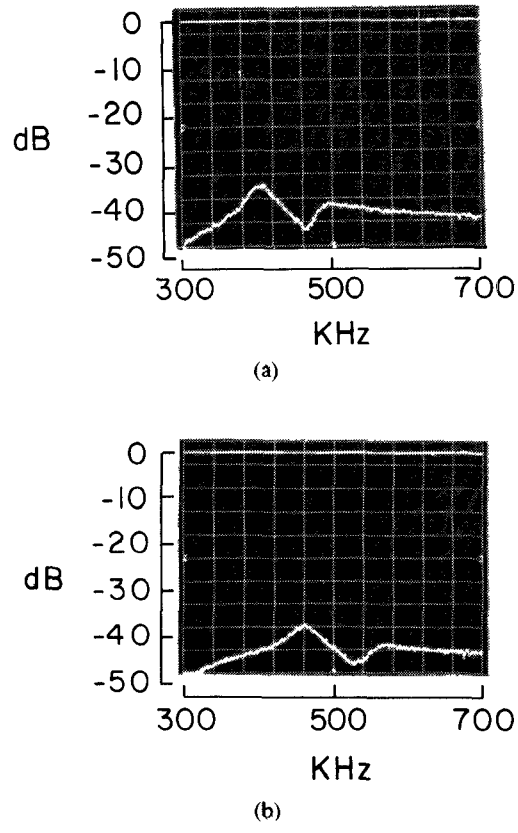


Fig. 20. (a) PSRR with respect to the positive supply. (b) PSRR for the negative supply.

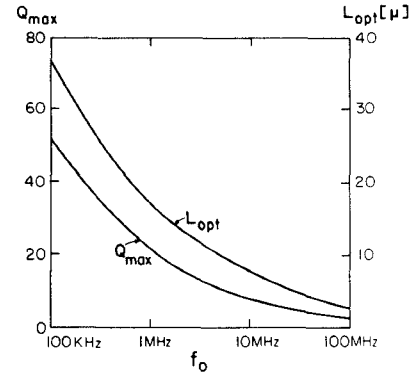


Fig. 21. The maximum achievable Q as a function of frequency. The optimum input transistor channel length for filters as a function of center frequency.

polysilicon etching), the maximum achievable Q can be improved.

The other curve shows the optimum input transistor channel length for different frequencies. From this curve it can be concluded that the implementation of filters with center frequencies up to 20 MHz can be realized in a 6 μm technology, and a 100 MHz filter requires a 3 μm technology.

A design approach to implement high-frequency continuous-time filters was presented. From the experimental performance of the filter it can be concluded that this technique is indeed a viable method for the implementation of high-frequency filters.

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From 1972 to 1974, she was working for the Berkeh Company, Tehran, Iran, and was responsible for their primary standard laboratory. In 1974 she joined the Radio Shahab Manufacturing Company in Tehran, where she was involved in the design of television and test equipment circuits. Since 1977 she has been a Teaching and Research Assistance at the University of California, Berkeley, while working toward a Ph.D. degree.

Paul R. Gray (S'65–M'69–SM'76–F'81), for a photograph and biography, see this issue, p. 819.

Random Error Effects in Matched MOS Capacitors and Current Sources

JYN-BANG SHYU, GABOR C. TEMES, FELLOW, IEEE, AND FRANCOIS KRUMMENACHER

***Abstract*—Explicit formulas are derived using statistical methods for the random errors affecting capacitance and current ratios in MOS integrated circuits. They give the dependence of each error source on the physical dimensions, the standard deviations of the fabrication parameters, the bias conditions, etc. Experimental results, obtained for both matched capacitors and matched current sources using a 3.5 μm NMOS technology, confirmed the theoretical predictions. Random effects represent the ultimate limitation on the achievable accuracy of switched-capacitor filters, D/A converters, and other MOS analog integrated circuits. The results indicate that a 9-bit matching accuracy can be obtained for capacitors and an 8-bit accuracy for MOS current sources without difficulty if the systematic error sources are reduced using proper design and layout techniques.**

Manuscript received June 8, 1984; revised July 30, 1984. This work was supported by the National Science Foundation under Grants ECS 81-05166 and ECS 83-15221 and by the Xerox Corporation and the University of California under MICRO Grant 104.

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I. Introduction

THE metal–oxide–semiconductor (MOS) technology employed in the large-scale integrated (LSI) fabrication of digital circuits has been also used recently to realize

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