HOMEWORK – SYNTHESIS, PLACE & ROUTE, POST-LAYOUT SIMULATION

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Purposes: Perform pre-synthesis simulation using *ModelSim*,
synthesis using *Synplify_Premier_DP*,
place & route using *Xilinx* and
post-layout simulation using *ModelSim*.

Tutorial

To begin, copy the appropriate files to the new subdirectory:

1. **cp ~bouldin/webhome/protected/551-hw3.tar.gz .**

2. Now, unzip and untar them:

. **gunzip 551-hw3.tar.gz; tar –xvf 551-hw3.tar**

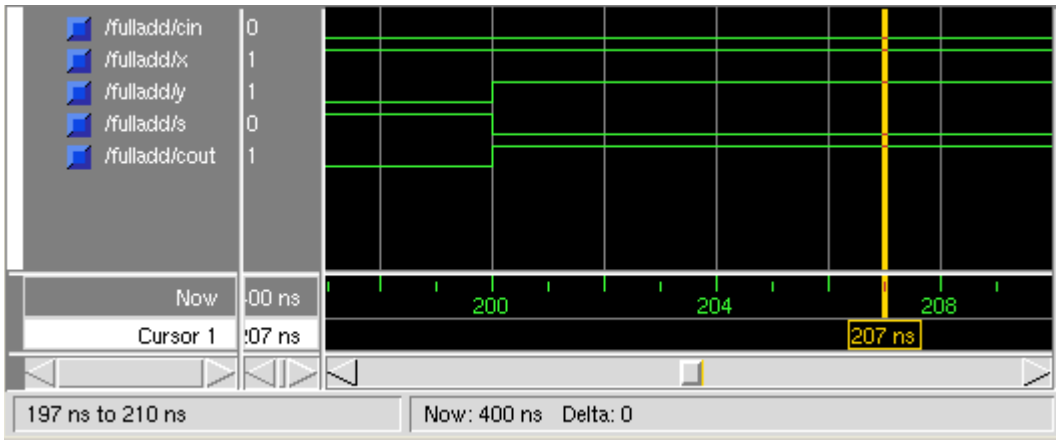
3. Move down to the subdirectory:

cd 551-hw3

Now, perform pre-synthesis simulation on fulladd.vhd by typing:

4. **./presynth-sim fulladd**

This will bring up the following window:



Note that the inputs and outputs both change instantly at 200 ns.

Now, synthesize the VHDL source file using *Synplify_Pro* into the Spartan3 part by typing:

5. **synplify_premier_dp –batch -tcl synplify-spartan3.tcl**

The synthesized net-list is now under a subdirectory, rev_1, so copy the appropriate files:

6. **cp spartan3-fit rev_1**; **cp spartan3-view rev_1**

7. **cp vsim-post-spartan3 rev_1; cp stim-fulladd.do rev_1**

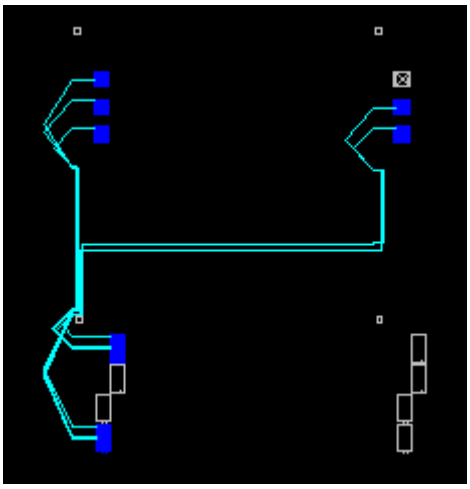
8. **cd rev_1**

Generate the Spartan3 layout using the *Xilinx* fitter:

9. ./**spartan3-fit fulladd**

View the layout by typing:

10. **./spartan3-view fulladd &**



Note the number of slices and longest path delay by observing:

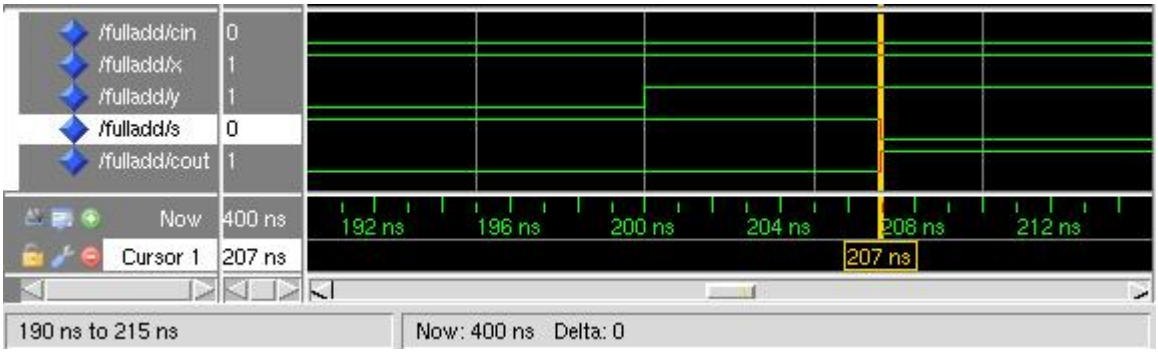
11. **grep Slices fulladd_r.par** **2 slices out of 1920**

more fulladd_r.twr **cin → cout 6.787 ns**

Peform post-layout simulation by typing:

12. ./v**sim-post-spartan3 fulladd**

Note that the outputs change at 207 ns instead of instantly at 200 ns:



APPENDIX

fulladd.vhd

```
-- Brown Example Appendix A.7a
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY fulladd IS
        PORT (      Cin, x, y       : IN     STD_LOGIC ;
                    s, Cout         : OUT  STD_LOGIC ) ;
END fulladd ;

ARCHITECTURE LogicFunc OF fulladd IS
BEGIN
        s <= x XOR y XOR Cin ;
        Cout <= (x AND y) OR (x AND Cin) OR (y AND Cin) ;
END LogicFunc ;
```

presynth-sim

```
#./presynth-sim
vlib work
vcom -work work fulladd.vhd
vsim fulladd -do stim-fulladd.do
```

stim-fulladd.do

```
add wave cin x y s cout
force cin 0
force x 0
force y 0
run 100
force cin 0
force x 1
force y 0
run 100
force cin 0
force x 1
force y 1
run 100
force cin 1
force x 1
force y 1
run 100
```

synplify-spartan3.tcl

```
#synplify_premier_dp -batch -tcl synplify-spartan3.tcl
project -new proj.prj
add_file fulladd.vhd
impl -add rev_1
impl -active "rev_1"
set_option -technology spartan3
set_option -part xc3s200
set_option -package ft256
set_option -grade -5
set_option -synthesis_onoff_pragma 0

#map options
set_option -frequency 50.00
set_option -fanout_limit 500
set_option -pipe 0
set_option -retiming 0
set_option -fixgatedclocks 0
project -run synthesis
```

spartan3-fit

```
#./spartan3-fit filename
source /usr/local/xilinx/10.1/ISE/settings64.sh
ngdbuild   $1.edf
map -cm speed  -timing $1.ngd
par $1.ncd -w $1_r.ncd
trce -u 100  $1_r.ncd -o $1_r.twr
netgen -sta -w $1_r.ncd $1_sta.v -ofmt verilog
netgen -sim -tb -w $1_r.ncd $1_sim.vhd -ofmt vhdl
```

spartan3-view

```
#spartan3-view filename
source /usr/local/xilinx/10.1/ISE/settings64.sh
fpga_editor $1_r.ncd
```

vsim-post-spartan3

```
#./vsim-post-spartan3 filename
vlib work
vmap simprim   /usr/local/xilinx/10.1/ISE/vhdl/mti_se/simprim
vcom -work work $1_sim.vhd
vsim $1 -do stim-$1.do -sdftyp $1_sim.sdf
```