A 4-MHz CMOS Continuous-Time Filter with On-Chip Automatic Tuning

FRANÇOIS KRUMMENACHER AND NORBERT JOEHL

Abstract — **This paper presents a third-order elliptic low-pass continuous-time filter with a 4-MHz cutoff frequency, integrated in a 3-μm p-well CMOS process. The design procedure is based on the direct simulation of a doubly terminated *LC* ladder filter by means of capacitors and fully balanced, current-controlled transconductance amplifiers with extended linear range. The on-chip automatic tuning circuit uses a phase-locked loop implemented with an 8.5-MHz controlled oscillator that matches a specific two-integrator loop of the filter. The complete circuit features 70-dB dynamic range (THD < −50 dB) and consumes only 16 mW from ±2.5-V supplies.**

I. Introduction

INTEGRATED continuous-time filters are suitable solutions to perform a variety of signal processing tasks. Examples include radio and video frequency filtering applications and anti-aliasing filters in digital or switched-capacitor (SC) systems.

Two main approaches to the design of such filters that are fully compatible with current CMOS technologies have been successfully used to date. One combines MOS transistors used as voltage-controlled resistors together with capacitors and MOS operational amplifiers to realize the so-called "MOSFET-C active filters" [1], [2] whereas the other one makes use of capacitors and MOS transconductance elements only [3], [4]. In any case, an automatic tuning circuitry is necessary to maintain precise filtering characteristics against process variations, temperature drift, aging, etc.

This paper is relevant to the second approach and describes a novel class *A* transconductance element with improved linearity performance and its application to continuous-time filtering at video frequencies. The automatic tuning control and related problems are also discussed in detail.

II. Basic Design Considerations

As a starting point, it is worth considering the simple differential pair integrator proposed in [3] (Fig. 1). In addition to its simplicity, tunability, and area efficiency, this integrator configuration potentially achieves the best high-frequency performance because it makes use of a single source-coupled differential pair to implement the voltage-to-current converter function (as opposed to configurations with multistage operational amplifiers which suffer from large amounts of excess phase at high frequency, causing unacceptable errors in the filter response).

Although requiring additional circuitry to provide for common-mode feedback, a balanced output will improve both the dynamic range and the power supply rejection which become critical parameters in high-frequency applications for mixed analog/digital systems.

One major disadvantage of this elementary integrator, however, is that in order to maintain harmonic or intermodulation distortions at acceptable levels and to limit the unity-gain frequency shift [3] due to the nonlinear behavior of the source-coupled pair, the current modulation in the transistors must be kept low. Consequently both the signal-to-noise ratio and the efficiency (the ratio of the maximum signal power to the supply power consumption) are limited.

Several circuit techniques for improving the linearity of MOS transconductance elements have been proposed in the literature. In [5], linearization is achieved by simply adding an auxiliary cross-coupled differential pair to the source-coupled pair and by properly scaling their W/L ratios and tail currents. Another possibility is to degenerate the source-coupled pair by means of a MOS transistor operating in the triode region [6]. A combination of both techniques yields even better linearity performance [6], [7]. Other linearization methods use grounded-source triode-mode MOST's [8], cross-coupled quad configurations [9], or class *AB* operation [10]–[12].

Although offering better linearity performance and lower quiescent power dissipation, class *AB* operation leads to increasing electromagnetic compatibility problems (e.g., crosstalk via supply lines and substrate) and is therefore not to be considered for filtering applications in the megahertz range and above. Solutions involving current mirroring [9]–[12] or sophisticated cascode devices [8] must also be rejected because they suffer from significant excess phase at high frequency.

Starting from the standpoint that simplicity and good high-frequency performance are the essential features of a

Manuscript received November 16, 1987; revised January 7, 1988. This work was supported by the Hasler Foundation, Bern (project AGEN 24).

The authors are with the Electronics Laboratory, Swiss Federal Institute of Technology (EPFL), DE-Ecublens, CH-1015 Lausanne, Switzerland.

IEEE Log Number 8819981.

0018-9200/88/0600-0750$01.00 ©1988 IEEE

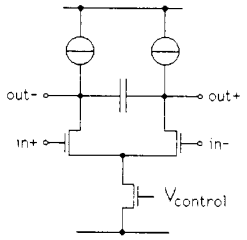


Fig. 1. Simple differential pair integrator.

linearized transconductance amplifier intended for video filtering applications, a new balanced voltage-to-current converter derived from [3] and [6] was developed. This circuit is described in the next section.

III. A New Linear CMOS Transconductor

The schematic diagram of a fully balanced transconductance amplifier with a novel four-transistor input stage (shown in thick lines) is depicted in Fig. 2. Transistors $M1$ and $M1'$, biased by current sources $M3$ and $M3'$, form the input differential pair, the transfer characteristic of which is linearized by the voltage-controlled degenerating "resistors" $M2$ and $M2'$. The common-mode output voltage is stabilized by $M5$ and $M5'$, which operate in the triode region [3].

In order to get a qualitative understanding of the behavior of this new input stage, the circuit is first analyzed using the simple square-law MOSFET model and assuming that $M1$, $M1'$, $M2$, and $M2'$ are in a common well (e.g., connected to V_{SS}). For convenience, the following parameters are introduced:

$$a = 1 + \beta_1/4\beta_2 \tag{1}$$

and

$$g_{m0} = \left.\frac{\partial I_{out}}{\partial V_{in}}\right|_{V_{in}=0} = \frac{I_{bias}}{a(V_{GS}-V_T)_{M1}}. \tag{2}$$

For low values of the input voltage V_{in}, transistors $M2$ and $M2'$ are working in the triode region and the following normalized transfer characteristic is easily obtained (here a purely differential input voltage is assumed):

$$i = v\sqrt{1-v^2/4} \tag{3}$$

where

$$v = g_{m0}V_{in}/I_{bias} \tag{4}$$

$$i = I_{out}/I_{bias}. \tag{5}$$

From the above equations, it may be concluded that within a limited input voltage range the transfer characteristic of the input transconductance element is similar to that of a conventional source-coupled pair biased at a gate overdrive voltage equal to $a(V_{GS}-V_T)_{M1}$. Deviation from this well-known behavior occurs when either $M2'$ (for $V_{in}>0$)

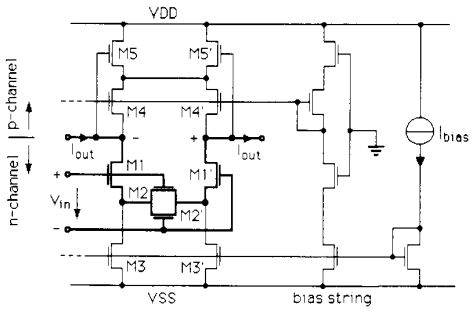


Fig. 2. Linearized CMOS differential transconductance amplifier.

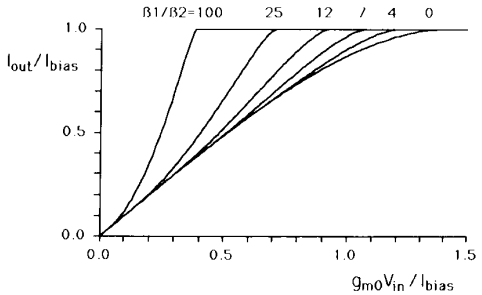


Fig. 3. Normalized i/v curves obtained from (1)–(8) for different values of the ratio β_1/β_2.

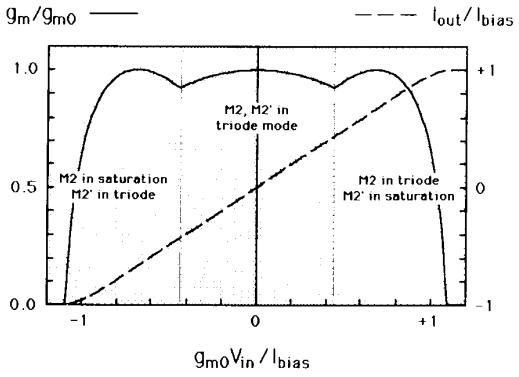


Fig. 4. Calculated i/v transfer characteristic and small-signal transconductance $g_m = \partial I_{out}/\partial V_{in}$ of the transconductor of Fig. 2 according to (1)–(8) for $\beta_1/\beta_2 = 6.7$.

or $M2$ (for $V_{in}<0$) enters the saturation region, that is when

$$|v| = \left|\frac{g_{m0}V_{in}}{I_{bias}}\right| > v_1 = \sqrt{\frac{a^2+a+0.5}{a^4+0.25}}. \tag{6}$$

The normalized transfer characteristic then becomes

$$i = \pm\frac{\left[av\sqrt{4a-2} \pm \sqrt{4a-1-a^2v^2}\right]^2}{(4a-1)^2} \tag{7}$$

where the positive (negative) sign holds for a positive

(negative) input voltage. The maximum output current ($I_{out} = I_{bias}$ or $i = 1$) is reached for

$$|v| = \left| \frac{g_{m0} V_{in}}{I_{bias}} \right| = v_2 = \frac{\sqrt{4a - 2}}{a}. \quad (8)$$

The resulting normalized i/v curves calculated for different values of the ratio β_1/β_2 are plotted in Fig. 3. The optimum value of the latter ratio for the best linearity performance appears to be around 7. Fig. 4 is another illustration of the behavior of the four-transistor input cell showing the variations of the small-signal transconductance $g_m = \partial I_{out}/\partial V_{in}$ (for $\beta_1/\beta_2 = 6.7$) according to the above equations. The inaccuracies of the model used become evident when considering the angular shape of the g_m curve at the transition from the triode to the saturation mode for $M2$ and $M2'$ and at the points where g_m approaches zero. These angles are smoothed when the deviations from the simple square-law model in the vicinity of the threshold and at the transition from the triode to the saturation region are taken into account. More accurate simulation and experimental data confirm that the ripple in the actual g_m curve is smaller than modeled in Fig. 4 and that it may be further reduced by lowering the quiescent gate overdrive voltage $V_{GS} - V_T$ of the transistors.

For example, with $\beta_1/\beta_2 = 6.7$ and $V_{GS} - V_T > 1$ V, g_m typically varies by ± 2.5 percent over 80 percent of the output current range ($|I_{out}| \leq 0.8 I_{bias}$). However, the linearity is improved when the transistors are biased at reduced current densities (i.e., 0.2 V $< V_{GS} - V_T <$ 0.5 V), which is often desirable for other reasons, such as to achieve higher dc voltage gain, lower bias current, or lower supply voltage. In this case, the deviations from the square-law model due to the proximity of the moderate inversion region are much more important and result in a significant reduction of the ripple in the transconductance characteristic (variations of less than ± 1 percent are achievable). On the other hand, the optimum ratio β_1/β_2 for the best linearity performance becomes slightly dependent on the quiescent gate overdrive voltages $V_{GS} - V_T$. This is a limitation of the technique since the dc bias point of the devices must be allowed to vary by a certain amount to compensate for fabrication tolerances and temperature variations. In the case of transconductor/capacitor filters the cutoff or center frequency f_c is proportional to the ratio of the transconductance g_m to the integrating capacitance C:

$$f_c \sim g_m/C \text{ with } g_m \sim \beta(V_{GS} - V_T) \sim \sqrt{\beta I_{bias}}. \quad (9)$$

Thus

$$V_{GS} - V_T \sim f_c C/\beta \quad (10)$$

and

$$I_{bias} \sim (f_c C)^2/\beta. \quad (11)$$

For a given frequency response (constant f_c), assuming that the tolerances on process parameters C and β are ± 10 and ± 20 percent, respectively, and that the circuit must operate over a 50°C temperature range with a temperature coefficient of typically 0.5 percent/°C for β (the temperature coefficient for C is usually negligible), the dc bias point of the input devices $M1$ and $M2$ may fall within the following limits:

$$\frac{(V_{GS} - V_T)_{max}}{(V_{GS} - V_T)_{min}} = \frac{C_{max}}{C_{min}} \frac{\beta_{max}}{\beta_{min}} \approx 2.4 \quad (12)$$

and

$$\frac{(I_{bias})_{max}}{(I_{bias})_{min}} = \frac{C_{max}^2}{C_{min}^2} \frac{\beta_{max}}{\beta_{min}} \approx 2.9. \quad (13)$$

Measurements made on an integrated version of the circuit of Fig. 2 will illustrate how these variations can affect the circuit performance.

If the input common-mode voltage is not constant with respect to the bulk potential, even-order terms will appear in the i/v transfer characteristic. These distortions may be minimized by increasing the bulk reverse voltage to reduce the body effect. For a purely differential mode input signal, the remaining even-order distortions would result from device mismatch, which has to be minimized by appropriate layout disposition.

In spite of the aforementioned limitations, this circuit offers an attractive combination of good high-frequency behavior, linearity, and low power dissipation for a reduced circuit complexity.

The complete transconductance circuit of Fig. 2 was fabricated in a 3-μm p-well CMOS process. The design parameter values were $g_{m0} = 150$ μA/V and $I_{bias} = 100$ μA, so that $(V_{GS} - V_T)_{M1,2} \approx 0.27$ V. With $L_1 = L_2 = 5$ μm, this corresponds to $W_1 = 396$ μm and $W_2 = 66$ μm ($\beta_1/\beta_2 = 6$). As can be seen from the experimental data shown in Fig. 5, the nonlinearity stays well below 1 percent of the full-scale output current up to 80-percent current modulation ($I_{out}/I_{bias} \leq 0.8$). This holds for a single (unbalanced) input (Fig. 5(b)) as well as for a differential (balanced) one (Fig. 5(a)).

In Fig. 6, the measured small-signal transconductance $g_m = \partial I_{out}/\partial V_{in}$ is also plotted as a function of the input voltage for different bias currents. With the nominal bias conditions (Fig. 6(a)), g_m does not vary by more than ± 0.8 percent for $I_{out}/I_{bias} \leq 0.65$. For higher bias currents, the "hump" in the middle of the g_m curve is enhanced (Fig. 6(b)) suggesting that for the transistors operating more deeply in strong inversion, the optimum ratio β_1/β_2 is slightly larger than 6. On the contrary, that "hump" tends to disappear at lower current densities (see Fig. 6(c)) where the optimum β_1/β_2 is smaller than 6. In the two latter cases the ripple in the transconductance characteristic has raised up to ± 1.6 percent for $I_{out}/I_{bias} \leq 0.65$.

In this implementation, input transistors $M1$, $M1'$, $M2$, and $M2'$ are in a common p-well connected to V_{SS}. Consequently, the transconductance is slightly dependent on the

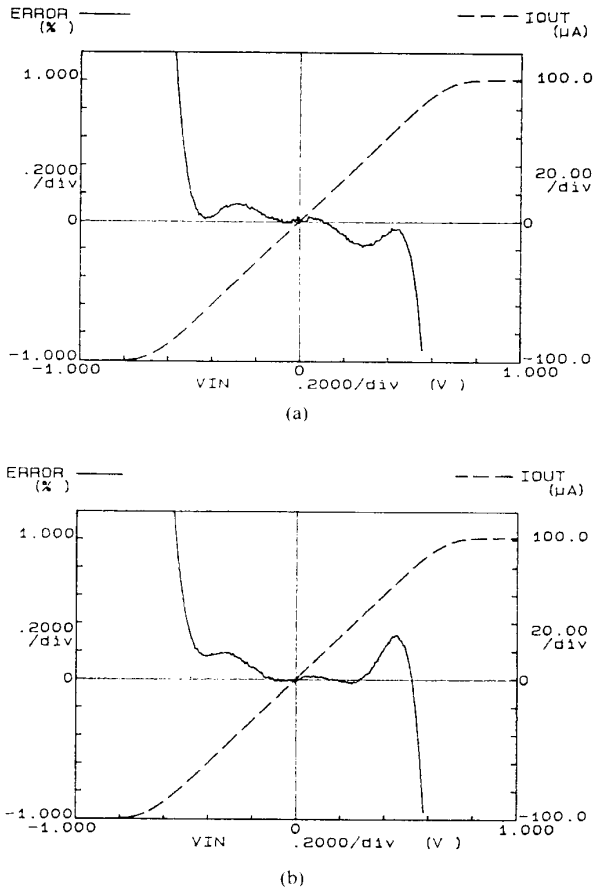


Fig. 5. Measured transfer characteristics of the transconductor of Fig. 2 for $V_{DD} = -V_{SS} = 2.5$ V, $I_{bias} = 100$ μA (a) with a differential input and (b) with a single input. The nonlinearity error is expressed here as a percentage of the full-scale current I_{bias}.

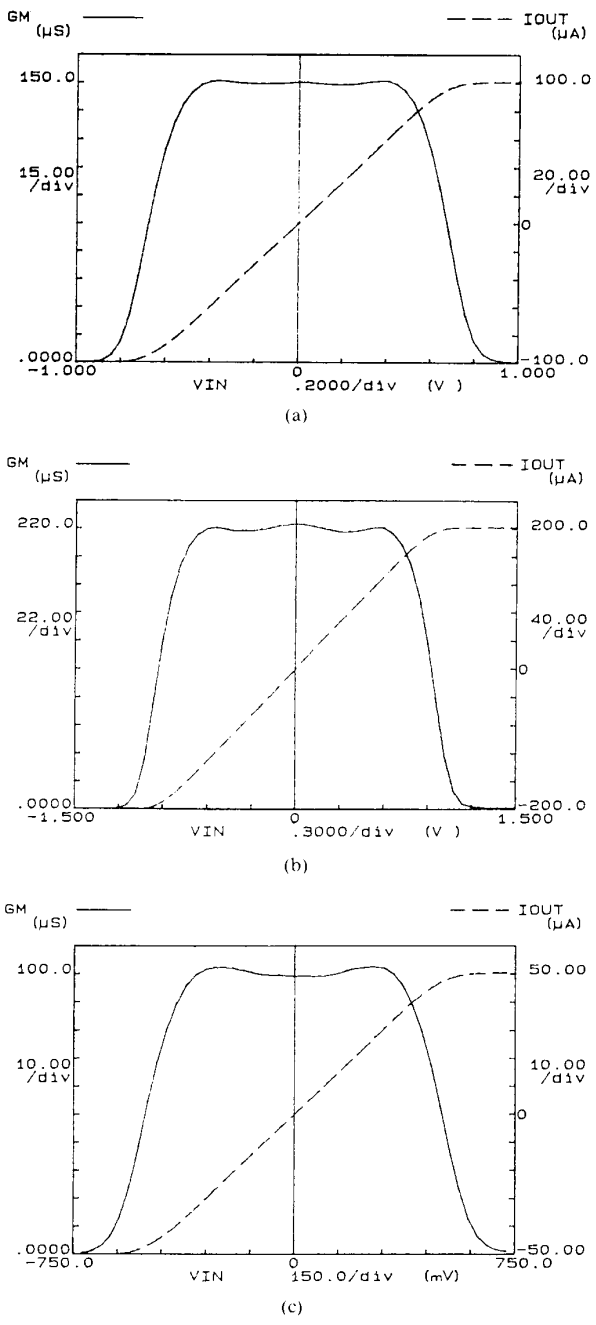


Fig. 6. Small-signal transconductance $g_m = \partial I_{out}/\partial V_{in}$ for different bias conditions: (a) $V_{DD} = -V_{SS} = 2.5$ V, $I_{bias} = 100$ μA; (b) $V_{DD} = -V_{SS} = 4$ V, $I_{bias} = 200$ μA; and (c) $V_{DD} = -V_{SS} = 2.5$ V, $I_{bias} = 50$ μA.

dc input common-mode voltage (body effect). This dependence, which is found to be less than 2 percent/V, may reduce the supply rejection capability but it does not degrade the linearity performance.

Other performance characteristics of the integrated transconductance amplifier are summarized in Table I. The most limiting factors for filter applications are likely to be the low dc voltage gain (37 dB) and the transconductor matching accuracy of 0.7 percent (standard deviation). The latter should be compared to the typical 0.2-percent capacitor matching accuracy obtained with the same process.

IV. Filter Implementation

The filter synthesis method starts from the third-order *LC* ladder meeting the filter specifications (Fig. 7(a)). The first step towards integration is to simulate the inductor with a gyrator–capacitor combination (Fig. 7(b)). Next, to make possible the use of fully balanced active elements, the series capacitive path C^* is transformed into two symmetric branches with twice the initial capacitor value, so as to keep the same reactance level (Fig. 7(c)).

Each gyrator may then be implemented with a closed-loop connection of two balanced transconductors. Two more transconductance amplifiers, each connected in unity-gain configuration, are used to simulate the termination resistors. This yields the circuit depicted in Fig. 8, where the input transconductance element has been doubled to compensate for the inherent 6-dB loss of the passive *LC* prototype and the voltage between nodes 2

TABLE I
TYPICAL CHARACTERISTICS OF THE INTEGRATED TRANSCONDUCTANCE AMPLIFIER OF FIG. 2
($V_{DD} = -V_{SS} = 2.5$ V, $I_{bias} = 100\ \mu$A)

transconductance	$g_m = 150\ \mu$A/V
output conductance	$g_0 = 2\ \mu$A/V
DC voltage gain	$g_m/g_0 = 75$
equivalent differential input capacitance	$C_{in} = 0.42$ pF
equivalent differential output capacitance	$C_{out} = 0.22$ pF
Miller capacitance	$C_M = 0.13$ pF
input offset voltage (standard deviation)	$V_{os} = 2$ mV
transconductance matching accuracy (standard deviation)	$\Delta g_m/g_m = 0.7\ \%$

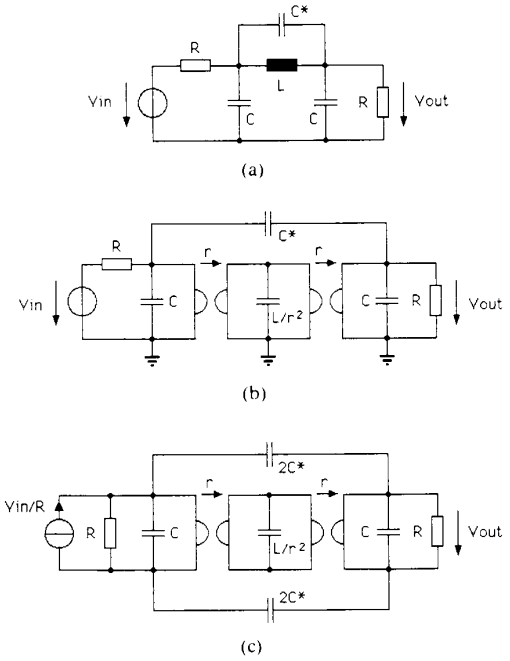


Fig. 7. Filter synthesis: (a) third-order elliptic low-pass *LC* ladder prototype; (b) gyrator–capacitor filter derived from (a); and (c) balanced version of (b).

and 2′ has been scaled down by a factor of 2 to avoid a 5.5-dB gain peaking around 2.5 MHz (this was done by doubling both the capacitance between nodes 2 and 2′ and the transconductance of the two amplifiers, the inputs of which are connected to these nodes). For a 4-MHz cutoff frequency and with unit transconductance elements of 150 μA/V, the capacitor values range from approximately 3 to 11 pF, to which the input and output stray capacitances of the transconductors contribute about 30–40 percent.

As opposed to filter synthesis methods known as indirect simulation or "voltage transfer simulation" methods where voltages and currents in the *LC* ladder prototype are simulated with voltages (as for most switched-capacitor filters), the approach used here is referred to as direct impedance simulation (voltages and currents in the *LC* ladder branches are simulated by voltages and currents, respectively). As it may appear from the above example, this approach is not applicable to any kind of filter structure because the gyrator implementation involves transconductance amplifiers with nonzero input and output parasitic capacitances.

In the case of low-pass *LC* ladders, a direct substitution of inductors by gyrator–capacitor combinations (see Fig. 7) is possible since a shunt capacitor naturally appears on both the input and the output ports of each gyrator. The parasitic input and output capacitances of the transconductors then may be identified to functional capacitances in the passive prototype and they can be properly accounted for in the filter design. For most bandpass filters structures, however, a preliminary transformation of the ladder's series arms by means of additional gyrators is required before inductance simulation can be performed without introducing uncontrollable distortions in the filter response [13].

V. AUTOMATIC TUNING CONTROL CIRCUITRY

Automatic tuning is of critical importance to control the frequency response of continuous-time filters. Such a circuit is conveniently implemented by means of a phase-locked loop using either a voltage-controlled filter (Fig. 9(a)) or a voltage-controlled oscillator (Fig. 9(b)).

In the first case, an external reference signal of well-controlled frequency is applied to a second-order filter section which is similar to those used in the filter to be tuned. The frequency-dependent input–output phase characteristics of this reference filter are then exploited to tune the circuit [3]. For this reason, any offset in the phase comparator will result in a frequency tuning error. A rough calculation shows that for a typical ± 25-percent capture range (which is reasonable with respect to the variations in process parameters), the quality factor of a second-order reference filter must be less than 2 [3]. From the corresponding phase response, it becomes apparent that an offset of 2° in the phase detection will result in a tuning error of about 1 percent. This puts stringent requirements on the phase comparator accuracy and speed performance.

Another disadvantage of this first configuration is that harmonic distortion in the reference signal will, to a certain extent, introduce additional tuning errors. This is because the harmonics will not come out from the reference filter (the selectivity of which is limited for the reasons stated above) with the same phase shift as the fundamental frequency. When multiplied with the incoming signal, these residual out-of-phase harmonics will alter the result of the phase comparison. A quantitative analysis [14] has shown that for a second-order bandpass reference filter with a quality factor of 2, the harmonics of a square-wave reference signal would introduce a systematic tuning error of approximately 0.5 percent.

In the conventional approach (Fig. 9(b)), the multiplier or phase comparator has to compare the *frequency* of the signal coming out from the voltage-controlled oscillator with that of the reference signal. As opposed to the preced-

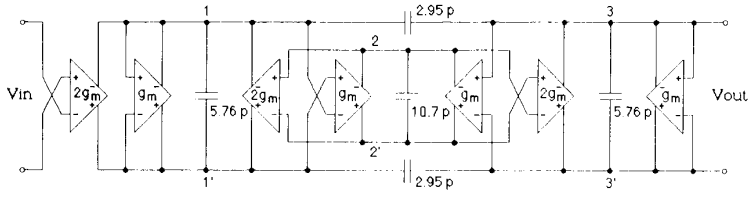
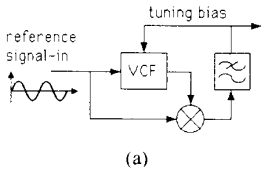


Fig. 8. Balanced transconductor-C active filter obtained from the circuit of Fig. 7(c) ($g_m = 150\ \mu A/V$ for 4-MHz cutoff frequency).



(a)

(b)

Fig. 9. Automatic tuning control methods using phase-locked loops: (a) PLL with an auxiliary voltage-controlled filter (VCF), and (b) conventional PLL using a voltage-controlled oscillator (VCO).

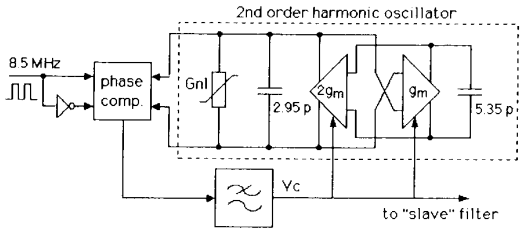
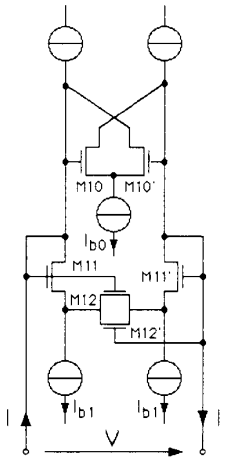
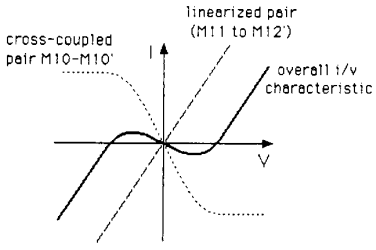


Fig. 10. Automatic tuning circuit for the filter of Fig. 8. The nonlinear conductance G_{NL} used in the second-order harmonic oscillator is intended for amplitude regulation.



(a)



(b)

Fig. 11. (a) MOS implementation of the nonlinear amplitude limiting conductance G_{NL} and (b) i/v characteristics of the circuit elements involved in (a).

ing PLL configuration, *absolute* phase accuracy is not necessary since only the phase *variations* of one signal with respect to the other must be detected. The requirements on the phase comparator are thus relaxed. The main problem then is the implementation of a voltage-controlled oscillator that is well-matched to the filter to be tuned. The best candidate is usually a second-order harmonic oscillator [1], the amplitude regulation of which must be carefully considered since harmonic distortion and nonlinearities in the transconductors would shift the effective oscillation frequency, thus introducing a tuning error.

For the above reasons, the automatic tuning circuit for the 4-MHz filter uses the latter PLL arrangement. The key design issues were the following (Fig. 10):

1) considering unavoidable capacitive coupling and limited power supply rejection, the reference frequency has been set to 8.5 MHz, close to the transmission zero within the filter stopband. In this way the feedthrough from the oscillator to the filter is expected to be minimized;
2) as good matching properties between the filter and the oscillator are required, the latter was built around a specific two-integrator loop which has been implemented using the same unit transconductance elements and with approximately the same parasitic-to-functional capacitor ratio and layout disposition; and
3) finally, to avoid systematic tuning errors, the oscillation amplitude has been limited to 70 percent of the linear portion of the i/v characteristic of the transconductors by means of a simple nonlinear circuit, the function of which is explained hereafter.

Fig. 11(a) shows the actual implementation of the nonlinear conductance G_{NL} used for amplitude regulation in the

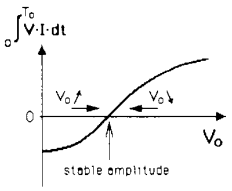


Fig. 12. Typical equivalent "energy" dissipated into the amplitude limiting network G_{NL} of Fig. 11 over one oscillation period T_0, as a function of the peak oscillation amplitude V_0.

two-integrator oscillator of Fig. 10. To obtain the desired nonlinear characteristic (Fig. 11(b)), the cross-coupled MOS differential pair $M10$, $M10'$, is added to a linearized transconductance stage ($M11$ to $M12'$) connected in unity gain.

For small signals, this circuit is equivalent to a negative conductance: it will therefore ensure oscillations build up when connected to the two-integrator loop which behaves like a passive LC resonant circuit. The amplitude of the oscillations will increase until the current I flowing through the nonlinear conductance G_{NL} has no more components at the resonant frequency f_0 of the two-integrator loop. Considering that thanks to the filtering action of the latter the voltage V across G_{NL} is purely sinusoidal regardless of the waveform of the current I, a stable oscillation amplitude is obtained when [15]

$$\int_0^{T_0} V \cdot I \cdot dt = 0$$

with

$$V = V_0 \cdot \sin(2\pi f_0 t)$$

and

$$T_0 = 1/f_0. \tag{14}$$

The above integral, which represents the equivalent "energy" dissipated into the nonlinear conductance G_{NL} over one oscillation period T_0, is plotted in Fig. 12 as a function of the peak oscillation amplitude V_0 for a typical implementation.

Considering our application, the design objectives for the circuit of Fig. 11 will be to ensure a well-controlled oscillation amplitude (within the linear range of the transconductors used in the two-integrator loop) while keeping the harmonic distortion at an acceptable level (e.g., a third-order harmonic distortion of 2 percent will lower the oscillation frequency by 0.16 percent [15, ch. 3]).

To achieve the same linearity performance, transistors $M11$ to $M12'$ must operate at the same gate overdrive voltage as the input stage (transistors $M1$ to $M2'$ in Fig. 2) of the other linearized transconductance elements used in the oscillator and in the filter. Low harmonic distortion is then obtained by limiting the bias current I_{b1} to a small fraction (between 10 and 20 percent) of the bias current of the other transconductors.

In order to keep a good control of the oscillation amplitude, the bias current and device sizes of the auxiliary cross-coupled pair $M10$ and $M10'$ must be chosen in such a way that the resulting "energy" function (see Fig. 12) presents a maximum slope around zero (i.e., at stable oscillation amplitude). Simple analysis shows that this is achieved when the small-signal transconductance of differential pair $M10$ and $M10'$ is about 1.4 times as large as the equivalent conductance of the linearized network $M11$, $M11'$, $M12$, and $M12'$. The stable peak oscillation amplitude, which must be set within the linear range of the transconductors, is then approximately equal to 1.6 $(V_{GS} - V_T)_{M10}$.

The limited quality factor of the two-integrator resonator is adequately described by a parallel parasitic conductance and may thus be properly accounted for by consequently correcting the equivalent conductance of the linearized network $M11$, $M11'$, $M12$, and $M12'$.

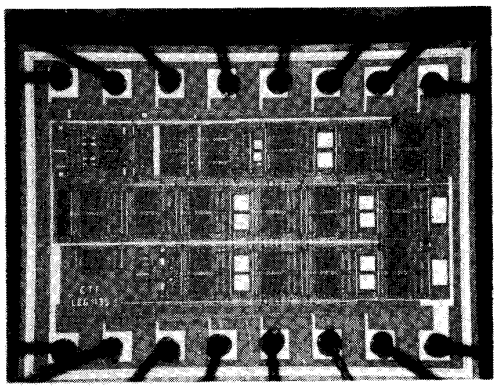


Fig. 13. Photomicrograph of the integrated 4-MHz filter.

VI. Experimental Results

The above-described filter, including automatic tuning control, has been designed for 4-MHz cutoff frequency and fabricated in a 3-μm single-poly single-metal p-well CMOS process. Fig. 13 is a photomicrograph of the complete circuit: the filter itself occupies the lower two-thirds of the 0.9×1.2-mm^2 chip whereas the automatic tuning circuitry is located in the upper third. Buffers using the available n-p-n vertical bipolar transistor have been added on the chip for measurement purposes.

A typical frequency response of the filter (including the on-chip voltage followers) for three different temperatures is reported in Fig. 14. Computer simulation showed that the deviations from the ideal response (like the average 0.3- to 0.7-dB loss in the passband) are due to the limited dc gain of the transconductance amplifiers ($A_{dc} \approx 70$ at 25°C) and to the variations thereof with bias current and temperature. The mean frequency of the transmission zero is found to be within 1.5 percent of its designed value; the spread around that value is about 1 percent (standard deviation).

The performance characteristics of the filter are summarized in Table II. The total harmonic distortion, measured for a balanced-driven input, is shown in Fig. 15 for

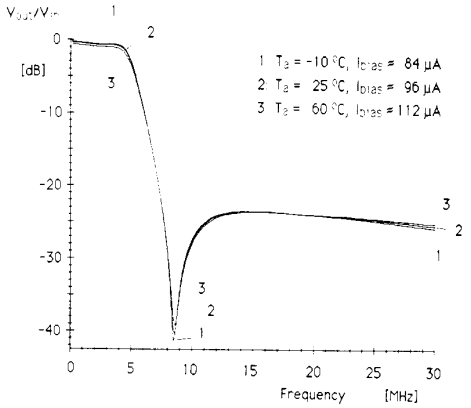


Fig. 14. Measured frequency response of the integrated filter ($V_{DD} = -V_{SS} = 2.5$ V, reference signal frequency = 8.5 MHz).

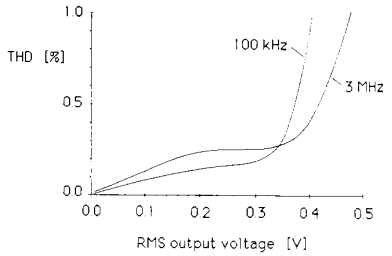


Fig. 15. Measured harmonic distortion of the integrated filter.

TABLE II
TYPICAL PERFORMANCE CHARACTERISTICS OF THE INTEGRATED 4-MHz FILTER
($V_{DD} = -V_{SS} = 2.5$ V, $f_{ref} = 8.5$ MHz, $T_a = 25$°C)

passband ripple (0 - 4 MHz)		0.6 dB
stopband rejection (f ≥ 8 MHz)		> 23 dB
max output voltage (THD < -50 dB)		350 mV_{RMS}
RMS output noise (400 Hz - 40 MHz)		100 µV
reference signal feedthrough (f = 8.5 MHz)		60 µV
dynamic range		70 dB
supply rejection at 4 MHz	for V_{DD}	37 dB
	for V_{SS}	34 dB
total power dissipation		16 mW
chip area		1.1 mm^2

100 kHz, which is practically dc, and for 3 MHz. The latter frequency corresponds to a peak gain of about 3 dB at internal nodes 1 and 1′ (see Fig. 8); in this case, however, the harmonics fall outside the passband. The distortion characteristic obtained with a 1-MHz input signal (for which most of the harmonics are still inside the passband) is situated in between the two other curves; for the sake of clearness it has not been reported on this figure. In any case the THD stays below 0.3 percent up to 1-$V_{p\text{-}p}$ (350 mV_{rms}) output voltage. With a single (unbalanced) input signal, the distortion for the same output voltage is found to be approximately twice as large.

The total output noise power in the 400-Hz to 40-MHz band is 100 µV. This value does not include feedthrough from the automatic tuning circuit which is responsible for an additional 60-µV signal at 8.5 MHz. The resulting dynamic range is then evaluated to 70 dB.

The power supply rejection at 4 MHz is better than 34 dB for both supplies and the complete circuit dissipates only 16 mW from ±2.5-V supplies.

VII. Conclusions

A new differential voltage-to-current converter has been proposed and experimented. The circuit is built around a simple four-transistor core cell and represents a significant improvement over previous realizations in terms of maximum signal-to-noise ratio, minimum supply voltage, and power consumption while preserving simplicity and good high-frequency performance. It has been used for the realization of a video frequency continuous-time filter but it might also find application in other types of continuous-time signal processing circuits where simple but reasonably accurate *V*-to-*I* converters are required.

The expectable performance of MOS continuous-time filters in the megahertz range has been illustrated by a specific example. In the circuit presented, the accuracy of the filter response is limited by the low dc gain of the transconductance amplifiers used; it is believed that for filtering applications requiring a higher selectivity some kind of automatic loss compensation circuitry will be necessary. In any case, filter accuracy is ultimately limited by transconductor matching.

Good dynamic range, low power dissipation, and reduced chip area indicate that such filters may be incorporated into a VLSI chip. With present MOS technologies, switched-capacitor filters appear to be limited to video frequencies, whereas continuous-time filters are likely to be able to operate at still higher frequencies (see, for example, [16]). Recent digital video filters of comparable performance [17] typically consume ten times more power and ten times more silicon area.

Although the design methodologies for continuous-time filters are well-known and exact, one must be aware that for high-frequency applications accurate device-level modeling is essential for first time success.

References

[1] M. Banu and Y. Tsividis, "An elliptic continuous-time CMOS filter with on-chip automatic tuning," *IEEE J. Solid-State Circuits*, vol. SC-20, pp. 1114–1121, Dec. 1985.

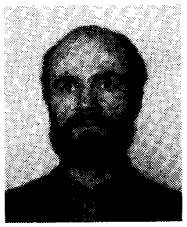
[2] Y. Tsividis, M. Banu, and J. Khoury, "Continuous-time MOSFET-C filters in VLSI," *IEEE J. Solid-State Circuits*, vol. SC-21, pp. 15–30, Feb. 1986.

[3] H. Khorramabadi and P. R. Gray, "High-frequency CMOS continuous-time filters," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 939–948, Dec. 1984.

[4] A. P. Nedungadi and R. L. Geiger, "High-frequency voltage controlled continuous-time low-pass filter using linearized CMOS integrators," *Electron. Lett.*, vol. 22, pp. 729–730, July 1986.

[5] H. Khorramabadi, "High-frequency CMOS continuous-time filters," Ph.D. dissertation, Univ. of Calif., Berkeley, Feb. 1985.

[6] Y. Tsividis, Z. Czarnul, and S. C. Fang, "MOS transconductors and integrators with high linearity," *Electron. Lett.*, vol. 22, pp. 245–246, Feb. 1986.
[7] Z. Czarnul, S. C. Fang, and Y. Tsividis, "Improving linearity in MOS fully-integrated continuous-time filters," in *Proc. IEEE ISCAS'86* (San Jose, CA), 1986.
[8] J. L. Pennock, "CMOS triode transconductor for continuous-time active integrated filters," *Electron. Lett.*, vol. 18, pp. 817–818, Aug. 1985.
[9] A. Nedungadi and T. R. Viswanathan, "Design of linear transconductance elements," *IEEE Trans. Circuits Syst.*, vol. CAS-31, pp. 891–894, Oct. 1984.
[10] C.-S. Park and R. Schaumann, "A high-frequency CMOS linear transconductance element," *IEEE Trans. Circuits Syst.*, vol. CAS-33, pp. 1132–1138, Nov. 1986.
[11] K. Bult and H. Wallinga, "A class of analog CMOS circuits based on the square-law characteristic of an MOS transistor in saturation," *IEEE J. Solid-State Circuits*, vol. SC-202, pp. 357–365, June 1987.
[12] E. Seevinck and R. F. Wassenaar, "A versatile CMOS linear transconductor/square-law function circuit," *IEEE J. Solid-State Circuits*, vol. SC-202, pp. 366–377, June 1987.
[13] N. Joehl and F. Krummenacher, "Filtres continus MOS integrés à large échelle," *AGEN-Mitteilungen*, no. 43, pp. 49–55, May 1986.
[14] O. Rey, "Circuit de verrouillage en fréquence pour filtre continu," M.S. thesis, Swiss Federal Inst. of Technology, Lausanne, Switzerland, Dec. 1985.
[15] W. A. Edson, *Vacuum-Tube Oscillators*. New York: Wiley, 1953.
[16] Y. P. Tsividis, "Minimal transistor-only integrated VHF active filter," *Electron. Lett.*, vol. 23, pp. 777–778, July 1987.
[17] U. Kleine and M. Böhner, "A high-speed wave digital filter using carry-slave arithmetic," in *ESSCIRC'87 Dig. Tech. Papers*, Sept. 1987, pp. 43–46.



François Krummenacher was born in Lausanne, Switzerland, on April 29, 1955. He received the M.S. and Ph.D. degrees in electrical engineering from the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, in 1979 and 1985, respectively.

Since 1979 he has been with the Electronics Laboratory of EPFL, working in the field of low-power and high-performance analog CMOS integrated circuit design. From April to October 1983 he was with the Electrical Engineering Department of the University of California, Los Angeles, where he was involved in the design of MOS switched-capacitor circuits. He is currently responsible for the research activities at the Electronics Laboratory of EPFL.

Norbert Joehl was born in Geneva, Switzerland, on May 5, 1959. He received the M.S. degree in electrical engineering from the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, in 1985.

Since 1985 he has been a Research Assistant at EPFL where he is currently working towards the Ph.D. degree on the subject of MOS continuous-time filters for VLSI circuits.