Platform Express User's Guide

Software Version 1.1f

Release 1.1f

November 2002



Copyright © Mentor Graphics Corporation 2002. All rights reserved.

This document contains information that is proprietary to Mentor Graphics Corporation. The original recipient of this document may duplicate this document in whole or in part for internal business purposes only, provided that this entire notice appears in all copies. In duplicating any part of this document, the recipient agrees to make every reasonable effort to prevent the unauthorized use and distribution of the proprietary information.

End-User License Agreement Trademark Information This document is for information and instruction purposes. Mentor Graphics reserves the right to make changes in specifications and other information contained in this publication without prior notice, and the reader should, in all cases, consult Mentor Graphics to determine whether any changes have been made.

The terms and conditions governing the sale and licensing of Mentor Graphics products are set forth in written agreements between Mentor Graphics and its customers. No representation or other affirmation of fact contained in this publication shall be deemed to be a warranty or give rise to any liability of Mentor Graphics whatsoever.

MENTOR GRAPHICS MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OR MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

MENTOR GRAPHICS SHALL NOT BE LIABLE FOR ANY INCIDENTAL, INDIRECT, SPECIAL, OR CONSEQUENTIAL DAMAGES WHATSOEVER (INCLUDING BUT NOT LIMITED TO LOST PROFITS) ARISING OUT OF OR RELATED TO THIS PUBLICATION OR THE INFORMATION CONTAINED IN IT, EVEN IF MENTOR GRAPHICS CORPORATION HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

RESTRICTED RIGHTS LEGEND 03/97

U.S. Government Restricted Rights. The SOFTWARE and documentation have been developed entirely at private expense and are commercial computer software provided with restricted rights. Use, duplication or disclosure by the U.S. Government or a U.S. Government subcontractor is subject to the restrictions set forth in the license agreement provided with the software pursuant to DFARS 227.7202-3(a) or as set forth in subparagraph (c)(1) and (2) of the Commercial Computer Software - Restricted Rights clause at FAR 52.227-19, as applicable.

Contractor/manufacturer is: Mentor Graphics Corporation 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777.

This is an unpublished work of Mentor Graphics Corporation.

Table of Contents

About this Manual

Using the Documentation	xiii
Using Acrobat	
Using JavaHelp	
Typographical Conventions	
Manual Organization	xvii
Related Publications	xvii
About the Platform Express User's Guide	xviii

Chapter 1 Introduction to Platform Express

Overview1-1
About Platform Express1-1
Understanding the Design and Verification Cycle1-1
Automating the Design Cycle1-2
Designing with Various Platform Cores1-2
Setting up and Invoking Platform Express1-3
Licensing1-3
Defining Environment Variables1-4
Invoking Platform Express1-5
Platform Express Quick Tour1-6
Graphical Design Editor1-7
Component Browser1-8
Memory Map Pane1-8
Output Pane1-8
Clearing the Contents of the Output Pane1-8
Copying the Contents of the Output Pane1-9
Additional User Interface Elements1-9
Menu Bar1-9
File Menu1-9
Edit Menu1-10
Tools Menu1-10
Settings Menu1-11
Help Menu1-12
Button Bar1-12

Status Bar	1-12
Size-Configurable Panes	1-13
Understanding the Design Process	
Step One: Create the Design	
Step Two: Build the Design	
Step Three: Invoke the Co-Verification Environment	

Chapter 2 Creating Designs

Overview	2-1
Before You Begin	2-1
Defining User Preferences	2-2
Defining Project Settings	2-2
Changing Current Project Settings	2-3
Changing Default Project Settings	2-3
Creating a New Design	2-4
Opening an Existing Design	2-9
Using the Design Editor	2-9
Working with Componets	2-10
Color Coding for Components	2-11
Creating Component Instances	2-11
Configuring Components	2-12
Configuring the Pin Settings	2-12
Deleting Components	2-13
Accessing Component Information	2-13
Accessing the Details Window	2-14
Working with Connectors	2-15
Creating Connections	2-15
Connecting an Unconnected Component	2-16
Deleting Connections	2-16
Working With Buses	2-16
Bus Views	2-17
Automatic Bus Connections	2-18
Changing Bus Connections	2-18
Bus Bridges	2-18
Multiple Bus Connections	2-19

Master and Slave Components	2-19
Configuring Buses	2-19

Chapter 3 Building Designs

Overview	3-1
Before you begin	3-1
Configuring the Build	3-2
Defining all configurable components	3-2
Defining configurable components separately	3-2
Setting Driver Signals	
Configuring the Required Drivers	
Configuring the Decoder Selection	
Defining the Pin Configuration	
Pin Configuration Example	
Using the Scatter Loader	
Adding Execution Regions	3-11
Scatter Loader Data Types	
Remapping Address Ranges	
Configuring Software Memory	
Saving Your Design	
Hardware Design Files	
Software Design Files	
Building your Design	

Chapter 4 Verifying Designs

Overview	4-1
Before you begin	4-1
Invoking a Co-Verification Session	
Using the Co-Verification Session	
Starting HW/SW Simulators Examples	4-7

Chapter 5 Use Case Example

Overview	5-	-1	
Set up your environment			

Invoke Platform Express	
Begin Your Design	
Select the Core	
Add a Memory Component	5-3
Save the Design	5-7
Design Explanation	
Build Your Design	5-7
Simulate Your Design	5-8
Verify Your Design	
Cycle through the Design Flow	5-9

Appendix A Directory Structures

Overview	A-1
Platform Express Directory Structure	A-1
Directory Structure of Generated Design	

Appendix B Frequently Asked Questions (FAQs)

Overview	B-1
Product Questions	B-1
General Usage	
Error Messages	

Appendix C Build Log File

Appendix D Using the Documentation Generator

Overview	D-1
About PxDoc	
Installing PxDoc	
Using PxDoc	
To generate documentation with PxDoc:	
Accessing the Generated Documentation	
Location of Generated Files	

Sample of Generated Documentation	D-5
Customizing the Documentation Generator	D-8

Appendix E Contacting the SupportCenter

North America Support	E-1
International Support	
Product Licensing Assistance	

Glossary

Address block	
Address space	1-3
Bus	
Bus Bridge	
Component Library	
Interrupt Controller	1-4
Interrupt Service Routine (ISR)	1-4
Literal Pool	
Memory Map	1-4
Scatter Loader	
Test Bench	

Trademark Information

End-User License Agreement

List of Figures (cont.)

Figure 1. Ja	avaHelp viewer interface	XV
Figure 1-1.	Design and Verification Flow	1-3
Figure 1-2.	Platform Express Interface	1-7
Figure 1-3.	Platform Express, with Maximized Design Editor	1-14
Figure 1-4.	Seamless Co-Verification Environment	1-17
Figure 2-1.	Component Browser	2-6
Figure 2-2.	Example Core Configuration Dialog Box	2-7
Figure 2-3.	Simple Design with core and peripherals	2-9
Figure 2-4.	Details window	2-15
Figure 3-1.	Required Driver Configuration dialog box	3-5
Figure 3-2.	Configure Decoder Selection Dialog Box	3-7
Figure 3-3.	Pin Configuration dialog box	3-9
Figure 3-4.	Scatter Loader dialog box	
Figure 3-5.	Add Execution Region dialog box	3-13
Figure 3-6.	Sofware Memory Configuration Panel	
Figure 4-1.	Seamless CVE Interface	4-3
Figure 4-2.	XRAY Debugger interface	4-4
Figure 4-3.	ModelSim interface	4-5
Figure 4-4.	Wave viewer interface	4-6
Figure D-1.	PxDoc Dialog Box	D-4
Figure D-2.	Sample Memory Map documentation, Netscape	D-6
Figure D-3.	Sample Memory Map Documentation, Java	D-7

List of Figures (cont.)

List of Figures (cont.)

List of Tables (cont.)

Table 1-1. Invocation Switches	1-5
Table 1-2. File Menu	1-9
Table 1-3. Edit Menu	1-10
Table 1-4. Tools Menu	1-10
Table 1-5. Settings Menu	1-11
Table 1-6. Help Menu	
Table 2-1. Project Settings	2-4
Table 3-1. Configuration Dialog Boxes	3-2
Table 3-2. Scatter Loader Data Types	
Table A-1. Platform Express Installation	A-1
Table A-2. Directory Structure of Platform Express Design	A-4
Table D-1. Generated HTML Filenames	

List of Tables (cont.)

About this Manual

The Platform Express User's Guide describes how to use Platform Express to quickly create platform-based designs based on open source or other third-party components. This manual is targeted to hardware and software engineers working in the Electronic Design Automation (EDA) industry. As such, this manual assumes a basic knowledge of System-On-Chip (SoC) embedded-processor electronic designs.

Using the Documentation

To accommodate differences in accessibility, viewing, and printing, the Platform Express User's Guide is delivered in two formats:

- Adobe PDF
- Sun JavaHelp

The technical content in each format is essentially the same. The two formats are provided as alternate delivery mechanisms of the same content.

Using Acrobat

The Adobe PDF format requires the Adobe Acrobat Reader application. The Adobe Acrobat Reader, which is available at no cost, is available at:

http://www.adobe.com/products/acrobat/readermain.html

The PDF version of the User's Guide is available in the /doc directory of your Platform Express installation. The User's Guide in PDF format is ideal for printing because it maintains the page paradigm.

Using JavaHelp

The User's Guide in JavaHelp is easily accessible from the Help menu of the Platform Express user interface. No third-party application is required. The Platform Express online help is ideal for accessing documentation directly from the Platform Express interface, and is customized for online viewing. For better printing results, use the PDF format instead of JavaHelp.

Select **Help > User's Guide** to invoke the JavaHelp viewer and display the first help topic. The viewer window contains two panes: the Content pane and the Navigation pane.

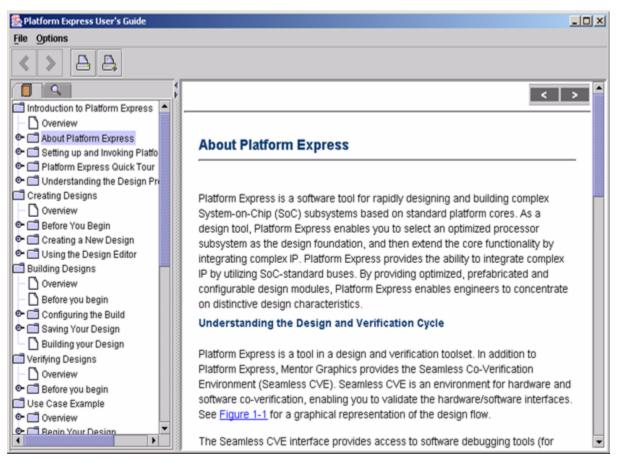


Figure 1. JavaHelp viewer interface

Content Pane

Contains topic text. Within the topic text, there may be blue, underlined links that you can click to display related topics.

• Navigation Pane

Provides two tabs: Contents and Search; and four buttons: Back, Next, and two Print buttons.

o Contents Tab

Displays the Table of Contents. In the table of contents, click on a topic title to display that topic's contents in the Content pane. Double-click a folder to display the topic tree.

• Search Tab

Displays the Search tab and invokes the global search tool. Search through the entire User's Guide for an item by entering text in the Find box and pressing Return. The viewer displays titles of all topics containing the item in the Navigation pane. Click on a topic title to display the topic.

o Previous and Next buttons

Cycle forwards and backwards through previously displayed topics in the order in which they were displayed.

• Print buttons: Print and Print Setup

The left **Print** button displays a print dialog box for configuring and initiating printing; the right **Print Setup** button sets the page format.

Typographical Conventions

Convention	Meaning	Example
<i>italic</i> text	Indicates a variable or user- supplied argument.	-f filename
square brackets []	Encloses optional commands, parameters, or arguments.	filename [<i>list</i>]
menu > menu choice > sub-menu choice	Shows the top-level menu on the main menu, to a menu choice, to a sub-menu choice.	File > Save
Bold	Indicates selectable items within the interface, such as menus.	In the File menu, select New .



Screen captures in the *Platform Express User's Guide* reflect the Solaris platform with the Common Desktop Environment (CDE) windowing system. The actual appearance of GUI elements on other platforms may vary.

Manual Organization

The Platform Express User's Guide contains the following topics:

- Introduction to Platform Express
- Creating Designs
- Building Designs
- Verifying Designs
- Use Case Example
- Directory Structures
- Frequently Asked Questions (FAQs)
- Build Log File
- Using the Documentation Generator
- Contacting the SupportCenter

Related Publications

The following Mentor Graphics publications contain information relevant to the usage of Platform Express:

• The *Platform Express Installation Manual* explains how to install Platform Express and how to set up your environment.

- The *Platform Express Release Notes* contain changes and enhancements, as well as caveats specific to Platform Express or its operating environment.
- The *Platform Express Integrator's Guide* is targeted specifically to IP providers for the express purpose of integrating custom core components into the Platform Express interface. End-users creating designs with the provided third-party and open source components do not need the *Integrator's Guide*.
- The *Seamless CVE User's and Reference Manual* contains an overview of the product, explains how to prepare designs for cosimulation, and provides procedures for workstation and design configuration and workstation configuration.

About the Platform Express User's Guide

Product Version: 1.1f

Release Date: November 2002

Chapter 1 Introduction to Platform Express

Overview

This chapter contains conceptual and high-level procedural information on Platform Express. It contains the following sections:

- About Platform Express
- Setting up and Invoking Platform Express
- Platform Express Quick Tour
- Understanding the Design Process

About Platform Express

Platform Express is a software tool for rapidly designing and building complex System-on-Chip (SoC) subsystems based on standard platform cores. As a design tool, Platform Express enables you to select an optimized processor subsystem as the design foundation, and then extend the core functionality by integrating complex IP. Platform Express provides the ability to integrate complex IP by utilizing SoC-standard buses. By providing optimized, prefabricated and configurable design modules, Platform Express enables engineers to concentrate on distinctive design characteristics.

Understanding the Design and Verification Cycle

Platform Express is a tool in a design and verification toolset. In addition to Platform Express, Mentor Graphics provides the Seamless Co-Verification Environment (Seamless CVE). Seamless CVE is an environment for hardware and software co-verification, enabling you to validate the hardware/software interfaces. See Figure 1-1 for a graphical representation of the design flow.

The Seamless CVE interface provides access to software debugging tools (for example, XRAY Debugger and Green Hills MULTI), as well as to hardware logic simulation tools (for example, ModelSim and NCSim). Platform Express provides the essential functionality for designing and building complex SoC subsystems, and Seamless CVE provides the interface for design verification.

Automating the Design Cycle

Platform Express assists the system designer with tools that automate the design cycle. All relevant design elements are presented in detail within the Platform Express interface, accelerating design creation. The Design Editor is context-aware and allows on-the-fly configuration. After the design is created, Platform Express provides tools for automating the build of the design database and tool configuration files. The build files generated by Platform Express are used directly in concert with the Seamless Co-Verification environment. Platform Express provides the following automatic functionality:

- Bus decoding
- Bus bridging
- Interrupt bridging

Designing with Various Platform Cores

The Platform Express interface provides the flexibility of offering a selection of platform cores (for example, ARM966 and ARM926) to use as the basis of your design. The default Platform Express application ships with a number of libraries (which contain platform core components), and alternate third-party libraries are also available. Many platform cores are provided as "open source," while others are proprietary. (Proprietary components are shipped as simulation models and do not provide sources). For information on creating and implementing libraries, consult the *Platform Express Integrator's Guide*.

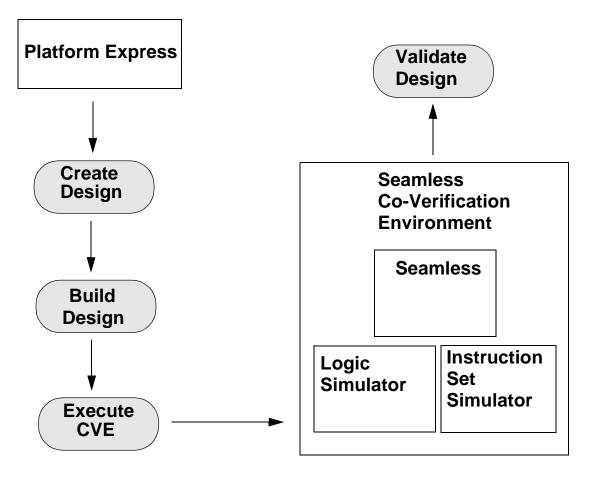


Figure 1-1. Design and Verification Flow

Setting up and Invoking Platform Express

Licensing

Platform Express utilizes the FlexLM License Manager software. Refer to the *Platform Express Installation Manual* for licensing information.

Defining Environment Variables

Platform Express is a Java SDK application. In addition to JAVAHOME, Platform Express utilizes environment variables to function properly. The required PXHOME environment variable points to the root directory of the Platform Express installation. Immediately after installing Platform Express, you must manually set the PXHOME environment variable.

Other optional environment variables which are relevant to Platform Express include:

• JAVAHOME

Points to your JRE or Java SDK installation.

PXPATH

Points to your component libraries.

• CVE_HOME

Points to your Seamless CVE installation.

MODELTECH

Points to your ModelSim installation.

• ARMTOOLS

Points to your ARM build tools, such as the ARM compiler.

For further information on defining your environment to run Platform Express, refer to the *Platform Express Installation Manual*.



Platform Express is validated against specific versions of Seamless CVE. Consult the *Platform Express Release Notes* to ensure you have installed a version of Seamless CVE that has been certified to work with Platform Express.

Invoking Platform Express

To invoke Platform Express, enter the following:

\$PXHOME/bin/px

For enhanced control of the Platform Express invocation, additional commandline switches are available:

```
$PXHOME/bin/px [-d] [-v] [-l logfilename] [-i] [-G
generatorchain] [[-b|-r] designname]
```

See Table 1-1 for a listing and description of the invocation switches.

Switch	Description
-d	Enables debug message output. Use the -l option to specify output to a log file. Otherwise, the messages appear in the output pane.
-v	Enables additional (verbose) debug messages, including the names of generators as they execute during the build. Use the -1 option to specify output to a log file. Otherwise, the messages appear in the output pane.
-1	Creates a log file. A default log file is created (or overwritten) unless a logfilename is specified. The default log file is located in your home directory in .pxrc/pxlogfile.
logfilename	Specifies the filename and optional path for debug messages.
-i	Ignores generator errors and continues build. If not used, the build stops if an error occurs.

Table 1-1. Invocation Switches

Switch	Description
-G	Invokes Platform Express in batch mode. All required drivers must be specified in the design before using this option.
generatorchain	One of Build or Execute.
-b	Automatically builds designname.
-r	Automatically executes a co-verification session on designname.
designname	The root directory of an existing Platform Express design.

 Table 1-1. Invocation Switches

Platform Express Quick Tour

The following is an overview of the Platform Express Graphical User Interface (GUI). In addition to the standard menu bar, tool bar, and status bar of modern application interfaces, the Platform Express interface is composed of four basic elements:

- Graphical Design Editor
- Component Browser
- Memory Map Pane
- Output Pane

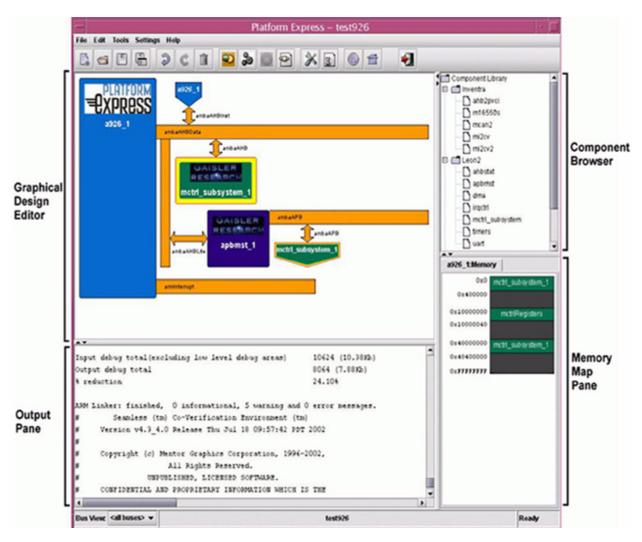


Figure 1-2. Platform Express Interface

Graphical Design Editor

The Graphical Design Editor enables you to create a block diagram of your design. The components in the design editor are configurable. To configure the components in the design editor, right-click on a component and select the desired configuration.

Component Browser

The component browser lists all the available platform cores. (The available platform cores vary depending on your installed libraries.) Initially, only core platforms are visible. Additional components (such as memory, bus bridges, interrupt controllers, and peripherals) become visible *after* you have selected a core platform and placed it in the Design Editor.

Memory Map Pane

Memory and other peripheral components automatically connect to the appropriate bus on the platform. The memory map pane is a Read-Only pane that displays where a given component fits into the platform address space in relation to other components. The memory map pane displays address locations in hexadecimal format.

Output Pane

The output pane functions as a standard output display. Build statuses are automatically displayed in the output pane.



The contents of the output pane do not clear automatically when you close the current design.

Clearing the Contents of the Output Pane

- 1. Right-click within the output pane.
- 2. Select **Clear** from the context menu.

You cannot clear a selection of the output pane. The Clear function deletes the entire contents.

Copying the Contents of the Output Pane

- 1. Select the desired contents in the output pane.
- 2. Right-click within the output pane.
- 3. Select **Copy** from the context menu.
- 4. Paste the contents into a text editor or shell.

Additional User Interface Elements

In addition to the graphical design editor, component browser, output pane, and memory map pane, there are several common elements in the Platform Express interface:

- Menu Bar
- Button Bar
- Status Bar

Menu Bar

The main menu bar is used for creating and saving designs, configuring tool settings, and building and executing finished designs.

File Menu

Menu Item	Description
New	Closes current design and creates a new design using your default project settings.
Open	Opens an existing design (*.plx).
Save	Saves the current design.

Table 1-2. File Menu

Save As	Allows you to save the current design with a new name.
Exit	Exits Platform Express.

Edit Menu

Table 1-3. Edit Menu

Menu Item	Description
Undo	Undoes the last change.
Redo	Undoes the last Undo.
Delete	Deletes the selected component.

Tools Menu

Table 1-4. Tools Menu

Menu Item	Description
Build	Builds the current design, using the specified verification tools.
Execute	Simulates the current design; executes Seamless CVE.
Stop	Stops the current build.



Depending on your installed components, you may see additional items on the Tools menu. For example, the Platform Express Documentation Generator (which is an add-on component) is accessible from the Tools menu. See Appendix D, Using the Documentation Generator, for more information.

Settings Menu

N	Description
Menu Item	Description
User Preferences	Configures Platform Express environment settings; does not affect the settings of the current design.
Project Settings	Configures design-related settings for the current design.
Save As Default	Saves the current design settings as the default for all your new designs.
Log Messages	Configures the level of log message output. The three choices are:
	• None: outputs no messages
	• Info: sets logmask to "8"
	• Debug: sets logmask to "4"
	The logmask is a filter setting that defines which types of messages are displayed. The "8" logmask displays informational messages only. The "4" logmask displays the most in- depth messages, useful for debugging.
Configure All	Configures all design-related settings for the current design. This dialog box enables you to configure <i>all</i> settings of your design from a single location. The three top-level settings are:
	• design
	• component
	• bus

Help Menu

Menu Item	Description	
User's Guide	Invokes JavaHelp and loads the User's Guide.	
About	Displays Platform Express version numbers and legal information.	
Px Web	Invokes a browser and loads the Platform Express website.	

Table 1-6. Help Menu

Button Bar

Contains buttons for managing designs and configuring Platform Express.

Status Bar

The status bar has three active areas, from left to right:

- Bus View menu, which allows the Design Editor to show all buses or only one bus type.
- Displays the current design name.
- Displays one of the following states:
 - Ready
 - Building
 - Executing



The states displayed in the Status Bar are dependent on the generation tool. As the generation tool may vary, the values displayed in the Status bar that reflect the state may vary.

Size-Configurable Panes

The Platform Express interface is configurable. Resize the Design Editor, Component Library, Memory Map, and Output panes by dragging the dotted bars between the panes:

.....

Minimize or restore panes by clicking the arrows in the bar next to the pane(s):

....

Figure 1-3 depicts the Platform Express interface with the Design Editor expanded (and the Component Library, Memory Map, and Output panes minimized).

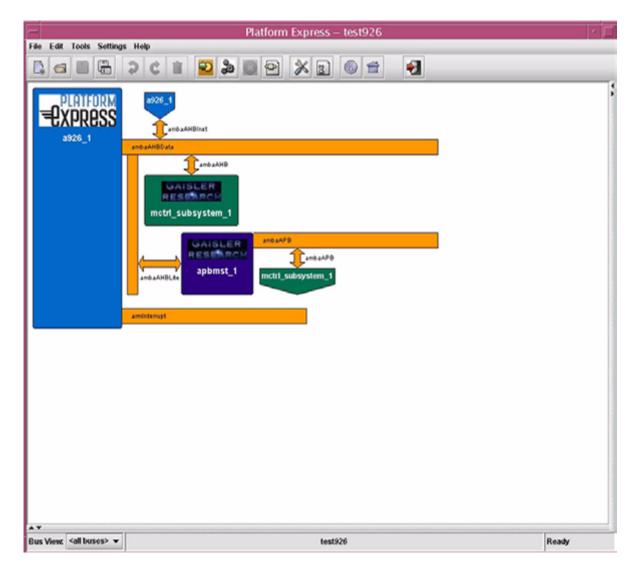


Figure 1-3. Platform Express, with Maximized Design Editor

Understanding the Design Process

The platform design cycle consists of three main processes:

- 1. Creating the Design
- 2. Building the Design
- 3. Executing the Co-Verification Environment

Step One: Create the Design

Platform Express provides a set of platform cores and complex IP as building blocks to create your design. The Component Browser lists your licensed platform cores. After you have selected the desired core platform and moved it to the graphical design editor, the Component Browser automatically lists all the associated memories and peripherals.

- 1. Select the platform core on which to base your design.
- 2. Double-click or drag-and-drop the desired platform core into the design editor.
- 3. Specify addresses and other information in the core's configuration dialog box.

Once the platform is in the design editor, you may begin adding memory and peripheral components to the desired buses. Most components have dialog boxes that allow you to specify addresses and other configuration information.

Step Two: Build the Design

Platform Express generates an HDL system design based on the contents of the Design Editor and the component configurations. To initiate the build process, select **Tools > Build** or click the **Build** button on the toolbar. The generated design files include most of the basic requirements of an embedded system design, such as component instantiation and connection within a top-level design, decode logic, and interrupt setup.

Step Three: Invoke the Co-Verification Environment

Platform Express provides an interface for executing a co-verification environment that invokes Seamless CVE. All the required scripts and configuration files, which are necessary for running the co-verification session, are automatically generated by Platform Express. Use the co-verification environment to verify the design you created and built with Platform Express. To execute the co-verification session, select **Tools > Execute** or click the **Execute** button on the toolbar. When you invoke a co-verification session, the following applications are automatically loaded:

- Seamless CVE
- Logic simulator interface (for example, ModelSim)
- Wave viewer

In addition, log windows also appear. Depending on your environment, you may have to issue additional commands to invoke the Instruction Set Simulator (ISS). For example, to invoke the XRAY Debugger ISS, enter the following command at the ModelSim command prompt:

run -all



Platform Express relies on environmental settings to invoke Seamless CVE. Ensure that you have set all the required environment variables to properly execute a co-verification session. For more detailed information, consult the *Platform Express Installation Manual*.

wave – default
Ele Edit Cursor Zoom Compare France France ModelSim SE PLUS 5.5f
Eile Edit Design View Project Bun Compare Macro Options Window Help
📕 top_anbaapb_1_pr U
<pre>incorrect address decoding . Time: 0 ns Iteration: 1 Instance: /pxdestbench/top_1/ pxdecoder_ambaahb_1 . "Warning: NUMERIC_STD.">=": metavalue detected, r eturning FALSE . Time: 0 ns Iteration: 1 Instance: /pxdestbench/top_1/ pxdecoder_ambaahb_1 . "Warning: NUMERIC_STD.">=": metavalue detected, r eturning FALSE . Time: 0 ns Iteration: 1 Instance: /pxdestbench/top_1/ pxdecoder_ambaahb_1 . "Werning: NUMERIC_STD.">=": metavalue detected, r eturning FALSE . Time: 0 ns Iteration: 1 Instance: /pxdestbench/top_1/ pxdecoder_ambaahb_1 . CVE NOTE: Instance '/pxdestbench/top_1/a926_1/uarm 926ejs" waiting for connection from software process . CVE NOTE: Instance '/pxdestbench/top_1/a926_1/uarm 926ejs" connected to software process . Time: 0 ns Delta: 3 </pre>
Go Step Next StepI NextI GoRtn Stop Up Down Cancel Conn+ HW-Step HW-Next HW-StepI HW-NextI HW-Go HW-Break
Import interrupt_handler 15 IMPORT IImage\$\$R0\$\$Basel ; Start of ROM 16
17 <u>B Reset_Handler</u>
Elle Setur Octimice Man Profession -
Eile Setup Optimize View Preference Help General Setup CPU Setup Optimization Run Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup Image: Setup
Name Proc Type Address : e/componentLibrary/
pxtestbench.top_1.a926_1.uARM926EJS arm926ejs_rev0 Memory
cve>

Figure 1-4. Seamless Co-Verification Environment

Chapter 2 Creating Designs

Overview

This chapter contains procedural and conceptual information on creating a design with Platform Express. It contains the following sections:

- Before You Begin
- Creating a New Design
- Using the Design Editor

Before You Begin

This chapter assumes you have properly installed Platform Express (including libraries), and have configured your environment to run Seamless CVE. Check that you have defined the following environement variables: PXHOME, PXPATH, CVE_HOME, MODELTECH (for ModelSim logic simulation), and ARMTOOLS (if you are using ARM tools). Consult the *Platform Express Installation Manual* for complete instructions.

Defining User Preferences

Before creating your first design, check your user preferences. User preference settings affect the operation of Platform Express. (All of your designs use the same user preferences.)

To configure user preferences, select **Settings** > **User Preferences**:

Browser Command

The Browser Command is the system command for invoking an Internet browser (such as Netscape), directly from within the Platform Express interface. (To invoke the browser, right-click a component in the Design Editor, select Browse, and then select a menu choice.) The direct browser access enables you to view information and documentation provided by third-party core vendors.

To define a browser, enter the full path to the browser and all command parameters, including an embedded URL tag (\$url). The URLs from the component configuration files will be inserted when the browser is invoked.

Defining Project Settings

Before creating your first design, check your project settings. When you invoke Platform Express, it creates a directory named .pxrc in your home directory (if .pxrc does not already exist). Your default project settings are stored in the .pxrc directory. Platform Express applies your default project settings to all new projects. (The words *project* and *design* are used interchangeably.)



A warning appears if the .pxrc directory does not exist:

```
[WARN] - Error opening settings file
"/user/michael/.pxrc/preferences.xml"
/user/michael/.pxrc/preferences.xml (No such
file or directory)
[WARN] - Error opening settings file
"/user/michael/.pxrc/projectSettings.xml"
/user/michael/.pxrc/projectSettings.xml (No such
file or directory)
```

Changing Current Project Settings

- 1. Select **Settings** > **Project Settings**.
- 2. In the Edit Properties dialog box, enter the desired settings.
- 3. Click OK.

The new project settings are stored in the project directory when you save your design.

Changing Default Project Settings

- 1. Select **Settings** > **Project Settings**.
- 2. In the Edit Properties dialog box, enter the desired settings.
- 3. Click OK.
- 4. Select **Settings > Save As Default**.

The design settings are listed in Table 2-1.

Setting Name	Description	Default
HDL Top Module Name	Name of HDL top module.	top
HDL Language	One of: VHDL, Verilog.	VHDL
Clock Period	Period, in nanoseconds, for one-shot or clock signals that require drivers.	40 ns
Clock Pulse Offset	Pulse offset, in nanoseconds, for clock signals that require drivers.	10 ns
Clock Pulse Value	Pulse value for clock signals that require drivers.	0
Clock Pulse Duration	Pulse duration, in nanoseconds, for clock signals that require drivers.	20 ns
Reset Offset	In nanoseconds.	40 ns
Reset Assertion Value	Reset assertion value.	0
Current Verification Environment	Used by Tools > Build . ModelSim or NCSim.	ModelSim

Table 2-1. Project Settings

Creating a New Design

To create a design with Platform Express, you use three areas of the interface:

• Graphical Design Editor

Create, view, and save your design, starting from a new or existing design.

• Component Browser

Select the components for your design.

• Memory Map Pane

Displays how the components map into your design's memory space. The memory map refreshes when components are added or component configurations are modified. The memory map is "Read-Only"; you cannot edit it directly.



If a design is already open, select **File** > **New** or click the **New** button. This step clears the Design Editor and allows you to create a new design. Platform Express applies the default design settings to all new designs.

- 1. Browse the available core platforms from the list of components in the component browser.
- 2. Double-click the desired core or click-and-drag the component to the design editor.

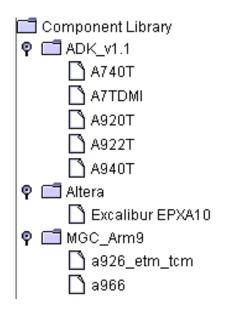


Figure 2-1. Component Browser

3. Enter your selections in the provided core configuration dialog box.

See Figure 2-2 for a sample configuration dialog box based on the ARM926 core.

4. Click OK.



The fields in the core configuration dialog boxes vary depending on the selected core.

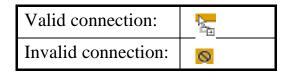
a926_1 Basic Con	figuration – Basic	
Boot Output Name	a926.x	
compiler	armcc	
compilerFlags	-c-g-I\${PXVAR_COMP	
assembler	armasm	
assemblerFlags	-g-I\${PXVAR_COMPON	
linker	armlink	
linkerFlags	-Xref -elf -map -info total	
Linker Command File Name	linkerCommandFile	
Linker Command Line Switch	-scatter	
Enable Linker Command File	V	
Current Model	Modelsim VHDL 🛛 👻	
Modelsim Pli Libraries	\${CVE_HOME}/lib/arm9:	
Ncsim Pli Build Command	make -f \${CVE_HOME}/r	
Boot source file	software/boot/init.s	
Boot source file	software/boot/reset_vect	
Boot source file	software/boot/interrupt_r	
ок	Cancel	

Figure 2-2. Example Core Configuration Dialog Box

When the dialog box closes, the core appears in the design editor.

5. Add memory and peripheral components to the buses.

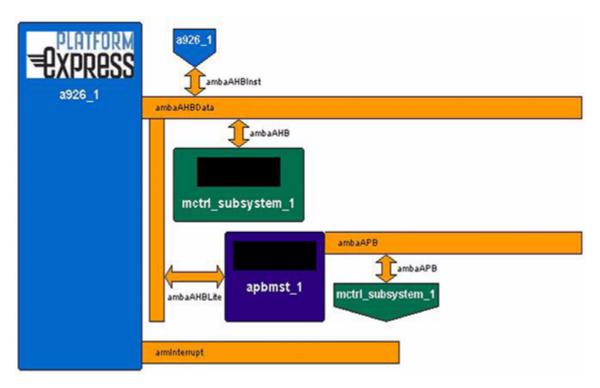
Drag components from the component browser into the Design Editor. As you drag the component over the buses, the cursor changes to indicate a valid or invalid connection.



If you drop the component while a bus is highlighted, the component attaches to that bus. If you drop a component while no bus is highlighted, Platform Express makes the required connections by default.

1. If prompted with a dialog box, specify the component's Base Address or other configuration settings and click OK.

When you close the dialog box, the component automatically connects to the selected bus on the platform. Figure 2-3 shows a simple design in the Design Editor.





Opening an Existing Design

- 1. Select **File** > **Open**.
- 2. Navigate to the desired design (a file with the *.plx extension).

You can also open a design from a shell by invoking Platform Express with a specified design (*.plx). For more information on invocation switches, refer to Table 1-1.

Using the Design Editor

The Design Editor pane is the working space for creating and manipulating your design. You can add and configure components and buses in the Design Editor. Figure 2-3 shows a basic design in the Design Editor. After you have placed components into the Design Editor, you can right-click on the components and buses for further configuration.

The Design Editor enables you to build a design with the following building blocks:

- Components
- Connectors
- Buses

The Design Editor does not allow:

- Repositioning of components, except when moving them to a new bus
- Re-routing of connections

Working with Componets

The Platform Express Component Browser displays a list of components containing platform cores, memories, and peripherals. (Refer to the Component Browser to browse the available cores for your design.) The components in the Component Browser are essentially the building blocks of your design. These components have bus interfaces. The bus interfaces connect to buses. The connections to buses are represented by connectors.

When you begin a design, only platform cores are visible in the Component Browser. Once a platform has been placed in the Design Editor, additional components appear in the Component Browser, and you can begin adding memory and peripheral components and buses. Only those components that can be connected to the currently available buses appear in the Component Browser. Components can be connected directly or through bus bridges.

Besides adding components, you may need to configure components, including master and slave components, or add bus bridges to adapt the components to the buses in the design.

Color Coding for Components

Color-coding of the cores, memories and peripherals is provided as a means for distinguishing them. Platform cores are blue. Any component that provides a bus bridge is displayed in one of eight shades of purple. All other components are assigned one of eight shades of green. Buses and connectors in the Design Editor are displayed in yellow.

Creating Component Instances



The available platform cores listed in the Component Browser vary depending on your installed libraries. If you do not see components which you believe are installed, check your PXPATH environment variable.

Insert a component into the Design Editor in one of the following ways:

- Double-click the component name in the Component Browser.
- Right-click on the component name in the Component Browser and select **Add** from the context menu.
- Select the component and drag it to the Design Editor.

Memory and peripheral components automatically connect to the appropriate bus on the core. All other connections designated as required in the component's definition file are made, such as clock and interrupt connections. If the component has connections that are not required, those connections are not made automatically.

The memory map is automatically updated when you add a component to a core. It shows where the component fits into the core address space in relation to the other components.

Configuring Components

Most components have dialog boxes that appear automatically when you place a component in the Design Editor. The configuration dialog box allows you to specify addresses and other parameters. These parameters are described and defined in the component data sheets available from the component vendor or on the component vendor's website. (To go to a component vendor's website, right-click on the component and select an entry under the Browse menu.)

- 1. In the Design Editor, select the desired component.
- 2. Right-click on the component and select **Configure** > **Basics** from the context menu.
- 3. Enter the desired parameters, based on data sheets provided by the vendor.
- 4. Click OK.

Configuring the Pin Settings

- 1. In the Design Editor, select the desired component.
- 2. Right-click on the component and select **Configure** > **Pins** from the context menu.
- 3. Select pins to export to the test bench.
- 4. Click OK.

Unconnected pins are not automatically connected or exported to the test bench. Pin names for pins that may be exported are displayed in bold.



Setting values for required drivers overwrites default values only if the driver is connected to the pin.

Deleting Components

You can delete a component by selecting the desired component and performing one of the following actions:

- Press the Del key on your keyboard.
- Select **Edit > Delete**.
- Right-click and select **Delete** from the context menu.
- Click the **Delete** button on the toolbar.

When you delete a component with a bus, the "delete" action is propagated throughout the design. The component's bus is deleted, which then deletes all the connections associated with the bus, which then deletes all the components that had a required connection to the bus.

Accessing Component Information

From the Platform Express interface, you can access information about a component directly from the vendor's web site. For example, to access information from the ARM web site:

- 1. Select the desired ARM-based component in the Design Editor.
- 2. Right-click and select **Browse** > + **ARM926EJS Technical Refenence Manual** from the context menu.

Platform Express invokes a browser and loades the specified URL.



The exact menu choice of the context menu varies depending on the selected core.

Accessing the Details Window

You can also display the Details window that contains information on the selected core. The Details window displays details about the component or bus such as instance names, types, and connections.

- 1. Select the desired component in the Design Editor.
- 2. Right-click and select **Details** from the context menu.

-	Componen	t Details
Name: Version: Path: Instance Name:		le/pxLibraries/PxArm9/componentLibrary/
Bus Interfaces:		
Bus Typ Instand Connect	nce Name: pe: se Name of Connected Bus:	anbaAHBData anbaAHB anbaAHB_1 a926_1 a926_1 a926_1 apbmst_1
Bus Typ Instand Connect	e Name of Connected Bus:	a926_1
Interfa Bus Typ Instand	ace Name:	armInterrupt armInterrupt
	nvironment Selected: Mo elected: vh	delsim
•	Cia	ise

Figure 2-4. Details window

Working with Connectors

Creating Connections

When you instantiate a component, Platform Express automatically creates all the required connections. A bus ("Bus A") can be dragged to another compatible bus ("Bus B"). This action removes "Bus A" and inserts a secondary master

connection on "Bus B." The bus interface that was previously represented by "Bus A" becomes connected to "Bus B" and is now represented by a connector.

Connecting an Unconnected Component

• Drag the component to a bus.

Platform Express automatically selects the component interface to connect to the bus, and displays the bus interface ID next to the connector.

• To change the component interface, right-click the bus interface ID and select the desired bus interface.

(This works *only* if there is more than one available, compatible bus interface. If so, an asterisk appears next to the bus interface ID. It is changed by clicking the interface ID, not the connector.)

Deleting Connections

When you delete a required connection, the component to which it belongs is automatically deleted. You can delete a connection by selecting the desired connection and performing one of the following actions:

- Press the Del key on your keyboard.
- Select Edit > Delete.
- Right-click and select **Delete** from the context menu.
- Click the **Delete** button on the toolbar.

When you delete a required connection, the component to which it belongs is deleted automatically.

Working With Buses

A *bus* refers to a path used for transmitting signals from any of several sources to any of several destinations. A *bus bridge* is a component with a master bus

interface and a slave bus interface in which signals arriving on the slave interface are translated into signals on the master interface. This allows slaves connected to the master interface to respond to signals from the master of the bus to which the slave interface is connected.

The Design Editor provides several ways of working with buses:

- Bus Views
- Automatic Bus Connections
- Changing Bus Connections
- Bus Bridges
- Multiple Bus Connections

Bus Views

The Design Editor displays the bus connections for all components in the design. It provides platform-defined views, which may include:

- All buses (default view)
- System bus only
- Interrupt bus only
- Reset bus only
- Timer bus only

You can switch between the various views using the Bus View menu in the status bar. Depending on the platform characteristics specified by the vendor in the core component's definition file, some buses may only be visible in the "all buses" view.

Automatic Bus Connections

As the component is dragged over the buses, the cursor changes, indicating where the component can or cannot be attached.

If a component is dropped while a bus is highlighted, the component attaches to that bus. If no bus is highlighted when the component is dropped, Platform Express selects a bus to connect to.

If a component can be connected to more than one available bus, Platform Express automatically connects to one of the buses. Afterwards, you can move the component to a different bus, if desired.

Changing Bus Connections

To change a component's bus connection, drag the connector (not the component) to the preferred bus.

To make connections to additional buses, drag the component to the preferred bus. If the component has additional connections available for that bus type, it remains connected to the original bus and an additional connection is made to the second bus. If the component does not have any additional connections available for that bus type, it is not moved.

Bus Bridges

Bus bridges create a bus-to-bus connection that allows components that can only connect to one bus type to connect to a different bus type. Bus bridges are displayed perpendicular to the parent bus, with the extension parallel to the parent bus.

If you add a component that requires a bus bridge to connect to an existing bus, a bus bridge selection dialog box may appear, and a dialog box for configuring the bus bridge may also appear. After the bus bridge is configured, the new bus and the component appear in the Design Editor.

Multiple Bus Connections

Components with connections to multiple buses (for example, to the system and interrupt buses) are represented once for each bus type. The first representation contain all labels and logos. Subsequent representations are arrow-shaped, with the instance name only. All representations are highlighted if any of them is selected. Components with multiple connections to a single bus show all connections from a single representation.

Master and Slave Components

Bus interfaces can be masters or slaves. Unconnected master interfaces are represented as buses. Primary bus masters appear as components on the left side of the Design Editor. Secondary bus masters are displayed above the bus. Bus slave components are displayed below the bus. When the maximum number of master or slave components have been added to a bus, an error message appears.

Configuring Buses

Right-click on the bus and select **Configure** > **Decoder Selection** or **Required Drivers** from the context menu to configure the bus. The required drivers are used when you build the design. The "Decoder Selection" determines which decoder module to apply to the selected bus. (The default selection is based on the HDL language you have chosen for your design.)



The full path to the decoder is stored in the design. If you move the location of the libraries or the design, you may have to reconfigure the decoders.

The Required Drivers configure the generated drivers for unconnected bus pins, or for bus pins that require a driver. There are three types of drivers: Clock, Reset, and Fixed Value. The Clock and Reset drivers are exported to the test bench level. You can select whether to export the Fixed Value driver. See Configuring the Decoder Selection and Configuring the Required Drivers in Chapter 3 for more information.

Chapter 3 Building Designs

Overview

This chapter contains procedural information on configuring and building your design with Platform Express. It contains the following sections:

- Before you begin
- Configuring the Build
- Building your Design

Before you begin

This chapter assumes that you have properly installed Platform Express (including libraries), and have configured your environment to run Seamless CVE and any other required build tools (for example, ARM compilers and assemblers). Check that you have defined the following environement variables: PXHOME, PXPATH and MODELTECH. Consult the *Platform Express Installation Manual* for complete instructions. This chapter also assumes that you have created a design. See Chapter 2, Creating Designs, for information.



You cannot perform a build unless your environment is properly configured. For example, if you select an ARM core, your environment must be configured to run the ARM tools.

Configuring the Build

The configurable design elements of your project are entirely dependent on the core platform you have selected for your design. Before building, you may need to set signals for driving unconnected pins, specify where to load the software, or generate code for remapping address ranges.

Defining all configurable components

Select **Settings > Configure All** to access all of the configurable components of your entire design. The Required Configuration dialog box appears. The Required Configuration dialog box enables you to configure your entire project from one dialog box interface. The following configurable top-level elements are:

- Design
- Component
- Bus

The exact fields listed in the Required Configuration dialog depend on the core and other modules of your design.

Defining configurable components separately

In addition to the all-encompassing Required Configuration dialog, other separate build configuration dialogs include:

Dialog Box Name	Access	Purpose
<pre><design file="" name="">Project Settings Configuration — Basic</design></pre>		Define settings for the current project.

Table 3-1. Configuration Dialog Boxes

Dialog Box Name	Access	Purpose
< <i>core name</i> >Basic Configuration — Basic	Right-click on the core and select Configure > Basics from the context menu.	Define basic settings for the selected component.
< <i>core name</i> >Pin Configuration — Pins	Right-click on the core and select Configure > Pins from the context menu.	Select which pins to export to the test bench.
<core name="">Scatter Loader Configuration — Scatter Loader Panel</core>	Right-click on the core and select Configure > Scatter Loader from the context menu.	Define the load addresses for software modules.
<core name="">Software Memory Configuration — Software Memory Configuration Panel</core>	Right-click on the core and select Configure > Software Memory from the context menu.	Define custom memory configurations.
 <bus_name>Decoder Selection Configuration — Decoder Selection Panel</bus_name>	Right-click on a bus and select Configure > Decoder Selection from the context menu.	Choose the decoder module to apply for the selected bus.
<i><bus_name< i="">>Required Driver Configuration</bus_name<></i>	Right-click on a bus and select Configure > Required Drivers from the context menu.	Configure the generated drivers for unconnected bus pins (or for pins marked as <i>requiresDriver</i>).

Table 3-1. Configuration Dialog Boxes

Setting Driver Signals

Drivers can be connected to components or buses. There are three types of drivers:

• Fixed

- Single-shot
- Clocks

If not otherwise configured using the Required Drivers or Pin Configuration dialog boxes, single-shot and clock drivers will be initialized with the design's default values.

Pins with complex drivers (for example, clock drivers and single-shot drivers) must be exported to the test bench to be configured. The HDL code generated for complex drivers cannot be synthesized. Pins with simple (fixed value) drivers may be initialized in Platform Express or exported to the test bench. The pin drivers will only be created if the pin is not connected to a bus. If the pin is connected to a bus, the bus decoder logic must drive the pins as necessary.

Configuring the Required Drivers

At the beginning of the build process, Platform Express verifies that all required signal levels and the duration for certain signals within your design (as required by the components' definition files) have been configured either by default or by the user. (The "Required Driver Configuration" dialog box appears if any required signals have not been configured.)

To manually access the "Required Drivers" dialog box:

- 1. Select the desired bus.
- 2. Right-click on the bus and select **Configure** > **Required Drivers** from the context menu.

The Required Driver Configuration dialog box appears.

ami	baAHB_1 Required Driver Configuration	
Configure bus - Required Driver - Required Driver - ambaAHB_1 - ambaAHI - ambaAHI	10.0 20.0 10.0 Phase 1: Value : 1 For : 10.0 ns Value : 1 For : 10.0 ns Phase 2: Value : 0 For : 20.0 ns Value : 0 For : 20.0 ns Value : 1 For : 10.0 ns	ns V
•		
	OK Cancel	

Figure 3-1. Required Driver Configuration dialog box

3. In the "Required Drivers" folder in the left-hand column, select the desired driver from the bus folder.

By default, the first driver in the bus folder is displayed automatically.

4. In each "Value:" field(s), supply a value for each required signal (delineated in the dialog box with "Phase N").

The allowed values for the "Value" field are: 0, 1 or nothing.

- 5. In the "For:" field corresponding to each "Value:" field, enter the desired duration.
- 6. In the drop-down menu to the right of each "For:" field, select one of the following time units:

> ns (nanosecond: one billionth)

- > fs (femtosecond: one quadrillionth)
- > ps (picosecond: one trillionth)
- > us (microsecond: one millionth)
- > ms (millisecond: one thousandth)
- > sec (second)
- > min (minute)
- > hr (hour)
- 7. Click OK.

You must specify all required signals *before* building your design.

Configuring the Decoder Selection

The "Decoder Selection" refers to the specific decoder module that is applied to a given bus. The default selection is based on the current design's HDL language.

- 1. Select the desired bus.
- 2. Right-click on the bus and select **Configure > Decoder Selection** from the context menu.

The Configure Decoder Selection dialog box appears.

Name	Language	Path		
arminterrupt_v1.0	vhdl	export/home/leritz/Px1.1e/pxLibraries/Utility/componentLibrary/decoder/armInterrupt.xml		
arminterrupt_v1.0	verilog	/export/home/leritz/Px1.1e/pxLibraries/Utility/componentLibrary/decoder/armInterrupt_vlog.xml		
		,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		

Figure 3-2. Configure Decoder Selection Dialog Box

3. Select the desired decoder from the list and click **OK**.



The values in the Name, Language and Path fields in the "Configure Decoder Selection" dialog box are Read-Only.

Defining the Pin Configuration

Some pins in a component's definition file may be specified to allow exporting. Exported pins emerge in the HDL-generated code. Unconnected pins are not automatically connected or exported.

- 1. Select the desired component.
- 2. Right-click on the component.
- 3. Select **Configure** > **Pins** from the context menu to set pin driver values.



Pins that can be configured use a bold font for their values.

Pin Configuration Example

In Figure 3-3, DRDMAADDR, IRDMAEN, DBGEN, DBGEIBKPT, INITRAM, BIGENDINIT, and DBGnTRST are all configurable pins.

Exported	Pin Name	Value	Strength	
	DRADDR	N/A	N/A	٦
	CPINSTR	N/A	N/A	1
	DHREADY	N/A	N/A	
	CPPASS	N/A	N/A	1
	IRIDLE	N/A	N/A	7
	DHWDATA	N/A	N/A	1
	DHBURST	N/A	N/A	1
	DRDMAADDR	0x00000	N/A	1
	ETMDA	N/A	N/A	1
	IRDMAEN	0	N/A	1
	DHRDATA	N/A	N/A	1
	DHGRANT	N/A	N/A	1
	DHADDR	N/A	N/A	1
	DBGINSTREXEC	N/A	N/A	7
	ETMCHSD	N/A	N/A	7
	DBGEN	1	N/A	1
	DBGIEBKPT	0	N/A	1
	IHRESP	N/A	N/A	1
	INITRAM	0	N/A	٦
	nCPMREQ	N/A	N/A	
	BIGENDINIT	0	N/A	1
	HRESETn	N/A	N/A	-
	ETMIABORT	N/A	N/A	1
	DBGnTRST	1	N/A	

Figure 3-3. Pin Configuration dialog box

Using the Scatter Loader

The scatter loader is used to specify the load addresses for software modules. (See Table 3-2 for a list of supported data types in the scatter loader.)

Follow these steps to access and manipulate the data in the scatter loader dialog box:

1. Right-click on the platform core and select **Configure > Scatter Loader** from the context menu.

The Scatter Loader Configuration - Scatter Loader Panel dialog box appears with the current CPU.

- 2. Assign software modules to execution regions by highlighting unassigned files in the left panel, highlighting a target execution region in the right panel, and clicking the add (>>>) button.
- 3. Remove software modules by highlighting the filename in the right panel and clicking the remove (<<<).

Platform Express creates default load and execution regions based on the memory map of the address space.

Unassigned Files	Memory Image Files
Sources	Execution Regions LoadRegion_1 (0x00000) Root (0x00000) interrupt_handler.o CONST interrupt_handler.o CODE a926_a926Diags.o CODE pxDiagnostics.o CODE pxDiagnostics.o CODE pintToPort.o CODE pinto CONST reset_vectors.o CONST reset_vectors.o CODE init.o CONST init.o CODE a926_a926Diags.o CONST a926_a926Diags.o DATA a926Diags.o DATA a926Diags.o DATA a926_a926Diags.o DATA a926_a926Diags.o DATA a926_a926Diags.o DATA a926_a926Diags.o BSS printToPort.o DATA a926_a926Diags.o BSS printToPort.o DATA a926_a926Diags.o DATA

Figure 3-4. Scatter Loader dialog box

Adding Execution Regions

Each memory unit in your design is displayed in its own Load Region. (See the Memory Image Files column in the Scatter Loader dialog box.) To place code into

a given Load Region, you must ensure that it is also placed in an Execution Region.



Platform Express automatically creates an Execution Region for the default RAM and ROM in the design.

Follow these steps to add a new software Execution Region:

- 1. Right-click on the platform core and select **Configure > Scatter Loader** from the context menu.
- 2. Select the desired Load Region folder in the Memory Image Files column.
- 3. Click the **Add Execution Region** button below the Memory Image Files column.

The Add Execution Region dialog box appears.

- Add Executi	on Region 🛛 🕐 🗖
Execution Region Name	
Execution Region Base Address	0x40000000
ОК	Cancel

Figure 3-5. Add Execution Region dialog box

- 4. Enter a name and base address for the new execution region.
- 5. Click **OK**.

Scatter Loader Data Types

The Scatter Loader uses a limited set of data types. Table 3-2 lists the set of data types.

Data Type	Description
CODE (RO-CODE)	Read-Only Instruction Code: for loading into ROM only.
CONST (RO-DATA)	Constant Data - Strings, Constants, and Literal Pool data: can be loaded into either ROM or RAM.
DATA (RW)	Read/Write areas of your code: for loading into RAM only.
BSS (ZI)	ZI (Zero Initialization) Read/Write areas of code: for loading into RAM only.

Table 3-2. Sca	tter Loader	Data	Types
----------------	-------------	------	-------

Remapping Address Ranges

Platform Express provides support for peripherals that can change the address where they reside based on the state of other signals (remap signals). The bus decoder generates the appropriate HDL code.

Configuring Software Memory

Platform Express enables you to add custom memory configurations with the "Software Memory Configuration Panel." (See Figure 3-6.) You have the ability to add, edit and remove your custom software memory. The Memory Map Pane immediately refreshes to display your custom software memory configuration. Custom software memory configurations appear in blue.

- 1. Right-click on the core and select **Configure > Software Memory** from the context menu.
- 2. In the Software Memory Configuration dialog box, click Add.
- 3. In the Software Memory Properties dialog, enter a value for the Name, Address, and Size fields.
- 4. Click OK.
- 5. Click OK again.

a926_1 Software Memory Configuration – Software Memo		
Address Space Name Memory -		
Name	Address	Range
	Add Remove E	-clit

Figure 3-6. Sofware Memory Configuration Panel

Saving Your Design

When you save a design, Platform Express creates a project directory for your design. Platform Express names the project directory using the design name, *project_name*, which you specified when you saved your design. The project directory can include:

- The project design file. *project_name.plx*, which is created when you select **File** > **Save**, and specifies:
 - Components contained in your design
 - o Parameters for those components
 - o Component and interrupt connections

Platform Express uses the information in the project design file to build the design.

- The project settings that apply specifically to that project.
- The *verificationEnv* directory, which is created when you select **Tools** > **Build**, contains the following subdirectories:
 - o verificationEnv/{simulator}/hdl

where {simulator} is either Modelsim or Ncsim.

Contains Verilog and VHDL source files for your hardware design.

o verificationEnv/software

Contains software source code and related include files for the software design that is to be executed on your design. There is a subdirectory for each supported simulator containing build scripts, compiled HDL, and Seamless configuration files. Refer to "Appendix A, Directory Structures," for a complete list of directories.

o *verificationEnv*/exec



If you select **Tools > Build** before you have saved your design, Platform Express creates a unique directory for the design.The directory name begins with plx.

Hardware Design Files

Hardware design files are top-level HDL files that instantiate components and define how the platform core connects to any decoders, bus bridges, and interrupt-handling structures in your design.

- Decoder-logic HDL design files, which implement the interconnection logic between components and the platform buses.
- Top-level HDL
- Build scripts

• HDL test bench

Software Design Files

Software design files can contain:

- Boot code, both assembly language (for cores) and C-language (for peripherals and memories).
- Build scripts for compiling, linking, and assembling.
- Top-level C-language code for calling initialization and diagnostics functions.
- Interrupt-service routines.

Use the Scatter Loader to specify where to load the software. See Using the Scatter Loader for more information.

Building your Design

Platform Express builds the design files based on the the component definition files, project settings, scatter loader, and any other configuration settings that you make during design creation. Building a design generates hardware *and* software files, and can also set up signals for driving unconnected pins, and generate code for remapping address ranges.



The **Tools** > **Build** menu is disabled until you have inserted a platform core into the Design Editor.

1. Select **Tools** > **Build**.

The Output pane displays the build status. See Appendix C, Build Log File, for an example log from a successful build.

2. To stop the build process before it completes, select **Tools** > **Stop**.

After a design has been built with no errors, it can be run in batch mode from the command line. Refer to Table 1-1 for a complete list of invocation switches.

Chapter 4 Verifying Designs

Overview

This chapter contains high-level conceptual and basic procedural information on verifying a design created with Platform Express. It contains the following sections:

- Invoking a Co-Verification Session
- Using the Co-Verification Session

This chapter does not cover specific usage instructions for Seamless CVE. For application-specific functionality, refer to the *Seamless CVE User's Guide and Reference Manual*, which is supplied in both PDF and HTML, and is accessible online from the **Help** menu in the Seamless CVE main window.

Before you begin

This chapter assumes that you have properly installed Platform Express (including libraries), and have configured your environment to run Seamless CVE and any other required build tools (for example, ARM compilers and assemblers). Check that you have defined the following environement variables: PXHOME, PXPATH and MODELTECH. Consult the *Platform Express Installation Manual* for complete instructions. This chapter also assumes that you have created and successfully built a design. See Chapter 2, Creating Designs, and Chapter 3, Building Designs, for information.

Invoking a Co-Verification Session



The **Tools** > **Execute** menu is disabled until you have successfully built your design. If you have not built your design, you must Select **Tools** > **Build** *before* selecting **Tools** > **Execute**.

Before attempting to invoke a co-verification session, ensure that you have properly built your design. Refer to Chapter 4, "Building Designs," for more information.

To launch a hardware/software co-verification session that uses Seamless CVE, select **Tools** > **Execute** or click the **Execute** button from the Platform Express interface. If your environment is configured properly, Platform Express invokes the Seamless co-verification tools, which use the design files generated during the Platform Express build process.



Platform Express uses environment variables to invoke Seamless CVE. If Platform Express fails to invoke Seamless CVE, the likely cause is an improperly configured environment. Consult the *Platform Express Installation Manual* for information on environment settings.

	Seamless CVE -	- run.cve	•
<u>File Setup Optim</u>	ize <u>V</u> iew <u>P</u> referer	nce	<u>H</u> elp
General Setup	CPU Setup ∫= <mark>⊮</mark> ∰	Optimizatio	n Run
Processor List: -			
	ame a926_1.uARM926EJS	Proc Type Sarm926ejs_rev0 M	Address : A Memory
cve>			

Figure 4-1. Seamless CVE Interface

See Figure 4-1 for a screen captures of the Seamless CVE interface. Other applications within the Seanless Co-Verification Environment include the XRAY Debugger (Figure 4-2), ModelSim (Figure 4-3), and the Wave viewer (Figure 4-4).

After a design has been executed with no errors, it can be built and loaded into Seamless in batch mode from the command line. Refer to the *Platform Express Installation Manual* for information on invocation switches.

	xray ·	– Code = @	arm926	ejs_rev0:R	DI–1.5 [Unattacl	ned]	· ·
∏ <u>F</u> ile	<u>E</u> dit Fi	nd <u>V</u> iew	Tools	Debug	Windows		<u>H</u> elp
File: mpone	nt/a926/1	.0/softwar	e/boot/r	eset_vect	ors.s Line:[
Gol Step	Next St	tepI Next	I GoRtn	Stop Ur	Down Cancel	Conn+	HW-Step
and it assessed		HW-NextI					
	the croppe						
14		MPORT inte					
15 16	11	MPORT [Ima	дерркорр	Basel ; S	tart of ROM		
17	В	Res	et_Handl	er			
18	В		efined_H				
19	B		_Handler				
20	B		fetch_Handl				
22	_	OP			served vector		
23	В		_Handler				
24	В	FIQ	_Handler				
25 26	A1	LIGN					
					0		
ASM ASM	A SEC A P	eset_vecto	15.57		IK		
inc> bi T	estMain						
And and a second se	ile /expor	rt/home/le	ritz/Px1	.1d_final.	_release/pxhome	/compone	ntLibrary/
Stop> [H
					[

Figure 4-2. XRAY Debugger interface

Mod	elSim SE PLUS 5.5f
<u>F</u> ile <u>E</u> dit <u>D</u> esign <u>V</u> iew <u>P</u> roject	<u>Run Compare Macro Options Window</u> <u>H</u> elp
🕹 🧉 i 🔁 i 🔃 🚺 🚺	1 D. D. X P. 7
 pxtestbench: pxtestbench(top_1: top(platformexpr Package cve_direct Package tech_virtex Package tech_generic Package tech_atc35 	incorrect address decoding # Time: 0 ns Iteration: 1 Instance: /pxtestbench/top_1/ pxdecoder_ambaahb_1 # ** Warning: NUMERIC_STD.">=": metavalue detected, r eturning FALSE # Time: 0 ns Iteration: 1 Instance: /pxtestbench/top_1/ pxdecoder_ambaapb_1 # CVE NOTE: Instance "/pxtestbench/top_1/a926_1/uarm 926ejs" waiting for connection from software process # CVE NOTE: Instance "/pxtestbench/top_1/a926_1/uarm 926ejs" connected to software process.
Now: 0 ns Delta: 3	sim:/pxtestbench

Figure 4-3. ModelSim interface

-			e – de					•
<u>Eile Edit C</u> ursor <u>Z</u> oom	Compare	<u>B</u> ookmark	Format	Window				
≠∎∉ % ∿® ≠1≠1>1	K A	ויביבר	00	Q Q B K		. D. X	1	 + +
<pre>top_ambaapb_1_pr top_ambaapb_1_pr top_ambaabb_1_pr top_ambaahb_1_hr a926_1_dhaddr a926_1_dhburst a926_1_dhburst a926_1_dhburst a926_1_dhlock a926_1_dhlock a926_1_dhrott a926_1_dhrott a926_1_dhready a926_1_dhready a926_1_dhresp a926_1_dhresp a926_1_dhresp a926_1_dhrest a926_1_dhrest a926_1_dhwdata a926_1_dhwdata a926_1_dhwdata a926_1_dhwdata a926_1_dhwdata a926_1_dhwdata a926_1_dhwdata a926_1_dhburst a926_1_ihburst a9</pre>	U U							
	0	ns	1.1.1	1 1 1	00	1.1.1	1 1	1
	0	ns Ons						

Figure 4-4. Wave viewer interface

Using the Co-Verification Session

The actual design verification is conducted with Seamless CVE, using files generated by Platform Express. A Seamless co-verification session consists of three major processes:

- Seamless CVE, which coordinates the hardware and software simulation processes and provides optimizations that speed simulation.
- An Instruction-Set Simulator (ISS), which models the processor's instruction set and executes target processor code. Examples of supported instruction set simulators include the XRAY Debugger from Mentor Graphics and MULTI from Green Hills Software.
- A logic simulator, which simulates the hardware design, including a Seamless-compatible bus interface model of the processor and Seamless compatible memories. Examples of supported logic simulators include ModelSim from Model Technology and NC-Sim from Cadence Design Systems.

The co-verification process requires an interaction between the hardware and software simulations. The software simulator must execute instructions and the hardware simulator must run the corresponding logic simulation for the co-verification to progress.

The simulators may start automatically, because of the default behavior for the simulator, or because of commands contained in scripts that Platform Express generates and specifies as part of the simulator invocation. Alternatively, it may be necessary to start co-verification by clicking the **Run** button on the Seamless main window. When Seamless starts co-verification, the **Run** button changes from red to green.

It may also be necessary to start simulation manually from the hardware and software simulators.

Starting HW/SW Simulators Examples

- To start the ModelSim hardware simulator, move the cursor to the ModelSim command line and enter the command run 10000.
- To start an ISS software simulator, from the graphical user interface of the ISS/debugger:
 - \circ click the Go button.

or

• repeatedly click the **Step Instruction** button.

For detailed information on the Seamless Co-verification Environment (CVE), refer to the *Seamless CVE User's Guide and Reference Manual*, which is supplied in both PDF and HTML, and is accessible online from the **Help** menu in the Seamless CVE main window.

Chapter 5 Use Case Example

Overview

This chapter contains a step-by-step tutorial for creating a design with Platform Express using the PxArm9 component library. This "use case" scenario provides step-by-step procedures as well as some conceptual explanations behind the procedures.

Set up your environment

This "Use Case" uses the following components and tools:

- PxARM9 Library
- ARM Build tools
- Seamless CVE
- ModelSim (logic simulator)
- XRAY (instruction set simulator)

Use the following commands to set up your environment, using your specific path locations.

- 1. setenv PXHOME /user/name/platform_express/pxhome
- 2. setenv PXPATH

/user/name/platform_express/pxLibraries/AMBA:/user/name/pl atform_express/pxLibraries/Inventra:/user/name/platform_ex press/pxLibraries/Leon2:/user/name/platform_express/pxLibr aries/PxArm9:/user/name/platform_express/pxLibraries/Utili ty:/export/home/leritz/Px1.1e/pxLibraries/PxSample

3. setenv MODELTECH /user/name/model_5.5f/modeltech

- 4. setenv CVE_HOME /user/name/seamless_cve/cve_home.ss5
- 5. setenv ARMTOOLS /user/name/arm_tools/arm2.51/ss5/bin

Invoke Platform Express

\$PXHOME/bin/px

Begin Your Design

The following procedures require you to select components from the Component Browser. You will also manipulate the components in the Design Editor.

Select the Core

- 1. In the Component Browser, open the PxArm9 folder.
- 2. Double-click the ARM926EJ-S core.
- 3. In the "Configure a926 Basic" dialog box, accept the default values and click OK.

	ambaAHBData
-GAPRGDD a926_1	ambaAHBInst
	arminterrupt

The ARM926 core appears in the design editor. Notice that the Component Browser refreshes with all the available IP components that are compatible with the ARM926 core. Also notice that the memory map pane refreshes to display the occupied address locations. The available address locations are also displayed.

Add a Memory Component

- 1. In the Component Browser, open the Leon2 folder.
- 2. Double-click the mctrl_subsystem memory component.
- 3. In the "Bus Bridge Required" dialog box, click OK.



4. In the "Configure apbmst - Basic" dialog box, accept ModelSim as the logic simulator model and click OK.

— Configure apbmst – Basi				
Current Model	Modelsim VHDL 🔻			
ОК	Cancel			

5. In the "Configure mctrl_subsystem - Basic" dialog box, enter a value for the "Control Registers Base Address" field.

For example: 0x1000000

Accept the default values for the Current Model, PROM Size, SRAM Size, and Enable SDRAM Controller.

Control Registers Base Address:	
Current Model	Modelsim VHDL 👻
PROM Size (base address 0x0):	4M 👻
SRAM Size (base address 0x40000000):	4M 👻
Enable SDRAM Controller:	False 👻

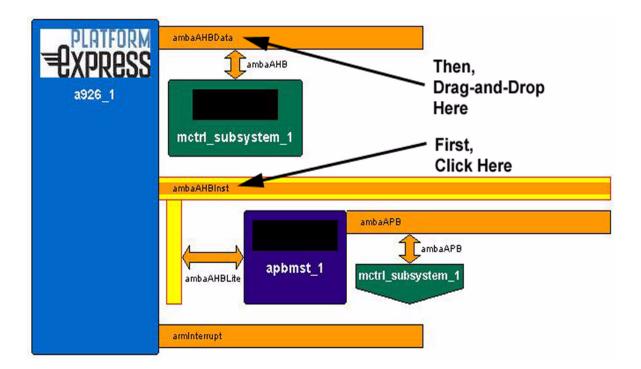
Your design now looks like this in the Design Editor:

EXPRESS a926_1	ambaAHBData ambaAHB ambaAHB mctrl_subsystem_1
	ambaAHBInst ambaAPB ambaAHBLite apbmst_1 apbmst_1 apbmst_1 aminterrupt

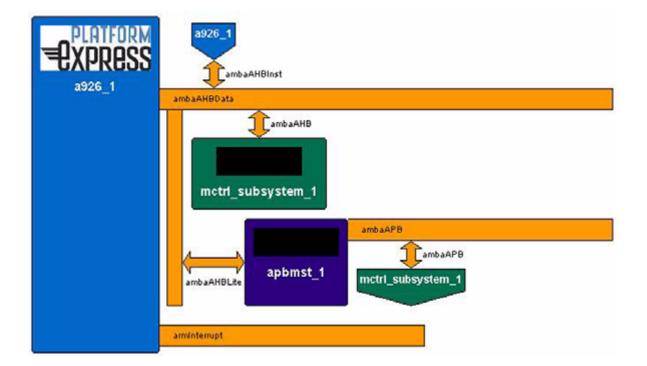
And the Memory Map Pane now looks like this:

a926_1:Memo	ry
0x0	mctrl_subsystem_1
0x400000	
0x10000000	mctrlRegisters
0x10000040	
0x40000000	mctrl_subsystem_1
0x40400000	
OxFFFFFFFF	

6. Click the ambaAHBInst bus and drag-and-drop it on the ambaAHBData bus. (See the figure below.)



Your design now appears as follows:



Save the Design

Select **File > Save** and provide a design name in the Save dialog box.

Design Explanation

The preceding design has two buses: one for instruction, the other for data. In this design, all peripherals are accessible to both the instruction bus and the data bus. This particular scenario (in which ROM must be visible to both AMBA buses) is specific to the ARM926 core.

Build Your Design

- 1. Select **Tools > Build** to execute the build of your newly-created design.
- 2. In the "Required Configuration" dialog box, accept all the default values and click OK.

The Output pane displays the build log. (See Appendix C, Build Log File, for a complete build log of a successful build.) The last few lines of your successful build should be something like:

```
Debug Area Optimization Statistics

Input debug total(excluding low level debug areas)

10976 (10.72Kb)

Output debug total 8416

(8.22Kb)

% reduction

23.32%

ARM Linker: finished, 0 informational, 5 warning and 0

error messages.
```

The build process generates the following:

• HDL description of the design

- software, such as low-level design diagnostics
- complete Seamless CVE configuration files (including the logic simulator and instruction set simulator configuration files)

As part of the build process, Platform Express identifies all the software code modules in your design and places them appropriately into ROM and RAM. The build process also checks several other design details, including which bus decoders to use, as well as clock and reset stimuli.

Simulate Your Design

After the build process is complete, you can now verify that the design works. Select **Tools > Execute** to invoke the Seamless Co-Verification Environment (CVE). The following applications are loaded:

- Seamless CVE
- ModelSim
- Waveform viewer

To invoke the XRAY Debugger, issue the following command from the ModelSim command prompt:

run -all

Verify Your Design

Use Seamless CVE to begin verifying your design created with Platform Express. For example, you may want to examine the HDL design hierarchy created in ModelSim.

- 1. In ModelSim main window, select **View > Structure**.
- 2. In the Structure window, expand the "top_1" component.

Note that each bus in the design has a component called "pxdecoder_*busname*."

3. In the ModelSim main window, select **View > Source**.

A source window appears with the "top.vhd" HDL displayed.

4. When are finished with your Seamless CVE session, select File > Exit from the Seamless CVE window.



Before you make any enhancements to your Platform Express design, you must close Seamless CVE. Until the verification process has stopped, you cannot add components or reconfigure existing components.

Cycle through the Design Flow

Now that you have completed one design cycle, you can make changes and enhancements to your Platform Express design and cycle through the design flow again.

Appendix A Directory Structures

Overview

This appendix contains the directory structures of:

- the default Platform Express installation
- the directories created from a build of a design

Platform Express Directory Structure

The following is the default list of directories and sub-directories in \$PXHOME:

Directory	Description
Pxkey	Key file used for licensing
api	Application Programming Interface for component developers and integrators
bin	Contains Platform Express startup command (px) and a script for the default browser
doc	Online help files and schema diagrams for component developers
etc	Miscellaneous files
images	Icon image files

Table 1-1	Platform	Express	Installation
	1 lationin		instanation

Directory	Description
mgls	Mentor Graphics licensing server
schema	XML schema documents
tools/bin	Tools and applications for component developers and integrators.

Table 1-1. Platform Express Installation

Directory Structure of Generated Design

Select **File** > **Save** to save your design files after you have built your design. A directory is created with your project name (for example, myProject). Your design is saved in the project directory (for example, myProject.plx).



The design file must have the same name as the project directory and must have the .plx extension.

After the design is built and saved, the resulting directory structure is similar to the following:

```
myProject
myProject.plx
  |--verificationEnv
      --Modelsim
         --exec
         --hdl
             --work
                --a926
               |--arm926ejs
               |--arm926ejs_lib
                --arm926ejs_rev0_engine_e
               --pxconfig_pxtestbench
               --pxconfig_top
                --pxdecoder_ambaahb_1_module
               --pxdecoder_ambaapb_1_module
                --pxtestbench
               --top
          --software
            --a926_Memory
               |
|--coreDiagnostics
|
|--_a926_1
```

Directory	Description
myProject	Root project directory (example project name)
verificationEnv	Contains generated design files.
Ncsim	Contains design for NC-sim simulation (if selected)
Modelsim	Contains design for Modelsim simulation (if selected)
exec	Contains generated files for Seamless CVE execution
hdl	Generated HDL files, build scripts and compiled models
software	Generated software files, build scripts, object files and executable images

Table 1-2. Directory Structure of Platform Express Design

Appendix B Frequently Asked Questions (FAQs)

Overview

As an alternate approach to traditional documentation, the *Platform Express User's Guide* contains a list of Frequently Asked Questions (FAQs) to assist the user with common questions and/or problems. This set of FAQs is categorized by:

- Product Questions
- General Usage
- Error Messages

Product Questions

Q. Can I use other co-verification tools besides Seamless CVE?

A. No, Platform Express is designed specifically to work with the Seamless Co-Verification environment.

Q. Can I use other logic simulators besides ModelSim?

A. Yes, in addition to ModelSim, Platform Express currently works with NCSim. Support for other logic simulators is planned for future releases.

General Usage

Q. Can I simultaneously run more than one instance of Platform Express?

A. Yes, as long as you do not try to open the same design in two separate invocations of Platform Express.

Platform Express supports only one instance of a design at a time. Future releases of Platform Express will support file locking, which will gracefully warn the user when a design is already open.

Q. I've successfully built my design. How do I know if it built correctly?

A. Barring any error messages in the output pane, you can assume your design was built correctly. Refer to "Appendix C, Build Log File," to review a sample log file from a properly-built design.

Q. I've properly defined the PXPATH environment variable. Why aren't the libraries displayed in the Component Browser?

A. Check the Output pane's log messages for validation errors on the libraries. If there are no errors, remember that peripheral and memory components are not displayed in the Component Browser until you have instantiated the platform core. Refer to "Chapter 2, Creating Designs," for instructions on instantiating the platform core.

Q. Why didn't the Instruction Set Simulator (ISS) of the Seamless CVE automatically load when I selected **Tools > Execute**?

A. Some Instruction Set Simulators do not start immediately when Seamless starts. You may need to start the logic simulator and advance until the processor comes out of reset. For example, for ModelSim, enter the following at the command prompt:

```
run -all
```

Error Messages

Q. I've defined my environment to point to my Seamless CVE and ModelSim installation. Why am I still getting build errors? For example, I'm getting the following error below:

```
##
           Platform Express, Version 1.1d
##
           SoC Verification Division
##
##
##
           Mentor Graphics Corporation
##
##
##
## Generated on: September 19, 2002 3:46:21 PM PDT
##
## Generated by: leritz
##
## Modelsim HDL compile script
##
if [ -f pxenv ] ; then . ./pxenv; fi
if [ ! -d work ] ; then vlib ./work; fi
./compileHdl.sh: vlib: not found
cveRunsh:cve:not found
```

A. Ensure that you have defined the bin directories of Seamless CVE, ModelSim, and any other required build tools (such as ARM tools) in your path. For example, the following path statement enables Platform Express to invoke the Seamless CVE tools:

```
setenv PATH
/user/tools/modeltech/bin:/user/tools/cve_home.ss5/bin
```

Q. I've defined my environment to point to my Seamless CVE and ModelSim installation, and also included the bin directories of Seamless CVE and ModelSim in my path. Why am I still getting errors?

A. Ensure that you are using the supported versions of Seamless CVE and logic simulators. Platform Express is certified to run with specific versions only. Consult the *Platform Express Release Notes* for the latest information on supported Seamless CVE and logic simulator versions.

Q. Why do I get the following error message when I invoke Platform Express?

```
[ERROR] - Validation failed on path
/export/home/leritz/Px1.1d_3/pxhome/pxLibraries
```

A. When it is invoked, Platform Express loads the libraries defined by the PXPATH environment variable. The PXPATH variable is a colon-separated list of paths in which each path points to the top of a component library. For example:

```
setenv PXPATH
/home/user/apps/pxLibraries/AMBA:/home/user/apps/pxLibraries/
INVENTRA:/export/home/leritz/Px1.1d3/pxLibraries/Utility
```



Do not install component libraries (pxLibraries) in a sub-directory under PXHOME.

If you do not set the PXPATH variable, the primary default is as follows: if the current working directory (where you invoked Platform Express) contains a subdirectory named pxLibraries, a default PXPATH is constructed from all the subdirectories of ./pxLibraries. The secondary default is as follows: if there is a directory named pxLibraries in the same parent as PXHOME, then a default PXPATH is constructed from all the subdirectories of \$PXHOME/..pxLibraries.

Appendix C Build Log File

Overview

This appendix contains the output of a log file from a successful build. The following design example was based on the PxArm9 library, using ARM tools. Review this log file for an example of a properly-built design.

```
##
               Px Generated File
##
##
           Platform Express, Version 1.1d
##
           SoC Verification Division
##
##
##
           Mentor Graphics Corporation
##
##
##
## Generated on: October 3, 2002 10:28:40 AM PDT
##
## Generated by: leritz
##
## Modelsim HDL compile script
##
if [ -f pxenv ] ; then . ./pxenv; fi
if [ ! -d work ] ; then vlib ./work; fi
vmap work ./work
Modifying modelsim.ini
           ${CVE_HOME}/vsim_vhdl/arm926ejs_rev0.vhd
vcom
      -93
Model Technology ModelSim SE vcom 5.5f Compiler 2002.01 Jan 7
2002
-- Loading package standard
-- Compiling entity arm926ejs_rev0_engine_e
```

-- Compiling architecture engine a of arm926ejs rev0 engine e -- Loading package textio -- Loading package std logic 1164 -- Compiling entity arm926ejs -- Compiling architecture model of arm926ejs -- Loading entity arm926ejs_rev0_engine_e -- Compiling package arm926ejs lib vcom -93 \${a926_1}/componentLibrary/component/a926/1.0/hdlsrc/A926_mod .vhd Model Technology ModelSim SE vcom 5.5f Compiler 2002.01 Jan 7 2002 -- Loading package standard -- Loading package std_logic_1164 -- Loading package arm926ejs_lib -- Compiling entity a926 -- Compiling architecture struct of a926 -- Loading package textio -- Loading entity arm926ejs vcom -93 PxDecoder_ambaAPB_1_module.vhd Model Technology ModelSim SE vcom 5.5f Compiler 2002.01 Jan 7 2002 -- Loading package standard -- Loading package std_logic_1164 -- Loading package numeric std -- Compiling entity pxdecoder_ambaapb_1_module -- Compiling architecture platformexpress of pxdecoder_ambaapb_1_module vcom -93 PxDecoder_ambaAHB_1_module.vhd Model Technology ModelSim SE vcom 5.5f Compiler 2002.01 Jan 7 2002 -- Loading package standard -- Loading package std_logic_1164 -- Loading package numeric std -- Loading package attributes -- Loading package std_logic_misc -- Compiling entity pxdecoder_ambaahb_1_module -- Compiling architecture platformexpress of pxdecoder_ambaahb_1_module vcom -93 top.vhd Model Technology ModelSim SE vcom 5.5f Compiler 2002.01 Jan 7 2002 -- Loading package standard

-- Loading package std logic 1164 -- Compiling entity top -- Compiling architecture platformexpress of top -- Loading package arm926ejs lib -- Loading entity a926 -- Loading package std_logic_arith -- Loading package target -- Loading package device -- Loading package textio -- Loading package config -- Loading package sparcv8 -- Loading package iface -- Loading package amba -- Loading entity leon2_apbmst -- Loading package std_logic_unsigned -- Loading entity mctrl subsystem -- Loading package numeric_std -- Loading entity pxdecoder_ambaapb_1_module -- Loading package attributes -- Loading package std_logic_misc -- Loading entity pxdecoder ambaahb 1 module -- Compiling configuration pxconfig_top -- Loading entity top -- Loading architecture platformexpress of top vcom -93 pxtestbench.vhd Model Technology ModelSim SE vcom 5.5f Compiler 2002.01 Jan 7 2002 -- Loading package standard -- Loading package std_logic_1164 -- Compiling entity pxtestbench -- Compiling architecture platformexpress of pxtestbench -- Loading entity top -- Compiling configuration pxconfig_pxtestbench -- Loading entity pxtestbench -- Loading architecture platformexpress of pxtestbench -- Loading configuration pxconfig_top pli parameter value=\${CVE_HOME}/lib/arm926ejs_rev0_vsim_vlog.slib val=\${CVE_HOME}/lib/arm926ejs_rev0_vsim_vlog.slib ########### ## Px Generated File ##

Platform Express, Version 1.1d ## SoC Verification Division ## ## ## Mentor Graphics Corporation ## ## ## ## Generated on: October 3, 2002 10:28:59 AM PDT ## **##** Generated by: leritz ## ## Software compile script ## ########### if [-f pxenv] ; then . ./pxenv; fi armasm -g -I\${a926_1_1}/software/include -I\${a926_1}/common/include \${a926_1_1}/software/boot/init.s -o \${PX BUILD}/init.o armasm -g -I\${a926_1_1}/software/include -I\${a926_1}/common/include \${a926_1_1}/software/boot/reset_vectors.s -o \${PX BUILD}/reset vectors.o armcc -c -g -I\${a926_1_1}/software/include -I\${a926 1}/common/include \${a926_1_1}/software/boot/interrupt_handler.c -o \${PX_BUILD}/interrupt_handler.o "/export/home/leritz/Px1.1d_final_release/pxLibraries/PxArm9/ componentLibrary/component/a926/1.0/software/boot/interrupt_h andler.c", line 6: Warning: inventing 'extern int printToPort();' /export/home/leritz/Px1.1d final release/pxLibraries/PxArm9/c omponentLibrary/component/a926/1.0/software/boot/interrupt_ha ndler.c: 1 warning, 0 errors, 0 serious errors armcc -c -g -I\${apbmst_1_1}/software/include -I\${apbmst_1}/common/include -DFUNCNAME=apbmstCoreDiagnostics_1 \${PX_BUILD_1}/apbmst.c -o \${PX BUILD}/apbmst apbmst.o armcc -c -g -I\${a926_1_1}/software/include -I\${a926_1}/common/include -DFUNCNAME=a926Diags_1 \${PX BUILD 2}/a926Diags.c -o \${PX BUILD}/a926 a926Diags.o

armcc -c -q -I\${a926 1 1}/software/include -I\${a926_1}/common/include \${PX_BUILD_3}/printToPort.c -o \${PX BUILD}/printToPort.o "/mnt/techpub/work/leritz/Px_work/lab_files/from_jerry/test92 6/verificationEnv/Modelsim/software/a926_Memory/coreDiagnosti cs/_a926_1/printToPort.c", line 25: Warning: variable 'i' declared but not used /mnt/techpub/work/leritz/Px_work/lab_files/from_jerry/test926 /verificationEnv/Modelsim/software/a926_Memory/coreDiagnostic s/ a926 1/printToPort.c: 1 warning, 0 errors, 0 serious errors armcc -c -g -I\${a926_1_1}/software/include -I\${a926_1}/common/include \${PX_BUILD_3}/pxDiagnostics.c -o \${PX_BUILD}/pxDiagnostics.o "/mnt/techpub/work/leritz/Px_work/lab_files/from_jerry/test92 6/verificationEnv/Modelsim/software/a926_Memory/coreDiagnosti cs/_a926_1/pxDiagnostics.c", line 9: Warning: inventing 'extern int apbmstCoreDiagnostics_1();' "/mnt/techpub/work/leritz/Px_work/lab_files/from_jerry/test92 6/verificationEnv/Modelsim/software/a926_Memory/coreDiagnosti cs/_a926_1/pxDiagnostics.c", line 21: Warning: inventing 'extern int a926Diags_1();' "/mnt/techpub/work/leritz/Px_work/lab_files/from_jerry/test92 6/verificationEnv/Modelsim/software/a926_Memory/coreDiagnosti cs/_a926_1/pxDiagnostics.c", line 32: Warning: inventing 'extern int pxDiagsEnd();' /mnt/techpub/work/leritz/Px_work/lab_files/from_jerry/test926 /verificationEnv/Modelsim/software/a926_Memory/coreDiagnostic s/_a926_1/pxDiagnostics.c: 3 warnings, 0 errors, 0 serious errors armlink \${PX_BUILD}/init.o \

\${PX_BUILD}/reset_vectors.o \
\${PX_BUILD}/interrupt_handler.o \
\${PX_BUILD}/apbmst_apbmst.o \
\${PX_BUILD}/a926_a926Diags.o \
\${PX_BUILD}/printToPort.o \
\${PX_BUILD}/pxDiagnostics.o \

```
-Xref -elf -map -info totals -scatter
${PX_BUILD}/linkerCommandFile -o a926.xARM Linker: (Warning)
"/mnt/techpub/work/leritz/Px work/lab files/from jerry/test92
6/verificationEnv/Modelsim/software/a926 Memory/linkerCommand
File", line 13 (near column 33) No AREAs selected by
'a926Diags.o(...)'.
ARM Linker: (Warning)
"/mnt/techpub/work/leritz/Px_work/lab_files/from_jerry/test92
6/verificationEnv/Modelsim/software/a926_Memory/linkerCommand
File", line 23 (near column 35) No AREAs selected by
'apbmst_apbmst.o(...)'.
ARM Linker: (Warning)
"/mnt/techpub/work/leritz/Px_work/lab_files/from_jerry/test92
6/verificationEnv/Modelsim/software/a926_Memory/linkerCommand
File", line 28 (near column 36) No AREAs selected by
'a926 a926Diags.o(...)'.
ARM Linker: (Warning)
"/mnt/techpub/work/leritz/Px_work/lab_files/from_jerry/test92
6/verificationEnv/Modelsim/software/a926_Memory/linkerCommand
File", line 29 (near column 31) No AREAs selected by
'a926Diags.o(...)'.
ARM Linker: (Warning)
"/mnt/techpub/work/leritz/Px_work/lab_files/from_jerry/test92
6/verificationEnv/Modelsim/software/a926_Memory/linkerCommand
File", line 30 (near column 39) No AREAs selected by
'interrupt_handler.o(...)'.
Inter-AREA References
init.o(Init2) refers to pxDiagnostics.o(C$$code) for TestMain
init.o(Init2) refers to reset_vectors.o(reset_vectors) for
```

```
Boot
init.o(Init2) refers to init.o(Stacks)
init.o(.debug_info) refers to init.o(.debug_abbrev)
init.o(.debug_info) refers to init.o(Init2)
init.o(.debug_line) refers to init.o(.debug_line)
init.o(.debug_line) refers to init.o(Init2)
reset_vectors.o(reset_vectors) refers to init.o(Init2) for
Reset_Handler
reset_vectors.o(reset_vectors) refers to
interrupt_handler.o(C$$code) for interrupt_handler
reset_vectors.o(reset_vectors) refers to
reset_vectors.o(reset_vectors) refers to
reset_vectors.o(reset_vectors) refers to
```

reset vectors.o(.debug info) refers to init.o(.debug abbrev) reset_vectors.o(.debug_info) refers to reset_vectors.o(reset_vectors) reset_vectors.o(.debug_info) refers to reset_vectors.o(.debug_line) reset_vectors.o(.debug_line) refers to reset vectors.o(reset vectors) interrupt_handler.o(C\$\$code) refers to printToPort.o(C\$\$code) for printToPort interrupt handler.o(.debug line) refers to interrupt_handler.o(C\$\$code) interrupt_handler.o(.debug_info) refers to interrupt_handler.o(.debug_loc) interrupt_handler.o(.debug_info) refers to interrupt_handler.o(C\$\$code) interrupt_handler.o(.debug_info) refers to interrupt_handler.o(.debug_line) interrupt_handler.o(.debug_info) refers to interrupt_handler.o(.debug_macinfo) interrupt_handler.o(.debug_info) refers to interrupt_handler.o(.debug_abbrev) interrupt_handler.o(.debug_pubnames) refers to interrupt_handler.o(.debug_info) interrupt_handler.o(.debug_frame) refers to interrupt_handler.o(C\$\$code) apbmst_apbmst.o(C\$\$code) refers to printToPort.o(C\$\$code) for printToPort apbmst_apbmst.o(.debug_line) refers to apbmst_apbmst.o(C\$\$code) apbmst_apbmst.o(.debug_info) refers to apbmst_apbmst.o(.debug_loc) apbmst_apbmst.o(.debug_info) refers to apbmst_apbmst.o(C\$\$code) apbmst apbmst.o(.debug info) refers to apbmst_apbmst.o(.debug_line) apbmst_apbmst.o(.debug_info) refers to apbmst_apbmst.o(.debug_macinfo) apbmst_apbmst.o(.debug_info) refers to interrupt_handler.o(.debug_abbrev) apbmst apbmst.o(.debug pubnames) refers to apbmst_apbmst.o(.debug_info) apbmst_apbmst.o(.debug_frame) refers to apbmst apbmst.o(C\$\$code)

```
a926 a926Diags.o(.debug line) refers to
a926_a926Diags.o(C$$code)
a926_a926Diags.o(.debug_info) refers to
a926_a926Diags.o(C$$code)
a926_a926Diags.o(.debug_info) refers to
a926_a926Diags.o(.debug_line)
a926 a926Diags.o(.debug info) refers to
a926_a926Diags.o(.debug_macinfo)
a926_a926Diags.o(.debug_info) refers to
interrupt handler.o(.debug abbrev)
a926_a926Diags.o(.debug_pubnames) refers to
a926_a926Diags.o(.debug_info)
a926_a926Diags.o(.debug_frame) refers to
a926_a926Diags.o(C$$code)
printToPort.o(C$$code) refers to printToPort.o(C$$data)
printToPort.o(.debug_line) refers to printToPort.o(C$$code)
printToPort.o(.debug_info) refers to printToPort.o(C$$data)
printToPort.o(.debug_info) refers to printToPort.o(C$$code)
printToPort.o(.debug_info) refers to
printToPort.o(.debug_line)
printToPort.o(.debug_info) refers to
printToPort.o(.debug_macinfo)
printToPort.o(.debug_info) refers to
interrupt_handler.o(.debug_abbrev)
printToPort.o(.debug_pubnames) refers to
printToPort.o(.debug_info)
printToPort.o(.debug_frame) refers to printToPort.o(C$$code)
pxDiagnostics.o(C$$code) refers to pxDiagnostics.o(C$$data)
pxDiagnostics.o(C$$code) refers to printToPort.o(C$$code) for
printToPort
pxDiagnostics.o(C$$code) refers to a926_a926Diags.o(C$$code)
for a926Diags_1
pxDiagnostics.o(C$$code) refers to apbmst_apbmst.o(C$$code)
for apbmstCoreDiagnostics 1
pxDiagnostics.o(.debug_line) refers to
pxDiagnostics.o(C$$code)
pxDiagnostics.o(.debug_info) refers to
pxDiagnostics.o(C$$data)
pxDiagnostics.o(.debug_info) refers to
pxDiagnostics.o(C$$code)
pxDiagnostics.o(.debug_info) refers to
pxDiagnostics.o(.debug_loc)
```

```
pxDiagnostics.o(.debug info) refers to
pxDiagnostics.o(.debug_line)
pxDiagnostics.o(.debug_info) refers to
pxDiagnostics.o(.debug_macinfo)
pxDiagnostics.o(.debug_info) refers to
interrupt_handler.o(.debug_abbrev)
pxDiagnostics.o(.debug pubnames) refers to
pxDiagnostics.o(.debug_info)
pxDiagnostics.o(.debug_frame) refers to
pxDiagnostics.o(C$$code)
AREA map of root:
Base
         Size
                  Type RO? Name
0
         10
                  DBUG RO
                            .debug_abbrev from object file
init.o
10
         27c
                  DBUG RO
                            .debug_abbrev from object file
interrupt_handler.o
                            .debug_frame from object file
         4c
                  DBUG RO
0
interrupt_handler.o
4c
         4c
                  DBUG RO
                            .debug frame from object file
apbmst_apbmst.o
                            .debug_frame from object file
98
         3c
                  DBUG RO
a926_a926Diags.o
d4
         3c
                  DBUG RO
                            .debug_frame from object file
printToPort.o
110
                  DBUG RO
                            .debug_frame from object file
         64
pxDiagnostics.o
                           .debug_info from object file init.o
0
         c4
                  DBUG RO
c4
                            .debug_info from object file
                  DBUG RO
         CC
reset_vectors.o
190
         120
                  DBUG RO
                            .debug_info from object file
interrupt_handler.o
                            .debug info from object file
2b0
         108
                  DBUG RO
apbmst_apbmst.o
                            .debug_info from object file
3b8
         f4
                  DBUG RO
a926_a926Diags.o
                            .debug_info from object file
4ac
         144
                  DBUG RO
printToPort.o
                            .debug_info from object file
5£0
         164
                  DBUG RO
pxDiagnostics.o
                           .debug_line from object file init.o
0
         184
                  DBUG RO
```

.debug_line from object file 184 184 DBUG RO reset_vectors.o .debug line from object file 308 198 DBUG RO interrupt handler.o .debug_line from object file 4a0 184 DBUG RO apbmst_apbmst.o .debug_line from object file 624 184 DBUG RO a926_a926Diags.o DBUG RO .debug_line from object file 7a8 19c printToPort.o .debug_line from object file 944 1b8 DBUG RO pxDiagnostics.o 2c DBUG RO .debug_loc from object file 0 interrupt_handler.o 2c 38 DBUG RO .debug_loc from object file apbmst_apbmst.o 64 38 DBUG RO .debug_loc from object file pxDiagnostics.o .debug_macinfo from object file 0 1c0 DBUG RO interrupt_handler.o 1c0 210 DBUG RO .debug_macinfo from object file apbmst_apbmst.o .debug_macinfo from object file 3d0 1d4 DBUG RO a926_a926Diags.o .debug_macinfo from object file 5a4 1c0 DBUG RO printToPort.o .debug_macinfo from object file 764 DBUG RO 1c0 pxDiagnostics.o .debug_pubnames from object file 0 28 DBUG RO interrupt_handler.o .debug_pubnames from object file 28 30 DBUG RO apbmst_apbmst.o .debug_pubnames from object file 58 24 DBUG RO a926_a926Diags.o 7c 24 DBUG RO .debug_pubnames from object file printToPort.o a0 30 DBUG RO .debug_pubnames from object file pxDiagnostics.o

AREA map of Root:

Base Size Type RO? Name

68 CODE RO reset_vectors from object file 0 reset_vectors.o CODE RO C\$\$code from object file 68 58 interrupt_handler.o CODE RO C\$\$code from object file с0 118 apbmst_apbmst.o C\$\$code from object file 1d8 10 CODE RO a926_a926Diags.o 1e8 1cCODE RO C\$\$code from object file printToPort.o CODE RO C\$\$code from object file 204 100 pxDiagnostics.o 304 84 CODE RO Init2 from object file init.o

AREA map of Application0x40000000:

Base	Size	Type	RO?	Name
40000000	4	DATA	RW	C\$\$data from object file
printToP	ort.o			
4000004	4	DATA	RW	C\$\$data from object file
pxDiagnos	stics.o			
40000008	40	DATA	RW	Stacks from object file init.o
40000048	800	DATA	RW	<pre>irq_vectors2 from object file</pre>
reset_ve	ctors.o			

Image entry point : 0 Entry area : "reset_vectors" from object file reset_vectors.o code inline inline 'const' RW 0-Init debuq size data strings data data data data 44 Object totals 540 320 0 2120 8416 0

Debug Area Optimization Statistics

Input debug total(excluding low level debug areas) 10976 (10.72Kb) Output debug total 8416 (8.22Kb) % reduction

23.32%

ARM Linker: finished, 0 informational, 5 warning and 0 error messages.

Appendix D Using the Documentation Generator

Overview

This appendix contains the conceptual and procedural information on the Platform Express Documentation Generator. It contains the following sections:

- About PxDoc
- Installing PxDoc
- Using PxDoc
- Sample of Generated Documentation
- Customizing the Documentation Generator

About PxDoc

The Platform Express Documentation Generator (also called "PxDoc") is an addon component that enables you to generate design documentation in HTML. The Documentation Generator accesses design data and generates HTML pages based on the elements of your design.

The generated documentation adheres to the 3.2 HTML standard and is not browser-specific. Using a browser, you can access the generated documentation from any filesystem, or by means of a web server. Because PxDoc is not included with the basic Platform Express package, you must acquire and install the PxDoc package in order to access it from the Platform Express interface.

Installing PxDoc

The PxDoc package is delivered as an additional component library. To enhance your installation of Platform Express with the PxDoc component library, follow these steps:

- 1. Save your work and exit Platform Express.
- 2. Download the PxDoc component library from the following URL:

http://www.mentor.com/platform_ex/download/download.cfm

- 3. Copy the PxDoc directory to your \$PXPATH directory.
- 4. Edit your \$PXPATH environment variable to include PxDoc.
- 5. Invoke Platform Express.

Using PxDoc

After you have successfully installed the pxDoc component, the Tools menu is enhanced with the following menu items related to PxDoc:

• Documentation

Invokes the PxDoc dialog box.

• Mem DocGen

Automatically builds and displays the memory map documenation.

• Part DocGen

Automatically builds and displays the parts list documenation.

• Pin DocGen

Automatically builds and displays the pin list documenation.

To generate documentation with PxDoc:

PxDoc automatically overwrites any previous versions of the
generated documentatoin. You are not prompted with an
"overwrite" warning.

1. Select **Tools > Documentation**.

The Generate PxDoc dialog box appears.

Generate	Vendor	Name	Path
2	Mentor	Mem DocGen	/export/home/leritz/Px1.1e/pxLibraries/PxDoc/componentLibrary/ger
~	Mentor	Part DocGen	/export/home/leritz/Px1.1e/pxLibraries/PxDoc/componentLibrary/ger
r	Mentor	Pin DocGen	/export/home/leritz/Px1.1e/pxLibraries/PxDoc/componentLibrary/ger

Figure D-1. PxDoc Dialog Box

- 2. In the Generate column, select the desired choices from the list:
- memory map
- parts list
- pin list

By default, all three choices are selected.

- 1. Select either the **View in external browser** or **View in Java Browser** radio button.
- 2. Click OK.

The status bar reports "Generating Documents." The output pane displays the path of the generated documentation.

Accessing the Generated Documentation

Immediately after PxDoc generates the HTML files, the generated documentation displays automatically (either with the external browser as defined by the user preferences or with the internal Java browser). If you generated two or more files, the browser or viewer displays the list of the generated HTML files. If you generated only one file, that file is automatically displayed in the brower.



If the external browser fails to invoke for any reason, the Java viewer is displayed instead.

Location of Generated Files

If you close the browser or viewer, you can access the documentation from the filesystem. The HTML files are written to the following location:

<project_dir>verificationEnv/<Modelsim|Ncsim>/doc/

Table 4-1. Generated HTML Filenames

Part	Filename
Memory map	mem.html
Parts list	part.html
Pin list	pin.html

Sample of Generated Documentation

See Figure D-2 and Figure D-2 for sample generated documentation.

File Edit View 0	3o Window		letscap		ano									H
			amh blateou		Drint	C.		Chan		04	~~			
	load Hor		arch Netsca	-	Print		urity	Shop		St		1.000	*	
📲 Bookmarks 🐰	-						_		-	iles.	/10 7		Wha	t's Rela
WebMail Calendar	Radio Peopl	e Yello	w Pages D	ownlo	ad Cu	stomia	S	Sun	Se	archa	and E)irecto	ry Be	st of the
Memory M Summary	100000													
Instance Name	humber of I	eristen	*											
a926 1	0	ango an												
apbmst 1	0													
mctrl subsystem 1	4													
Number of i	instances: 3													
Instance Name : mctr Register Name		_sub: Absol	ute Size	D	ead/W		-	eset			Des	script	ion	
memoryConfigurationRegister1		0x0	32	readWrite			N/A	4	Rom and loca configuration.					
memoryConfigurationRegister2		0x0	32	32 readWrite			N/A	4	SRAM and SDRAM configuration.					
memoryConfigurationRegister3		0x0	32	read	Write		N/A	1	Reload value for SDRAM refresh counter.			M		
writeProtectionRegis	ter	0x0	32	32 readWrite			N/A	Υ.	Protects memory and I/O are from accidental overwriting.					
			Numb	erofr	egiste	rs: 4								0-
30 to Summary Tabl	e													
Register Details														
	1.00	1.1	S See a											
Register Name : me	moryConfi	guration	nRegister	3										
Bit Mop:			24	23	22	21	20	19	18	17	16	15	14	13 12
Bit Map: 31 30 29 28 27 26	25		24			·	Write	Waits	State	pror	nRea	dWai	tState	0.00
	25 promWriteI	Inable]		prom	Width	prom	wince			1.				
31 30 29 28 27 26			Reserved1	prom /Wri	te	Value	s			Des	cript			
31 30 29 28 27 26 Reserved2 Field Name	promWriteI		Reserved1 th Read	Wri	te	Value	s "000	000	, "000	Des	-		=15.	
31 30 29 28 27 26 Reserved2	promWriteF Bit Offset I	Bit Wid	Reserved1 th Read rea	/Wri	te e	Value	s "000 Res		, *00 0	Des 01"=	1 "	1111"		

Figure D-2. Sample Memory Map documentation, Netscape

		Mem D	ocGen	-							
Memory Map											
Summary Table											
Instance NameNumber of Regist	ers										
a926 1	0										
apbmst_1	0										
metri subsystem i	4										
Number of instances: 3											
Instance Name : mctrl su	hevet	1									
					_						
	solute A		readWr	Vrite Access	N/A			410.001	1/0		
memoryConfigurationRegister1	0x0		readWr					Rom and local I/O con SRAM and SDRAM of			
nemoryConfigurationRegister2 nemoryConfigurationRegister3	0x0				N/A		cload value for SDR				
miteProtectionRegister	0x0		readWr		N/A	-	rotects memory and				
which rotechola cegiste	0.40	52		Number of r			1010003	mano	y and		
Jo to Summary Table					-Grand						
Register Details											
apsia seas											
Register Name : memoryConfiguration	Register	1									
- mil C											
hit Map:											
31 30 29 28 27	26	25		24	23	22	21	20	19		
Reserved2		promWrit	eEnable	Reserved1	prom	Width	promWriteWaitS				
Reservenz	promovite	ermanie	Reserveur	prom	wium	promwritewaits					
	Width	Read/Writ	e Access	Values							
Field Name Bit OffsetBit			rite	N/A "000	0"-0 "	0001"-	1 "1	111"-1	15		
Field Name Bit OffsetBit promReadWaitState 0	4	readW	1100	1411 000	v v,				12.		
The function of the former of	4 1	readW readW	rite	N/A Reser	rved						

Figure D-3. Sample Memory Map Documentation, Java

Customizing the Documentation Generator

PxDoc can be customized in terms of style and output to deliver the desired documentation. You must be a licensed Integrator to customize the Documentation Generator. Consult the *Platform Express Integrator's Guide* for further information.

Appendix E Contacting the SupportCenter

Technical support is available to all customers who have a support contract. Before contacting technical support, gather the following information:

- License ID
- Platform and version
- Product and version
- Any test files
- Exact steps or procedures causing the problem

North America Support

In North America, refer to the online SupportCenter at:

http://www.mentor.com/supportnet/

This website provides technical support information, including a solutions database, application notes, FAQs, patches, and an online form for submitting a technical support request.

International Support

For customer support outside North America, contact your local Mentor Graphics sales organization, or refer to the following website:

http://www.mentor.com/supportnet/support_offices.html

Product Licensing Assistance

Refer to the SupportCenter to obtain new product licenses or to address questions or issues related to product licensing. Include the following information with your request:

- Your name.
- Company name, address, telephone number, and email address.
- List of products you want to license or upgrade.
- Name of server(s) that you plan to use (if different from your current server, including any new licensing server configurations).
- The host ID numbers of client and licensing server workstations for node-locked licenses.
- The host ID number of the licensing server workstation for all floating licenses.

International customers should contact their local Mentor Graphics sales office for product licensing assistance.

Glossary

Address block

A two-dimensional block placed inside an address space. It has a two dimensional offset component defining its location in relation to the base of the address space in units of address and bit offset. It also has a size component to indicate how much of the address space it occupies in dimensions of address and bit width.

Address space

A two-dimensional magnitude in units of address and bit width. May be occupied by smaller address blocks.

Bus

A path used for transmitting signals from any of several sources to any of several destinations.

Bus Bridge

A Platform Express component having a master bus interface and a slave bus interface where signals arriving on the slave interface are translated into signals on the master interface. This allows slaves connected to the master interface to respond to signals from the master of the bus to which the slave interface is connected.

Component Library

A collection of files and directories that can be used by Platform express to create and validate SoC designs. Component libraries can include IP (components), bus definitions, decoder templates, generators and generator chains.

Interrupt Controller

A hardware module responsible for collecting interrupt requests from different components in the design and selects the proper one(s) to send to the processor.

Interrupt Service Routine (ISR)

An Interrupt Service Routine (ISR) is a software function that is called and run in response to an interrupt received by the processor.

Literal Pool

Constant and string information built into compiled source code. In most cases, the constants and strings in the code are required to be relatively close to the instruction code in the Memory Map. (Literal pools are specific to ARM processors.)

Memory Map

A representation of an address space and the address blocks it contains. Memory maps are usually represented graphically.

Scatter Loader

A module whose function is to arrange the software compiled objects in different load and execution regions.

Test Bench

(Also known as a "test harness" or "test fixure"). An HDL model used to verify the correct behavior of a hardware model. A test bench generates simulation input stimuli for the model test and applies this input stimuli to the model under test. Then it applies this input stimuli and collates output responses. Finally, it compares output responses with expected values and (possibly) automatically gives a pass or fail indication.

Trademark Information

Mentor Graphics Trademarks

The following names are trademarks, registered trademarks, and service marks of Mentor Graphics Corporation:

3D DesignTM, A World of LearningSM, ABISTTM, Arithmetic BISTTM, AccuPARTnerTM, AccuPartsTM, AccuSim®, ADEPTTM, ADVanceTM MS, ADVanceTM RFIC, AMPLETM, Analog AnalystTM, Analog StationTM, AppNotesSM, ARTgridTM, ArtRouterTM, ARTshapeTM, ASICPlanTM, ASICVector InterfacesTM, AspireTM Assess2000SM, AutoActive®, AutoCellsTM, AutoDissolveTM, AutoFilterTM, AutoFlowTM, AutoLibTM, AutoLinearTM, AutoLinkTM, AutoLogicTM, AutoLogic BLOCKSTM, AutoLogic FPGA™, AutoLogic VHDL®, AutomotiveLib™, AutoPAR®, AutoTherm®, AutoTherm Duo™, AutoThermMCM™, AutoView™, Autowire Station™, AXEL™, AXEL Symbol GenieTM, BISTArchitectTM, BIST CompilerSM, BIST-In-PlaceSM, BIST-ReadySM, Board ArchitectTM, Board DesignerTM, Board LavoutTM, Board LinkTM, Board Process Library™, Board Station®, Board Station Consumer™, BOLD Administrator™, BOLD Browser™, BOLD Composer™, BSDArchitect™, BSPBuilder™, Buy on Demand™, Cable Analyzer™, Cable Station™, CAECO Designer™, CAEFORM™, Calibre®, Calibre CB™, Calibre DESIGNrev™, Calibre DRC™, Calibre DRC-H™, Calibre FRACTUREh™, Calibre FRACTUREj™, Calibre FRACTUREk™, Calibre FRACTUREm™, Calibre FRACTUREt™, Calibre Interactive™, Calibre DITHOView[™], Calibre TVS[™], Calibre MOV-I[™], Calibre MOV[™], Calibre MGC[™], Calibre OPC[™], Calibre OPC[™] Station®, CAPITALTM, CAPITAL AnalysisTM, CAPITAL BridgesTM, CAPITAL DocumentsTM, CAPITAL HTM, CAPITAL HarnessTM, CAPITAL Harness SystemsTM, CAPITAL H the complete desktop engineer®, CAPITAL Insight[™], CAPITAL Integration[™], CAPITAL Manager[™], CAPITAL Manufacturer[™], CAPITAL Support[™]. CAPITAL SystemsTM, Cell BuilderTM, Cell Station[®], CellFloorTM, CellGraphTM, CellPlaceTM, CellPowerTM, CellRouteTM, CentricityTM, CEOCTM, ChaseXTM CheckMate[™], CHEOS[™], Chip Station[®], ChipGraph[™], CommLib[™], CommLib BMC[™], Concurrent Board ProcessSM, Concurrent Design Environment[™], Connectivity Dataport[™], Continuum[™], Continuum[™], Continuum[™], CoreAlliance[™], CoreAlliance[™], CoreBIST[™], Core Builder[™], Core Factory[™], Co-Verification Environment[™], CTIntegrator[™], DataCentric Model[™], DataFusion[™], Datapath[™], Data Solvent[™], dBUG[™], Debug Detective[™], DC Analyzer[™], Design Architect[®], Design Architect[®], CoreAlliance[™], CoreAlliance[™], CoreAlliance[™], CoreAlliance[™], CoreBist[™], Core Builder[™], Core Builder[™], Core Builder[™], Core Builder[™], Core Builder[™], CoreAlliance[™], CoreAlliance[™], CoreAlliance[™], CoreAlliance[™], CoreBist[™], Core Builder[™], Core Builder[™], CoreAlliance[™], C Design Roke, Design Capture™, Design Manager™, Design Station®, Design View™, DestRoker, Design Roke, Design Capture™, DeSign Station®, Design View™, DestRoker, Design Capture™, DFTArkitect™, DFTAr ImmunitySM, EDGE (Engineering Design Guide for Excellence)SM, EDTTM, EldoTM, EldoNetTM, ePartnersTM, EParts[®], Empowering SolutionsTM, Engineer's DesktopTM, Engineer (View™, ENRead™, ENWrite™, ESim™, Exemplar™, Exemplar Logic™, Expedition™, Expert2000^{su}, Explorer CAECO Layout™, Explorer CheckMate™, Explorer Datapath™, Explorer Lsim™, Explorer Lsim FabLinkTM, Falcon[®], Falcon Framework[®], FastScanTM, FastStartTM, FastTrack ConsultingSM, First-Pass Design SuccessTM, First-Pass successSM, FlexSimTM, FlexTestTM, FDL (Flow Definition Language)™, FlowTabs™, FlowXpert™, FORMA™, FormalPro™, FPGA Advantage®, FPGAdvisor™, FPGA BoardLink™, FPGA Builder™, PPGASim™, PPGA Station®, FrameConnect™, Galie0®, Gate Station®, GateGraph™, GatePlace™, GateRoute™, GDT©, GDT Core®, GDT Designer™, GDT Developer™, GENIE™, GenWare™, Geom Genie™, HDL2Graphics™, HDL Architect™, HDL Architect Station™, HDL Author™, HDL Designer™, HDL Designer SeriesTM, HDL DetectiveTM, HDL InventorTM, HDL PilotTM, HDL ProcessorTM, HDL SimTM, HDLWriteTM, Hardware Modeling LibraryTM, HIC rulesTM, Hierarchical InjectionTM, Hierarchy InjectionTM, HotPlot[®], Hybrid DesignerTM, Hybrid Station[®], IBDTM, IC Design StationTM, IC DesignerTM, IC Layout StationTM, IC Station[®], IBDTM, IC Design StationTM, IC DesignerTM, IC Layout StationTM, IC Station[®], IBDTM, IC Design StationTM, IC DesignerTM, IC Layout StationTM, IC Station[®], IBDTM, IC Design StationTM, IC DesignerTM, IC StationTM, IC ICbasic[™], ICblocks[™], ICcheck[™], ICcompact[™], ICdevice[™], ICextract[™], ICGen[™], ICgraph[™], ICLink[™], IClister[™], ICplan[™], ICRT Controller Lcompiler[™], ICrules[™], ICtrace™, ICverify™, ICview™, ICX™, ICX Active™, ICX Custom Model™, ICX Custom Modeling™, ICX Plan™, ICX Pro™, ICX Project Modeling™, ICX SentryTM, ICX Standard LibraryTM, ICX VerifyTM, ICX VisionTM, IDEA SeriesTM, Idea Station[®], INFORM[®], IFXTM, InexiaTM, Integrated Product Development[®], Integra Station™, Integration Tool Kit™, INTELLITEST®, Interactive Layout™, Interconnect Table™, Interface-Based Design™, IntraStep™, Inventra™, InventralPX™, Inventra Soft Cores™, IP Engine ™, IP Evaluation Kit™, IP Factory™, IP -PCB™, IP QuickUse™, IPSim™, IS_Analyzer™, IS_Floorplanner™ IS_MultiBoardTM, IS_OptimizerTM, IS_SynthesizerTM, ISD CreationSM, ITKTM, It's More than Just ToolsSM, Knowledge CenterSM, Knowledge-SourcingSM, LAYOUTTM, LNLTM, LBISTTM, LBISTArchitectTM, Language Neutral LicensingTM, LcTM, LcoreTM, Leaf Cell ToolkitTM, LedTM, LED LAYOUTTM, Leonardo@, LeonardoInsightTM LeonardoSpectrum[™], LIBRARIAN[™], Library Builder[™], Logic Analyzer on a Chip[™], Logic Builder[™], Logical Cable[™], LogicLib[™], *logio*[™], Lsim[™], Lsim ZM[™], Lsim Power Analyst[™], Lsim-Review[™], Lsim-Switch[™], Lsim-XL[™], Mach PA[™], Mach TA[™], Manufacture View[™], Manufacturing AdvisorTM, Manufacturing CableTM, MaskComposeTM, MaskPE®, MBISTTM, MBISTArchitectTM, MBIST Full-SpeedTM, MBIST FlexTM, MBIST ManagerTM, MCM DesignerTM, MCM Station[®], MDVTM, MegaFunctionTM, Memory BuilderTM, Memory Builder ConductorTM, Memory Builder MozartTM, Memory DesignerTM, Memory Model Builder[™], Mentor[™], Mentor Graphics[®], Mentor Graphics Support CD[™], Mentor Graphics SupportBuiletin[™], Mentor Graphics SupportCenter[™], Mentor Graphics SupportFaxSM, Mentor Graphics SupportNet-EmailSM, Mentor Graphics SupportNet-FTPSM, Mentor Graphics SupportNet-TelnetSM, Mentor Graphics We Mean Business™, MicroPlan™, MicroPoure™, Microtec®, Mixed-Signal Pro™, ModelEditor™, ModelSim®, ModelSim LNL™, ModelSim VHDL™, ModelSim VLOGTM, ModelSim SETM, ModelStation[®], Model TechnologyTM, ModelViewerTM, ModelViewerPlusTM, MODGENTM, Monet[®], MslabTM, MsviewTM, MS AnalyzerTM, MS Architect[™], MS-Express[™], MSIMON[™], MTPIsm, Nanokernel®, NetCheck[™], NETED[™], Nucleus[™], Online Knowledge Centersm, OpenDoorsm, Opsim[™] OutNet[™], P&RIntegrator[™], PACKAGE[™], PARADE[™], ParallelRoute-Autocells[™], ParallelRoute-MicroRoute[™], PathLink[™], Parts SpeciaList[™], PCB-Generator[™], PCB IGES[™], PCB Mechanical Interface[™], PDLSim[™], Personal Learning Program[™], Physical Cable[™], Physical Test Manager: SITE[™], PLA LcompilerTM, Platform ExpressTM, PLDSynthesisTM, PLDSynthesis IITM, Power AnalystTM, Power Analyst StationTM, Power To Create[®], PrecisionTM, Precision SynthesisTM, Precision HLSTM, Precision PNRTM, Precision PTCTM, Pre-SiliconTM, ProjectXpertTM, ProtoBoardTM, ProtoViewTM, QualityIBISTM, QuickCheckTM, Synthesis¹¹⁰, Precision PLS¹¹⁰, Precision PNR¹¹⁰, PR¹¹⁰, PR¹¹⁰ View Compiler, SVCTM, SchemgenTM, SDFTM (Software Data Formatter), SDL2000 LcompilerTM, Scamless[®], Scamless C-BridgeTM, Scaml Seamless CVETM, Seamless ExpressTM, Selective PromotionTM, SignaMask OPCTM, Signal SpyTM, Signal VisionTM, Signature SynthesisTM, Simulation ManagerTM, SimExpressTM, SimUlotTM, Sim ViewTM, SiteLine2000SM, SmartMaskTM, SmartPartsTM, SmartRouterTM, SmartScriptsTM, SmartshapeTM, SNXTM, SneakPath AnalyzerTM, SOS InitiativeTM, Source ExplorerTM, SpeedGate DSVTM, SpiceNetTM, SST Velocity[®], Standard Power Model Format (SPMF)TM, Structure RecoveryTM, Super CTM, Super IC StationTM, Support Services BaseLineSM, Support Services ClassLineSM, Support Services AutitudesSM, Support Services OpenLineSM, Support Services PrivateLineSM, Support Services SiteLineSM, Support Services TechLineSM, Support Services RemoteLineSM, Symbol GenieTM, SYMEDTM SynthesisWizardTM, System ArchitectTM, System Design StationTM, System Modeling BlocksTM, Systems on Board InitiativeTM, System VisionTM, Target ManagerTM Tau®, TeraCell™, TeraPlace™, TeraPlace-GF™, TechNotes™, The Ultimate Tool for HDL Simulation™, TestKompress™, Test Station®, Test Structure Builder™, The Ultimate Site For HDL Simulation™, TimeCloser™, Timing Builder™, TNX™, ToolBuilder™, TrueTiming™, Vlog™, V-Express™, V-Net™, VHDLnet™ VHDLwrite™, Verinex™, ViewCreator™, ViewWare®, Virtual Library™, Virtual Target™, Virtual Test Manager:TOP™, VR-Process™, VRTX®, VRTXmc™, VRTXoc™, VRTXsa™, VRTX3a®, Waveform DataPort™, We Make TMN Easy™, Wiz-o-matic™, WorkXpert™, xCalibre™, xCalibrate™, Xconfig™, XlibCreator™, Xpert[™], Xpert API[™], Xpert Builder[™], Xpert Dialogs[™], Xpert Profiler[™], XRAY[®], XRAY MasterWorks[®], XSH[®], Xtrace[®], Xtrace Daemon[™], Xtrace Protocol[™], Zeelan®, Zero Tolerance Verification™, Zlibs™

Third-Party Trademarks

The following names are trademarks, registered trademarks, and service marks of other companies that appear in Mentor Graphics product publications:

Adobe, the Adobe logo, Acrobat, the Acrobat logo, Exchange, FrameMaker, FrameViewer, PostScript, and Reader are registered trademarks of Adobe Systems Incorporated in the United States and/or other countries.

Altera, ByteBlaster, Excalibur, and Quartus are trademarks or registered trademarks of Altera Corporation in the United States and other countries.

AM188, AMD, AMD-K6, and AMD Athlon Processor are trademarks of Advanced Micro Devices, Inc.

Apple and Laserwriter are registered trademarks of Apple Computer, Inc.

ARIES is a registered trademark of Aries Technology.

AMBA, ARM, ARMulator, ARM7TDMI, ARM7TDMI-S, ARM9TDMI, ARM9E-S, ARM946E-S, ARM966E-S, EmbeddedICE, StrongARM, TDMI, and Thumb are trademarks or registered trademarks of ARM Limited.

ASAP, Aspire, C-FAS, CMPI, Eldo-FAS, EldoHDL, Eldo-Opt, Eldo-UDM, EldoVHDL, Eldo-XL, Elga, Elib, Elib-Plus, ESim, Fidel, Fideldo, GENIE, GENLIB, HDL-A, MDT, MGS-MEMT, MixVHDL, Model Generator Series (MGS), Opsim, SimLink, SimPilot, SpecEditor, Success, SystemEldo, VHDeLDO and Xelga are registered trademarks of ANACAD Electrical Engineering Software, a unit of Mentor Graphics Corporation.

Avant! and Star-Hspice are trademarks of Avant! Corporation.

AVR is a registered trademark of Atmel Corporation.

Cadence, Affirma signalscan, Allegro, Analog Artist, Composer, Concept, Design Planner, Dracula, GDSII, GED, HLD Systems, Leapfrog, Logic DP, NC-Verilog, OCEAN, Physical DP, Pillar, Silicon Ensemble, Spectre, Verilog, Verilog XL, Veritime, and Virtuoso are trademarks or registered trademarks of Cadence Design Systems, Inc.

CAE+Plus and ArchGen are registered trademarks of Cynergy System Design.

CalComp is a registered trademark of CalComp, Inc.

Canon is a registered trademark of Canon, Inc. BJ-130, BJ-130e, BJ-330, and Bubble Jet are trademarks of Canon, Inc.

Centronics is a registered trademark of Centronics Data Computer Corporation.

ColdFire and M-Core are registered trademarks of Motorola, Inc.

Ethernet is a registered trademark of Xerox Corporation.

Foresight and Foresight Co-Designer are trademarks of Nu Thena Systems, Inc.

FLEXIm is a trademark of Globetrotter Software, Inc.

GenCAD is a trademark of Teradyne Inc.

Hewlett-Packard (HP), LaserJet, MDS, HP-UX, PA-RISC, APOLLO, DOMAIN and HPare registered trademarks of Hewlett-Packard Company.

HCL-eXceed and HCL-eXceed/W are registered trademark of Hummingbird Communications. Ltd.

HyperHelp is a trademark of Bristol Technology Inc.

Installshield is a registered trademark and service mark of InstallShield Corporation.

IBM, PowerPC, and RISC Systems/6000 are trademarks of International Business Machines Corporation.

I-DEAS and UG/Wiring are registered trademarks of Electronic Data Systems Corporation.

IKON is a trademark of Tahoma Technology.

IKOS and Voyager are registered trademarks of IKOS Systems, Inc.

Imagen, QMS, QMS-PS 820, Innovator, and Real Time Rasterization are registered trademarks of MINOLTA-QMS Inc. imPRESS and UltraScript are trademarks of MINOLTA-QMS Inc.

ImageGear is a registered trademark of AccuSoft Corporation.

Infineon, TriCore, and C165 are trademarks of Infineon Technologies AG.

Intel, i960, i386, and i486 are registered trademarks of Intel Corporation.

Java and all Java-based trademarks and logos are trademarks or registered trademarks of Sun Microsystems, Inc.

Linux is a registered trademark of Linus Torvalds.

MemoryModeler MemMaker are trademarks of Denali Software, Inc.

MIPS is a trademark of MIPS Technologies, Inc.

MS-DOS, Windows 95, Windows 98, Windows 2000, and Windows NT are registered trademarks of Microsoft Corporation.

MULTI is a registered trademark of Green Hills Software, Inc.

NEC and NEC EWS4800 are trademarks of NEC Corp.

Netscape is a trademark of Netscape Communications Corporation.

Novas, Debussy, and nWave are trademarks or registered trademarks of Novas Software, Inc.

OakDSPCore is a registered trademark for DSP Group, Inc.

Oracle, Oracle8i, and SQL*Plus are trademarks or registered trademarks of Oracle Corporation.

OSE is a registered trademark of OSE Systems.

PKZIP is a registered trademark of PKWARE, Inc.

Pro/CABLING and HARNESSDESIGN are trademarks or registered trademarks of Parametric Technology Corporation.

Quantic is a registered trademark of Quantic EMC Inc.

QUASAR is a trademark of ASM Lithography Holding N.V.

Red Hat is a registered trademark of Red Hat Software, Inc.

SCO and the SCO logo are trademarks or registered trademarks of Caldera International, Inc.

Sneak Circuit Analysis Tool (SCAT) is a registered trademark of SoHaR Incorporated.

SPARC is a registered trademark, and SPARCstation is a trademark, of SPARC International, Inc.

Sun Microsystems, Sun Workstation, and NeWS are registered trademarks of Sun Microsystems, Inc. Sun, Sun-2, Sun-3, Sun-4, OpenWindows, SunOS, SunView, NFS, and NSE are trademarks of Sun Microsystems, Inc.

SuperH is a trademark of Hitachi, Ltd.

Synopsys, Design Compiler, DesignWare, Library Compiler, LM-family, PrimeTime, SmartModel, Speed-Model, Speed Modeling, SimWave, and Chronologic VCS are trademarks or registered trademark of Synopsys, Inc.

TASKING is a registered trademark of Altium Limited.

Teamwork is a registered trademark of Computer Associates International, Inc.

Tensilica and Xtensa are registered trademarks of Tensilica, Inc.

Times and Helvetica are registered trademarks of Linotype AG.

TimingDesigner and QuickBench are registered trademarks of Forte Design Systems

Tri-State, Tri-State Logic, tri-state, and tri-state logic are registered trademarks of National Semiconductor Corporation.

UNIX, Motif, and OSF/1 are registered trademarks of The Open Group in the United States and other countries.

Versatec is a trademark of Xerox Engineering Systems, Inc.

ViewDraw, Powerview, Motive, and PADS-Perform are registered trademarks of Innoveda, Inc. Crosstalk Toolkit (XTK), Crosstalk Field Solver (XFX), Pre-Route Delay Quantifier (PDQ), and Mentor Graphics Board Station Translator (MBX) are trademarks of Innoveda, Inc.

Visula is a registered trademark of Zuken-Redac.

VxSim, VxWorks and Wind River Systems are trademarks or registered trademarks of Wind River Systems, Inc.

XVision is a registered trademark of Tarantella, Inc.

X Window System is a trademark of MIT (Massachusetts Institute of Technology).

Z80 is a registered trademark of Zilog, Inc.

ZSP and ZSP400 are trademarks of LSI Logic Corporation.

Other brand or product names that appear in Mentor Graphics product publications are trademarks or registered trademarks of their respective holders.

Updated 5/14/02

End-User License Agreement

IMPORTANT - USE OF THIS SOFTWARE IS SUBJECT TO LICENSE RESTRICTIONS CAREFULLY READ THIS LICENSE AGREEMENT BEFORE USING THE SOFTWARE

This license is a legal "Agreement" concerning the use of Software between you, the end-user, either individually or as an authorized representative of the company purchasing the license, and Mentor Graphics Corporation, Mentor Graphics (Ireland) Limited, Mentor Graphics (Singapore) Private Limited, and their majority-owned subsidiaries ("Mentor Graphics"). USE OF SOFTWARE INDICATES YOUR COMPLETE AND UNCONDITIONAL ACCEPTANCE OF THE TERMS AND CONDITIONS SET FORTH IN THIS AGREEMENT. If you do not agree to these terms and conditions, promptly return or, if received electronically, certify destruction of Software and all accompanying items within 10 days after receipt of Software and receive a full refund of any license fee paid

END-USER LICENSE AGREEMENT

- 1. **GRANT OF LICENSE**. The software programs you are installing, downloading, or have acquired with this Agreement, including any updates, modifications, revisions, copies, and documentation ("Software") are copyrighted, trade secret and confidential information of Mentor Graphics or its licensors who maintain exclusive title to all Software and retain all rights not expressly granted by this Agreement. Mentor Graphics or its authorized distributor grants to you, subject to payment of appropriate license fees, a nontransferable, nonexclusive license to use Software solely: (a) (in machine-readable, object-code form; (b) for your internal business purposes; and (c) on the computer hardware or at the site for which an applicable license fee is paid, or as authorized by Mentor Graphics. A site is restricted to a one-half mile (800 meter) radius. Mentor Graphics' then-current standard policies, which vary depending on Software, license fees paid or service plan purchased, apply to the following and are subject to change: (a) relocation of Software; (b) use of Software or for a restricted period of time (such limitations may be communicated and technically implemented through the use of authorization codes or similar devices); (c) eligibility to receive updates, modifications, and revisions; and (d) support services provided. Current standard policies are available upon request.
- 2. **ESD SOFTWARE**. If you purchased a license to use embedded software development (ESD) Software, Mentor Graphics or its authorized distributor grants to you a nontransferable, nonexclusive license to reproduce and distribute executable files created using ESD compilers, including the ESD run-time libraries distributed with ESD C and C++ compiler Software that are linked into a composite program as an integral part of your compiled computer program, provided that you distribute these files only in conjunction with your compiled computer program. Mentor Graphics does NOT grant you any right to duplicate or incorporate copies of Mentor Graphics' real-time operating systems or other ESD Software, except those explicitly granted in this section, into your products without first signing a separate agreement with Mentor Graphics for such purpose.

3. BETA CODE

- 3.1.Portions or all of certain Software may contain code for experimental testing and evaluation ("Beta Code"), which may not be used without Mentor Graphics' explicit authorization. Upon Mentor Graphics' authorization, Mentor Graphics grants to you a temporary, nontransferable, nonexclusive license for experimental use to test and evaluate the Beta Code without charge for a limited period of time specified by Mentor Graphics. This grant and your use of the Beta Code shall not be construed as marketing or offering to sell a license to the Beta Code, which Mentor Graphics may choose not to release commercially in any form.
- 3.2. If Mentor Graphics authorizes you to use the Beta Code, you agree to evaluate and test the Beta Code under normal conditions as directed by Mentor Graphics. You will contact Mentor Graphics

periodically during your use of the Beta Code to discuss any malfunctions or suggested improvements. Upon completion of your evaluation and testing, you will send to Mentor Graphics a written evaluation of the Beta Code, including its strengths, weaknesses and recommended improvements.

- 3.3. You agree that any written evaluations and all inventions, product improvements, modifications or developments that Mentor Graphics conceives or makes during or subsequent to this Agreement, including those based partly or wholly on your feedback, will be the exclusive property of Mentor Graphics. Mentor Graphics will have exclusive rights, title and interest in all such property. The provisions of this subsection shall survive termination or expiration of this Agreement.
- 4. RESTRICTIONS ON USE. You may copy Software only as reasonably necessary to support the authorized use. Each copy must include all notices and legends embedded in Software and affixed to its medium and container as received from Mentor Graphics. All copies shall remain the property of Mentor Graphics or its licensors. You shall maintain a record of the number and primary location of all copies of Software, including copies merged with other software, and shall make those records available to Mentor Graphics upon request. You shall not make Software available in any form to any person other than your employer's employees and contractors, excluding Mentor Graphics' competitors, whose job performance requires access. You shall take appropriate action to protect the confidentiality of Software and ensure that any person permitted access to Software does not disclose it or use it except as permitted by this Agreement. Except as otherwise permitted for purposes of interoperability as specified by the European Union Software Directive or local law, you shall not reverse-assemble, reverse-compile, reverse-engineer or in any way derive from Software any source code. You may not sublicense, assign or otherwise transfer Software, this Agreement or the rights under it without Mentor Graphics' prior written consent. The provisions of this section shall survive the termination or expiration of this Agreement.

5. LIMITED WARRANTY

- 5.1. Mentor Graphics warrants that during the warranty period Software, when properly installed, will substantially conform to the functional specifications set forth in the applicable user manual. Mentor Graphics does not warrant that Software will meet your requirements or that operation of Software will be uninterrupted or error free. The warranty period is 90 days starting on the 15th day after delivery or upon installation, whichever first occurs. You must notify Mentor Graphics in writing of any nonconformity within the warranty period. This warranty shall not be valid if Software has been subject to misuse, unauthorized modification or installation. MENTOR GRAPHICS' ENTIRE LIABILITY AND YOUR EXCLUSIVE REMEDY SHALL BE, AT MENTOR GRAPHICS' OPTION, EITHER (A) REFUND OF THE PRICE PAID UPON RETURN OF SOFTWARE TO MENTOR GRAPHICS OR (B) MODIFICATION OR REPLACEMENT OF SOFTWARE THAT DOES NOT MEET THIS LIMITED WARRANTY, PROVIDED YOU HAVE OTHERWISE COMPLIED WITH THIS AGREEMENT. MENTOR GRAPHICS MAKES NO WARRANTIES WITH RESPECT TO: (A) SERVICES; (B) SOFTWARE WHICH IS LOANED TO YOU FOR A LIMITED TERM OR AT NO COST; OR (C) EXPERIMENTAL BETA CODE; ALL OF WHICH ARE PROVIDED "AS IS."
- 5.2. THE WARRANTIES SET FORTH IN THIS SECTION 5 ARE EXCLUSIVE. NEITHER MENTOR GRAPHICS NOR ITS LICENSORS MAKE ANY OTHER WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO SOFTWARE OR OTHER MATERIAL PROVIDED UNDER THIS AGREEMENT. MENTOR GRAPHICS AND ITS LICENSORS SPECIFICALLY DISCLAIM ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.
- 6. LIMITATION OF LIABILITY. EXCEPT WHERE THIS EXCLUSION OR RESTRICTION OF LIABILITY WOULD BE VOID OR INEFFECTIVE UNDER APPLICABLE STATUTE OR REGULATION, IN NO EVENT SHALL MENTOR GRAPHICS OR ITS LICENSORS BE LIABLE FOR INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES (INCLUDING LOST PROFITS OR SAVINGS) WHETHER BASED ON CONTRACT, TORT OR ANY OTHER LEGAL

THEORY, EVEN IF MENTOR GRAPHICS OR ITS LICENSORS HAVE BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. IN NO EVENT SHALL MENTOR GRAPHICS' OR ITS LICENSORS' LIABILITY UNDER THIS AGREEMENT EXCEED THE AMOUNT PAID BY YOU FOR THE SOFTWARE OR SERVICE GIVING RISE TO THE CLAIM. IN THE CASE WHERE NO AMOUNT WAS PAID, MENTOR GRAPHICS AND ITS LICENSORS SHALL HAVE NO LIABILITY FOR ANY DAMAGES WHATSOEVER.

7. LIFE ENDANGERING ACTIVITIES. NEITHER MENTOR GRAPHICS NOR ITS LICENSORS SHALL BE LIABLE FOR ANY DAMAGES RESULTING FROM OR IN CONNECTION WITH THE USE OF SOFTWARE IN ANY APPLICATION WHERE THE FAILURE OR INACCURACY OF THE SOFTWARE MIGHT RESULT IN DEATH OR PERSONAL INJURY. YOU AGREE TO INDEMNIFY AND HOLD HARMLESS MENTOR GRAPHICS AND ITS LICENSORS FROM ANY CLAIMS, LOSS, COST, DAMAGE, EXPENSE, OR LIABILITY, INCLUDING ATTORNEYS' FEES, ARISING OUT OF OR IN CONNECTION WITH SUCH USE.

8. INFRINGEMENT

- 8.1. Mentor Graphics will defend or settle, at its option and expense, any action brought against you alleging that Software infringes a patent or copyright in the United States, Canada, Japan, Switzerland, Norway, Israel, Egypt, or the European Union. Mentor Graphics will pay any costs and damages finally awarded against you that are attributable to the claim, provided that you: (a) notify Mentor Graphics promptly in writing of the action; (b) provide Mentor Graphics all reasonable information and assistance to settle or defend the claim; and (c) grant Mentor Graphics sole authority and control of the defense or settlement of the claim.
- 8.2. If an infringement claim is made, Mentor Graphics may, at its option and expense, either (a) replace or modify Software so that it becomes noninfringing, or (b) procure for you the right to continue using Software. If Mentor Graphics determines that neither of those alternatives is financially practical or otherwise reasonably available, Mentor Graphics may require the return of Software and refund to you any license fee paid, less a reasonable allowance for use.
- 8.3. Mentor Graphics has no liability to you if the alleged infringement is based upon: (a) the combination of Software with any product not furnished by Mentor Graphics; (b) the modification of Software other than by Mentor Graphics; (c) the use of other than a current unaltered release of Software; (d) the use of Software as part of an infringing process; (e) a product that you design or market; (f) any Beta Code contained in Software; or (g) any Software provided by Mentor Graphics' licensors which do not provide such indemnification to Mentor Graphics' customers.
- 8.4. THIS SECTION 8 STATES THE ENTIRE LIABILITY OF MENTOR GRAPHICS AND ITS LICENSORS AND YOUR SOLE AND EXCLUSIVE REMEDY WITH RESPECT TO ANY ALLEGED PATENT OR COPYRIGHT INFRINGEMENT BY ANY SOFTWARE LICENSED UNDER THIS AGREEMENT.
- 9. TERM. This Agreement remains effective until expiration or termination. This Agreement will automatically terminate if you fail to comply with any term or condition of this Agreement or if you fail to pay for the license when due and such failure to pay continues for a period of 30 days after written notice from Mentor Graphics. If Software was provided for limited term use, this Agreement will automatically expire at the end of the authorized term. Upon any termination or expiration, you agree to cease all use of Software and return it to Mentor Graphics or certify deletion and destruction of Software, including all copies, to Mentor Graphics' reasonable satisfaction.
- 10. **EXPORT**. Software is subject to regulation by local laws and United States government agencies, which prohibit export or diversion of certain products, information about the products, and direct products of the products to certain countries and certain persons. You agree that you will not export in any manner any Software or direct product of Software, without first obtaining all necessary approval from appropriate local and United States government agencies.

- 11. **RESTRICTED RIGHTS NOTICE**. Software has been developed entirely at private expense and is commercial computer software provided with RESTRICTED RIGHTS. Use, duplication or disclosure by the U.S. Government or a U.S. Government subcontractor is subject to the restrictions set forth in the license agreement under which Software was obtained pursuant to DFARS 227.7202-3(a) or as set forth in subparagraphs (c)(1) and (2) of the Commercial Computer Software Restricted Rights clause at FAR 52.227-19, as applicable. Contractor/manufacturer is Mentor Graphics Corporation, 8005 Boeckman Road, Wilsonville, Oregon 97070-7777 USA.
- 12. **THIRD PARTY BENEFICIARY**. For any Software under this Agreement licensed by Mentor Graphics from Microsoft or other licensors, Microsoft or the applicable licensor is a third party beneficiary of this Agreement with the right to enforce the obligations set forth in this Agreement.
- 13. **CONTROLLING LAW**. This Agreement shall be governed by and construed under the laws of Ireland if the Software is licensed for use in Israel, Egypt, Switzerland, Norway, South Africa, or the European Union, the laws of Japan if the Software is licensed for use in Japan, the laws of Singapore if the Software is licensed for use in Singapore, People's Republic of China, Republic of China, India, or Korea, and the laws of the state of Oregon if the Software is licensed for use in the United States of America, Canada, Mexico, South America or anywhere else worldwide not provided for in this section
- 14. **SEVERABILITY**. If any provision of this Agreement is held by a court of competent jurisdiction to be void, invalid, unenforceable or illegal, such provision shall be severed from this Agreement and the remaining provisions will remain in full force and effect.
- 15. **MISCELLANEOUS**. This Agreement contains the entire understanding between the parties relating to its subject matter and supersedes all prior or contemporaneous agreements, including but not limited to any purchase order terms and conditions, except valid license agreements related to the subject matter of this Agreement which are physically signed by you and an authorized agent of Mentor Graphics. This Agreement may only be modified by a physically signed writing between you and an authorized agent of Mentor Graphics. Waiver of terms or excuse of breach must be in writing and shall not constitute subsequent consent, waiver or excuse. The prevailing party in any legal action regarding the subject matter of this Agreement shall be entitled to recover, in addition to other relief, reasonable attorneys' fees and expenses.

(10/99 rev B)

А Acrobat using xiii **ARMTOOLS** environment variable 4 B Batch mode 6 Browser defining the default browser 2 Build log 1 Building designs 1 Building your design 17 Bus bridges 18 **Bus connections** automatic 18 multiple 19 Bus views 17 **Buses** configuring 19 С Component browser 8 Components color-coding of 11 configuring 12 creating 11 deleting 13 master and slave 19 Configuring pin settings 12 Connectors creating 15 deleting 16 **Co-verification** 7 Creating the design 1 CVE HOME environment variable 4 D Decoder selection configuring 6 Design saving 15 Design and verification cycle 1

Design and verification flowchart 3 Directory structure of generated design 2 of Platform Express Installation 1 Documentation generator 1 E **Environment Variables** setting 4 Error messages 2 Example simple design 9 Execute Seamless CVE 2 **Execution** regions adding 11 G Generatorchain 6 Graphical design editor 7 Η Hardware design files 16 Hardware/Software co-verification 7 Home directory .pxrc directory 2 I Invocation switches 5 J Java SDK 4 JavaHelp using xiv JAVAHOME environment variable 4 L Library not displaying in component browser 2 Licensing 3 Load addresses defining for software modules 9 Logfiles creating 5 Logging debug 5

verbose 5 Logic simulator 7 Logmask setting 11 Μ Master and Slave components 19 Memory map pane 8 Menu bar Edit menu 10 File menu 9 Settings menu 11 Tools menu 10 Minimizing panes 13 ModelSim unable to invoke 2 MODELTECH environment variable 4 Multiple instances of Platform Express 1 0 Opening existing design file 9 Output pane clearing the 8 copying the contents of 9 Р Panes size-configurable 13 Pin configuration defining 7 example 7 Pin settings configuring 12 Platform cores open source 2 proprietary 2 **Platform Express** graphical user interface 7 invoking 5 licensing 3 running in batch mode 6

Project settings 2 **PxDoc** installing 2 location of generated HTML 5 using 2 PXPATH environment variable 4 R **Required** drivers configuring 4 S Scatter loader 9 data types 13 Seamless CVE unable to invoke 2 Setting driver signals 3 SoC 1 Software design files 17 Software memory configuring 14 Software modules 9 Status bar 12 System-on-Chip 1 Т **Technical Support** Contacting the SupportCenter 1 Tutorial 1 Typographic conventions xvi U User preferences 2 V Verifying the design 1 W Working With Buses 16 Х XRAY Debugger 2, 7 invoking 16