BSIM: Berkeley Short-Channel IGFET Model for MOS Transistors

BING J. SHEU, MEMBER, IEEE, DONALD L. SCHARFETTER, FELLOW, IEEE, PING-KEUNG KO, MEMBER, IEEE, AND MIN-CHIE JENG

Abstract **—The Berkeley Short-channel IGFET Model (BSIM), an accurate and computationally efficient MOS transistor model, and its associated characterization facility for advanced integrated-circuit design are described. Both the strong-inversion and weak-inversion components of the drain-current expression are included. In order to speed up the circuit-simulation execution time, the dependence of the drain current on the substrate bias has been modeled with a numerical approximation. This approximation also simplifies the transistor terminal charge expressions. The charge model was derived from its drain-current counterpart to preserve consistency of device physics. Charge conservation is guaranteed in this model.**

The model parameters are extracted by an automated parameter-extraction program. Use of this model to analyze device characteristics from several NMOS and CMOS processes has resulted in good agreement between measured and modeled results for transistors with effective channel lengths as small as 1 μm. Enhancements for submicrometer applications have been pointed out.

I. Introduction

COMPUTER-AIDED design tools have become indispensable in integrated-circuit design. The Simulation Program with Integrated Circuit Emphasis (SPICE) program [1] has been widely accepted for circuit analysis since its introduction a decade ago. Circuit-simulation execution time has been substantially reduced through algorithm improvement and hardware enhancements in the past few years. Novel circuit-simulation algorithms, such as the iterated-timing-analysis method [2] and the waveform-relaxation method [3], promise to offer more than an order of magnitude speed-up as compared with the conventional circuit simulator SPICE2. The dedicated-hardware approach, such as multiprocessor-based simulation schemes [4], [5], also drastically reduces the circuit-simulation time.

Device modeling plays an important role in VLSI circuit design because computer-aided circuit analysis results are only as accurate as the models used. In the past, the SPICE2 program has provided three built-in MOS transistor models [6]. The Level-1 model, which contains fairly simple expressions, is most suitable for preliminary analysis. The Level-2 model, which contains expressions from detailed device physics, does not work well for small-geometry transistors. The Level-3 model represents an attempt to pursue the semi-empirical modeling approach, which only approximates device physics and relies on the proper choice of the empirical parameters to accurately reproduce device characteristics.

Many articles on MOS transistor modeling have appeared in the literature [7]–[16] and efforts to model ever smaller and more complex MOS transistors continue at a rapid pace. MOS transistor models widely used in circuit analysis are essentially semi-empirical in nature. Terms with strong physical meaning are employed to model the fundamental physical effects while parameters are judiciously introduced to embrace subtle device characteristics. This approach serves best for circuit-analysis purposes especially as two- and three-dimensional small-geometry effects become more important.

In this paper, the development of a simple and accurate short-channel MOS transistor model, the Berkeley Short-channel IGFET Model (BSIM), and its associated characterization facility for advanced integrated-circuit design are described. The BSIM builds upon AT&T Bell Laboratories' CSIM with substantial enhancements [17]–[19]. The characterization facility includes a fully automated parameter-extraction program and implementation of the complete model, which includes expressions for dc and capacitance characteristics and extrinsic components, in SPICE2. Since a fully device-physics-oriented modeling approach usually makes parameter extraction particularly difficult, the semi-empirical approach was adopted in developing BSIM to cope with the rapid advances of technologies and to make automated parameter extraction possible. An analytical representation with 17 electrical parameters per device size was found to be adequate for modeling the dc characteristics. The parameter-extraction program generates a process file which contains a set of parameter values for circuit analysis. Circuit designers need only describe the layout geometries of transistors and parasitic elements to execute circuit simulation. Use of BSIM to analyze device characteristics from several NMOS and CMOS processes has resulted in good agreement between mea-

Manuscript received July 18, 1986; revised February 27, 1987. This work was supported by the Semiconductor Research Corporation.

B. J. Sheu was with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720. He is now with the Department of Electrical Engineering and Information Sciences Institute, University of Southern California, Los Angeles, CA 90089.

D. L. Scharfetter was with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720. He is now with Automated Characterization Systems Inc., Cupertino, CA 95014.

P.-K. Ko and M.-C. Jeng are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720.

IEEE Log Number 8714877.

0018-9200/87/0800-0558$01.00 ©1987 IEEE

sured and modeled results with effective channel lengths down to 1 μm.

II. The BSIM Formulation

The formulation of BSIM is based on the device physics of small-geometry MOS transistors. Special effects included are:

a) vertical field dependence of carrier mobility;
b) carrier velocity saturation;
c) drain-induced barrier lowering;
d) depletion charge sharing by the drain and the source;
e) nonuniform doping for ion-implanted devices;
f) channel-length modulation;
g) subthreshold conduction; and
h) geometric dependencies.

The eight drain-current parameters which directly appear in the threshold-voltage and drain-current expressions are as follows:

- V_{FB} flat-band voltage,
- ϕ_S surface-inversion potential,
- K_1 body-effect coefficient,
- K_2 source and drain depletion charge sharing coefficient,
- η drain-induced barrier lowering coefficient,
- U_0 vertical field mobility degradation coefficient,
- U_1 velocity saturation coefficient, and
- μ_0 carrier mobility.

A. Strong-Inversion Component

Five drain-current parameters, V_{FB}, ϕ_S, K_1, K_2, and η, model the threshold voltage:

$$V_{th} = V_{FB} + \phi_S + K_1\sqrt{\phi_S - V_{BS}} - K_2(\phi_S - V_{BS}) - \eta V_{DS}. \tag{1}$$

Parameter K_1 is equivalent to parameter γ in textbook models [20], [21]. The K_1 and K_2 terms together model the nonuniform doping effect. In addition, to model the drain-induced barrier lowering effect, η also partially accounts for the channel-length modulation effect.

Another three drain-current parameters, U_0, U_1 and μ_0, appear directly in the drain-current expressions. In BSIM, mobility parameter μ_0 is a function of the substrate and drain biases. A detailed description of the mobility dependence will be given later. In order to speed up circuit-simulation execution time, the 3/2 power dependence of the drain current on the substrate bias has been replaced by the numerical approximation proposed in [17]–[19]. The drain-current expressions in various operation regions are summarized below.

1. Cutoff Region [$V_{GS} \leqslant V_{th}$]:

$$I_{DS} = 0. \tag{2}$$

2. Triode Region [$V_{GS} > V_{th}$ *and* $0 < V_{DS} < V_{DSAT}$]:

$$I_{DS} = \frac{\mu_0}{[1 + U_0(V_{GS} - V_{th})]} \cdot \frac{C_{ox}\dfrac{W}{L}}{\left(1 + \dfrac{U_1}{L}V_{DS}\right)}\left((V_{GS} - V_{th})V_{DS} - \frac{a}{2}V_{DS}^2\right) \tag{3}$$

where

$$a = 1 + \frac{gK_1}{2\sqrt{\phi_S - V_{BS}}} \tag{4}$$

and

$$g = 1 - \frac{1}{1.744 + 0.8364(\phi_S - V_{BS})}. \tag{5}$$

3. Saturation Region [$V_{GS} > V_{th}$ *and* $V_{DS} \geqslant V_{D\,SAT}$]:

$$I_{DS} = \frac{\mu_0}{[1 + U_0(V_{GS} - V_{th})]} \cdot \frac{C_{ox}\dfrac{W}{L}(V_{GS} - V_{th})^2}{2aK} \tag{6}$$

where

$$K = \frac{1 + v_c + \sqrt{1 + 2v_c}}{2}$$

$$V_{D\,SAT} = \frac{V_{GS} - V_{th}}{a\sqrt{K}} \tag{7}$$

and

$$v_c = \frac{U_1}{L} \cdot \frac{(V_{GS} - V_{th})}{a}. \tag{8}$$

The body-effect coefficient "a" makes BSIM a close numerical approximation of the standard textbook model over a reasonable range of V_{BS} and V_{DS}. Detailed derivation of the BSIM expressions can be found in the appendices.

B. Including the Weak-Inversion Component

Previous SPICE2 MOS transistor models include subthreshold conduction by matching the strong-inversion component with the weak-inversion component at a transition point close to the threshold voltage. Discontinuity of drain-current derivatives exists, as has been pointed out by Antognetti *et al.* [22], which jeopardizes the convergence of the simulation. Proper matching of the strong-inversion component and the weak-inversion component is not a trivial task because it has to be done on a multidimensional basis with respect to the gate, drain, and substrate biases. In BSIM, the total drain current is modeled as the linear sum of a strong-inversion component $I_{DS,S}$ and a weak-inversion component $I_{DS,W}$, which is given by

$$I_{DS,\text{total}} = I_{DS,S} + I_{DS,W}. \tag{9}$$

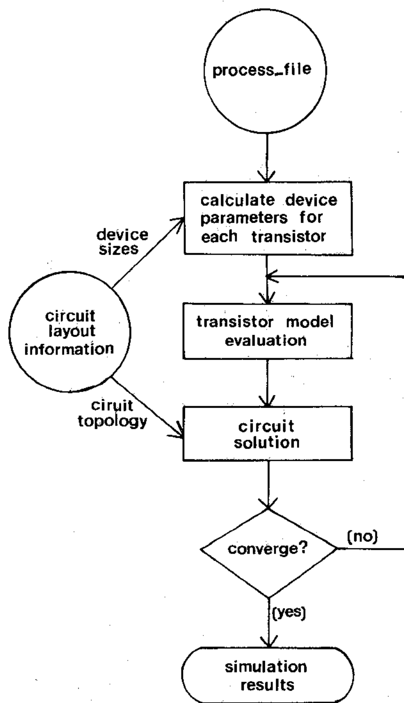


Fig. 1. Data flow in the process-oriented circuit simulation.

The weak-inversion component can be further expressed as

$$I_{DS,W} = \frac{I_{\exp} \cdot I_{\text{limit}}}{I_{\exp} + I_{\text{limit}}} \tag{10}$$

where

$$I_{\exp} = \mu_0 C_{ox} \frac{W}{L} \left(\frac{kT}{q} \right)^2 \cdot e^{1.8} e^{(q/kT)(V_{GS} - V_{th})/n} \left[1 - e^{-V_{DS}(q/kT)} \right] \tag{11}$$

and

$$I_{\text{limit}} = \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(3 \frac{kT}{q} \right)^2. \tag{12}$$

The factor $e^{1.8}$ is empirically chosen to achieve best fits in the subthreshold characteristics with minimum effect on the strong-inversion characteristics [23]. The subthreshold parameters n_0, n_B, and n_D are used to model the subthreshold-slope coefficient

$$n = n_0 + n_B V_{BS} + n_D V_{DS}. \tag{13}$$

This approach does not introduce any discontinuity in the drain-current expression and first derivatives, and thus does not hamper convergence in circuit simulation.

C. Parameter Preprocessing

1. Conversion from Size-Independent Parameters to Electrical Parameters: Fig. 1 shows the data flow in the process-oriented circuit-simulation approach. For each device type in a process file, the 51 size-independent parameters are used to find the 17 size-dependent electrical parameters. At the initial data-processing stage, the simulation program stores 17 electrical parameters for each transistor according to the formula:

$$P_i = P_{0i} + \frac{P_{Li}}{L_{DRN} - \Delta L} + \frac{P_{Wi}}{W_{DRN} - \Delta W}. \tag{14}$$

Here L_{DRN} and W_{DRN} are drawn channel length and width, while ΔL and ΔW are net size changes due to various fabrication steps. The three components P_{0i}, P_{Li}, and P_{Wi} of each electrical parameter P_i represent, respectively, its offset value, channel-length sensitivity, and channel-width sensitivity. For the subthreshold conduction, there are nine additional size-independent parameters in the process file from which three subthreshold parameters per transistor can be obtained. Subthreshold parameters are also processed using (14). In circuit simulation, this initialization step only needs to be done once for each transistor.

2. Reduction from Bias-Independent Parameters to Drain-Current Parameters: At the model-evaluation step, the 17 electrical parameters of each transistor are mapped to eight drain-current parameters. Parameters V_{FB}, ϕ_S, K_1, and K_2 are kept intact. The rules to map U_0, U_1, η, and μ_0 are listed below:

$$U_0 = U_{0Z} + U_{0B} V_{BS} \tag{15}$$

$$U_1 = U_{1Z} + U_{1B} V_{BS} + U_{1D}(V_{DS} - V_{DD}) \tag{16}$$

$$\eta = \eta_Z + \eta_B V_{BS} + \eta_D (V_{DS} - V_{DD}). \tag{17}$$

Parameter μ_0 is obtained by quadratic interpolation through three data points: μ_0 at $V_{DS} = 0$, μ_0 at $V_{DS} = V_{DD}$, and the sensitivity of μ_0 to the drain bias at $V_{DS} = V_{DD}$, with

$$\mu_0|_{(\text{at } V_{DS}=0)} = \mu_Z + \mu_{ZB} V_{BS} \tag{18}$$

and

$$\mu_0|_{(\text{at } V_{DS}=V_{DD})} = \mu_S + \mu_{SB} V_{BS}. \tag{19}$$

A second-order polynomial function is used in this interpolation.

III. Comparison of Measured and Modeled Results

An integrated system for automated extraction of BSIM parameters has been developed. The extraction software obtains parameter values and forms a process file for circuit analysis. Fig. 2 shows the role of such an integrated system in the advanced integrated-circuit design. The parameter-extraction system hardware consists of three major elements: a desktop computer, an H-P 4145B semiconductor parameter analyzer, and a probe station.

The BSIM extraction program employs a local extraction technique. In each biasing region, only parameters with related physical origins are extracted together, instead of letting all the parameter values change on the fly as is

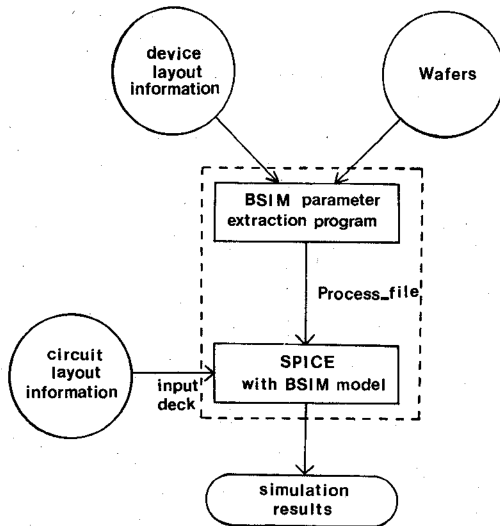


Fig. 2. A fully integrated approach for computer-aided parameter extraction and circuit design.

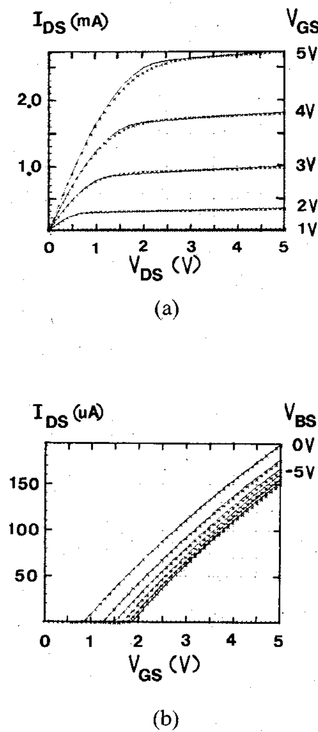


Fig. 3. Measured and modeled output characteristics of a $W_{DRN} = 20$-μm and $L_{DRN} = 3.5$-μm n-channel transistor. $T_{ox} = 30.0$ nm. (a) I_{DS} versus V_{DS} at $V_{BS} = 0$ V. (b) I_{DS} versus V_{GS} at $V_{DS} = 0.1$ V.

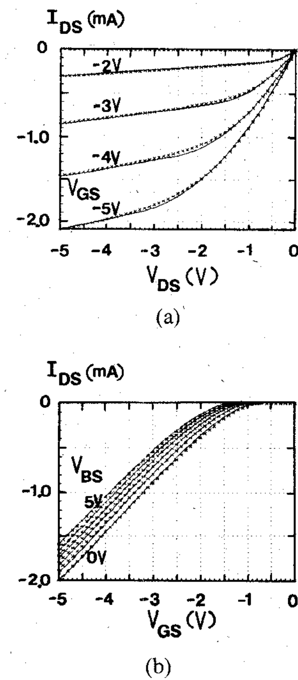


Fig. 4. Measured and modeled output characteristics of a $W_{DRN} = 20$-μm and $L_{DRN} = 2$-μm p-channel transistor. $T_{ox} = 30.0$ nm. (a) I_{DS} versus V_{DS} at $V_{BS} = 2.0$ V. (b) I_{DS} versus V_{GS} at $V_{DS} = -3.0$ V.

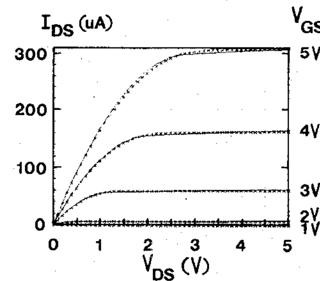


Fig. 5. Output characteristics of a $W_{DRN} = 20$-μm and $L_{DRN} = 20$-μm n-channel transistor at $V_{BS} = -2.0$ V. $T_{ox} = 30.0$ nm.

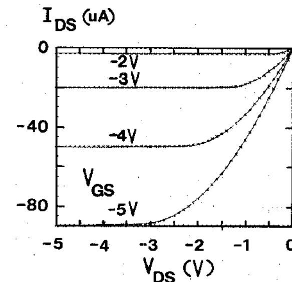


Fig. 6. Output characteristics of a $W_{DRN} = 20$-μm and $L_{DRN} = 20$-μm p-channel transistor at $V_{BS} = 2.0$ V. $T_{ox} = 30.0$ nm.

done in the global fitting approaches [24]–[27]. This makes BSIM and the associated parameter-extraction software an excellent tool for statistical studies of transistor characteristics [28]–[30]. The extraction software addresses the following issues effectively: program modularity, efficiency, accuracy, and user friendliness [31].

Experiments were carried out using devices fabricated at various industrial firms. Fig. 3 shows a comparison of measured and modeled output characteristics of a $W_{DRN} =$ 20-μm and $L_{DRN} = 3.5$-μm n-channel transistor. Modeled results are plotted with solid lines while measured data are displayed with cross marks. Fig. 4 shows a similar comparison for a $W_{DRN} = 20$-μm and $L_{DRN} = 2$-μm p-channel transistor. Comparisons of large-geometry n- and p-channel transistors are shown in Figs. 5 and 6, respectively. The gate-oxide thickness of the transistors is 30.0 nm.

Comparison of measured and modeled total drain current for a $W_{DRN} = 3$-μm and $L_{DRN} = 4$-μm n-channel

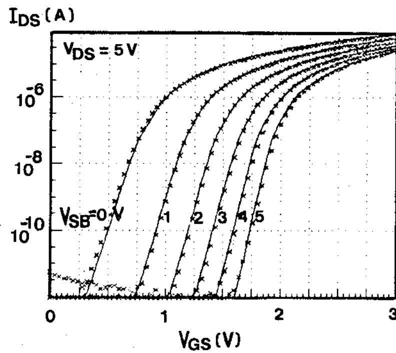


Fig. 7. Comparison of measured and modeled total drain current for a $W_{DRN} = 3$-μm and $L_{DRN} = 4$-μm n-channel transistor with $T_{ox} =$ 30.0 nm.

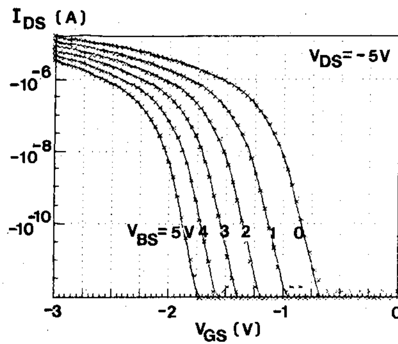


Fig. 8. Comparison of measured and modeled total drain current for a $W_{DRN} = 2$-μm and $L_{DRN} = 4$-μm p-channel transistor with $T_{ox} =$ 30.0 nm.

transistor is shown in Fig. 7. A similar comparison is shown in Fig. 8 for a $W_{DRN} = 2$-μm and $L_{DRN} = 4$-μm p-channel transistor. With threshold voltages properly determined, agreement between measured and modeled results in the subthreshold region is excellent.

IV. The Charge-Based Capacitance Model and SPICE2 Implementation

The capacitance model for BSIM conserves charge and has a nonreciprocal property. Charge conservation is guaranteed by using terminal charges as the state variables. The total stored charge in each of the gate, bulk, and channel regions is obtained by integrating the distributed charge densities over the area of the active region. Selected plots of MOS transistor capacitances normalized to the total gate-oxide capacitance WLC_{ox} are shown in Fig. 9. The capacitance values are continuous at the boundary of the triode and saturation regions.

The BSIM has been implemented in the SPICE program [32], [33]. Experimental results show that the BSIM greatly reduces program execution time as compared with the popular SPICE2 Level-2 MOSFET model. A comparison of selected SPICE2 simulation execution times is listed in Table I. A DEC VAX-11/780 computer is used in the comparison.

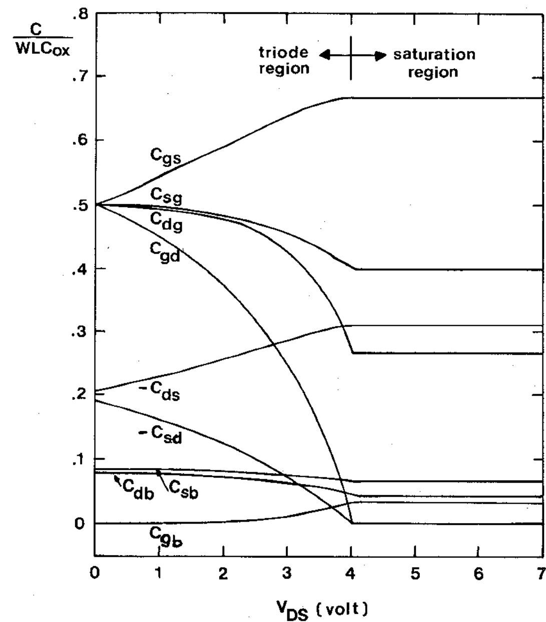


Fig. 9. Selected plots of normalized capacitances versus the drain bias. The parameter values are $V_{BS} = -3.0$ V, $V_{GS} = 6.0$ V, $a = 1.131$, $V_{th}(V_{BS} = -3.0 \text{ V}) = 1.4$ V, $K_1 = 0.63$ $V^{1/2}$, and $\phi_S = 0.62$.

TABLE I
A Comparison of Selected SPICE2 Simulation Execution Times

Circuit Description	BSIM (sec.)	MOS LEV-2 Model (sec.)
Ratioless Dynamic Logic Ckt.	24.50	29.75
Five Stage Inverter Chain	18.30	44.25
MOS Amplifier (dc & ac)	40.02	52.70
MOS Amplifier (transient)	75.08	137.50
One Stage Op-Amp	15.83	70.77
Binary-to-Octal Decorder	262.37	586.28
Telecommunication Ckt.	1784.83	2717.32

V. Discussion

Enhancements can be made to extend BSIM for submicrometer device applications. Inclusion of the source–drain series resistance and improvement of the drain-current expression to take into account the buried-channel effect are particularly important. The velocity saturation effect has drastically changed the transistor capacitance characteristics. The present capacitance model needs to be enhanced to more completely model short-channel effects.

In a VLSI chip, around 60 percent of the silicon area is consumed by interconnection lines. Accurate modeling and parameter extraction for interconnection lines are extremely important. The substrate current, which is a good monitor of hot-electron effects, is the next candidate

to be included in advanced circuit-simulation models. With a substrate current model available, circuit designers will have a very powerful tool to tackle the hot-carrier problems in the circuit environment.

VI. Conclusion

The BSIM has four important features. First, it is based on a solid understanding of device physics. Second, the model formulation is very simple, which makes it suitable for the simulation of both digital and analog circuits. Third, the model can be easily enhanced to include new effects. Fourth, the model parameters for a family of devices can be obtained automatically by a dedicated parameter-extraction program which generates a process file. Complete expressions for transistor dc characteristics, capacitance characteristics, and extrinsic-element characteristics are all included in BSIM. By using BSIM, substantial improvements in circuit-simulation accuracy and execution time can be achieved. This new model, coupled with its inherent autocharacterization characteristics and immediate applicability to new processes, forms the basis for a standard interface between IC process facilities and integrated circuit designers.

Appendix A
Model Derivation

The BSIM builds upon AT&T Bell Laboratories' CSIM [18], [19]. The channel-charge expression has the simplified form

$$Q_c = -C_{ox}(V_{GS} - V_{th} - a\phi_n). \quad \text{(A1)}$$

If we use the continuous velocity-saturation curve (see Fig. 10) [34], which can be expressed as

$$v = \frac{\mu_0 E_y}{\left(1 + \frac{E_y}{E_c}\right)}$$

with

$$v \to v_{sat} \equiv \mu_0 E_C$$

when

$$E_y \to \infty \quad \text{(A2)}$$

to best portray the device characteristics, then the drain-current expression in the triode region becomes

$$I_{DS} = \beta\left[(V_{GS} - V_{th} - I_{DS}R_{sat})V_{DS} - \frac{a}{2}V_{DS}^2\right] \quad \text{(A3)}$$

where

$$R_{sat} = \frac{1}{WC_{ox}v_{sat}}. \quad \text{(A4)}$$

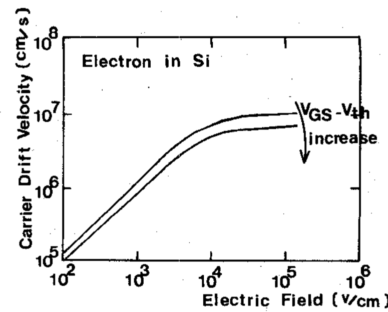


Fig. 10. Carrier velocity versus electric field [34].

Equation (A3) can be rearranged as

$$I_{DS} = \frac{\beta}{\left(1 + \frac{U_1}{L}V_{DS}\right)}\left[(V_{GS} - V_{th})V_{DS} - \frac{a}{2}V_{DS}^2\right] \quad \text{(A5)}$$

where

$$\frac{U_1}{L} = \beta R_{sat}. \quad \text{(A6)}$$

The conventional definition of saturation voltage $V_{D\,SAT}$ is obtained from (A1) with $Q_c = 0$. This condition is not realistic for modern short-channel devices. A more realistic assumption is that at the point in the channel where ϕ_n goes to $V_{D\,SAT}$ the channel current is limited by velocity saturation, i.e.,

$$Q_c = -\frac{I_{D\,SAT}}{Wv_{sat}} = -C_{ox}(V_{GS} - V_{th} - aV_{D\,SAT}). \quad \text{(A7)}$$

Substitution of the above expression into (A1) yields an upper limit for the drain-current integration formula as

$$\phi_n \to V_{DAT} = \frac{1}{a}\left[(V_{GS} - V_{th}) - I_{D\,SAT}R_{sat}\right]. \quad \text{(A8)}$$

By carrying out the drain-current integration with this upper limit, the following expression for the drain current in the saturation region can be obtained:

$$I_{D\,SAT} = \beta\left[(V_{GS} - V_{th} - I_{D\,SAT}R_{sat})V_{D\,SAT} - \frac{aV_{D\,SAT}^2}{2}\right]. \quad \text{(A9)}$$

Equation (A9) can be rearranged as

$$I_{D\,SAT} = \frac{\beta}{2a}(V_{GS} - V_{th} - I_{D\,SAT}R_{sat})^2 \quad \text{(A10)}$$

which is a quadratic equation for $I_{D\,SAT}$. To facilitate comparison with the usual expression, we define

$$I_{D\,SAT} = \frac{\beta(V_{GS} - V_{th})^2}{2aK} \quad \text{(A11)}$$

where K is obtained by equating (A10) and (A11), i.e.,

$$K^2 - K\left[1+\frac{U_1}{L}\cdot\frac{(V_{GS}-V_{th})}{a}\right] + \left(\frac{U_1}{L}\right)^2\cdot\frac{(V_{GS}-V_{th})^2}{(2a)^2} = 0 \quad \text{(A12)}$$

or

$$K = \frac{1+v_c+\sqrt{1+2v_c}}{2} \quad \text{(A13)}$$

where

$$v_c = \frac{U_1}{L}\cdot\frac{(V_{GS}-V_{th})}{a}. \quad \text{(A14)}$$

If $v_c \ll 1$, then

$$K \to 1+\frac{U_1}{L}\cdot\frac{(V_{GS}-V_{th})}{a}. \quad \text{(A15)}$$

If $v_c \gg 1$, then

$$K \to \frac{U_1}{L}\cdot\frac{(V_{GS}-V_{th})}{2a} \quad \text{(A16)}$$

and

$$I_{D\,\mathrm{SAT}} \to C_{ox}v_{\mathrm{sat}}W(V_{GS}-V_{th}). \quad \text{(A17)}$$

The above expression is well known, and states that in the limit of carrier velocity being fully saturated at v_{sat}, the saturation current is linear instead of squared with respect to $V_{GS}-V_{th}$, and its value is independent of the channel length. One can obtain the saturation drain voltage from (A8) and (A11):

$$V_{D\,\mathrm{SAT}} = \frac{(V_{GS}-V_{th})}{a\sqrt{K}}. \quad \text{(A18)}$$

In the case of $U_1/L\cdot(V_{GS}-V_{th}) \ll 1$

$$V_{D\,\mathrm{SAT}} \to \frac{V_{GS}-V_{th}}{a}. \quad \text{(A19)}$$

In the case of $U_1/L\cdot(V_{GS}-V_{th}) \gg 1$

$$V_{D\,\mathrm{SAT}} \to \sqrt{\frac{2(V_{GS}-V_{th})}{a}\cdot\frac{L}{U_1}}. \quad \text{(A20)}$$

Appendix B
Numerical Approximation of the Substrate-Bias Effect

The aim here is to find an accurate approximation of $F(V_{DS}, \phi_S - V_{BS})$ over a reasonable voltage range of V_{DS} and $(\phi_S - V_{BS})$ [17]–[19]. For convenience, let $V_A \equiv \phi_S - V_{BS}$. The function

$$F(V_{DS}, V_A) = \frac{2}{3}\left[(V_{DS}+V_A)^{3/2} - (V_A)^{3/2}\right] \quad \text{(B1)}$$

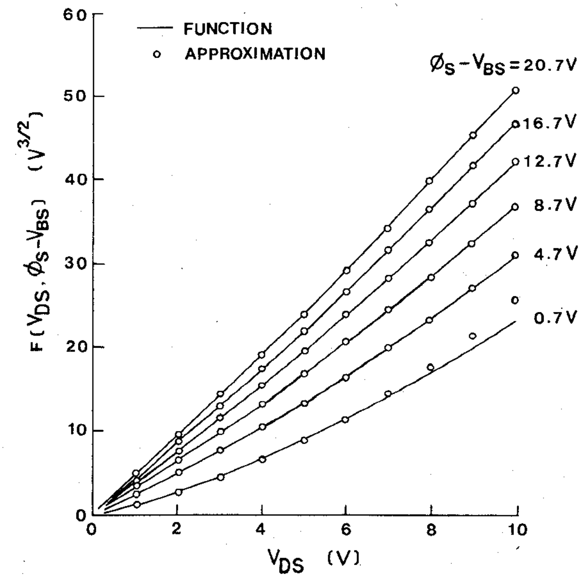


Fig. 11. Approximating the function $F(V_{DS}, \phi_S - V_{BS})$.

can be expanded as

$$F(V_{DS}, V_A) = \sqrt{V_A}\,V_{DS} + \frac{0.25V_{DS}^2}{\sqrt{V_A}} + \cdots. \quad \text{(B2)}$$

The above expansion is invalid when V_A is much greater than V_{DS}. To alleviate this problem, the expansion is changed to

$$F(V_{DS}, V_A) = \sqrt{V_A}\,V_{DS} + \frac{0.25gV_{DS}^2}{\sqrt{V_A}} \quad \text{(B3)}$$

where $g(V_A)$ is determined by requiring the expansion in (B3) to give the best fit to $F(V_{DS}, V_A)$ in the desired voltage range.

The value of V_A is considered in the range 0.7–20.7 V at 2-V increments. For each fixed V_A, a parameter g is determined such that the expansion

$$\sqrt{V_A}\,V_{DS} + \frac{0.25gV_{DS}^2}{\sqrt{V_A}}$$

will give the best fit to $F(V_{DS}, V_A)$ in a least-square sense, over a range of V_{DS} from 0 to 10 V at 0.5-V increments. It is found that g can be accurately expressed as a function of V_A in the following form:

$$\frac{1}{1-g} = P_1 + P_2\cdot V_A \quad \text{(B4)}$$

where P_1 and P_2 are determined by a least-square fitting over the range of V_A from 0.7 to 20.7 V. The results are

$$P_1 = 1.744 \quad \text{(B5)}$$

and

$$P_2 = 0.8364. \quad \text{(B6)}$$

The root-mean-square error of the approximation in (B3) using the above value of P_1 and P_2 is 2 percent and is illustrated by Fig. 11.

ACKNOWLEDGMENT

The authors wish to thank Prof. D. O. Pederson and Prof. D. A. Hodges for their continuous encouragement and Dr. H. C. Poon for his initial work on the AT&T Bell Laboratories' CSIM model. The efforts made by B. S. Messenger, R. C.-L. Liu, J. R. Pierret, A. H. Fung, and T. K. Young are appreciated.

REFERENCES

[1] L. W. Nagel, "SPICE2: A computer program to simulate semiconductor circuits," Electron. Res. Lab., Univ. of Calif., Berkeley, Memo ERL-M520, May 1975.
[2] R. A. Saleh, J. E. Kleckner, and A. R. Newton, "Iterated timing analysis and SPLICE1," presented at the IEEE Int. Conf. Computer-Aided Design, Santa Clara, CA., Sept. 1983.
[3] J. White and A. Sangiovanni-Vincentelli, "RELAX2: A new waveform relaxation approach for the analysis of LSI MOS circuits," presented at the IEEE Int. Symp. Circuits and Systems, Newport Beach, Ca, May 1983.
[4] J. T. Deutsch and A. R. Newton, "A multiprocessor implementation of relaxation-based electrical circuit simulation," presented at the ACM/IEEE 21st Design Automation Conf., Albuquerque, NM, June 1984.
[5] J. T. Deutsch, "Algorithms and architecture for multiprocessor-based circuit simulation," Electron. Res. Lab., Univ. of Calif., Berkeley, Memo ERL-M85/39, May 1985.
[6] A. Vladimirescu and S. Liu, "The simulation of MOS integrated circuits using SPICE2," Electron. Res. Lab., Univ. of Calif., Berkeley, Memo ERL-M80/7, Oct. 1980.
[7] H. K. J. Ihantola and J. L. Moll, "Design theory of a surface effect transistor," *Solid-State Electron.*, vol. 7, pp. 423–430, June 1964.
[8] H. C. Pao and C. T. Sah, "Effects of diffusion current on characteristics of metal-oxide (insulator)-semiconductor transistors (MOST)," *Solid-State Electron.*, vol. 9, pp. 927–937, 1966.
[9] Y. A. El-Mansy, "Modeling of insulated-gate field-effect transistors," Ph.D. dissertation, Carleton Univ., Ottawa, Ont., Canada, Nov. 1974.
[10] J. R. Brews, "A charge-sheet model of the MOSFET," *Solid-State Electron.*, vol. 21, pp. 345–355, 1978.
[11] R. M. Swanson and J. D. Meindl, "Ion-implanted complementary MOS transistor in low voltage circuits," *IEEE J. Solid-State Circuits*, vol. SC-7, pp. 146–153, Apr. 1972.
[12] R. R. Troutman, "Subthreshold design considerations for IGFET's," *IEEE J. Solid-State Circuits*, vol. SC-9, no. 2, pp. 55–60, Apr. 1974.
[13] G. W. Taylor, "Subthreshold conduction in MOSFET," *IEEE Trans. Electron Devices*, vol. ED-25, vol. 3, pp. 337–350, Mar. 1978.
[14] G. W. Taylor, "A unified device model for a short-channel MOSFET," presented at the IEEE 39th Annual Device Research Conf., 1981.
[15] W. Fichtner, "Three-dimensional numerical modeling of small-size MOSFET's," presented at the IEEE 39th Annual Device Research Conf., 1981.
[16] S. Liu, "A unified CAD model for MOSFETs," Electron. Res. Lab., Univ. of Calif., Berkeley, Memo ERL-M81/31, May 1981.
[17] H. C. Poon, private communication, 1979.
[18] S. Liu and L. W. Nagel, "Small-signal MOSFET models for analog circuit design," *IEEE J. Solid-State Circuits*, vol. SC-17, no. 6, pp. 983–998, Dec. 1982.
[19] B. J. Sheu, D. L. Scharfetter, and H. C. Poon, "Compact short-channel IGFET model (CSIM)," Electron. Res. Lab., Univ. of Calif., Berkeley, Memo ERL-M84/20, Mar. 1984.
[20] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 2nd ed. New York: Wiley, 1984, p. 63.
[21] D. A. Hodges and H. G. Jackson, *Analysis and Design of Digital Integrated Circuits*. New York: McGraw-Hill, 1983, p. 47.
[22] P. Antognetti, D. D. Cavigia, and E. Profumo, "CAD model for threshold and subthreshold conduction in MOSFETs," *IEEE J. Solid-State Circuits*, vol. SC-17, no. 3, pp. 454–458, June 1982.
[23] A. H.-C. Fung, "A subthreshold conduction model for BSIM," Electron. Res. Lab., Univ. of Calif., Berkeley, Memo. ERL-M85/22, Mar. 1985.
[24] K. Doganis and D. L. Scharfetter, "General optimization and extraction of IC device model parameters," *IEEE Trans. Electron Devices*, vol. ED-30, no. 9, pp. 1219–1228, Sept. 1983.
[25] D. E. Ward and K. Doganis, "Optimized extraction of MOS model parameters," *IEEE Trans. Computer-Aided Des.*, vol. CAD-1, no. 4, pp. 163–168, Oct. 1982.
[26] E. Khalily, P. H. Decher, and D. A. Teegarden, "TECAP: An interactive device characterization and model development system," in *Proc. IEEE Int. Conf. Computer-Aided Design*, Nov. 1984, pp. 149–151.
[27] P. Yang and P. K. Chatterjee, "An optimal parameter extraction program for MOSFET models," *IEEE Trans. Electron Devices*, vol. ED-30, no. 9, pp. 1214–1219, Sept. 1983.
[28] N. Herr, B. Garbs, and J. J. Barnes, "A statistical modeling approach for simulation of MOS VLSI circuit designs," in *IEDM Tech. Dig.*, 1982, pp. 290–293.
[29] P. Yang and P. Chatterjee, "Statistical modeling of small geometry MOSFETs," in *IEDM Tech. Dig.*, 1982, pp. 286–289.
[30] P. Cox, P. Yang, S. S. Mahant-Shetti, and P. K. Chatterjee, "Statistical modeling for efficient parametric yield estimation of MOS VLSI circuits," *IEEE Trans. Electron Devices*, vol. ED-32, no. 2, pp. 471–478, Feb. 1985.
[31] M.-C. Jeng, B. J. Sheu, P. K. Ko, and D. L. Scharfetter, "Parameter extraction for Berkeley short-channel IGFET model (BSIM)," in preparation.
[32] B. J. Sheu, D. L. Scharfetter, and P. K. Ko, "SPICE2 implementation of BSIM," Electron. Res. Lab., Univ. of Calif., Berkeley, Memo ERL-M85/42, May 1985.
[33] B. J. Sheu, "MOS transistor modeling and characterization for circuit simulation," Ph.D. dissertation, Electron. Res. Lab., Univ. of Calif., Berkeley, Memo ERL-M85/22, Oct. 1985.
[34] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley-Interscience, 1981, p. 46.

Bing J. Sheu (S'81–M'85) was born in Taiwan in 1955. He received the B.S.E.E. degree in 1978 from the National Taiwan University, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1983 and 1985, respectively.

In 1981 he was involved in integrated-circuit design for a speech recognition system at Threshold Technology Inc., Cupertino, CA. From 1982 to 1985 he was a Research Assistant in the Electronics Research Laboratory, the University of California, Berkeley, working on integrated-circuit design. In 1985 he joined the faculty in Electrical Engineering at the University of Southern California, Los Angeles, as an Assistant Professor. Since 1983 he has served as a consultant to the electronics industry. His research interests include computer-aided design of analog and digital integrated circuits, and transistor modeling with automated parameter extraction for circuit simulation.

Dr. Sheu is a member of Phi Tau Phi.

Donald L. Scharfetter (S'61–M'63–SM'75–F'76) obtained the B.S, M.S., and Ph.D. degrees in electrical engineering from Carnegie-Mellon University, Pittsburgh, PA, in 1960, 1961, and 1962, respectively.

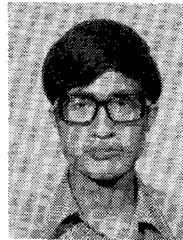
He was with Bell Telephone Laboratories, Murray Hill, NJ, from 1962 to September 1977, where he was Manager of the design group responsible for Bell Labs first microprocessor, Manager of the CMOS standard-cell based semi-custom design group, and had management responsibility for design of a family of 1-ns ECL MSI circuits. From 1972 to 1974 he managed the group responsible for Bell Lab's IC process, device, and circuit design aids. Earlier work provided fundamental understanding of Schottky barrier diodes, bipolar transistors, and microwave (avalanche) diodes. For the academic year 1977–1978 he held the position of Professor of Electrical Engineering at Carnegie-Mellon University, and was a consultant to Xerox. He was employed by the Xerox Corporation at their Palo Alto, CA, Research Center from 1978 through 1983. Initially as Manager of Integrated Circuit Planning, he also had responsibility for process, device, and circuit-simulation design aids as well as testing and process characterization. Beginning in March of 1983, he spent a year as Mackay Professor of Electrical Engineering and Computer Sciences at the University of California, Berkeley, where he directed the BSIM project. In March of 1984 he formed Automated Characterization Systems, Cupertino, CA, to develop and market software for the characterization of MOS devices. He has published over 40 highly regarded technical

publications and has five issued patents. His current interests are in productivity improvement in the development of advanced CMOS integrated circuits.

Dr. Scharfetter is active in IEEE professional activities. He was Chairman of the 1981 International Devices Meeting, organized the first West Coast Test Workshop, and has served on the program committee of the International Solid-State Circuits Conference, the Device Research Conference, and the joint U.S. and Japanese Symposium on VLSI. His work on microwave (avalanche) diodes earned him the IEEE grade of Fellow.

Ping-Keung Ko (S'78–M'82) was born in Hong Kong in 1951. He received the B.Sc. (special honors) degree in physics in 1974 from the University of Hong Kong, and the Ph.D. degree in electrical engineering in 1982 from the University of California at Berkeley.

From 1982 to 1983 he was with the silicon-research group at Bell Laboratories, Holmdel, NJ, where he developed a submicrometer high-speed NMOS technology. In January 1984 he joined the Department of Electrical Engineering and Computer Sciences at the University of California at Berkeley where he is at presently an Associate Professor. His research interest is in high-speed integrated-circuit technologies and device modeling for circuit simulation.



Min-Chie Jeng was born in Taiwan in 1959. He received the B.S. degree from the Department of Electrical Engineering, National Taiwan University in 1980, and the M.S. degree from the University of Maryland in 1983. He is currently working toward the Ph.D. degree at the University of California, Berkeley.

From 1980 to 1982 he served in the Chinese Army as a Radar Maintenance Officer. In 1983 he was a Research Assistant in the Department of Electrical Engineering, University of Maryland, and a Guest Worker in the National Bureau of Standards, Gaithersburg, MD, working on ultrafast optoelectronic switchings. Since 1984 he has been a Research Assistant in the Electronics Research Laboratory, University of California, Berkeley. His main interests are MOS device physics, modeling, and parameter extraction.