Class E–A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers

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Abstract—The previous literature on tuned power amplifiers has not made clear the fundamental differences between amplifiers in which the output device acts 1) as a current source, or 2) as a switch. Previous circuits have often operated in contradiction to their design assumptions, resulting in the need for "cut-and-try" design. The new class of amplifiers described here is based on a load network synthesized to have a transient response which maximizes power efficiency even if the active device switching times are substantial fractions of the ac cycle. The new class of amplifiers, named "Class E,"[1] is defined and is illustrated by a detailed description and a set of design equations for one simple member of the class. For that circuit the authors measured 96 percent transistor efficiency at 3.9 MHz at 26-W output from a pair of Motorola 2N3735 TO-5 transistors. Advantages of Class E are unusually high efficiency, *a priori* designability, large reduction in second-breakdown stress, low sensitivity to active-device characteristics, and potential for high-efficiency operation at higher frequencies than previously published Class-D circuits. Harmonic output and power gain are comparable to those of conventional amplifiers.

I. INTRODUCTION

IN a high-efficiency power amplifier, increases of efficiency which at first might appear to be minor can be very important, e.g., increasing collector efficiency from 80 to 90 percent halves the collector power dissipation (reduction from 20 percent of the input power to 10 percent). That allows doubling the power output, or halving the number of output transistors and reducing the heat sink volume and weight by a factor of about 2.8, or halving the junction temperature rise and thereby decreasing the transistor failure rate.[2] The recent large increases of energy cost provide further incentive for reducing power losses in high-power fixed installations, and conservation of battery or generator power can be important for portable or remote equipment.

The major power loss is usually power dissipated in the output active device(s), e.g., transistors or vacuum tubes. To minimize that dissipation, one attempts to minimize: 1) the voltage across the device when current flows through it; 2) the current through the device when voltage exists across it; and 3) the duration of any unavoidable condition in which appreciable current and voltage exist simultaneously. Class-C amplifiers [1]–[8] apply 1) and 2). Class-D amplifiers [2], [15]–[21] apply 1), 2), and 3). Previous approaches to 3) have been only to reduce the device switching times. Our new class of high-efficiency amplifiers[3] is based on a load network which is synthesized to give a transient response which achieves 3) even if the device switching times are appreciable fractions of the ac cycle. For lack of space, we discuss here only briefly: 1) the largely-ignored *fundamental differences* between amplifiers using active devices a) as switches and b) as current sources, and the greatly different requirements placed on load network design by those two different cases; 2) the consequent invalidity of the assumptions upon which many designs are based; 3) evaluation of previous published work in tuned power amplifiers; and 4) design of the optimum transistor for use in this circuit. More details are available on request from the authors.

II. PREVIOUS WORK

A. Amplifiers Using Current-Source Active Devices

In designing a tuned Class-C power amplifier [1]–[8], the output active device is assumed to be a high-impedance current source, i.e., its output current is 1) determined primarily by the input drive and 2) substantially independent of the output voltage which results from the flow of that current in the load network. That network is designed so that its voltage response to the periodic current pulses is a sinusoid at the output frequency, with these properties: 1) the minimum of the voltage across the current source occurs at the time of the current pulse; and 2) at this minimum, the voltage is not less than a certain minimum permissible voltage, determined by the characteristics of the active device and required for the device to function as a current source as assumed. This voltage prevents "saturation" of a transistor or "bottoming" of a pentode or triode[4] vacuum tube, for example. If the active device

[1] The new name "Class E" is proposed because 1) the unique principles of load network operation for achieving high efficiency, which are the basis of our circuit operation, are not embodied in any of the previously defined Classes A through D and 2) although our amplifier uses switching active devices, in common with Class D, the definition of Class D by its inventor [15] does not involve our type of load network, and specifies operation of the switches at 50 percent duty ratio, which is not required in our circuit.

[2] For example, by a factor of ≈14 if the temperature rise is halved from 130°C to 65°C above a 50°C ambient (i.e., T_J is reduced from 180°C to 115°C). This factor is an average of values read from graphs for numerous VHF, UHF, and microwave RF power transistors in "RF and microwave power transistors—MTF projections," Communications Transistor Corp., San Carlos, Calif., Bull. 2.0.8.1B, Nov. 1972.

[3] The work reported here is the subject of patent applications by the authors. Licenses and further technical information are available to interested parties.

[4] Despite the fact that the triode plate resistance (r_p) may be comparable with the tank parallel load resistance (R_L), in most cases the triode acts essentially as a current source unless the tube is "bottomed" during the current pulse by incorrect circuit operation. Specifically, if the tank loaded Q is greater than $2\pi D R_L/r_p$, where D is the fraction of a cycle during which the current pulse flows, the current pulse magnitude will be 80 percent or more of the value it would have if the triode were a pure current source with infinite r_p. For example, for the typical case of $D = 0.1$ and $R_L/r_p = 4$, the triode can be considered to be a current source if the tank loaded Q is 2.5 or more, which is almost always the case.

TABLE I
USE OF CURRENT SOURCE VERSUS TWO-STATE SWITCH

Characteristic	Amplifier Using Current Source	Amplifier Using Two-State Switch
Active-device output-port ac impedance ($\partial V/\partial I$).	Always high.	"on": low "off": high.
Is the active device allowed to saturate?	No.	Often intentionally, when "on."
Desired voltage across the active device while conducting current.	Greater than a specified minimum value.	As low as can be obtained.
What determines the voltage across the active device while it is conducting current?	The voltage response of the load network input-port impedance to the current pulses delivered by the current source.	The voltage approaches zero because of the low-impedance property of the "on" switch, independent of the properties of the load network.
Does the voltage across the active device output port during current conduction depend on the load network input-port impedance?	Yes.	No.
What determines the current which flows through the active device when it is conducting current?	Only its input signal.	The load network to which its output port is connected.
To what criteria should the load network be designed?	The input-port voltage waveform produced in response to a specified repetitive current-pulse train injected into its input port.	The input-port voltage waveform produced by repetitive alternatively connected short-circuits and open-circuits at its input port. (The full use of this criterion is novel; details are in Section III of this paper.)

saturates, the basic design assumptions become invalid. This is the reason why so much "cut and try" is needed in contemporary RF power amplifier design.

Harmonic resonators can be added to the load network to improve the tradeoff between efficiency and conduction angle [9]-[14]; this provides approximately a flat-bottomed voltage waveform when the network is driven by the pulsed current source, extending the duration of the low-voltage condition and permitting a wider current pulse without severe loss of efficiency. This circuit, also, requires the minimum voltage across the current-source device.

All current-source amplifiers dissipate substantial power in the active device because the voltage across that device during the current pulse must be larger than the minimum permissible value, typically of the order of 10 percent of the dc supply voltage. Obtaining high efficiency requires that the current pulse amplitude and the load network be adjusted carefully to obtain an ac output voltage amplitude which is: 1) large enough to bring the active-device voltage as close to zero as allowable during the current pulse, but 2) not so large as to cause the device voltage to become less than the minimum permissible voltage, thereby causing the device to be no longer a high-impedance current source and thus to invalidate the design assumptions.

B. Amplifiers Using Active-Device Switches

Higher efficiency can be achieved by using the active device as an on/off switch instead of a high-impedance current source; the increased efficiency results from reducing the voltage which exists across the device while current is flowing through it. While a practical active-device current source requires at least a certain minimum permissible voltage across itself, an active-device switch may be operated at a much smaller "on"

voltage. Table I shows the *fundamental differences* between the use of a current source to drive a load network and the use of a switch to drive a *differently designed* load network. These important distinctions have been missed by many previous workers in this field; one exception is Rose [28]. Switching-mode and current-source active devices are sharply distinguished from each other by their output-port ac impedances: in a switching-mode device, the "on" state ac impedance (i.e., $\partial V/\partial I$) is low compared to the ac impedances in the surrounding circuit; in a current-source device, the ac impedance (exclusive of incidental reactances which are absorbed into the tuned circuit) is high compared to the surrounding circuit ac impedances, throughout the ac cycle.

Push-pull Class-D current-switching and voltage-switching circuits [2], [15]-[17] use parallel-tuned or series-tuned resonant circuits, respectively, driven by two on-off switches (e.g., transistors). The inputs are so driven that one switch is "on" while the other is "off," each switch being "on" for half of the ac cycle. These amplifiers are efficient, but suffer from the possibility of both transistors conducting simultaneously or being off simultaneously during the switching transient, leading to loss of efficiency at high frequencies and to the possibility of transistor destruction by second breakdown [16]. A further limitation on efficiency at high frequency and a potential cause of second breakdown for the voltage-switching amplifier is not mentioned by previous authors: the power dissipated and the simultaneous high voltage and high current imposed on the transistors in charging the output-to-ground capacitance plus the C_{ob} of both of the two switching transistors to almost the full supply voltage (V_{CC}), twice each ac cycle, at the operating frequency (f), in a charging time of a/f. The power dissipation is $(2f)(\frac{1}{2})(2C_{ob} + C_{output})(V_{CC} - 2V_{CE(sat)})^2$; the second-breakdown stress is a current typically

rising linearly from zero to $2(2C_{ob} + C_{output})(V_{CC} - 2V_{CE(sat)})$ f/a while the voltage falls parabolically from $(V_{CC} - V_{CE(sat)})$ to $V_{CE(sat)}$.

Timing problems of a pair of switches are avoided by using a single switch in a "single-ended" amplifier. References [18]–[21] describe single-ended circuits operated at up to 80 MHz, using load networks similar to those of current-source tuned power amplifiers. They do not consider the possibility of increasing the collector efficiency through unconventional design of the load network.

Single-ended amplifiers (e.g., [22]–[27]) typically are designed as current-source amplifiers, but many allow the active device to saturate during part of the time that it is conducting current, invalidating the design assumptions. If this happens (e.g., because excessive input drive is applied), the device may then accidentally act as an "on" switch during the time that it is saturated, but there are the undesirable possibilities of: 1) potentially destructive inverted-mode operation, 2) a mode of oscillation which has not heretofore been described in detail, or 3) a substantial increase in broad-band noise output.[5] Such an amplifier comprises: 1) an active device which is an "on" switch for part of the "on" time and a current source for the remainder of the ac cycle, together with 2) a load network designed on the assumption of a current-source active device. A load network designed to provide a specific response to a train of current pulses from a high-impedance current source cannot be expected, *a priori*, to yield optimum performance when driven by a cyclically-operated switch which provides an excitation completely different from that for which the network was designed. The widely acknowledged need for "cut-and-try" in tuned power amplifier design, and the observed sensitivity of circuit performance to individual variations in transistor characteristics, give experimental confirmation of this hypothesis that designing according to invalid assumptions may not yield optimum performance. The circuit described below operates as designed; it is not sensitive to variations in transistor characteristics.

III. DESCRIPTION OF THE NEW CIRCUIT OPERATION

A. General Principles

Fig. 1 is a block diagram of a single-ended switching-mode amplifier. The active device acts substantially as a switch when appropriately driven by the driver.[6] The active device output is represented as a nonideal single-pole single-throw switch: the "on" resistance (dc and/or ac) may be nonzero, the "off" resistance (dc and/or ac) may be noninfinite, and the turn-on and turn-off switching times may be nonzero. As
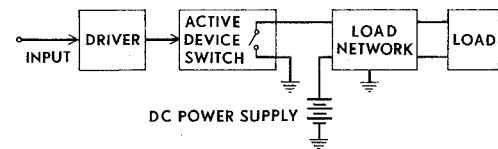

Fig. 1. Block diagram of single-ended switching-mode amplifier.

the switch is cyclically operated at the desired ac output frequency, dc energy from the power supply is converted to ac energy at the switching frequency (and harmonics thereof). To obtain maximum fundamental-frequency output, the switch duty ratio is made approximately 50 percent, i.e., the switch is "on" for approximately half of the ac period and "off" for the remainder of the period. The load network may include a low-pass or bandpass filter to suppress harmonics of the switching frequency at the load, and may transform the load impedance and/or accommodate load reactance.

A power amplifier which uses the active device as a switch is potentially highly efficient because the "on" and "off" states of the switch fulfill Conditions 1) and 2) of Section I. But in practical high-efficiency switching-mode amplifiers, even with proper driver design and choice of switching active device, the switching time of the device may be a considerable fraction of the ac cycle, and considerable power may be dissipated in the active device during switching, in violation of Condition 3). The novel principle of the tuned power amplifier described here is to avoid by design the simultaneous imposition of substantial voltage and substantial current on the switch, *even during switching intervals of substantial duration*, through the use of a load network synthesized to yield an optimal transient response to the cyclic operation of the switch.

Fig. 2(a) and (b) shows the desired waveforms of voltage across the switch and current through the switch, in a circuit of the Fig. 1 class arranged for maximum power efficiency. The following conditions are met by those waveforms.

1), 2) Conditions 1) and 2) of Section I: Those conditions are well known, and require only that the active device be chosen and the driver be designed so as to minimize the switch "on" voltage and "off" leakage current, respectively. Those conditions are substantially independent of the design of the load network.

3) The switching time of the switch is minimized: This condition is also well known, and may also be fulfilled by proper choice of the active device and proper design of the driver. This condition is somewhat dependent on the design of the load network, although previous work has not taken cognizance of this dependence. To the extent that the load network design does affect the switching time, it will be seen below that our load network causes the switching time to be decreased compared with that attained with prior-art load networks.

The load network is arranged to have the input-port transient response described in 4) through 8) below.

4) Voltage delay at switch turnoff: In the time interval during which the switch makes its transition from the "on" state to the "off" state, the voltage across the switch remains low for a time long enough that the current through the

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[5]The potentially destructive operating conditions and the oscillation are subjects of planned future papers by the authors. The noise effect has been observed in unpublished work on oscillators by M. Crandall of Microwave Associates, Inc., and others. The reasons for it, and experimental data, are subjects of a planned future paper by the authors. The mechanism believed to be responsible for this noise increase exists also in voltage-switching Class-D amplifiers, but does not exist in the authors' switching-mode amplifier.

[6]The drive waveform can be optimized on the criteria of efficiency, power gain, and freedom from transistor second breakdown. The optimum drive and resulting power gain for transistor switches and for vacuum-tube switches are subjects of planned future papers.
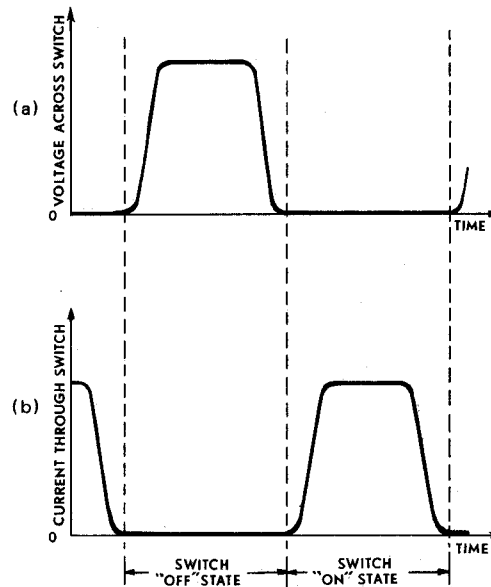
Fig. 2. Optimum waveforms in circuit of Fig. 1 arranged for maximum power efficiency. (a) Voltage across switch. (b) Current through switch.

switch has by then been reduced substantially to zero. Then the voltage increases. This assures that high voltage does not exist across the switch while the current through it is nonzero, thereby avoiding the energy loss which would have existed if the voltage had been allowed to start to increase before the current decrease to zero had been substantially completed.

5) Voltage return to zero at switch turnon: During the switch "off" state, the load network input-port transient response carries the voltage across the switch first upwards, and then downwards toward zero; this voltage reaches zero just prior to the start of the switch "on" state, i.e., just before current begins to flow in the switch. This avoids the energy dissipation which would have occurred if the switch current had begun flowing while the voltage across the switch was still high, and had thereafter discharged to ground, through the switch, the capacitance at the load network input port.[7]

6) Zero voltage slope at switch turnon: When the "off" state transient response reaches zero voltage across the switch, i.e., just before the beginning of the "on" state, it does so with approximately zero slope (i.e., $dv/dt \approx 0$). This permits accidental slight mistuning of the amplifier without severe loss of efficiency, i.e., there is a time interval during which the switch turnon can occur while still substantially meeting the condition of $v = 0$. Moreover, moderately slow turnon of the switch does not cause the switch to experience high power dissipation during turnon, because the voltage across the switch is not increasing rapidly during the time that the switch is turning on. Furthermore, the conditions $v = 0$ and $dv/dt = 0$ at the end of the "off" state together imply that the switch

current at the start of the "on" state will be zero, and that during the "on" state the switch current need increase from zero only gradually. In view of the limited di/dt capabilities of actual active-device switches, this zero starting current is desirable because it helps to minimize the active device switch turnon time, and hence further minimize dissipation during the turnon transient. Avoiding a substantial negative value of dv/dt at turnon time avoids imposing on the switch a requirement to conduct substantial current then in the reverse of the usual direction.

7), 8) The voltage and current transient response waveforms each have a flat top: It can be shown (available from the authors) that the optimum voltage and current waveforms are flat topped with short rise and fall times, the peak values being equal to or less than the maxima which the switch is able to withstand reliably, for the usual case in which the switch peak voltage and current capabilities define the allowable limits of operation.

The waveforms of Fig. 2, while superficially resembling the approximately square waves of a switching amplifier driving a resistive load, differ from the latter in one absolutely crucial respect: the delay of each waveform of Fig. 2 in increasing from zero until the other waveform has completed decreasing to zero. This is accomplished *only* by appropriate design of a nonresistive load network, and results in a considerable increase in efficiency if the transition time of the switch is an appreciable fraction of a half-cycle of the ac waveform. Note that Conditions 4) through 8) above are entirely independent, except that Condition 6) presupposes Condition 5), and any or all of them may be included in an amplifier incorporating these general principles. The ideal network can be approximated to any desired degree, using lumped and/or distributed elements. For example, the simple circuit described below used lumped elements and does not have flat-topped voltage and current waveforms [Conditions 7) and 8)]; the effect of

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[7]This capacitance includes intrinsic switch capacitance and circuit stray capacitance, as well as any capacitor purposely designed to be part of the tuned circuit. Note that each time a capacitance C, initially charged to a voltage V, is discharged by a switch, an energy $CV^2/2$ will be dissipated, *independent of the switch series resistance.* This causes a power loss of $CV^2f/2$, reducing efficiency.
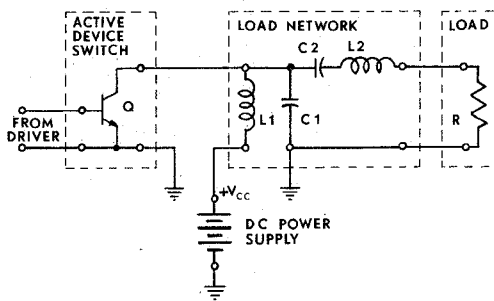
Fig. 3. Circuit diagram of simple member of the new class of high-efficiency amplifiers.

the flat-topped waveforms on efficiency is often smaller than that of the delays.

B. Description of a Simple Member of the New Class of Amplifiers

The above principles will now be illustrated by a simple member of this new class of amplifiers, shown in Fig. 3, and the modifications of it shown in Figs. 5, 6, and 7. $L1$ is a high-reactance V_{CC} shunt-feed choke. The sum of its shunt capacitance, the transistor output capacitance, and wiring capacitance is absorbed into $C1$ and is hereafter called C_{out}. At high enough frequencies, all of $C1$ may be supplied by C_{out}.[8] R may be the actual load, or may be the input-port resistance of a low-pass or bandpass filter inserted between the $C2$-$L2$ branch and the load to suppress harmonics of the switching frequency. Reactance of the load or of the input port of such a filter is absorbed into $L2$ and/or $C2$, as described in Section III-C below.

In the circuit of Fig. 3, the collector voltage is at $V_{CE(sat)}$ while the transistor is on, meeting Condition 1) of Section III-A above. When the transistor is switched off, the load network transient response is the response of a damped second-order system, the series connection of $L2$, R, and $C1 \cdot C2/(C1 + C2)$, starting with a set of given initial energies stored in $C1$, $C2$, and $L2$. ($L1$ is sufficiently large to act as a source of substantially constant current.) Some of the energy stored in $C1$, $C2$, and $L2$ is delivered to R (the network damping, but also the useful load) during the ringing transient.

$C1$ insures that in the time interval during which the transistor is being turned off, V_{CE} remains relatively low until after the collector current has reduced to zero, approximating (with a parabolic section) the delay of voltage rise shown in Fig. 2 and discussed above as Condition 4). High V_{CE} does not occur until after I_C has been cut off at low voltage and the base has become reverse-biased. Thus the BV_{CEV} rating applies to the "off" condition, rather than the lower BV_{CEO}

or BV_{CER} ratings as in some conventional amplifiers. This allows using a higher value of V_{CC}, thereby obtaining higher power output and higher efficiency.

Three possible kinds of transient response voltages are shown in Fig. 4, for three different values of damping corresponding to three different values of network loaded $Q(Q_L)$. With too much damping (Q_L too low) shown in Fig. 4(a)-(c), the voltage across $C1$ never returns to zero. Therefore the transistor must discharge $C1$ from some positive voltage V to a near-zero voltage when it is next turned on, requiring the power dissipation described in footnote 7. In addition, the transistor is subjected to simultaneous substantial collector-emitter voltage and substantial collector current (the "on" collector current which flows at that V_{CE} according to the input drive provided by the driver). This transient condition can cause second breakdown, potentially destructive to the transistor. Previous published circuits subjected the transistor to this power-dissipating and potentially-destructive condition (e.g., [29]; see V_{CE} waveform of Fig. 2 there). The circuit described here is specifically designed to avoid this undesirable condition, helping to assure reliability.

With too little damping (Q_L too high), shown in Fig. 4(d), V_{CE} swings below zero, placing the transistor in the inverted mode. If this voltage is below the base "off" voltage provided by the driver, the transistor is placed in the active inverted mode with the base–collector junction forward-biased and the base–emitter junction reverse-biased. The load will pull the base further negative by an amount which depends on the base signal source impedance and voltage, the load network transient response, and the transistor inverted-mode gain and cutoff frequency. Several outcomes are possible: 1) the BV_{EBX} rating may be exceeded and the transistor may be damaged; 2) BV_{ECX} (never specified) may be exceeded and the transistor may be damaged; 3) appreciable inverted collector current may flow [observable in Fig. 4(d)], dissipating power (hence reducing efficiency) and possibly damaging the transistor; or 4) no damage will result. This underswing can also occur in conventional Class-B and Class-C amplifiers. Both in conventional amplifiers and in amplifiers of the new class described here, damage can be prevented by adding a commutating diode between the collector and emitter as shown in Fig. 5(a), or between the base and emitter as shown in Fig. 5(b), or by designing the base drive circuit properly.[9]

With correct damping (Q_L correct), shown in Fig. 4(e), the peak negative-going V_{CE} just reaches $V_{CE(sat)}(\approx 0)$, avoiding the two above undesirable conditions. The correct damping also gives zero slope to the V_{CE} waveform as it reaches the

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[8]To the extent that the susceptance of $L1$ is not negligibly small in the frequency range of interest, $C1$ may be increased to provide the operating characteristics which are described here for the case of the $L1$ susceptance being negligibly small. In some cases it may be desirable to choose a value for $L1$ which yields appreciable susceptance, thereby increasing the required capacitance of $C1$, as, for example, if more than the value required for $C1$ with negligibly small $L1$ susceptance is already supplied by C_{out}.

[9]A useful result of adding the diode at the base rather than at the collector is that the resulting base current injects charge into the base region, preparing the transistor to conduct collector current in the normal direction when the subsequent "on" state begins. Depending on the design requirements and constraints of a particular application (including the turn-on drive available from the driver), it may be advantageous to choose Q_L slightly higher than optimum, to allow the load current to aid in turning on the transistor. However, use of this possibility to an excessive extent can lead to a mode of oscillation which can occur in conventional amplifiers with or without the base diode, and which appears not to have been reported previously; that is the subject of a planned future paper.
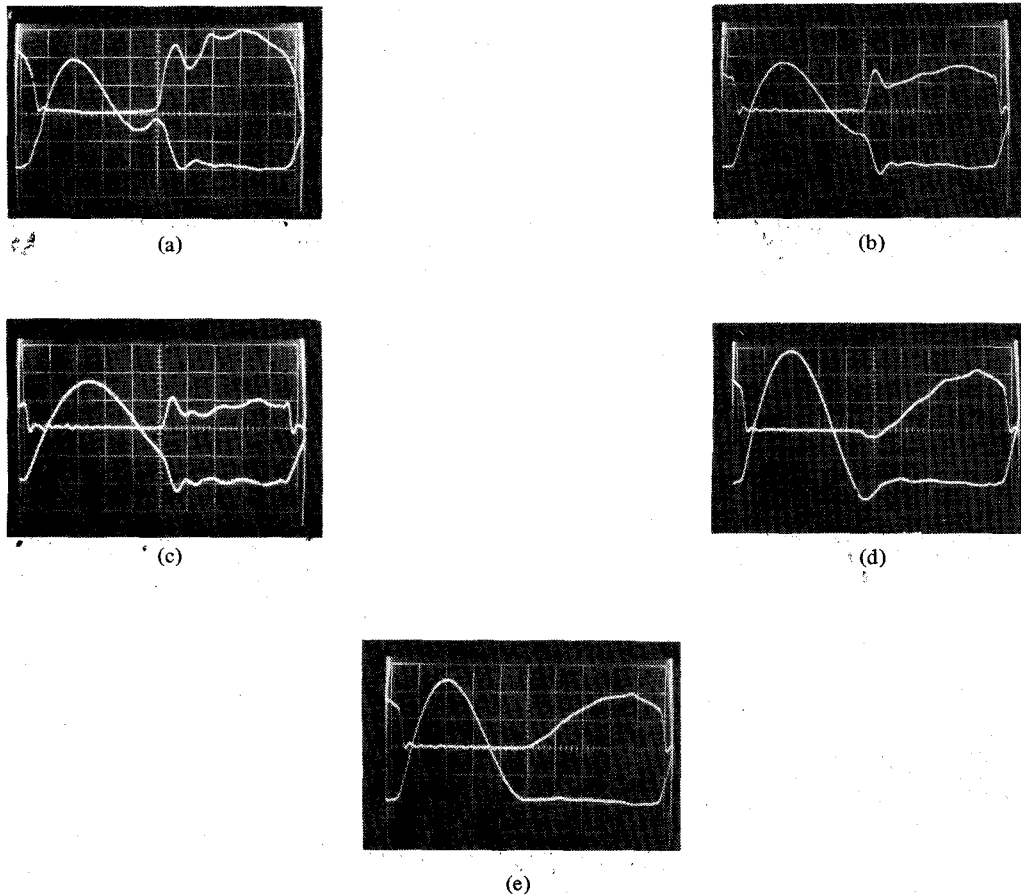
(a)

(b)

(c)

(d)

(e)

Fig. 4. V_{CE} (lower trace) and I_C (upper trace) for circuit of Fig. 3 operating at 10.5 MHz. Incorrect element values can cause positive voltage at transistor turnon, with zero-slope condition occurring (a) too early, (b) at correct time, or (c) too late; or they can cause (d) negative voltage at turnon. Correct element values give (e) zero-voltage, zero-slope condition at turnon. Vertical: 10 V or 0.5 A/div.; horizontal: 10 ns/div. Ringing after turnon in (a)–(d) is due to inductance of current-measuring instrumentation.
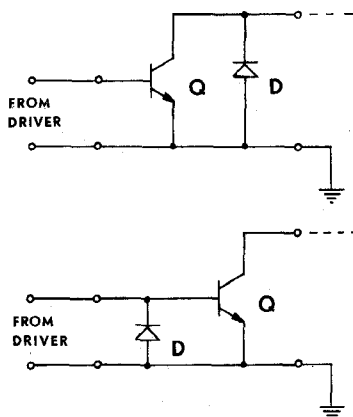

Fig. 5. Addition of commutating diode to transistor. (a) At collector. (b) At base.

zero value at the end of the "off" half-cycle. This zero value and zero slope realize Conditions 5) and 6) of Section III-A above.

A nearly sinusoidal fundamental-frequency current flows in the branch $L2$-$C2$-R. (The harmonic content is primarily

second harmonic, of amplitude $\approx 0.50/Q_L$ relative to the fundamental, e.g., ≈ 5.0 percent (-26 dB) for $Q_L = 10$.) The collector current waveform is approximately a section of a sine wave, as shown in Fig. 4(e); D below gives numerical details. Depending on the transistor storage time and the technique used to accommodate it, the transistor is operated in saturation or in the active region just outside of saturation.[10]

C. Circuit Element Values

The element values for the circuit of Fig. 3 are obtained by choosing the three variables $C1$, $C2$, and $L2$ to meet simultaneously the three following mathematical conditions.

1) $V_{CE} = 0$ at $t = (1 - D)(1/f)$ after switch turn-off time, where f is the operating frequency and D is the switch duty ratio, here taken as 50 percent.

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[10]If it is in the active region, the transistor is made to have a low output impedance while remaining active (i.e., to act as a switch as defined here) by use of a Baker clamp [30]. We recommend allowing the transistor to saturate (for higher efficiency) and coping with the storage time by proper circuit design. Storage time in RF power transistors appears not to have been discussed in the literature; that is the subject of a planned future paper.

TABLE II
ELEMENT VALUES FOR NEW DESIGN AND CONVENTIONAL DESIGN

Circuit Element	New Design	Conventional Design	Ratio New/Conventional
L2	1.72 μH	0.0403 μH	42.7
C1	162 pF	6111 pF	0.033
C2	200 pF	∞	≈1/∞
R	18.0 Ω	0.0422 Ω	42.7

2) $dV_{CE}/dt = 0$ at $t = (1 - D)(1/f)$ after switch turn-off time.

3) Q_L is any chosen value, which may be chosen as discussed immediately below. A specific $C1/C2$ ratio [see (4)] makes that chosen Q_L provide the proper damping shown in the "Q_L correct" curve of Fig. 4(e), yielding the zero-slope zero-value V_{CE} at turn-on time.

The choice of Q_L involves a tradeoff among 1) low harmonic content of the power delivered to R (high Q_L), 2) high efficiency (low Q_L), and 3) complexity of the filter (if any) used for additional harmonic suppression. An optimal design minimizes the total loss in the load network and the subsequent filter (if any) while meeting a specified maximum limit for harmonic output at the load. Equations will now be given for the element values of the Fig. 3 member of the new class; equations for the resulting performance are in Section III-D below. The derivations are too long to give here; they are available from the authors.[11] The equations here are for 50 percent duty ratio; modified ones hold for other values of duty ratio.

The values of R and V_{CC} are constrained by the requirement to deliver a specified power output to the load from the V_{CC} power supply; specifying either one dictates the other. For highest efficiency, the highest possible V_{CC} should be used, within the V_{CE} limitation of the transistor, as will be seen in (8) below. The maximum allowable V_{CC} can be found from (7). The value of R is found as[12]

$$R = \frac{(V_{CC} - V_{CE(sat)})^2}{P} \left(\frac{2}{\frac{\pi^2}{4} + 1} \right) = 0.577 \frac{(V_{CC} - V_{CE(sat)})^2}{P}.$$

(1)

Impedance transformation can be used if the load resistance is not equal to this value of R; see E below. The desired Q_L may be chosen freely, according to the design compromise to be

made between efficiency and harmonic content of the power delivered to the load. Then

$$L2 = Q_L R/2\pi f, \quad \text{from the definition of } Q_L.$$

(2)

To satisfy the conditions $V_{CE} = 0$ and $dV_{CE}/dt = 0$ at $t = 0.5/f$ after switch turnoff, given the chosen Q_L,

$$C1 = 1/2\pi fR \left(\frac{\pi^2}{4} + 1 \right) \left(\frac{\pi}{2} \right) = 1/2\pi fR 5.447,$$

(3)

and

$$C2 \approx \left(\frac{1}{(2\pi f)^2 L2} \right) \left(1 + \frac{1.42}{Q_L - 2.08} \right)$$

$$\approx C1 \left(\frac{5.447}{Q_L} \right) \left(1 + \frac{1.42}{Q_L - 2.08} \right).$$

(4)

Note that $L2$ is not resonant at f with $C2$ or with the series combination of $C1$ and $C2$. Load reactance (if any) is accommodated by absorbing it into $C2$ and $L2$: the inductance of $L2$ is decreased if the load series reactance is inductive, the capacitance of $C2$ is increased if the load reactance is capacitive, or both are done if the load is a combination of inductance and capacitance (e.g., a radio transmitting antenna or an ultrasonic transmitting transducer).[13]

Table II shows the circuit element values for amplifiers with the topology of Fig. 3 as realized with a conventional design (e.g., [22] or [26]) and with our design; the element values are seen to be greatly different. This example is for an amplifier to deliver 20 W at 10 MHz, using $Q_L = 6$, $V_{CC} = 27$ V dc, $L1 = $ RF choke, and $V_{CE(sat)} = 2$V.

D. Performance Equations and Experimental Results

The dc collector current of the transistor Q, while delivering ac power P, is

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[11]Equations (1)–(8) agree, in the limit case of $\{Q_L = \infty, V_{CE(sat)} = 0, t_f = 0\}$, with the results of an independent theoretical analysis of that case by F. H. Raab (unpublished). Equations (3), (5), (7), and (8) use Raab's derivation of $C1$. The quantities 1.42(±0.10), 2.08(±0.05), 0.82(±0.10), and 0.50(±0.09) in (4)–(8) are derived from experimental measurements by the authors and their colleague, M. Chessman.

[12]Here R is the total resistive load presented to the transistor: the sum of the input resistance of the load (or the filter, if used) and the series ac resistances of $L2$ and $C2$, plus an "equivalent" lumping of the ac losses of $L1$ and $C1$. P is the total power delivered by the transistor to R as just defined. DC losses in $L1$ are accounted for by using an effective value of V_{CC} which is lower than the dc power supply voltage by the value of the dc voltage drop in the dc resistance of $L1$.

[13]The impedance of an actual load may be more complicated than the series combination of a frequency-independent R and a frequency-independent L and/or C. Hence the effect of the load reactance may not be precisely the same as an effective increase in $L2$ and/or decrease in $C2$. However, for reasonably well-behaved load impedances, the net effect is only a small change in the voltage and current wave-shapes from those which would have existed if the output branch had consisted solely of frequency-independent elements $C2, L2$, and R. This is because by far the principal component of the current entering the load from $L2$-$C2$ is of frequency f; harmonic-frequency components are small. Therefore the impedances at f are the most influential ones; the impedances at harmonic frequencies have correspondingly less influence on the voltage waveforms.

$$I_{DC} = \frac{P}{V_{CC}} \left[\frac{1 - (2\pi A)^2/12}{1 - (2\pi A)^2/6 - \dfrac{V_{CE(\text{sat})}}{V_{CC}}(1 + A - (2\pi A)^2/6)} \right]$$

(5)

Fig. 6. Impedance transformation between load and switch by adding a winding to $L1$.

where $A \equiv (1 + 0.82/Q_L)ft_f$, and where f is the operating frequency and t_f is the collector current fall time (100 to 0 percent of a linear ramp) during transistor turnoff. The collector current waveshape is determined by the load network and is approximately a section of a sine wave (between $-32.5°$ and $+147.5°$ in angle) centered at $I = I_{DC}$. Current builds up gradually from zero at the beginning of the "on" half-cycle to a peak value of

$$I_{Cpk} = I_{DC} \left[1 + \left(\frac{\pi^2}{4} + 1 \right)^{1/2} (1 - 0.50/Q_L) \right]$$

$$= I_{DC} [1 + 1.862(1 - 0.50/Q_L)].$$

(6)

It then decays gradually to $2I_{DC}(1 + 0.82/Q_L)$, at which time the transistor is suddenly turned off by the drive signal applied to its base-emitter junction. The peak collector-emitter voltage is

$$V_{CEpk} = V_{CC} + \left[2\pi \arcsin \left(\frac{\pi^2}{4} + 1 \right)^{-1/2} - 1 \right]$$

$$\cdot [V_{CC} - V_{CE(\text{sat})}] = 3.562 \, V_{CC} - 2.562 \, V_{CE(\text{sat})}.$$

(7)

These peak and dc values must be within the safe operating region of the transistor. The most stressful condition is turnoff of $\approx 2I_{DC}$ linearly with time while V_{CE} is rising parabolically. The collector efficiency is $P/V_{CC}I_{DC}$, from (5),

$$\eta_c = \frac{1 - (2\pi A)^2/6 - \dfrac{V_{CE(\text{sat})}}{V_{CC}}(1 + A - (2\pi A)^2/6)}{1 - (2\pi A)^2/12}.$$

(8)

The authors measured 26-W output at 3.9 MHz from a parallelled pair of Motorola 2N3735 TO-5 transistors in the circuit of Fig. 3, with only 4 percent of the dc input power dissipated in the transistors. Inductor power losses were 3.5 percent in $L2$ and 0.7 percent in $L1$. All observations agreed with the above equations to within instrument accuracies. Circuit parameters were: $L1 = 63$ turns AWG 24 on Indiana General CF111-Q2 ferrite toroid ($\approx 68 \, \mu H + 0.1 \, \Omega$ dc), $L2 = 3.45 \, \mu H + 0.4 \, \Omega$ ac, $C1 = 713$ pF, $C2 = 600$ pF, $R = 10.3 \, \Omega$, and $V_{CC} = 23.1$ V dc.

E. Further Remarks

Impedance Transformation and C_{ob} Neutralization: Fig. 6 shows how additional windings change $L1$ to a transformer $T1$ which transforms the load impedance. Leakage inductance between the $T1$ windings can be absorbed into $L2$; this increases the efficiency by eliminating the losses of the portion of $L2$ replaced by the leakage inductance. Fig. 7(a)–(c) shows
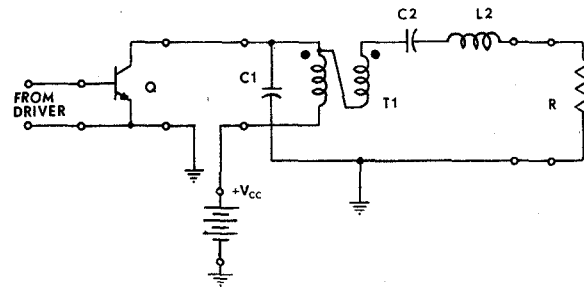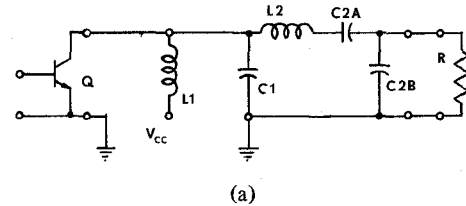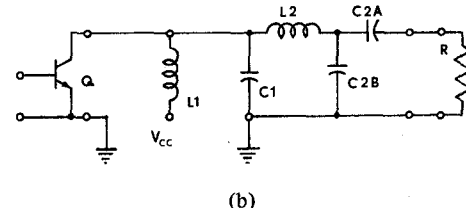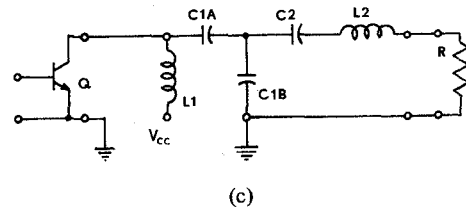

(a)

(b)

(c)

Fig. 7. Impedance transformation between load and switch by tapping a capacitor. (a) and (b) Tapping $C2$. (c) Tapping $C1$.

impedance transformation by effectively tapping $C1$ or $C2$; in some cases $C2A$ can be infinite. Neutralization of transistor C_{ob} (e.g., to reduce the current which must be supplied to C_{ob} by the driver) can be accomplished by capacitively coupling the transistor base to an inverting winding on $T1$.

Tuning: To operate across a frequency band, 1) provision may be made for varying $C1$, $C2$, and/or $L2$, 2) fixed element values can be used with some sacrifice of performance, or 3) more complex load networks can be used. The tradeoff factors are the same as in conventional amplifiers, but the design method is different; that is the subject of a planned future paper. Using a load network slightly more complex than that of Fig. 3, we achieved single-element tuning across a 1.6 : 1 frequency band, maintaining the turnon conditions $V = 0$ and $dV/dt = 0$ across the entire band.

Optimum Transistor Design: This circuit uses the transistor in a way quite different from that of conventional RF power amplifiers. Both RF power transistors and switching transistors (e.g., Motorola 2N3735, National Semiconductor 2N6376, RCA 2N5262) work well in this circuit, but neither class is

optimized in design and construction for this application. Changes in transistor design and packaging could yield a transistor which gives even better results in this type of circuit than what we have obtained so far. Further information is available from the authors.

Circuit Protection: As with other kinds of high-efficiency equipment, protection should be provided against accidental low-efficiency operation (i.e., accidental high power dissipation) if advantage is being taken of the normal high efficiency by reducing the heat-dissipation capability. The higher the operating efficiency, the more important this requirement becomes.

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