The Monolithic Op Amp: A Tutorial Study

JAMES E. SOLOMON, MEMBER, IEEE

Invited Paper

Abstract—A study is made of the integrated circuit operational amplifier (IC op amp) to explain details of its behavior in a simplified and understandable manner. Included are analyses of thermal feedback effects on gain, basic relationships for bandwidth and slew rate, and a discussion of pole-splitting frequency compensation. Sources of second-order bandlimiting in the amplifier are also identified and some approaches to speed and bandwidth improvement are developed. Brief sections are included on new JFET-bipolar circuitry and die area reduction techniques using transconductance reduction.

I. Introduction

THE integrated circuit operational amplifier (IC op amp) is the most widely used of all linear circuits in production today. Over one hundred million of the devices will be sold in 1974 alone, and production costs are falling low enough so that op amps find applications in virtually every analog area. Despite this wide usage, however, many of the basic performance characteristics of the op amp are poorly understood.

It is the intent of this study to develop an understanding for op amp behavior in as direct and intuitive a manner as possible. This is done by using a variety of simplified circuit models which can be analyzed in some cases by inspection, or in others by writing just a few equations. These simplified models are generally developed from the single representative op amp configuration shown in Figs. 1 and 2.

The rationale for starting with the particular circuit of Fig. 1 is based on the following: this circuit contains, in simplified form, all of the important elements of the most commonly used integrated op amps. It consists essentially of two voltage gain stages, an input differential amp and a common emitter second stage, followed by a class-AB output emitter follower which provides low impedance drive to the load. The two interstages are frequency compensated by a single small "pole-splitting" capacitor (see below) which is usually included on the op amp chip. In most respects this circuit is directly equivalent to the general purpose LM101 [1], μA 741 [2], and the newer dual and quad op amps [3], so the results of our study relate directly to these devices. Even for more exotic designs, such as wide-band amps using feedforward [4], [5], or the new FET input circuits [6], the basic analysis approaches still apply, and performance details can be accurately predicted. It has also been found that a good understanding of the limitations of the circuit in Fig. 1 provides a reasonable starting point from which higher performance amplifiers can be developed.

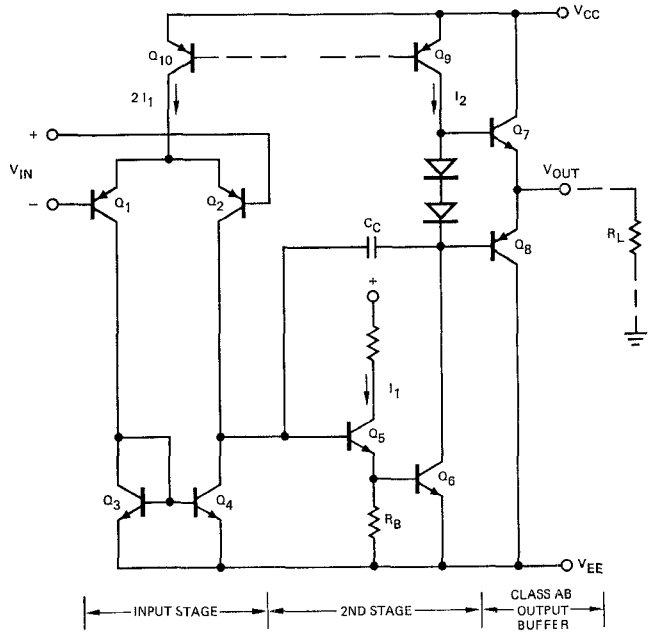


Fig. 1. Basic two-stage IC op amp used for study. Minimal modifications used in actual IC are shown in Fig. 2.

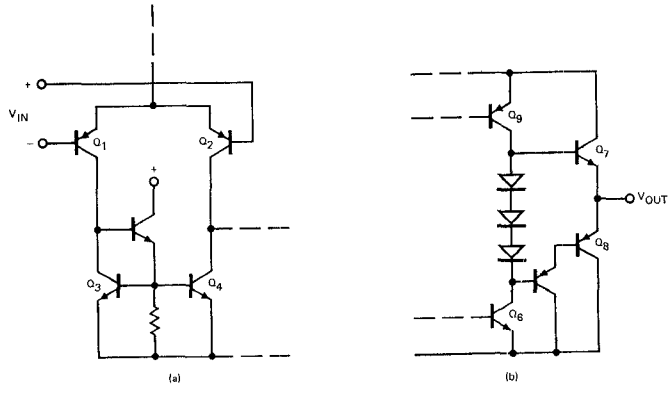
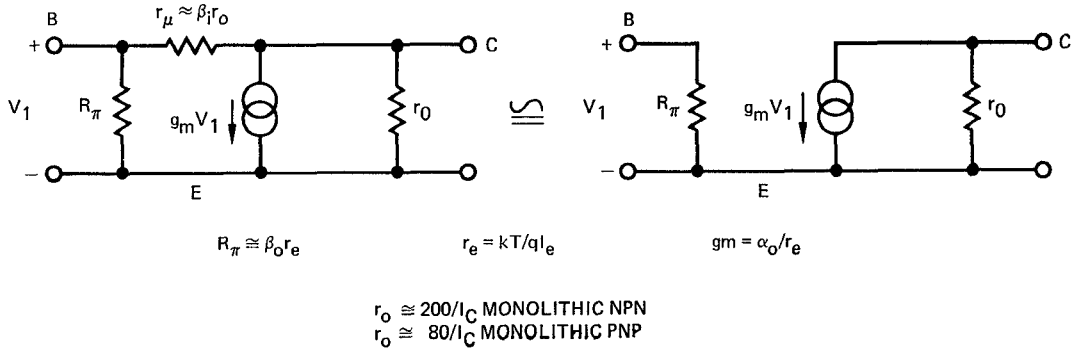


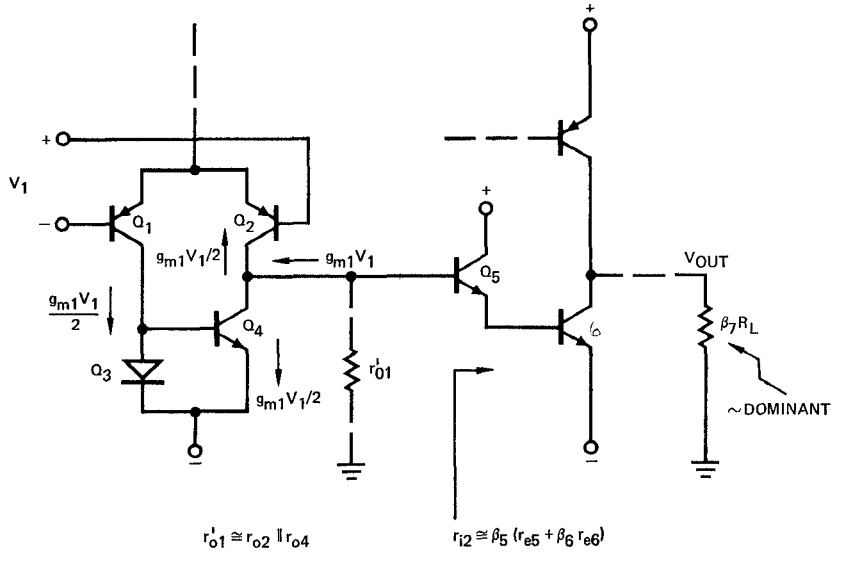
Fig. 2. (a) Modified current mirror used to reduce dc offset caused by base currents in $Q3$ and $Q4$ in Fig. 1. (b) Darlington p-n-p output stage needed to minimize gain fall-off when sinking large output currents. This is needed to offset the rapid β drop which occurs in IC p-n-p's.

The study begins in Section II, with an analysis of dc and low frequency gain. It is shown that the gain is typically limited by thermal feedback rather than elec-

Manuscript received July 1, 1974; revised August 8, 1974.
The author is with the National Semiconductor Corporation, Santa Clara, Calif. 95051.



(a)



(b)

Fig. 3. (a) Approximate π model for CE transistor at dc. Feedback element $r_\mu \cong \beta_i r_0$ is ignored since this greatly simplifies hand calculations. The error caused is usually less than 10 percent because β_i, the intrinsic β under the emitter, is quite large. Base resistance r_x is also ignored for simplicity. (b) Circuit illustrating calculation of electronic gain for op amp of Fig. 1. Consideration is given only to the fully loaded condition ($R_L \cong 2$ kΩ) where β_7 is falling (to about 50) due to high current density. Under this condition, the output resistance of $Q6$ and $Q9$ are nondominant.

trical characteristics. A highly simplified thermal analysis is made, resulting in a gain equation containing only the maximum output current of the op amp and a thermal feedback constant.

The next three sections apply first-order models to the calculation of small-signal high frequency and large-signal slewing characteristics. Results obtained include an accurate equation for gain-bandwidth product, a general expression for slew rate, some important relationships between slew rate and bandwidth, and a solution for voltage follower behavior in a slewing mode. Due to the simplicity of the results in these sections, they are very useful to designers in the development of new amplifier circuits.

Section VI applies more accurate models to the calculation of important second-order effects. An effort is made in this section to isolate all of the major contributors to bandlimiting in the modern amp.

In the final section, some techniques for reduction of op amp die size are considered. Transconductance reduction and layout techniques are discussed which lead to fabrication of an extremely compact op amp cell. An example yielding 8000 possible op amps per 3-in wafer is given.

II. Gain at DC and Low Frequencies

A. The Electronic Gain

The electronic voltage gain will first be calculated at dc using the circuit of Fig. 1. This calculation becomes straightforward if we employ the simplified transistor model shown in Fig. 3(a). The resulting gain from Fig. 3(b) is

$$A_V(0) = \frac{v_{out}}{v_{in}} \cong \frac{g_{m1}\beta_5\beta_6\beta_7 R_L}{1 + r_{i2}/r_{01}'} \tag{1}$$

where

$$r_{i2} \cong \beta_5(r_{e5} + \beta_6 r_{e6})$$

$$r_{01}' \cong r_{04}//r_{02}.$$

It has been assumed that

$$\beta_7 R_L < r_{06}//r_{09},\ g_{m1} = g_{m2},\ \beta_7 = \beta_8.$$

The numerical subscripts relate parameters to transistor Q numbers (i.e., r_{e5} is r_e of Q_5, β_6 is β_0 of Q_6, etc.). It has also been assumed that the current mirror transistors Q_3 and Q_4 have α's of unity, and the usually small loading of R_B has been ignored. Despite the several assumptions made in obtaining this simple form for (1), its accuracy is quite adequate for our needs.

An examination of (1) confirms the way in which the amplifier operates: the input pair and current mirror convert the input voltage to a current $g_{m1}v_{\text{in}}$ which drives the base of the second stage. Transistors Q_5, Q_6, and Q_7 simply multiply this current by β^3 and supply it to the load R_L. The finite output resistance of the first stage causes some loss when compared with second stage input resistance, as indicated by the term $1/(1 + r_{i2}/r_{01}')$. A numerical example will help our perspective: for the LM101A, $I_1 \cong 10$ μA, $I_2 \cong 300$ μA, $\beta_5 = \beta_6 \cong 150$, and $\beta_7 \cong 50$. From (1) and dc voltage gain with $R_L = 2$ kΩ is

$$A_V(0) \cong 625\,000. \tag{2}$$

The number predicted by (2) agrees well with that measured on a discrete breadboard of the LM101A, but is much higher than that observed on the integrated circuit. The reason for this is explained in the next section.

B. Thermal Feedback Effects on Gain

The typical IC op amp is capable of delivering powers of 50–100 mW to a load. In the process of delivering this power, the output stage of the amp internally dissipates similar power levels, which causes the temperature of the IC chip to rise in proportion to the output dissipated power. The silicon chip and the package to which it is bonded are good thermal conductors, so the whole chip tends to rise to the same temperature as the output stage. Despite this, small temperature gradients from a few tenths to a few degrees centigrade develop across the chip with the output section being hotter than the rest. As illustrated in Fig. 4, these temperature gradients appear across the input components of the op amp and induce an input voltage which is proportional to the output dissipated power.

To a first order, it can be assumed that the temperature difference $(T_2\text{-}T_1)$ across a pair of matched and closely spaced components is given simply by

$$(T_2 - T_1) \cong \pm K_T P_d \quad ^\circ\text{C} \tag{3}$$

where

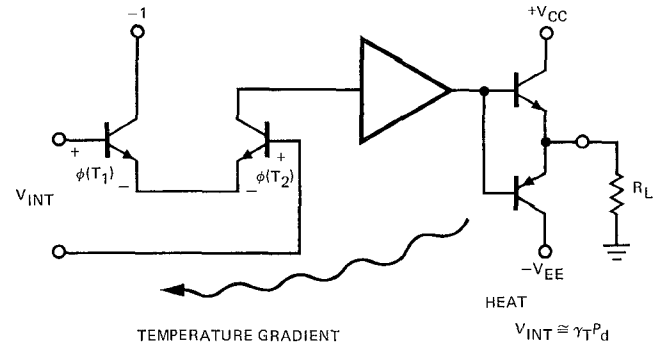


Fig. 4. Simple model illustrating thermal feedback in an IC op amp having a single dominant source of self-heat, the output stage. The constant $\gamma_T \cong 0.6$ mV/W and P_d is power dissipated in the output. For simplicity, we ignore input drift due to uniform heating of the package. This effect can be significant if the input stage drift is not low, see [7].

P_d power dissipated in the output circuit,
K_T a constant with dimensions of °C/W.

The plus/minus sign is needed because the direction of the thermal gradient is unknown. In fact, the sign may reverse polarity during the output swing as the dominant source of heat shifts from one transistor to another. If the dominant input components consist of the differential transistor pair of Fig. 4, the thermally induced input voltage V_{int} can be calculated as

$$V_{\text{int}} \cong \pm K_T P_d (2 \times 10^{-3})$$

$$\cong \pm \gamma_T P_d \tag{4}$$

where $\gamma_T = K_T(2 \times 10^{-3})$ V/W, since the transistor emitter-base drops change about -2 mV/°C.

For a thermally well designed IC op amp, in which the power output devices are made to approximate either a point or a line source and the input components are placed on the resulting isothermal lines (see below and Fig. 8), typical values measured for K_T are

$$K_T \approx 0.3 \ ^\circ\text{C/W} \tag{5}$$

in a TO-5 package.

The dissipated power in the class-AB output stage P_d is written by inspection of Fig. 4:

$$P_d = \frac{V_0 V_s - V_0^2}{R_L} \tag{6}$$

where

$$V_s = +V_{cc} \quad \text{when } V_0 > 0$$

$$V_s = -V_{ee} \quad \text{when } V_0 < 0.$$

A plot of (6) in Fig. 5 resembles the well-known class-AB dissipation characteristics, with zero dissipation occurring for $V_0 = 0$, $+V_{cc}$, $-V_{ec}$. Dissipation peaks occur for $V_0 = +V_{cc}/2$ and $-V_{ec}/2$. Note also from (4) that the thermally induced input voltage V_{int} has this same double-humped shape since it is just equal to a constant times P_d at dc.

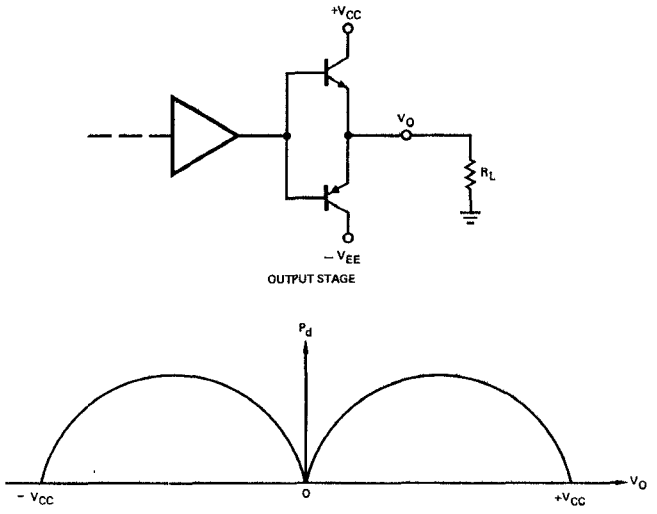


Fig. 5. Simple class-B output stage and plot of power dissipated in the stage, P_d, assuming device can swing to the power supplies. Equation (6) gives an expression for the plot.

Now examine Figs. 6(a) and (b) which are curves of open-loop V_0 versus V_{in} for the IC op amp. Note first that the overall curve can be visualized to be made up of two components: a) a normal straight line electrical gain curve of the sort expected from (1) and b) a double-humped curve similar to that of Fig. 5. Further, note that the gain characteristic has either positive or negative slope depending on the value of output voltage. This means that the thermal feedback causes the open-loop gain of the feedback amplifier to change phase by 180°, apparently causing negative feedback to become positive feedback. If this is really true, the question arises: which input should be used as the inverting one for feedback? Further, is there any way to close the amplifier and be sure it will not find an unstable operating point and latch to one of the power supplies?

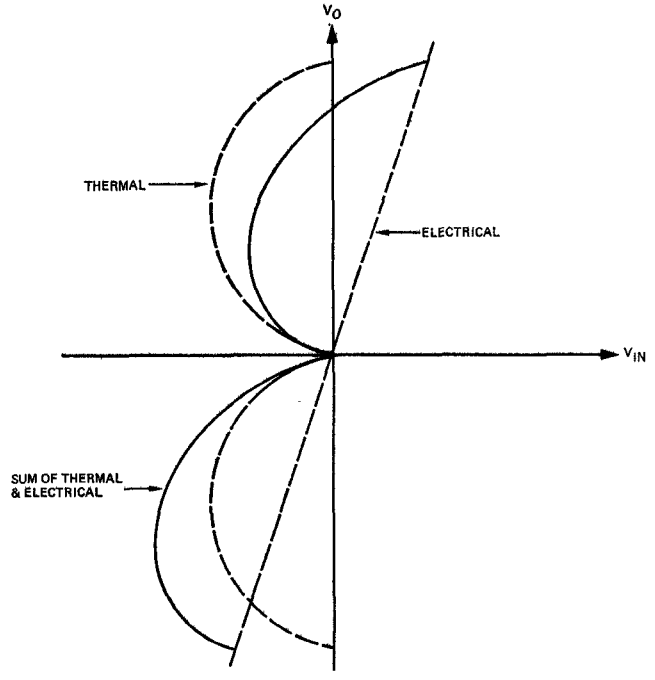
The answers to these questions can be found by studying a simple model of the op amp under closed-loop conditions, including the effects of thermal coupling. As shown in Fig. 7, the thermal coupling can be visualized as just an additional feedback path which acts in parallel with the normal electrical feedback. Noting that the electrical form of the thermal feedback factor is [see (4) and (6)]

$$\beta_T = \frac{\partial V_{\text{int}}}{\partial V_0} = \pm\frac{\gamma_T}{R_L}(V_S - 2V_0). \tag{7}$$

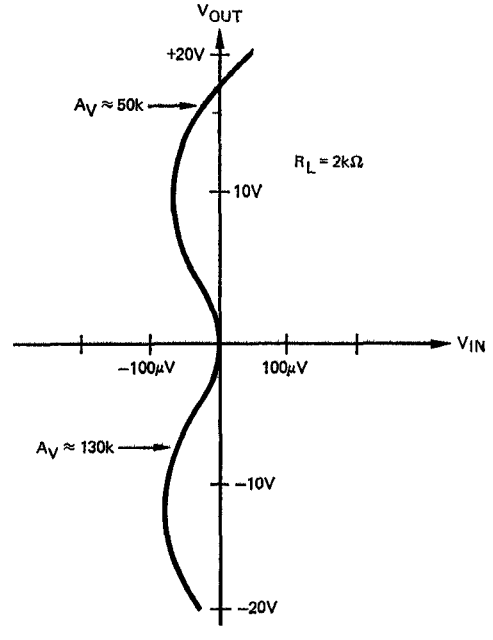
The closed-loop gain, including thermal feedback is

$$A_V(0) = \frac{\mu}{1 + \mu(\beta_e \pm \beta_T)} \tag{8}$$

where μ is the open-loop gain in the absence of thermal feedback [(1)] and β_e is the applied electrical feedback as in Fig. 7. Inspection of (8) confirms that as long as there is sufficient electrical feedback to swamp the thermal feedback (i.e., $\beta_e > \beta_T$), the amplifier will behave as a normal closed-loop device with characteristics determined principally by the electrical feedback (i.e., $A_V(0) \cong 1/\beta_e$). On the other hand, if β_e is small or nonexistant, the thermal term in (8) may dominate, giving an apparent open-loop gain characteristic determined by the thermal feedback factor β_T. Letting $\beta_e = 0$ and combining (7) and (8), $A_V(0)$ becomes



(a)



(b)

Fig. 6. (a) Idealized dc transfer curve for an IC op amp showing its electrical and thermal components. (b) Experimental open-loop transfer curve for a representative op amp (LM 101).

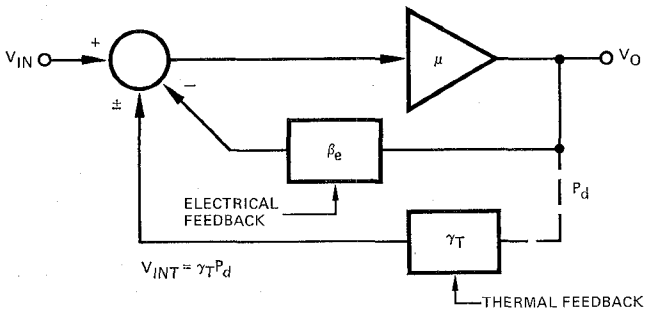


Fig. 7. Diagram used to calculate closed-loop gain with thermal feedback.

$$A_V(0) = \frac{\mu}{1 \pm \frac{\mu\gamma_T}{R_L}(V_S - 2V_0)}. \tag{9}$$

Recalling from (6) that V_0 ranges between 0 and V_S, we note that the incremental thermal feedback is greatest when $V_0 = 0$ or V_s, and it is at these points that the thermally limited gain is smallest. To use the amplifier in a predictable manner, one must always apply enough electrical feedback to reduce the gain below this minimum thermal gain. Thus, a *maximum usable gain* can be defined as that approximately equal to the value of (9) with $V_0 = 0$ or V_s which is

$$A_V(0)|_{\max} \cong \frac{R_L}{\gamma_T V_S} \tag{10}$$

or

$$A_V(0)|_{\max} \cong \frac{1}{\gamma_T I_{\max}}. \tag{11}$$

It was assumed in (10) and (11) that thermal feedback dominates over the open-loop electrical gain, μ. Finally, in (11) a maximum current was defined $I_{\max} = V_S/R_L$ as the maximum current which would flow if the amplifier output could swing all the way to the supplies.

Equation (11) is a strikingly simple and quite general result which can be used to predict the expected maximum usable gain for an amplifier if we know only the maximum output current and the thermal feedback constant γ_T.

Recall that typically $K_T \cong 0.3°C/W$ and $\gamma_T = (2 \times 10^{-3})$ $K_T \cong 0.6$ mV/W. Consider, as as example, the standard IC op amp operating with power supplies of $V_S = \pm 15$ V and a minimum load of 2 kΩ, which gives $I_{\max} = 15$ V/2 kΩ = 7.5 mA. Then, from (11), the maximum thermally limited gain is about:

$$A_V(0)|_{\max} \cong 1/(0.6 \times 10^{-3})(7.5 \times 10^{-3})$$
$$\cong 220\,000. \tag{12}$$

Comparing (2) and (12), it is apparent that the thermal characteristics dominate over the electrical ones if the minimum load resistor is used. For loads of 6 kΩ or more, the electrical characteristics should begin to dominate

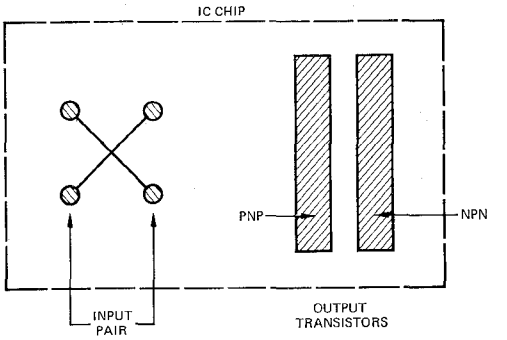


Fig. 8. One type layout in which a quad of input transistors is cross connected to reduce effect of nonuniform thermal gradients. The output transistors use distributed stripe geometries to generate predictable isothermal lines.

if thermal feedback from sources other than the output stage is negligible. It should be noted also that, in some high speed, high drain op amps, thermal feedback from the second stage dominates when there is no load.

As a second example, consider the so-called "power op amp" or high gain audio amp which suffers from the same thermal limitations just discussed. For a device which can deliver 1 W into a 16-Ω load, the peak output current and voltage are 350 mA and 5.7 V. Typically, a supply voltage of about 16 V is needed to allow for the swing loss in the IC output stage. $I_{\max}$ is then 8 V/16 Ω or 0.5 A. If the device is in a TO-5 package γ_T is approximately 0.6 mV/W, so from (11) the maximum usable dc gain is

$$A_V(0)|_{\max} \cong \frac{1}{(0.6 \times 10^{-3})(0.5)} \cong 3300. \tag{13}$$

This is quite low compared with electrical gains of, say, 100 000 which are easily obtainable. The situation can be improved considerably by using a large die to separate the power devices from the inputs and carefully placing the inputs on constant temperature (isothermal) lines as illustrated in Fig. 8. If one also uses a power package with a heavy copper base, γ_T's as low as 50 μV/W have been observed. For example, a well-designed 5-W amplifier driving an 8-Ω load and using a 24-V supply, would have a maximum gain of 13 000 in such a power package.

As a final comment, it should be pointed out that the most commonly observed effect of thermal feedback in high gain circuits is low frequency distortion due to the nonlinear transfer characteristic. Differential thermal coupling typically falls off at an initial rate of 6 dB/octave starting around 100–200 Hz, so higher frequencies are uneffected.

III. Small-Signal Frequency Response

At higher frequencies where thermal effects can be ignored, the behavior of the op amp is dependent on purely electronic phenomena. Most of the important small and large signal performance characteristics of the classical IC op amp can be accurately predicted from

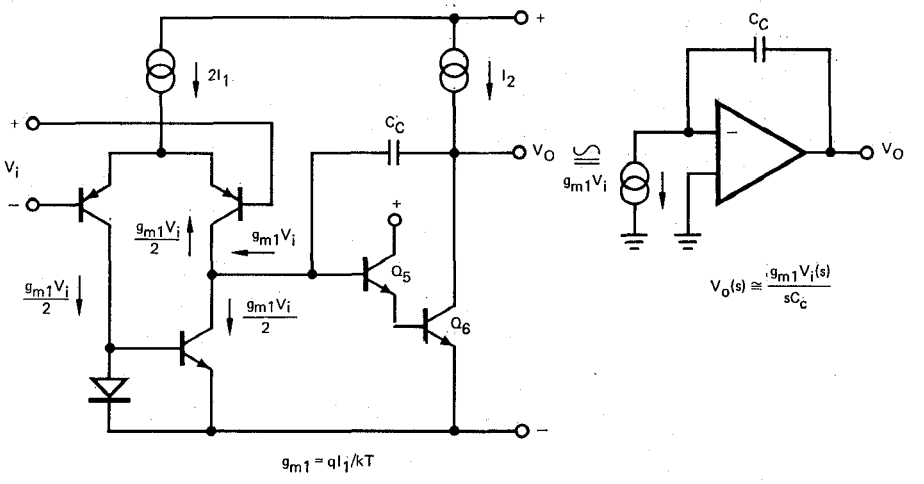


Fig. 9. First-order model of op amp used to calculate small signal high frequency gain. At frequencies of interest the input impedance of the second stage becomes low compared to first stage output impedance due to C_c feedback. Because of this, first stage output impedance can be assumed infinite, with no loss in accuracy.

very simple first-order models for the amplifier in Fig. 1[8]. The small-signal model that is used assumes that the input differential amplifier and current mirror can be replaced by a frequency independent voltage controlled current source, see Fig. 9. The second stage consisting essentially of transistors Q_5 and Q_6, and the current source load, is modeled as an ideal frequency independent amplifier block with a feedback or "integrating capacitor" identical to the compensation capacitor, C_c. The output stage is assumed to have unity voltage gain and is ignored in our calculations. From Fig. 9, the high frequency gain is calculated by inspection:

$$A_v(\omega) = \left|\frac{v_0}{v_i}(s)\right| = \left|\frac{g_{m1}}{sC_c}\right| = \frac{g_{m1}}{\omega C_c} \tag{14}$$

where dc and low frequency behavior have not been included since this was evaluated in the last section. Fig. 10 is a plot of the gain magnitude as predicted by (14). From this figure it is a simple matter to calculate the open-loop unity gain frequency ω_u, which is also the gain-bandwidth product for the op amp under closed-loop conditions:

$$\omega_u = \frac{g_{m1}}{C_c}. \tag{15}$$

In a practical amplifier, ω_u is set to a low enough frequency (by choosing a large C_c) so that negligible excess phase over the 90° due to C_c has built up. There are numerous contributors to excess phase including low f_t p-n-p's, stray capacitances, nondominant second stage poles, etc. These are discussed in more detail in a later section, but for now suffice it to say that, in the simple IC op amp, $\omega_u/2\pi$ is limited to about 1 MHz. As a simple test of (15), the LM101 or the μA741 has a first stage bias current I_1 of 10 μA per side, and a compensation capacitor for unity gain operation, C_c, of 30 pF. These amplifiers each have a first stage g_m which is half that

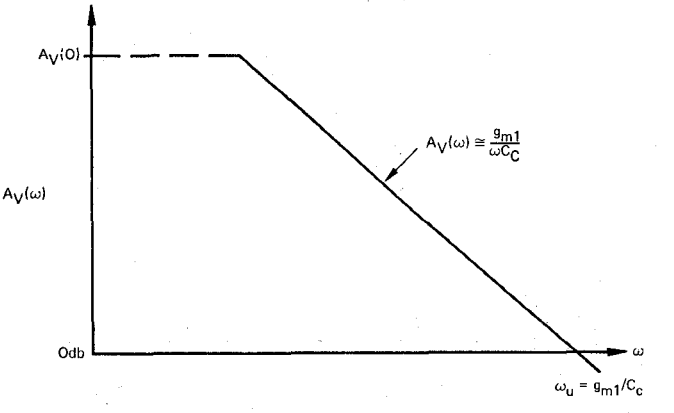


Fig. 10. Plot of open-loop gain calculated from model in Fig. 9. The dc and LF gain are given by (1), or (11) if thermal feedback dominates.

of the simple differential amplifier in Fig. 1 so $g_{m1} = qI_1/2kT$. Equation (15) then predicts a unity gain corner of

$$f_u = \frac{\omega_u}{2\pi} = \frac{g_{m1}}{2\pi C_c} = \frac{(0.192 \times 10^{-3})}{2\pi(30 \times 10^{-12})} = 1.02 \text{ MHz} \tag{16}$$

which agrees closely with the measured values.

IV. Slew Rate and Some Special Limits

A. A General Limit on Slew Rate

If an op amp is overdriven by a large-signal pulse or square wave having a fast enough rise time, the output does not follow the input immediately. Instead, it ramps or "slews" at some limiting rate determined by internal currents and capacitances, as illustrated in Fig. 11. The magnitude of input voltage required to make the amplifier reach its maximum slew rate varies, depending on the type of input stage used. For an op amp with a

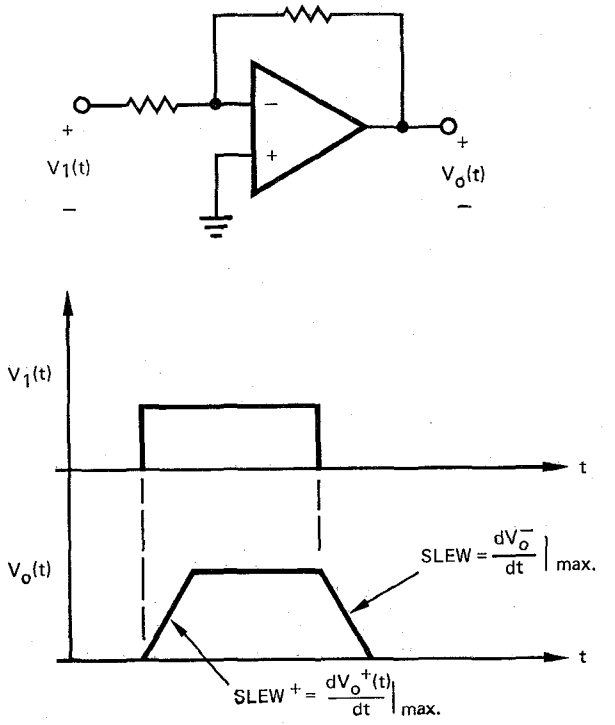


Fig. 11. Large signal "slewing" response observed if the input is overdriven.

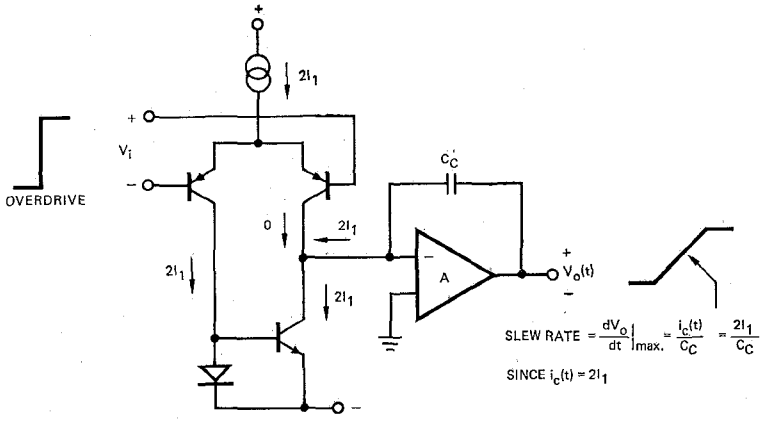


Fig. 12. Model used to calculate slew rate for the amp of Fig. 1 in the inverting mode. For simplicity, all transistor α's are assumed equal to unity, although results are essentially independent of α. An identical slew rate can be calculated for a negative-going output, obtained if the applied input polarity is reversed.

simple input differential amp, an input of about 60 mV will cause the output to slew at 90 percent of its maximum rate, while a μA741, which has half the input g_m, requires 120 mV. High speed amplifiers such as the LM 118 or a FET-input circuit require much greater overdrive, with 1–3 V being common. The reasons for these overdrive requirements will become clear below.

An adequate model to calculate slew limits for the representative op amp in the inverting mode is shown in Fig. 12, where the only important assumption made is that $I_2 \geq 2I_1$ in Fig. 1. This condition always holds in a well-designed op amp. (If one lets I_2 be less than $2I_1$, the slew is limited by I_2 rather than I_1, which results in lower speed than is otherwise possible.) Fig. 12 requires some modification for noninverting operation, and we will study this later.

The limiting slew rate is now calculated from Fig. 12. Letting the input voltage be large enough to fully switch the input differential amp, we see that all of the first stage tail current $2I_1$ is simply diverted into the integrator consisting of A and C_c. The resulting slew rate is then:

$$\text{slew rate} = \left.\frac{dv_0}{dt}\right|_{\max} = \frac{i_c(t)}{C_c}. \tag{17}$$

Noting that $i_c(t)$ is a constant $2I_1$, this becomes

$$\left.\frac{dv_0}{dt}\right|_{\max} = \frac{2I_1}{C_c}. \tag{18}$$

As a check of this result, recall that the μA741 has $I_1 = 10\ \mu A$ and $C_1 = 30$ pF, so we calculate:

$$\left.\frac{dv_0}{dt}\right|_{\max} = \frac{2 \times 10^{-5}}{30 \times 10^{-12}} = 0.67\ \frac{V}{\mu s} \tag{19}$$

which agrees with measured values.

The large and small signal behavior of the op amp can be usefully related by combining (15) for ω_u with (18). The slew rate becomes

$$\left.\frac{dv_0}{dt}\right|_{\max} = \frac{2\omega_u I_1}{g_{m1}}. \tag{20}$$

Equation (20) is a general and very useful relationship. It shows that, for a given unity-gain frequency, ω_u, the slew rate is determined entirely by just the ratio of first stage operating current to first stage transconductance, I_1/g_{m1}. Recall that ω_u is set at the point where excess phase begins to build up, and this point is determined largely by technology rather than circuit limitations. Thus, the only effective means available to the circuit designer for increasing op amp slew rate is to *decrease* the ratio of first stage transconductance to operating current, g_{m1}/I_1.

B. Slew Limiting for Simple Bipolar Input Stage

The significance of (20) is best seen by considering the specific case of a simple differential bipolar input as in Fig. 1. For this circuit, the first stage transconductance (for $\alpha_1 = 1$) is[1]

$$g_{m1} = qI_1/kT \tag{21}$$

so that

$$\frac{g_{m1}}{I_1} = q/kT. \tag{22}$$

Using this in (20), the maximum bipolar slew rate is

$$\left.\frac{dv_0}{dt}\right|_{\max} = 2\omega_u \frac{kT}{q}. \tag{23}$$

This provides us with the general (and somewhat dismal) conclusion that slew rate in an op amp with a simple bipolar input stage is dependent only upon the unity gain corner and fundamental constants. Slew rate can be increased only by increasing the unity gain corner, which we have noted is generally difficult to do. As a demonstration of the severity of this limit, imagine an op amp using highly advanced technology and clever design, which might have a stable unity gain frequency of 100 MHz. Equation (23) predicts that the slew rate for this advanced device is only

$$\left.\frac{dv_0}{dt}\right|_{\max} = 33\ \frac{V}{\mu s} \tag{24}$$

which is good, but hardly impressive when compared with the difficulty of building a 100-MHz op amp.[2] But, there are some ways to get around this limit as we shall see shortly.

C. Power Bandwidth

Our intuition regarding slew rate will be enhanced somewhat if we relate it to a term called "power bandwidth." Power bandwidth is defined as the maximum frequency at which full output swing (usually 10 V peak) can be obtained without distortion. For a sinusoidal output voltage $v_0(t) = V_p \sin \omega t$, the rate of change of output, or slew rate, required to reproduce the output is

$$\frac{dv_0}{dt} = \omega V_p \cos \omega t. \tag{25}$$

This has a maximum when $\cos \omega t = 1$ giving

$$\left.\frac{dv_0}{dt}\right|_{\max} = \omega V_p, \tag{26}$$

so the highest frequency that can be reproduced without slew limiting, $\omega_{\max}$ (power bandwidth) is

$$\omega_{\max} = \frac{1}{V_p}\left.\frac{dv_0}{dt}\right|_{\max}. \tag{27}$$

Thus, power bandwidth and slew rate are directly related by the inverse of the peak of the sine wave V_p. Fig. 13 shows the severe distortion of the output sine wave which results if one attempts to amplify a sine wave of frequency $\omega > \omega_{\max}$.

Some numbers illustrate typical op amp limits. For a μA741 or LM101 having a maximum slew rate of 0.67 V/μs, (27) gives a maximum frequency for an undistorted 10-V peak output of

$$f_{\max} = \frac{\omega_{\max}}{2\pi} = 10.7\ \text{kHz}, \tag{28}$$

which is a quite modest frequency considering the much higher frequency small signal capabilities of these devices. Even the highly advanced 100-MHz amplifier considered above has a 10-V power bandwidth of only 0.5 MHz, so it is apparent that a need exists for finding ways to improve slew rate.

D. Techniques for Increasing Slew Rate

1) Resistive Enhancement of the Bipolar Stage: Equation (20) indicates that slew rate can be improved if we reduce first stage g_{m1}/I_1. One of the most effective ways

[1] Note that (21) applies only to the simple differential input stage of Fig. 12. For compound input stages as in the LM101 or μA741, g_{m1} is half that in (21), and the slew rate in (23) is doubled.

[2] We assume in all of these calculations that C_c is made large enough so that the amplifier has less than 180° phase lag at ω_u, thus making the amplifier stable for unity closed-loop gain. For higher gains one can of course reduce C_c (if the IC allows external compensation) and increase the slew rate according to (18).

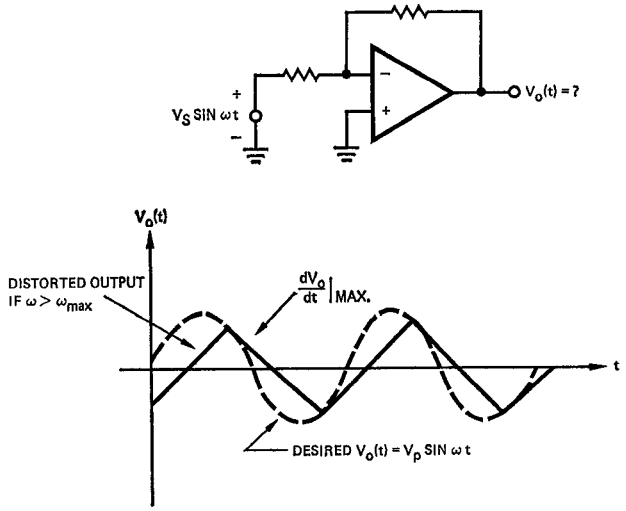


Fig. 13. Slew limiting effects on output sinewave that occur if frequency is greater than power bandwidth, ω_{max}. The onset of slew limiting occurs very suddenly as ω reaches ω_{max}. No distortion occurs below ω_{max}, while almost complete triangularization occurs at frequencies just slightly above ω_{max}.

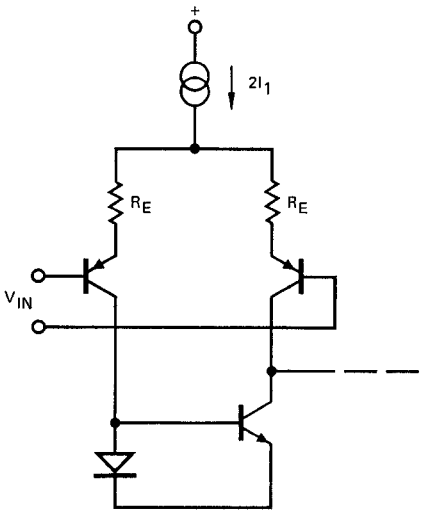


Fig. 14. Resistive degeneration used to provide slew rate enhancement according to (29).

of doing this is shown in Fig. 14, where simple resistive emitter degeneration has been added to the input differential amplifier [8]. With this change, the g_{m1}/I_1 drops to

$$\frac{g_{m1}}{I_1} = \frac{38.5}{1 + R_E I_1/26 \text{ mV}} \tag{29}$$

at 25°C.

The quantity g_{m1}/I_1 is seen to decrease rapidly with added R_E as soon as the voltage drop across R_E exceeds 26 mV. The LM118 is a good example of a bipolar amplifier which uses emitter degeneration to enhance slew rate [4]. This device uses emitter resistors to produce $R_E I_1 = 500$ mV, and has a unity gain corner of 16 MHz. Equations (20) and (29) then predict a maximum inverting slew rate of

$$\frac{dv_0}{dt}\bigg|_{max} = 2\omega_u \frac{I_1}{g_{m1}} = \omega_u = 100 \frac{\text{V}}{\mu\text{s}} \tag{30}$$

which is a twenty-fold improvement over a similar amplifier without emitter resistors.

A penalty is paid in using resistive slew enhancement, however. The two added emitter resistors must match extremely well or they add voltage offset and drift to the input. In the LM118, for example, the added emitter R's have values of 2.0 kΩ each and these contribute an input offset of 1 mV for each 4 Ω (0.2 percent) of mismatch. The thermal noise of the resistors also unavoidably degrades noise performance.

2) Slew Rate in the FET Input Op Amp: The FET (JFET or MOSFET) has a considerably lower transconductance than a bipolar device operating at the same current. While this is normally considered a drawback of the FET, we note that this "poor" behavior is in fact highly desirable in applications to fast amplifiers. To illustrate, the drain current for a JFET in the "current saturation" region can be approximated by

$$I_D \cong I_{DSS}(V_{GS}/V_T - 1)^2 \tag{31}$$

where

I_{DSS} the drain current for $V_{GS} = 0$,
V_{GS} the gate source voltage having positive polarity for forward gate-diode bias,
V_T the threshold voltage having negative polarity for JFET's.

The small-signal transconductance is obtained from (31) as $g_m = \partial I_D/\partial V_G$. Dividing by I_D and simplifying, the ratio g_m/I_D for a JFET is

$$\frac{g_m}{I_D} \cong \frac{2}{(V_{GS} - V_T)} = \frac{2}{-V_T}\left[\frac{I_{DSS}}{I_D}\right]^{1/2}. \tag{32}$$

Maximum amplifier slew rate occurs for minimum g_m/I_D and, from (32), this occurs when I_D (or V_{GS}) is maximum. Normally it is impractical to forward bias the gate junction so a practical minimum occurs for (32) when $V_{GS} \cong 0$ V and $I_D \cong I_{DSS}$. Then

$$\frac{g_m}{I_D}\bigg|_{min} \cong -\frac{2}{V_T}. \tag{33}$$

Comparing (33) with the analogous bipolar expression, (22), we find from (20) that the JFET slew rate is greater than bipolar by the factor

$$\frac{\text{JFET slew}}{\text{bipolar slew}} \approx \frac{-V_T}{2kT/q}\frac{\omega_{uf}}{\omega_{ub}} \tag{34}$$

where ω_{uf} and ω_{ub} are unity-gain bandwidths for JFET and bipolar amps, respectively. Typical JFET thresholds are around 2 V ($V_T = -2$ V), so for equal bandwidths (34) tells us that a JFET-input op amp is about forty times faster than a simple bipolar input. Further, if

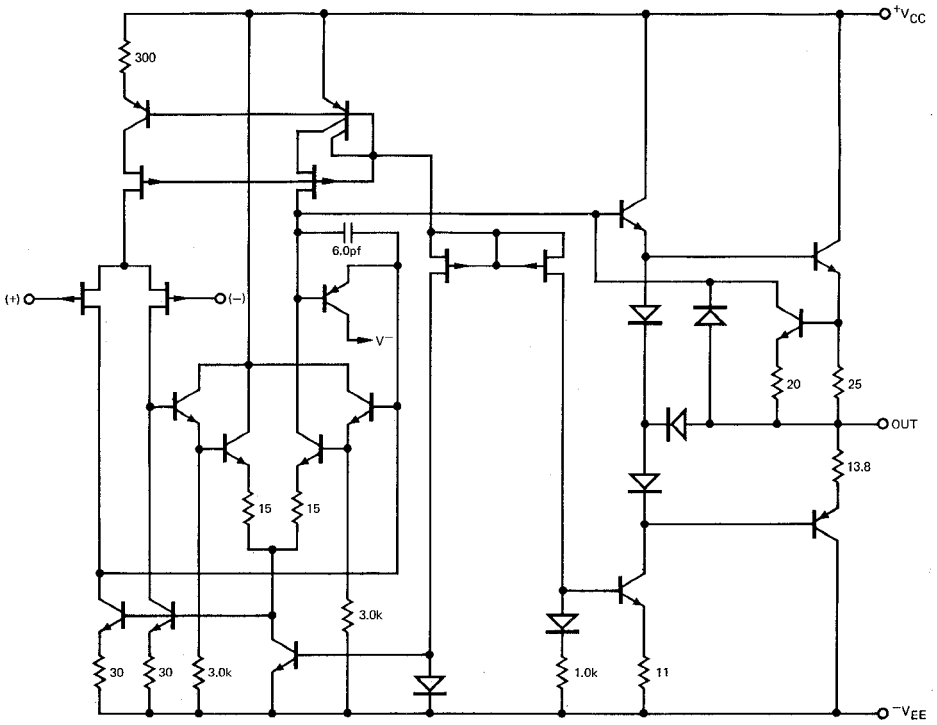


Fig. 15. Monolithic operational amplifier employing compatible p-channel JFET's on the same chip with normal bipolar components.

JFET's are properly substituted for the slow p-n-p's in a monolithic design, bandwidth improvements by at least a factor of ten are obtainable. JFET-input op amps, therefore, offer slew rate improvements by better than two orders of magnitude when compared with the conventional IC op amp. (Similar improvements are possible with MOSFET-input amplifiers.) This characteristic, coupled with picoamp input currents and reasonable offset and drift, make the JFET-input op amp a very desirable alternative to conventional bipolar designs.

As an example, Fig. 15, illustrates one design for an op amp employing compatible p-channel JFET's on the same chip with the normal bipolar components. This circuit exhibits a unity gain corner of 10 MHz, a 33 V/μs slew rate, an input current of 10 pA and an offset voltage and drift of 3 mV and 3 μV/°C [6]. Bandwidth and slew rate are thus improved over simple IC bipolar by factors of 10 and 100, respectively. At the same time input currents are smaller by about 10^3, and offset voltages and drifts are comparable to or better than slew enhanced bipolar circuits.

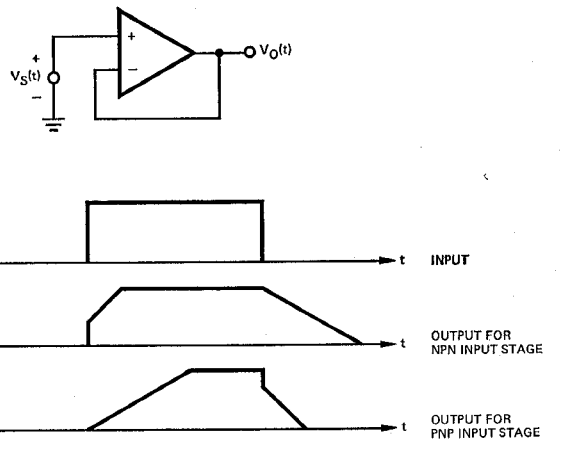


Fig. 16. Large signal response of the voltage follower. For an op amp with simple n-p-n input stage we get the waveform $v_{on}(t)$, which exhibits a step slew "enhancement" on the positive going output, and a slew "degradation" on the negative going output. For a p-n-p input stage, these effects are reversed as shown by $v_{op}(t)$.

V. Second-Order Effects: Voltage Follower Slew Behavior

If the op amp is operated in the noninverting mode and driven by a large fast rising input, the output exhibits the characteristic waveform in Fig. 16. As shown, this waveform does not have the simple symmetrical slew characteristic of the inverter. In one direction, the output has a fast step (slew "enhancement") followed by a "normal" inverter slewing response. In the other direction, it suffers a slew "degradation" or reduced slope when compared with the inverter slewing response.

We will first study slew degradation in the voltage follower connection, since this represents a worst case slewing condition for the op amp. A model which adequately represents the follower under large-signal conditions can be obtained from that in Fig. 12 by simply

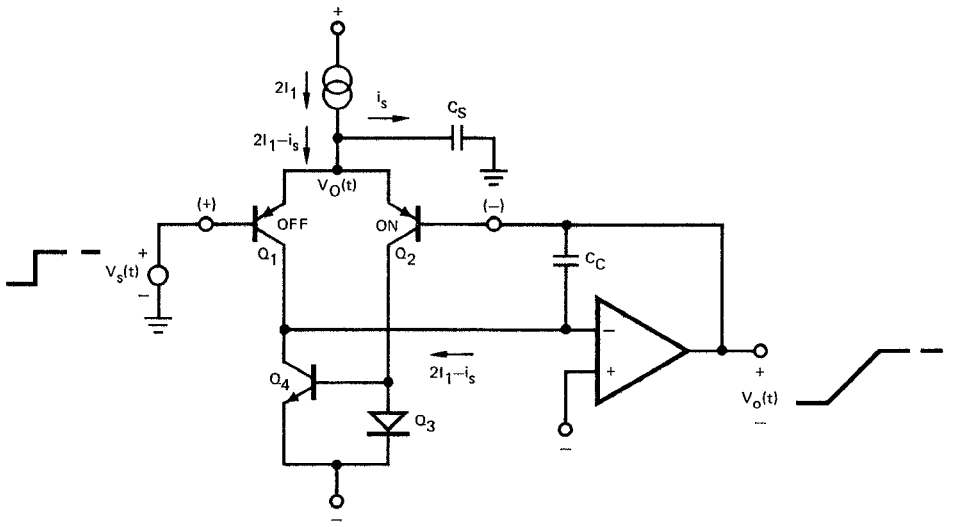


Fig. 17. Circuit used for calculation of slew "degradation" in the voltage follower. The degradation is caused by the capacitor C_s, which robs current from the tail, $2I_1$, thereby preventing the full $2I_1$ from slewing C_c.

tying the output to the inverting input, and including a capacitor C_s to account for the presence of any capacitance at the output of the first stage (tail) current source, see Fig. 17. This "input tail" capacitance is important in the voltage follower because the input stage undergoes rapid large-signal excursions in this connection, and the charging currents in C_s can be quite large.

Circuit behavior can be understood by analyzing Fig. 17 as follows. The large-signal input step causes Q_1 to turn OFF, leaving Q_2 to operate as an emitter follower with its emitter tracking the variational output voltage, $v_0(t)$. It is seen that $v_0(t)$ is essentially the voltage appearing across both C_s and C_c so we can write

$$\frac{dv_0}{dt} \cong \frac{i_c}{C_c} \cong \frac{i_s}{C_s}. \tag{35}$$

Noting that $i_c \cong 2I_1 - i_s$ (unity α's assumed), (35) can be solved for i_s:

$$i_s \cong \frac{2I_1}{1 + C_c/C_s} \tag{36}$$

which is seen to be constant with time. The degraded voltage follower slew rate is then obtained by substituting (36) into (35):

$$\left.\frac{dv_0}{dt}\right|_{\text{degr}} \cong \frac{i_s}{C_s} \cong \frac{2I_1}{C_c + C_s}. \tag{37}$$

Comparing (37) with the slew rate for the inverter, (18), it is seen that the slew rate is reduced by the simple factor $1/(1 + C_s/C_c)$. As long as the input tail capacitance C_s is small compared with the compensation capacitor C_c, little degradation occurs. In high speed amplifiers where C_c is small, degradation becomes quite noticeable, and one is encouraged to develop circuits with small C_s.

As an example, consider the relatively fast LM118 which has $C_c \cong 5$ pF, $C_s \cong 2$ pF, $2I_1 = 500$ μA. The calculated inverter slew rate is $2I_1/C_c \cong 100$ V/μs, and the degraded voltage follower slew rate is found to be $2I_1/(C_c + C_s) \cong 70$ V/μs. The slew degradation is seen to be about 30 percent, which is very significant. By contrast, a μA741 has $C_c \cong 30$ pF and $C_s \cong 4$ pF which results in a degradation of less than 12 percent.

The slew "enhanced" waveform can be similarly predicted from a simplified model. By reversing the polarity of the input and initially assuming a finite slope on the input step, the enhanced follower is analyzed, as shown in Fig. 18. Noting that Q_1 is assumed to be turned ON by the step input and Q_2 is OFF, the output voltage becomes

$$v_0(t) \cong -\frac{1}{C_c}\int_0^t [2I_1 + i_S(t)]\, dt. \tag{38}$$

The voltage at the emitter of Q_1 is essentially the same as the input voltage, $v_i(t)$, so the current in the "tail" capacitance C_s is

$$i_s(t) \cong C_s \frac{dv_i}{dt} \cong \frac{C_s V_{ip}}{t_1} \qquad 0 < t < t_1. \tag{39}$$

Combining (38) and (39), $v_0(t)$ is

$$-v_0(t) \cong \frac{1}{C_c}\int_0^t 2I_1\, dt + \frac{1}{C_c}\int_0^{t_1} \frac{C_s V_{ip}}{t_1}\, dt \tag{40}$$

or

$$-v_0(t) \cong \frac{C_s}{C_c} V_{ip} + \frac{2I_1 t}{C_c}. \tag{41}$$

Equation (41) tells us that the output has an initial negative step which is the fraction C_s/C_c of the input voltage. This is followed by a normal slewing response, in which the slew rate is identical to that of the inverter, see (18). This response is illustrated in Fig. 18.

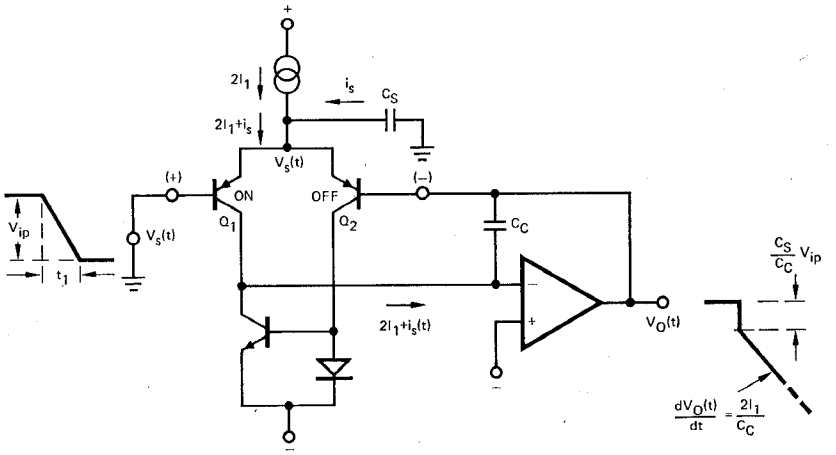


Fig. 18. Circuit used for calculation of slew "enhancement" in the voltage follower. The fast falling input causes a step output followed by a normal slew response as shown.

VI. Limitations on Bandwidth

In earlier sections, all bandlimiting effects were ignored except that of the compensation capacitor, C_c. The unity-gain frequency was set at a point sufficiently low so that negligible excess phase (over the 90° from the dominant pole) due to second-order (high frequency) poles had built up. In this section the major second-order poles which contribute to bandlimiting in the op amp are identified.

A. The Input Stage: p-n-p's, the Mirror Pole, and the Tail Pole

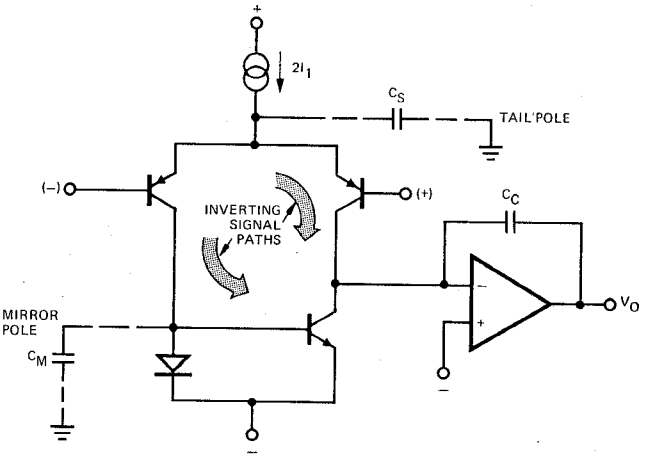
For many years it was popular to identify the lateral p-n-p's (which have f_t's $\cong$ 3 MHz) as the single dominant source of bandlimiting in the IC op amp. It is quite true that the p-n-p's do contribute significant excess phase to the amplifier, but it is not true that they are the sole contributor to excess phase [9]. In the input stage, alone, there is at least one other important pole, as illustrated in Fig. 19(a). For the simple differential input stage driving a differential-to-single ended converter ("mirror" circuit), it is seen that the inverting signal (which is the feedback signal) follows two paths, one of which passes through the capacitance C_s, and the other through C_m. These capacitances combine with the dynamic resistances at their nodes to form poles designated the mirror pole at

$$p_m \cong \frac{I_1}{C_m kT/q}, \tag{42}$$

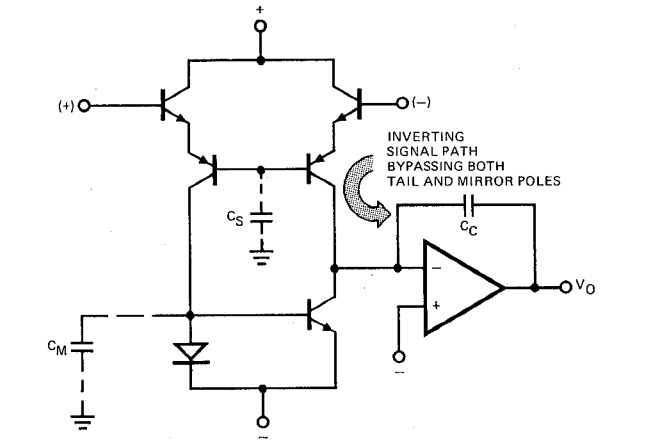
and the tail pole at

$$p_t \cong \frac{2I_1}{C_s kT/q}. \tag{43}$$

It can be seen that if one attempts to operate the first stage at too low a current, these poles will bandlimit the amplifier. If, for example, we choose $I_1 = 1$ μA, and assume $C_m \cong 7$ pF (consisting of 4-pF isolation ca-



(a)



(b)

Fig. 19. (a) Circuit showing "mirror" pole due to C_m and "tail" pole due to C_s. One component of the signal due to an inverting input must pass through either the mirror or tail poles. (b) Alternate circuit to Fig. 19(a) (LM101, μA741) which has less excess phase. Reason is that half the inverting signal path need not pass through the mirror pole or the tail pole.

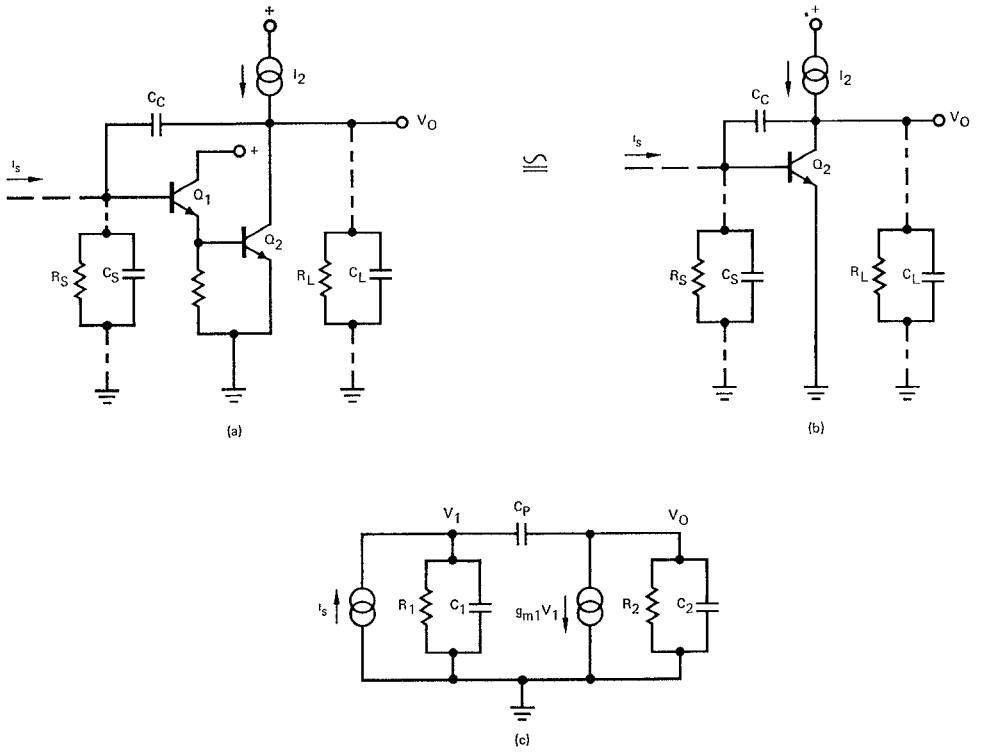


Fig. 20. Simplification of second stage used for pole-splitting analysis. (a) Complete second stage with input stage and output stage loading represented by R_s, C_s, and R_L, C_L, respectively. (b) Emitter follower ignored to simplify analysis. (c) Hybrid π model substituted for transistor in (b). Source and load impedances are absorbed into model with the total impedances represented by R_1, C_1, and R_2, C_2. Transistor base resistance is ignored and C_p includes both C_c and transistor collector-base capacitance.

pacitance and 3-pF emitter transition capacitance) and $C_s \cong 4$ pF,[3] $p_m/2\pi \cong 0.9$ MHz and $p_t/2\pi \cong 3$ MHz either of which would seriously degrade the phase margin of a 1-MHz amplifier.

If a design is chosen in which either the tail pole or the mirror pole is absent (or unimportant), the remaining pole rolls off only half the signal, so the overall response contains a pole-zero pair separated by one octave. Such a pair generally has a small effect on amplifier response unless it occurs near ω_u, where it can degrade phase margin by as much as 20°.

It is interesting to note that the compound input stage of the classical LM101 (and μA741) has a distinct advantage over the simple differential stage, as seen in Fig. 19(b). This circuit is noninverting across each half, thus it provides a path in which half the feedback signal bypasses both the mirror and tail poles.

[3] C_s can have a wide range of values depending on circuit configuration. It is largest for n-p-n input differential amps since the current source has a collector-substrate capacitance ($C_s \cong$ 3–4 pF) at its output. For p-n-p input stages it can be as small as 1–2 pF.

B. The Second Stage: Pole Splitting

The assumption was made in Section III that the second stage behaved as an ideal integrator having a single dominant pole response. In practice, one must take care in designing the second stage or second-order poles can cause significant deviation from the expected response. Considerable insight into the basic way in which the second stage operates can be obtained by performing a small-signal analysis on a simplified version of the circuit as shown in Fig. 20 [10]. A straightforward two-node analysis of Fig. 20(c) produces the following expression for v_{out}.

$$\frac{v_{out}}{i_s} = \frac{-g_m R_1 R_2 (1 - sC_p/g_m)}{1 + s[R_1(C_1 + C_p) + R_2(C_2 + C_p) + g_m R_1 R_2 C_p] + s^2 R_1 R_2 [C_1 C_2 + C_p(C_1 + C_2)]}. \tag{44}$$

The denominator of (44) can be approximately factored under conditions that its two poles are widely separated. Fortunately, the poles are, in fact, widely separated under most normal operating conditions. Therefore, one can assume that the denominator of (44) has the form

$$D(s) = (1 + s/p_1)(1 + s/p_2) = 1 + s(1/p_1 + 1/p_2) + s^2/p_1 p_2. \tag{45}$$

With the assumption that p_1 is the dominant pole and

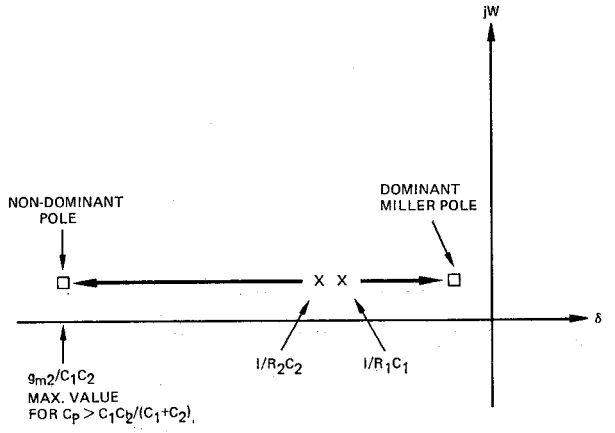


Fig. 21. Pole migration for second stage employing "pole-splitting" compensation. Plot is shown for increasing C_p and it is noted that the nondominant pole reaches a maximum value for large C_p.

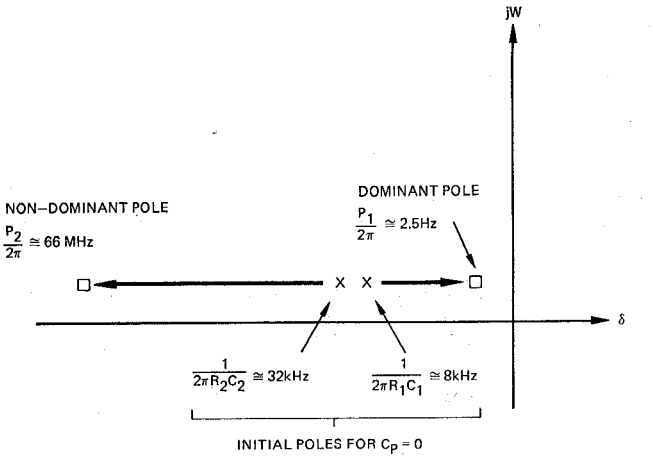


Fig. 22. Example of pole-splitting compensation in the μA741 op amp. Values used in (48) and (49) are: $g_{m2} = 1/87\ \Omega$, $C_p = 30$ pF, $C_1 \cong C_2 = 10$ pF, $R_1 = 1.7$ MΩ, $R_2 = 100$ kΩ.

p_2 is nondominant, i.e., $p_1 \ll p_2$, (45) becomes

$$D(s) \cong 1 + s/p_1 + s^2/p_1p_2. \tag{46}$$

Equating coefficients of s in (44) and (46), the dominant pole p_1 is found directly:

$$p_1 \cong \frac{1}{R_1(C_1 + C_p) + R_2(C_2 + C_p) + g_mR_1R_2C_p} \tag{47}$$

$$\cong \frac{1}{g_mR_1R_2C_p}. \tag{48}$$

The latter approximation, (48), normally introduces little error, because the g_m term is much larger than the other two. We note at this point that p_1, which represents the dominant pole of the amplifier, is due simply to the familiar Miller-multiplied feedback capacitance $g_mR_2C_p$ combined with input node resistance, R_1. The nondominant pole p_2 is found similarly by equating s^2 coefficients in (44) and (46) to get p_1p_2, and dividing by p_1 from (48). The result is

$$p_2 \cong \frac{g_mC_p}{C_1C_2 + C_p(C_1 + C_2)}. \tag{49}$$

Several interesting things can be seen in examining (48) and (49). First, we note that p_1 is inversely proportional to g_m (and C_p), while p_2 is directly dependent on g_m (and C_p). Thus, as either C_p or transistor gain are increased, the dominant pole decreases and the nondominant pole increases. The poles p_1 and p_2 are being "split-apart" by the increased coupling action in a kind of inverse root locus plot.

This *pole-splitting* action is shown in Fig. 21, where pole migration is plotted for C_p increasing from 0 to a large value. Fig. 22 further illustrates the action by giving specific pole positions for the μA741 op amp. It is seen that the initial poles (for $C_p = 0$) are both in the tens of kilohertz region and these are predicted to reach 2.5 Hz ($p_1/2\pi$) and 66 MHz ($p_2/2\pi$) after compensation is applied. This result is, of course, highly satisfactory since the second stage now has a single dominant pole effective over a wide frequency band.

C. Failure of Pole Splitting

There are several situations in which the application of pole-splitting compensation may not result in a single dominant pole response. One common case occurs in very wide-band op amps where the pole-splitting capacitor is small. In this situation the nondominant pole given by (49) may not become broadbanded sufficiently so that it can be ignored. To illustrate, suppose we attempt to minimize power dissipation by running the second stage of an LM118 (which has a small-signal bandwidth of 16 MHz) at 0.1 mA. For this op amp $C_p = 5$ pF, $C_1 \cong C_2 \cong 10$ pF. From (49), the nondominant pole is

$$\frac{p_2}{2\pi} \cong 16\ \text{MHz} \tag{50}$$

which lies right at the unity-gain frequency. This pole alone would degrade phase margin by 45°, so it is clear that we need to bias the second stage with a collector current greater than 0.1 mA to obtain adequate g_m. Insufficient pole-splitting can therefore occur; but the cure is usually a simple increase in second stage g_m.

A second type of pole-splitting failure can occur, and it is often much more difficult to cope with. If, for example, one gets over-zealous in his attempt to broadband the nondominant pole, he soon discovers that other poles exist within the second stage which can cause difficulties. Consider a more exact equivalent circuit for the second stage of Fig. 20(a) as shown in Fig. 23. If the follower is biased at low currents or if C_p, Q_2 g_m, and/or r_x are high, the circuit can contain at least four important poles rather than the two considered in simple pole splitting. Under these conditions, we no longer have a response with just negative real poles as in Fig. 21, but observe a root locus of the sort shown in Fig. 24. It is seen in this case that the circuit contains a pair of com-

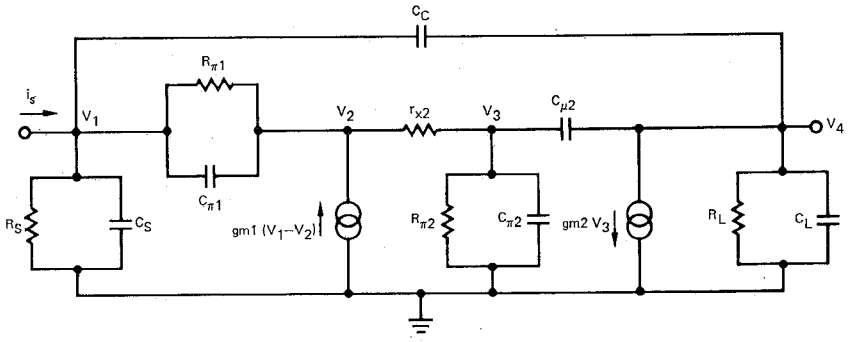


Fig. 23. More exact equivalent circuit for second stage of Fig. 20 (a) including a simplified π model for the emitter follower ($R\pi_1$, $C\pi_1$, g_{m1}) and a complete π for Q_2 (r_{x2}, $R\pi_2$, etc.).

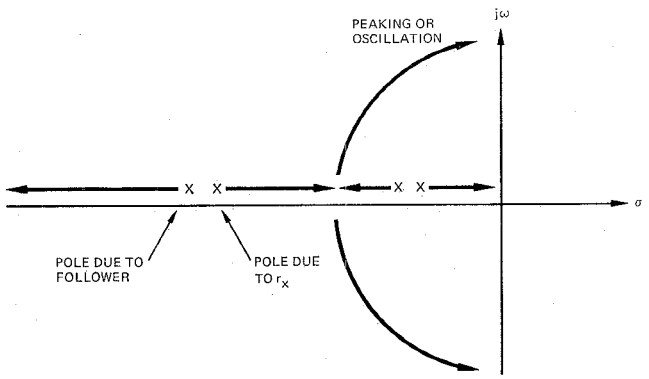


Fig. 24. Root locus for second stage illustrating failure of pole splitting due to high g_{m2}, r_{x2}, C_p, and/or low bias current in the emitter follower.

plex, possibly underdamped poles which, of course, can cause peaking or even oscillation. This effect occurs so commonly in the development of wide-band pole-split amplifiers that it has been (not fondly) dubbed "the second stage bump."

There are numerous ways to eliminate the "bump," but no single cure has been found which is effective in all situations. A direct hand analysis of Fig. 23 is possible, but the results are difficult to interpret. Computer analysis seems the best approach for this level of complexity, and numerous specific analyses have been made. The following is a list of circuit modifications that have been found effective in reducing the bump in the various studies: 1) reduce g_{m2}, r_{x2}, $C_{\mu 2}$, 2) add capacitance or a series RC network from the stage input to ground—this reduces the high frequency local feedback due to C_p, 3) pad capacitance at the output for similar reasons, 4) increase operating current of the follower, 5) reduce C_p, 6) use a higher f_t process.

D. Troubles in The Output Stage

Of all the circuitry in the modern IC op amp, the class-AB output stage probably remains the most troublesome. None of the stages in use today behave as well as one might desire when stressed under worst case conditions. To illustrate, one of the most commonly used output stages is shown in Fig. 2(b). The p-n-p's in this circuit are "substrate" p-n-p's having low current f_t's of around 20 MHz. Unfortunately, both β_0 and f_t begin to fall off rapidly at quite low current densities, so as one begins to sink just a few milliamps in the circuit, phase margin troubles can develop. The worst effect occurs when the amplifier is operated with a large capacitive load (>100 pF) while sinking high currents. As shown in Fig. 25, the load capacitance on the output follower causes it to have negative input conductance, while the driver follower can have an inductive output impedance. These elements combine with the capacitance at the interstage to generate the equivalent of a one-port oscillator. In a carefully designed circuit, oscillation is suppressed, but peaking (the "output bump") can occur in most amplifiers under appropriate conditions.

One new type of output circuit which does not use p-n-p's is shown in Fig. 26 [6]. This circuit employs compatible JFET's (or MOSFET's, see similar circuit in [11]) in a FET/bipolar quasi-complimentary output stage, which is insensitive to load capacitance. Unfortunately, this circuit is rather complex and employs extra process steps, so it does not appear to represent the cure for the very low cost op amps.

VII. The Gain Cell: Linear Large-Scale Integration

As the true limitations of the basic op amp are more fully understood, this knowledge can be applied to the development of more "optimum" amplifiers. There are, of course, many ways in which one might choose to optimize the device. We might, for example, attempt to maximize speed (bandwidth, slew rate, settling time) without sacrificing dc characteristics. The compatible JFET/bipolar amp of Fig. 15 represents such an effort. An alternate choice might be to design an amplifier having all of the performance features of the most widely used general purpose op amps (i.e., μA741, LM107, etc.), but having minimum possible die area. Such a pursuit is parallel to the efforts of digital large-scale integration (LSI) designers in their development of minimum area

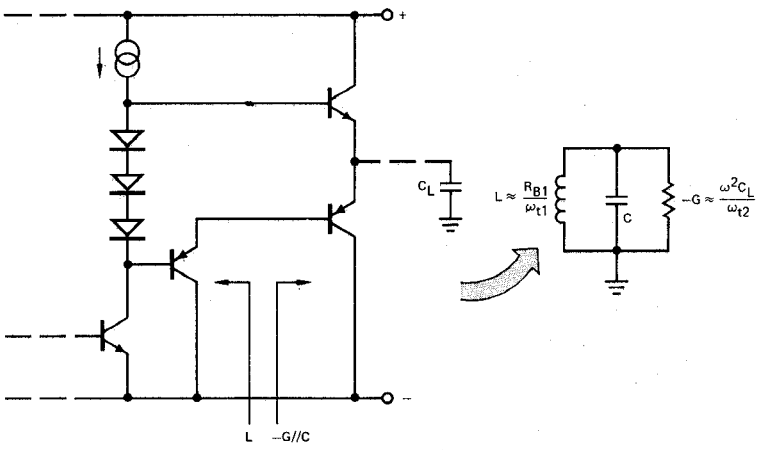


Fig. 25. Troubles in the conventional class-AB output stage of Fig. 2(b). The low f_t output p-n-p's interact with load capacitance to form the equivalent of a one-port oscillator.

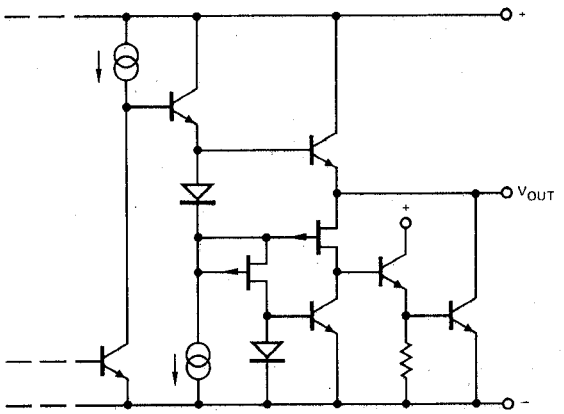


Fig. 26. The "BIFET" output stage employing JFET's and bipolar n-p-n's to eliminate sensitivity to load capacitance.

memory cells or gates. The object of such efforts, of course, is to develop lower cost devices which allow wide and highly economic usage.

In this section we briefly discuss certain aspects of the linear *gain cell*, a general purpose, internally compensated op amp having a die area which is significantly smaller than that of equivalent, present day, industry standard amplifiers.

A. Transconductance Reduction

The single largest area component in the internally compensated op amp is the compensation capacitor (about 30 pF, typically). A major interest in reducing amplifier die area, therefore, centers about finding ways in which this capacitor can be reduced in size. With this in mind, we find it useful to examine (15), which relates compensation capacitor size to two other parameters, unity gain corner frequency ω_u, and first stage transconductance g_{m1}. It is immediately apparent that for a fixed, predetermined unity gain corner (about $2\pi \times$ 1 MHz in our case), there is only one change that can be made to reduce the size of C_c: *the transconductance of the first stage must be reduced.* If we restrict our interest to simple bipolar input stages (for low cost), we recall the $g_{m1} = qI_1/kT$. Only by reducing I_1 can g_{m1} be reduced, and we earlier found in Section VI–A and Fig. 19(a) and (b) that I_1 cannot be reduced much without causing phase margin difficulties due to the mirror pole and the tail pole.

An alternate basic approach to g_m reduction is illustrated in Fig. 27 [12]. Here, a multiple collector p-n-p structure, which is easily fabricated in IC form, is used to split the collector current into two components, one component (the larger) of which is simply tied to ground, thereby "throwing away" a major portion of the transistor output current. The result is that the g_m of the transistor is reduced by the ratio of $1/(1 + n)$ (see Fig. 27), and the compensation capacitance can be reduced directly by the same factor. It might appear that the mirror pole would still cause difficulties since the current mirror becomes current starved in Fig. 27, but the effect is not as severe as might be expected. The

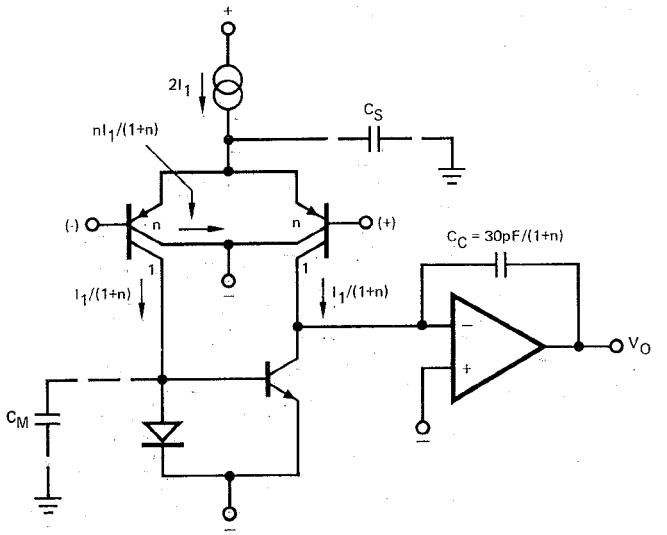


Fig. 27. Basic g_m reduction obtained by using split collector p-n-p's. C_c and area are reduced since $C_c = g_{m1}/\omega_u$.

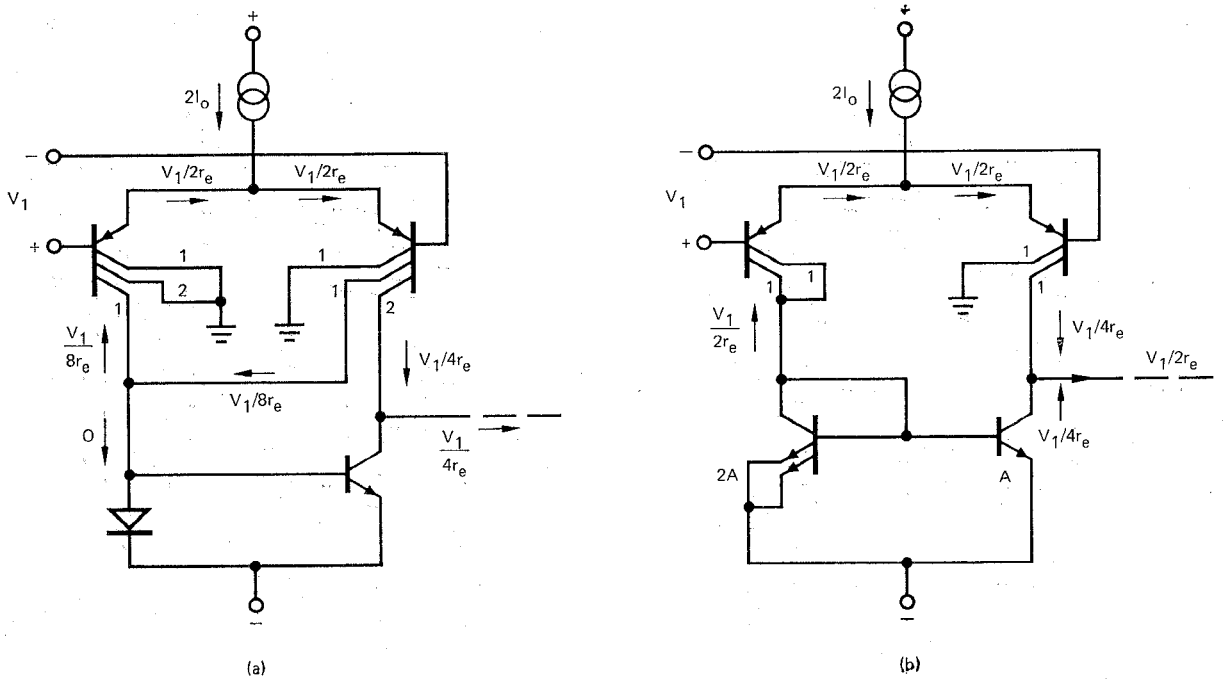


Fig. 28. Variations on g_m reduction. (a) Cross-coupled connection eliminates all ac current passing through the mirror, yet maintains dc balance. (b) This approach maintains high current on the diode side of the mirror, thereby broadbanding the mirror pole.

reason is that the inverting signal can now pass through the high current wide-band path, across the differential amp emitters and into the second stage, so at least half the signal current does not become bandlimited. This partial bandlimiting can be further reduced by using one of the circuits in Fig. 28(a) or (b).[4] In (a), the p-n-p collectors are cross coupled in such a way that the ac signal is cancelled in the mirror circuit, while dc remains completely balanced. Thus the mirror pole is virtually eliminated. The circuit does have a drawback, however, in that the uncorrellated noise currents coming from the two p-n-p's add rather than subtract at the input to the mirror, thereby degrading noise performance. The circuit in Fig. 28(b) does not have this defect, but requires care in matching p-n-p collector ratios to n-p-n

[4] The circuit in Fig. 28(a) is due to R. W. Russell and the variation in Fig. 28(b) was developed by D. W. Zobel.

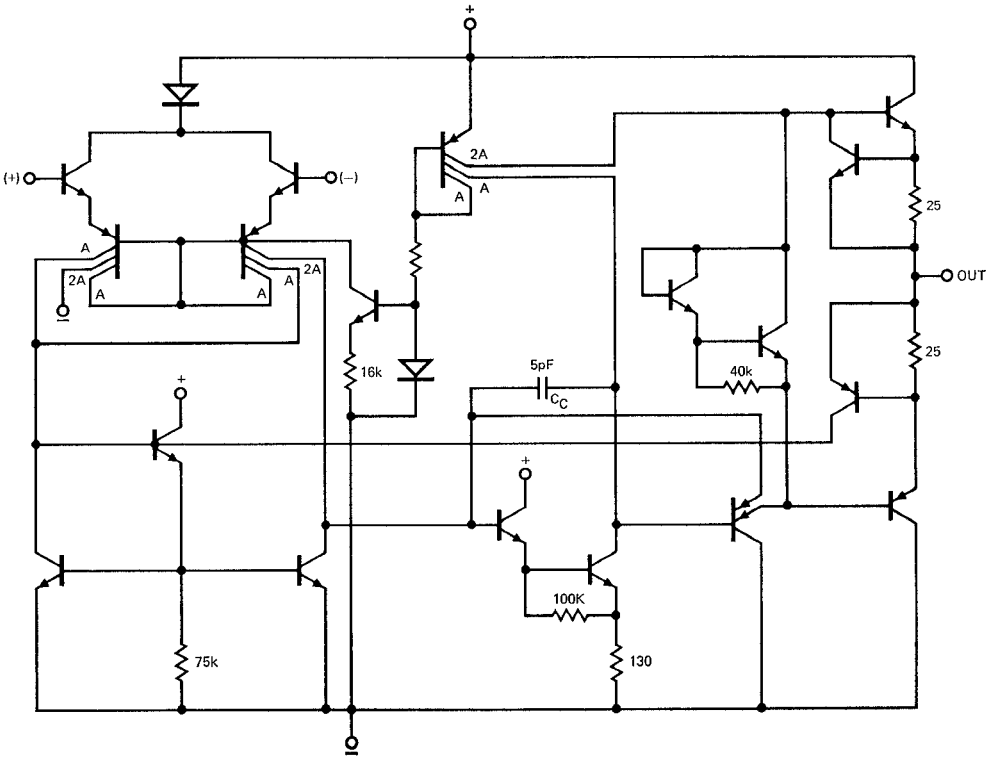


Fig. 29. Circuit for optimized gain cell which has been fabricated in one-fourth the die size of the equivalent μA741.

emitter areas. Otherwise offset and drift will degrade as one attempts to reduce g_m by large factors.

B. A Gain Cell Example

As one tries to make large reductions in die area for the gain cell, many factors must be considered in addition to novel circuit approaches. Of great importance are special layout/circuit techniques which combine a maximum number of components into minimum area.

In a good layout, for example, all resistors are combined into islands with transistors. If this is not possible initially, circuit and device changes are made to allow it. The resulting device geometries within the islands are further modified in shape to allow maximum "packing" of the islands. That is, when the layout is complete, the islands should have shapes which fit together as in a picture puzzle, with no waste of space. Further area reductions can be had by modifying the isolation process to one having minimum spacing between the isolation diffusion and adjacent p-regions.

An example of a gain cell which employs both circuit and layout optimization is shown in Fig. 29. This circuit uses the g_m reduction technique of Fig. 28(a) which results in a compensation capacitor size of only 5 pF rather than the normal 30 pF. The device achieves a full 1-MHz bandwidth, a 0.67-V/μs slew rate, a gain greater than 100 000, typical offset voltages less than 1 mV, and other characteristics normally associated with an LM107 or μA741. In quad form each amplifier requires an area of only 23 × 35 mils which is one-fourth the size of today's industry standard μA741 (typically 56 × 56 mils). This allows over 8000 possible gain cells to be fabricated on a single 3-inch wafer. Further, it appears quite feasible to fabricate larger arrays of gain cells, with six or eight on a single chip. Only packaging and applications questions need be resolved before pursuing such a step.

Acknowledgment

Many important contributions were made in the gain cell and FET/bipolar op amp areas by R. W. Russell. The author gratefully acknowledges his very competent efforts.

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James E. Solomon (S'57–M'61) was born in Boise, Idaho, on July 20, 1936. He received the B.S. and M.S. degrees in electrical engineering from the University of California, Berkeley, in 1958 and 1960, respectively.

In 1960 he joined the Motorola Systems Research Laboratory, Riverside, Calif., where he participated in the design of radar receivers, *S* band ECM equipment, missile control systems, wide-band and IF amplifiers. He transferred to the Semiconductor Products Division of Motorola, Phoenix, Ariz., in 1963, to do research in silicon microelectronics. From 1963 to 1971, he held the positions of Project Engineer, Manager of Linear Integrated Circuits R & D, and Manager for Consumer Integrated Circuits Development and Production. In 1971 he moved to National Semiconductor, Santa Clara, Calif., where he is presently responsible for linear standard product development and applications engineering. His efforts have resulted in the introduction of over 25 linear IC products, 17 issued patents, and the publication of numerous papers.

Mr. Solomon is a member of Eta Kappa Nu, Tau Beta Pi, and Phi Theta Kappa.

A Fast-Settling Monolithic Operational Amplifier Using Doublet Compression Techniques

RUSSELL J. APFEL AND PAUL R. GRAY, MEMBER, IEEE

Abstract—**A new high-speed monolithic operational amplifier is described which uses an improved feedforward circuit configuration to achieve a total acquisition time (slewing plus settling) of 650 ns with a 10-V input step without compromising dc performance or requiring costly nonstandard processing.**

I. Introduction

UNTIL recently, the poor frequency response of lateral p-n-p transistors in level shift circuits had seriously limited the bandwidth and slew rate obtainable in low cost, general purpose monolithic operational amplifiers. This limitation has been overcome in several recently reported operational amplifier circuits by including within the amplifier a parallel, ac coupled signal path around the p-n-p level shift stage which bypasses the stage at high frequencies. As a result, the unity-gain frequency of the amplifier is not limited by excess phase shift in the lateral p-n-p stage, and stable unity-gain bandwidths of up to 50 MHz [1] and slew rates of up to 120 V/μs [2] have been achieved in low cost amplifiers fabricated with a conventional bipolar IC process.

While feedforward techniques have yielded great improvements in stable bandwidth and slew rate, the improvement in amplifier settling time to high accuracies has not been correspondingly great. The settling time parameter is of great importance in certain classes of applications such as analog data acquisition and conversion systems [3]. The relatively poor settling time performance of these amplifiers results in part from imprecise cancellation of the pole associated with the rolloff of the p-n-p level shift stage, and the zero associated with the ac coupled feedforward stage, giving nonuniform open-loop response [4]. This paper will describe a monolithic operational amplifier which uses an improved feedforward technique to achieve a uniform open-loop frequency response, a total acquisition time (slewing plus settling) of 650 ns to 0.01 percent with a 10-V input step, and dc performance which is superior to most general-purpose operational amplifiers [5].

In Section II, the effects of pole-zero pairs in the open-loop frequency response on settling time in operational amplifiers are discussed. In Section III, an improved feedforward level shift configuration is described, and in Section IV the complete amplifier is described and experimental results presented.

Manuscript received May 31, 1974; revised August 1, 1974. This paper was presented at the International Solid-State Circuits Conference, Philadelphia, Pa., February 1974.

R. J. Apfel is with Fairchild Semiconductor, Mountain View, Calif. 94040.

P. R. Gray is with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, Calif. 94720.