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Andreas Moser joined the IBM Zurich Research Laboratory, Rüschlikon, Switzerland, in 1959, where he first worked in the field of thin magnetic-film memories. In 1966, work on applications of the metal-semiconductor field-effect transistor (MESFET) started in the Zurich Laboratory with special emphasis on the device characterization. Later, he was engaged in the development of high packing density MESFET memory cells and in high-speed GaAs, 1 μm gate length, normally off-type Schottky-barrier FET logic. In 1979, work on the characterization of nonvolatile memory effects in GaAs Schottky diodes was started. Since 1974, he has been involved in Josephson efforts at the Zurich Laboratory, where he is responsible for the memory logic circuitry and for the chip designs.

Bipolar Transistor Design for Optimized Power-Delay Logic Circuits

D. D. TANG AND PAUL M. SOLOMON

Abstract—The optimization of the vertical structure of bipolar transistors in LSI circuits is described in this paper. This design optimization scheme provides a procedure for tailoring the impurity doping profile of the transistor so that the performance of the logic circuit can be optimized at a specific power dissipation level and a given lithographic line width. It will be shown that the condition of the optimized circuit performance dictates a set of relationships between the transistor structure, the logic voltage swing, and the value of the circuit elements. This paper further discusses the relation between the circuit properties and the transistor size, which becomes smaller as the lithography advances. It is concluded that as the horizontal dimensions are reduced, the vertical dimension of the transistor must be reduced, the impurity density increased, and the current density increased in order to increase the circuit speed. A simple relationship between the lithographic line width and the vertical structure is given which enables one to predict the power-speed performance for the reduced structure.

I. Introduction

In THE past, bipolar transistor logic circuits were analyzed. Many generalized circuit design and optimization schemes and computer programs are published [1], [2]. However, in practice, the circuit design is frequently separated from the transistor design. Starting from the model of a given transistor structure, the circuit is designed by varying the circuit elements until the best circuit performance is obtained. The switching speed of the bipolar gates follows the constant power–delay line at the low power dissipation level. The switching speed reaches a maximum at a particular power dissipation level, and then decreases as the power level further increases. Frequently, the maximum speed occurs at a power level higher than the power dissipation capability of the chip. As the integration level of the integrated logic circuit increases, this problem becomes progressively serious.

It is the purpose of this paper to explore the possibility of incorporating the circuit performance information into the transistor design. The transistor structure is "synthesized" in such a way that a practical maximum speed will be achieved at a preselected power level or, more specifically, the collector current of the transistor.

It will be shown that:

1) the condition of optimized circuit performance at a given power level generally dictates the relationship between the device parameters.

2) there exists a simple procedure to synthesize the transistor structure which is optimized to the power–delay performance of the circuit.

In addition, we will discuss the performance of the bipolar circuit when the transistor size is reduced and under the conditions that: 1) the total power density per transistor is maintained relatively unchanged, and 2) the logic circuit remains at the maximum speed operating point. We will show that a coordinated shrinkage in the device structure can lead to a predictable bipolar logic gate performance.

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The authors are with the IBM T. J. Watson Research Center, Yorktown Heights, NY 10598.

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II. Relationship Between the Device Parameters and the Circuit Parameters

The logic circuit gate delay can be computed either with the numerical method or analytically [3]-[5]. The analytical delay equation is basically obtained from the differential equations that describe the node voltage or branch current of the circuit, which are reduced to lower order or simply reduced to the first order. Therefore, the gate delay can be analytically expressed as the sum of the RC time constants, each weighed by a constant determined by the circuit topology. The resistance includes load resistors and the resistance in the transistor equivalent circuit, and C includes load capacitors and the capacitors in the transistor equivalent circuit. However, the analytical delay equation derived from the above method usually has a limited accuracy. With the advent of the computer simulation technique, the delay equation of a logic gate can actually be derived from the sensitivity of the gate delay to the device parameters [6], [7]. This is more accurate over a given parameter range (about a factor of four); however, it lacks the insight of the analytical method. In the following section, a delay equation for the ECL logic gate, derived numerically, is presented as an example. This delay equation will subsequently be used in designing the transistor vertical profile for a transistor whose layout is shown in Fig. 1(a). The transistor is laid down with the minimum emitter stripe width obtainable from a given lithography. With the advent of the self-alignment [8] fabrication technology, the emitter-to-base distance is reduced to about 0.5 μm. This reduction of the emitter-base contact distance reduces the extrinsic base resistance to a value much less than the intrinsic base resistance. The collector area is also minimal for a given emitter size. Fully recessed oxide further cuts down the collector and the substrate capacitances. The equivalent circuit of the transistor is shown in Fig. 1(b).

A. The Relation Between the Delay of the ECL Gate and the Device-Circuit Parameters

The delay equation of the ECL gate shown in Fig. 1(c) obtained from the delay sensitivity of the transistor parameters is given as

$$T_d = k_1 \times R_1 C_c + k_2 \times R_1 C_e + k_3 \times R_1 C_s + k_4 \times R_1 C_1 + k_5 \times \tau + k_6 \times R_{bi} C_c + k_7 \times R_{bi} C_d + k_8 \times R_{bx} C_d \tag{1}$$

where

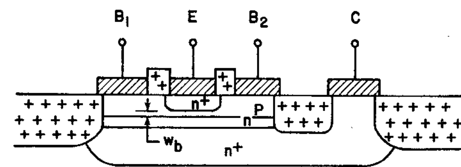
$$C_d = 2\tau I_c / V_1, \tag{2}$$

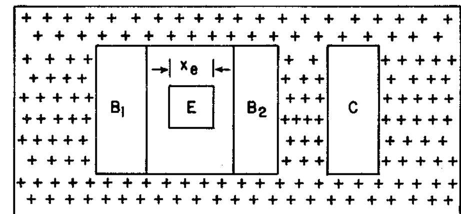
V_1 is the logic swing of the ECL gate, I_c is the collector current, τ is the charge storage time,

$$C_c = A_c (q \epsilon N_c / (2 V_{bi}))^{0.5} \tag{3}$$

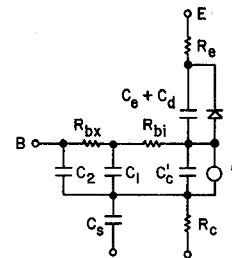
is the collector depletion capacitance, A_c is the collector area, q is the electron charge, ϵ is the dielectric constant, V_{bi} is the built-in voltage,

$$C_e = A_e (q^2 \epsilon a / (12 V_{bi}))^{0.66} \tag{4}$$

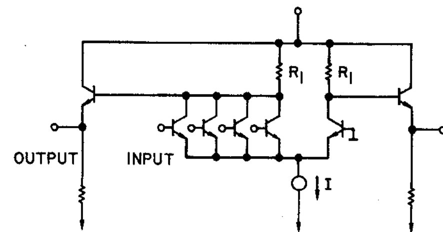




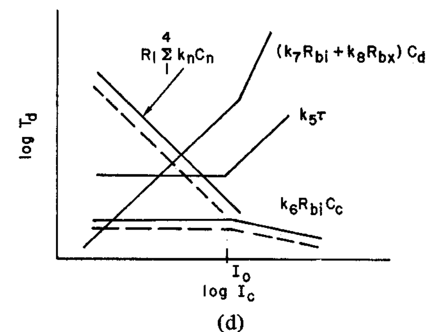
(a)



(b)



(c)



(d)

Fig. 1. (a) Bipolar transistor structure, side and top views; x_e is the emitter stripe width. (b) Equivalent circuit of the transistor, R_c and R_e are small and neglected in subsequent calculation. (c) ECL circuit topology; note that emitter-follower is included. (d) Asymptotic delay lines of the circuit.

is the emitter depletion capacitance, A_e is the emitter area, a is the slope of the emitter profile, C_1 is the circuit load capacitance, the C_s is the substrate capacitance,

$$R_1 = V_1 / I_c \tag{5}$$

is the resistance of the pull-up resistors at the collector, R_{bi} is the intrinsic base resistance, and R_{bx} is the extrinsic base

resistance. The k's are determined by the circuit topology. Also imbedded in the k's are Miller effects and voltage modulation of the depletion capacitances. The values of the k's are given in the Appendix. The charge control concept is applied to the diffusion capacitance. It is equal to the difference in stored charge between the on and off states of the transistor divided by the difference of the V_{be} between on and off states, which is equal to half the logic voltage swing of the ECL gate.

The asymptotic line of each term in the delay equation (1) is shown as a function of the collector current in Fig. 1(d). The terms related to R_1 decrease as current increases, since R_1 decreases as the current increases. This term also decreases as the area of the transistor decreases as a result of the reduction of the lithographic line width. The terms R_bC_d increase with current. These terms also decrease as the base width of the transistor decreases. At low injection, the terms $R_{bi}C_c$ and τ vary very slowly with current. At high injection [9], [10], τ increases and R_b decreases. The $R_{bi}C_c$ term rapidly becomes insignificant as the transistor size shrinks. Under most circumstances, the R_1C_c, τ, and $R_{bi}C_d$ terms in (1) are dominant. Equation (1) predicts an optimum operating point either when $k_1R_1C_c = k_7R_{bi}C_c$ for structures with large $R_{bi}C_d$ or when $k_1R_1C_c = k_5\tau$ otherwise. The first case gives a sharp minimum delay versus current, while the second gives a flat bottomed delay versus current. The optimum current is

$$I_c^2 = (k_1/k_7)(V_1^2C_c)/(\tau R_{bi}) \tag{6a}$$

when $R_{bi}C_d$ is large and

$$I_c = k_1 \times V_1C_c/(k_5 \times \tau) \tag{6b}$$

when τ is dominant. Thus, there exist relations between the transistor structure and the circuit parameters at the optimized power-delay operating point. Knowing this, one can tailor the transistor structure for a given operating current.

III. Interelation Between the Device Parameters for an Optimized ECL Gate Performance

A. The Relation Between the Charge Storage Time, the Collector Current, and the Collector Doping

The storage time is dominated by the stored charge in the neutral base region when the base width is wide (more than 0.5 μm). In such cases, the storage time is proportional to the square of the base width. As the base width is reduced to the 0.1 μm range, the mobile charge stored in the depletion region of the emitter-base junction [11] and in the depletion region of the base-collector cannot be neglected. Fig. 2(a) shows a simulated electron density in the base of an n-p-n transistor ($w_b = 0.13$ μm). This result is obtained from a numerical simulation computer program [12] which solves the Poisson equation and the current continuity equation of electrons and holes. There is a large amount of stored charges in the emitter-base depletion region which adds to the diffusion capacitance at the low current. The minority carrier concentration at the collector-base junction at a given current density is $J_c/(q \times v_s)$ where J_c is the current density and v_s is the saturation velocity of the carrier.

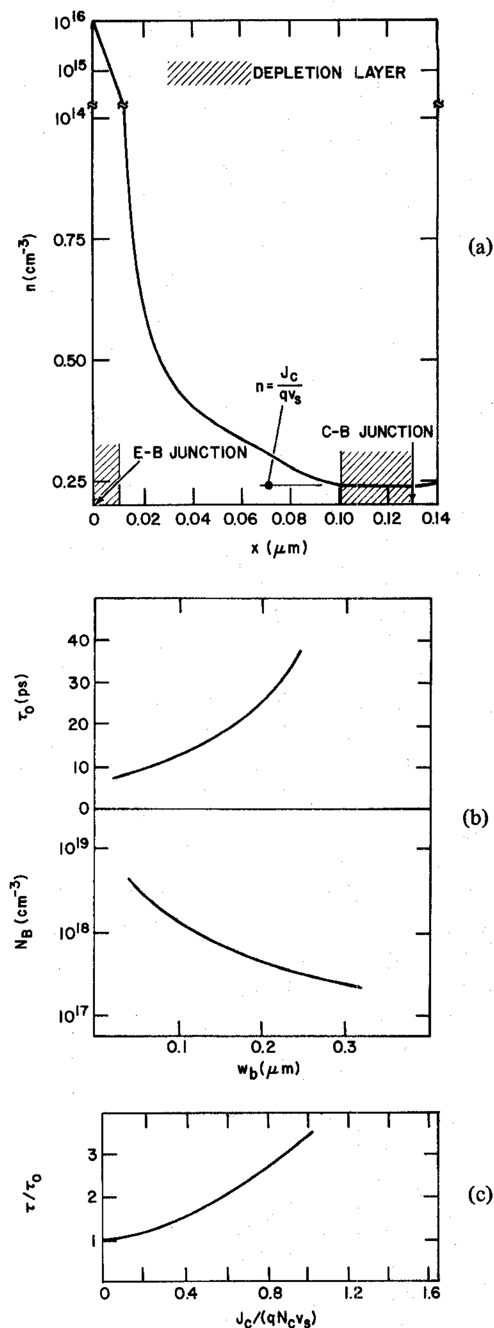


Fig. 2. (a) The distribution of the electrons inside the base of an n-p-n transistor; the base width is 0.13 μm. (b) Storage time constant at low current density and the peak base doping versus base width; the base doping is the peak base doping suggested by [14]; the voltage across the base-collector junction is 0 V. (c) Storage time constant versus collector current in a one-dimensional transistor.

Numerical computation of the charge storage time τ versus base width using the carrier mobilities given in [13] is shown in Fig. 2(b). Also shown in the same figure is the corresponding peak density of the base doping suggested in [14] as the punchthrough limit, assuming that the collector doping is much higher than that of the base. Since the collector doping is less than the base doping in most high performance transistors, the built-in voltage is mostly absorbed by the collector depletion layer, and a finite base sheet resistance remains. For the same base width, τ decreases as the sheet increases,

since the lower the base doping, the higher the diffusion coefficient and the narrower the neutral base region. When the minority carrier density in the base-collector junction approaches the doping density of the collector, the base broadens and the base storage time increases rapidly, which is known as the Kirk effect [9]. Fig. 2(c) shows the normalized charge storage time constant as a function of the normalized current density. Thus, to prevent strong base stretching, the collector doping should be kept greater than N_o and

$$N_o = I_c / A_e q v_s. \tag{7}$$

Since the collector capacitance contributes significantly to the power-delay product, the collector doping density should be reduced with the collector current density until the wiring capacitance becomes the dominant delay component. The ECL gate with emitter-follower output has a good current-driving capability (comparing the delay sensitivity coefficients k_1 of C_c and k_4 of C_l given in the Appendix); the delay contributed by C_l becomes significant only when C_l is one order greater than C_c. Fig. 3 shows how the circuit speed-power advantage can be realized by tailoring the transistor collector doping to the operating current. The solid line shows the circuit delay obtained from a circuit in which the transistor structure is fixed and only the value of the circuit elements are changed. The delay follows a constant power-delay product line. The delay at the lower current side can be reduced further if the collector doping and the collector capacitances are allowed to vary according to (7) and (3) at each current. The dotted line of Fig. 3 shows the delay versus current when both the circuit elements and the collector doping of the transistors are changed. Instead of approaching a constant power-delay product line, the delay is approximately proportional to $1/I_c^{0.5}$ as the current decreases.

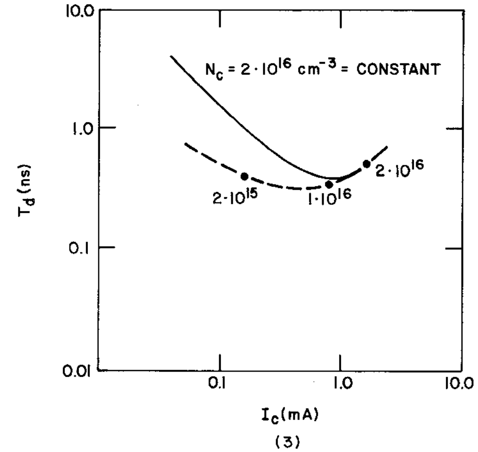


Fig. 3. Circuit delay versus collector current of the switching transistor. Solid line is the delay of the circuit which is built with one fixed transistor structure; its collector doping is 2×10^{16} 1/cm^3. The dotted line represents delay of group of circuits. Each circuit uses transistors with their collector doping density adjusted to the operating current according to (7).

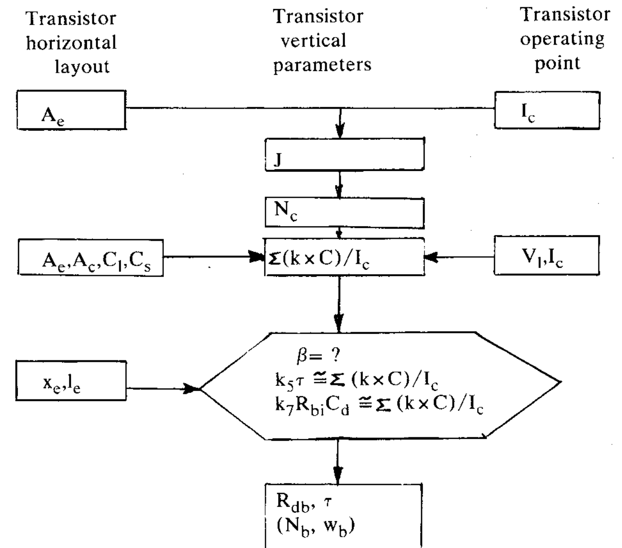


Fig. 4. Transistor design flowchart.

B. Relation Between the Transistor Emitter-Base Structure and the Collector Doping

The structure of the emitter-base can be characterized by the emitter stripe width, emitter depth, emitter doping, base width w_b, and the base sheet resistance R_{db} (or the average base doping density N_b). We shall assume further that the emitter doping is fixed and the emitter depth is deeper than the diffusion length of the carriers. The optimum base width and the base doping (thus, the base sheet resistance) depend somewhat on the transistor horizontal layout. However, for any layout, the base sheet resistance must be large enough to give the transistor sufficient collector current [14], and thus sufficient current gain. This current gain requirement thus sets the minimum value of base sheet resistance.

However, the base sheet resistance also determines the intrinsic base resistance, which is

$$R_{bi} = R_{db} x_e / (G \times l_e) \tag{8}$$

where G is a function of emitter geometry and x_e and l_e are the emitter stripe length and width, respectively. From (6a) and (8), the optimized base doping should satisfy

$$R_{db} \tau = (k_1 / k_7) \cdot (G \times l_e / x_e) \cdot V_l^2 C_c / I_c^2 \tag{9}$$

when $R_{bi} C_d$ is large. The requirements on the R_{db} imposed by the current gain and the circuit speed are mutually opposing, and a tradeoff should be made. For most designs, a range of R_{db} can be found for which both requirements can be satisfied. Under some conditions where large power is needed in order to obtain small delays, the constraints on R_{db} may not be met. One should either reduce the operating current with a corresponding reduction in the circuit speed or modify the emitter layout to reduce R_{bi}. For the other case, where τ is dominant (6b), the base width is of primary importance. The base doping density is allowed to be decreased further to enhance the current gain as long as the term $k_6 R_{bi} C_c$ is smaller than $k_5 \tau$ and the base punchthrough limit is exceeded.

The design procedure can thus be summarized as in Fig. 4. Starting from the desired current value and the emitter size from the transistor layout, the collector doping can be calculated. From this, the first four terms of the delay equation

associated with the depletion capacitances and the wiring capacitance are determined. From this delay, the choice of the R_{db} and τ (or the base-emitter structure) would be determined by weighing the contribution of $k_7 \times R_{bi}C_d$ and $k_5 \times \tau$ to the total delay at the operating current.

TABLE I
TRANSISTOR SIZE VERSUS POWER PERFORMANCE

Transistor	1	2	3	unit
min line	2 5	1	0.5	μm
I_c	0 50	0 20	0 10	mA
x_c	2 5	1	0 5	μm
A_e	2 5x2 5	1x1	0 5x0 5	μm^2
A_c	8 5x7 5	4x3	2 5x1 5	μm^2
N_c	$0\ 625 \times 10^{16}$	$1\ 56 \times 10^{16}$	$3\ 14 \times 10^{16}$	$1/cm^3$
R_l(kC's)*	103	67	55	pS
τ	19	12 5	10	pS
T_d				
ASTAP	320	170	126	pS
Eq(1)	333	159	112	pS

condition wiring capacitance is not included,
R_{db}=10 kilo-ohm/sq
R_{bx}=0 4 kilo-ohm/sq
C_e=1 75 fF/μm sq
C_s= 1 fF/μm sq
V_l=0 6 volt
* sum of the delay of the first four terms of Eq (1)

C. Relation Between the Current and the Transistor Size

As the lithographic technology advances, the transistor size is reduced according to the ground rule of the technology. The reduction of the lateral dimension reduces the area-dependent depletion capacitance. Its effect can be shown on the asymptotic delay plot in Fig. 1(d). The dotted lines show the delay components that are reduced as a result of reduction of the depletion capacitances. Let us consider the transistor layout in Fig. 1(a). The variation of the current at the minimum delay depends on whether $k_5 \times \tau$ is dominant or not. If τ is dominant, the minimum circuit delay will not be improved by reducing the horizontal dimensions. However, the operating current (the intersect between $R_1(k \times C)$ and $k_5\tau$) is reduced. In this case, since the current density is constant, the power-delay is improved. Speed can only be increased by reducing τ and increasing the current density. On the other hand, if $k_7 \times R_{bi}C_d$ is the dominant delay, the current at the minimum delay (the intersect between $R_1(k \times C)$ and $k_7 \times R_{bi}C_d$) decreases linearly with the emitter width or the square root of the collector capacitance. Thus, the circuit speed increases and the current density at the maximum speed is roughly inversely proportional to the emitter width. In all cases, where one component is dominant, reducing this component will tend to accentuate the previously neglected one. Good design should strive to keep the contribution of $k_5 \times \tau$ and $k_7 \times R_{bi}C_d$ to the total delay comparable to that from the terms associated with R_1 of (1). Further increases in circuit speed can be realized by reducing the base width, which reduces τ and C_d.

To illustrate the practicality of this design procedure, we examine the transistor structures of different sizes, each tailored to a given current. The layout of the transistors is the same as the one shown in Fig. 1(a). The R_{db} is also chosen to be constant to give a constant current gain (assuming the emitter vertical structure is fixed). Table I shows the transistor structures and the circuit performances. In the case of $x_e = 2.5$ μm, Fig. 3 indicates that the current has a minimum at 0.5 mA. The operating currents of the other two cases are allowed to decrease linearly with the emitter stripe width to achieve maximum speed. The corresponding collector doping increases due to the higher current density. Following the flowchart in Fig. 4, the delay contributed by the first four terms of (1) can be evaluated since the layout and doping of the collector are known. The delays due to $k_5 \times \tau$ and $k_7 \times R_{bi}C_d$ are comparable to the sum of the first four terms of (1) if τ is 12.5 and 10 pS for the cases of 1.0 and 0.5 μm emitter stripe widths, respectively. The corresponding base width is 0.12 and 0.07 μm for $x_e = 1.0$ and 0.5 μm, respectively. The base sheet resistance can be kept constant by increasing the base doping. The value of τ chosen above is not necessarily unique. The delay can be improved further if τ or the base width is made smaller. However, the improvement in the speed of the circuit due to the reduction in base width starts to diminish if the base width is reduced further. The delay calculated using ASTAP is compared with the result of the delay equation in the same table. Clearly, the accuracy of the design equation is acceptable. More importantly, we had found that the numerical analysis (ASTAP results) actually shows that the maximum circuit speed occurs at the same current level predicted from the simple design procedure. The value of the wiring capacitance is approximately proportional to the length of the wire. As the lithographic line width decreases, the circuit pitch reduces proportionally. Thus, the fraction of the gate delay due to the wiring remains constant.

There are other emitter-base designs. Each leads to different circuit power performance. For the case where the power dissipation has to be maintained constant per unit area (or I_c roughly proportional to collector area), there is no need for the reduction of τ as the transistor size is reduced. However, the speed of the circuit is expected to remain unchanged, as indicated in the asymptotic delay plot, Fig. 1(d).

IV. SUMMARY

In this paper, a simple transistor design procedure for the integrated bipolar logic circuit has been described. The design procedure provides a guideline to tailor the transistor structure so that the performance of the logic circuit is optimized at a given power dissipation level. It has been shown that with a given layout ground rule, there is a well-defined set of relations between the emitter-base structure and the collector doping density that is optimized to a given operating current. The flowchart of this design procedure is shown in Fig. 4. We further discuss the relation between circuit properties and the transistor size, which becomes smaller as the lithography advances. It is shown that as the lateral dimension of the transistor shrinks, the base width should shrink, and the base and the collector doping density should both be increased in order to realize the full speed advantage. One simple "coordinated shrinkage" procedure relating the emitter width and the vertical structure of the transistor is suggested. The suggested procedure for optimization is given whereby the current is varied inversely proportional to the emitter stripe width. The base

width (and thus the charge storage time) and the circuit delay are reduced more slowly than this (see Table I).

Appendix
The Coefficients of the ECL Delay Equation

The coefficients of (1) derived from the sensitivity of the circuit parameters to the delay of the gate shown in Fig. 1(c) are given as follows:

$$k_1 = 2.50 + 0.413 \times FO$$

$$k_2 = 0.24 \times FO$$

$$k_3 = 1.10$$

$$k_4 = 0.233$$

$$k_5 = 2.2 + 0.39 \times FO$$

$$k_6 = 1.27$$

$$k_7 = 5.19$$

$$k_8 = 2.21.$$

In (1), all units of capacitance are in femto farad, time is in picoseconds, resistance is in kilohms, voltage is in volts, and current is in milliamperes. The fan-in of the gate is 4 and the number of the fan-out is FO.

Acknowledgment

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D. D. Tang was born in China in 1946. He received the Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, in 1974.

He had been working in the area of microwave semiconductor devices and circuits before he joined the IBM T. J. Watson Research Center, Yorktown Heights, NY, in 1975, where he worked on the exploratory signal processing device utilizing a bulk acoustic-wave at microwave frequencies. He is presently a Research Staff member, and his interests are in the area of exploratory silicon devices and large-scale bipolar integrated circuits.

Paul M. Solomon studied electrical engineering at the University of Cape Town, Cape Town, South Africa, and graduated in 1967. He studied further at the Israel Institute of Technology, Haifa, and in 1973 he completed a D.Sc. dissertation on SiO_2 breakdown properties.

Since 1975 he has been at the IBM T. J. Watson Research Center, Yorktown Heights, NY, where he continued work on SiO_2 high field current instability mechanisms, discovering evidence of impact ionization in SiO_2 at high fields. More recently he has become interested in the problem of extrapolating bipolar performance to very small dimensions, and he has worked extensively with numerical circuit analysis and optimization programs available at IBM's T. J. Watson facility.