

CS/EE 5710/6710

CMOS Processing

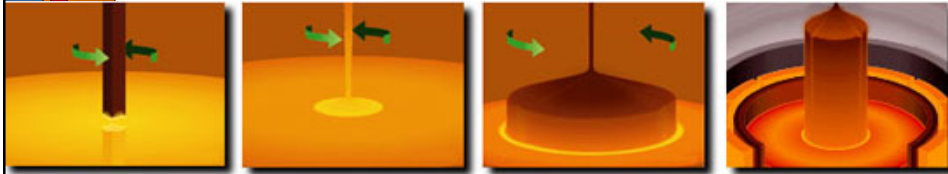
Growing the Silicon Crystal



Single Crystal Silicon Ingot

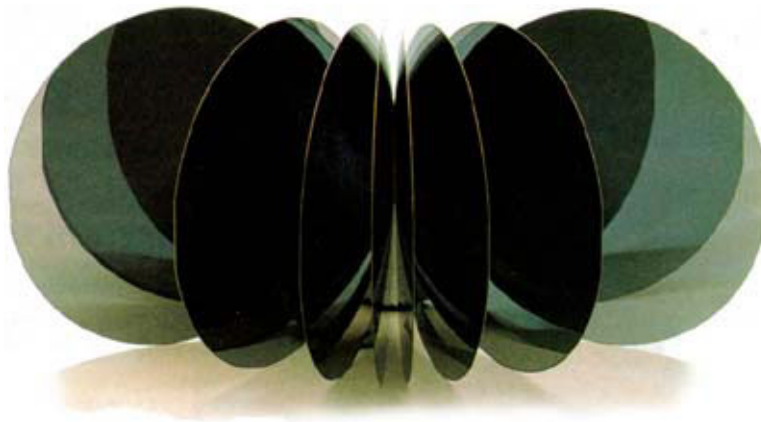
- ▶ Need single crystal structure
 - ▶ Single crystal vs. Polycrystalline silicon (Poly)

Czochralski Method



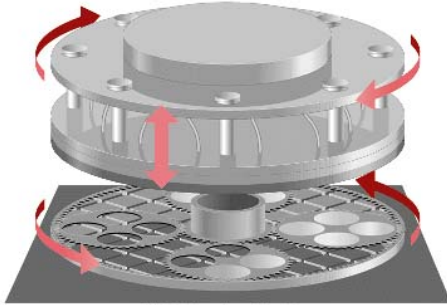
- ▶ Need single-crystal silicon to accept impurities correctly
 - ▶ Donor elements provide electrons
 - ▶ Acceptor elements provide holes
- ▶ Pull a single crystal of silicon from a puddle of molten polycrystalline silicon

Slice Crystal into Wafers



- ▶ Slice into thin wafers (.25mm - 1.0mm), and polish to remove all scratches

Lapping and Polishing

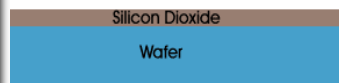


Water Polishing
(Strasbaugh Corporation)

Oxidation, Growing SiO₂



Oxidation Furnace
(Silicon Valley Group - Thermco Systems)

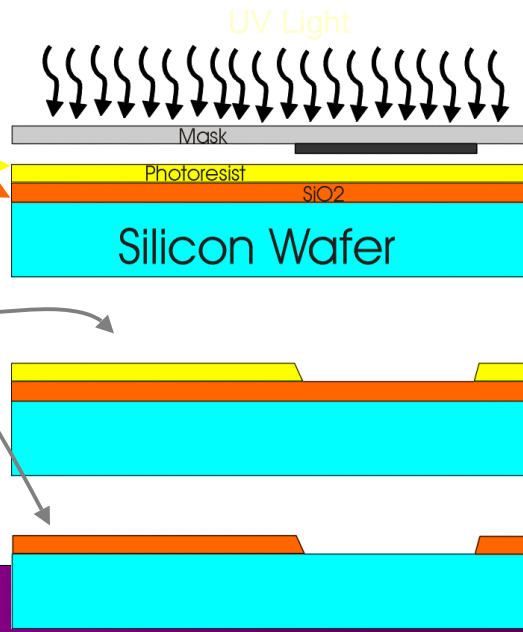


Oxidation Layering

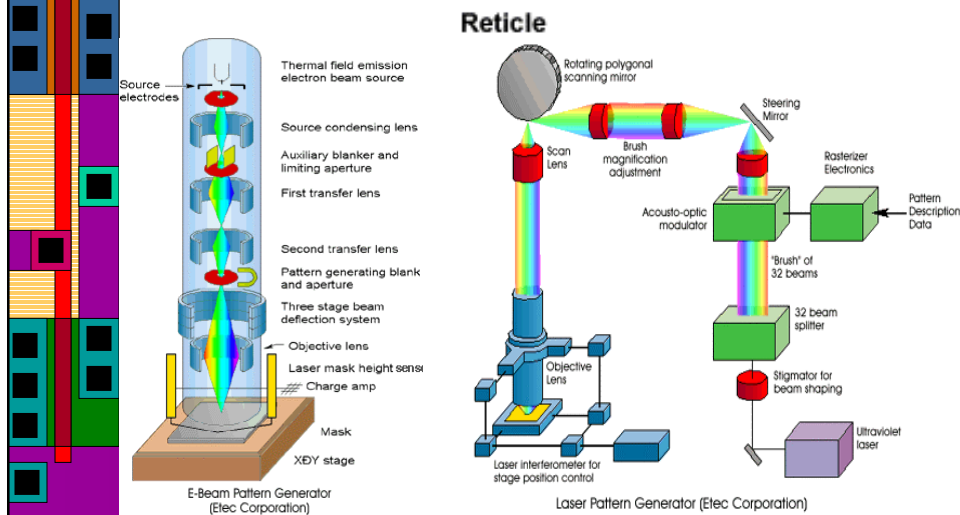
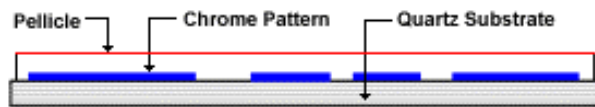
- ▶ Essential property of silicon is a nice, easily grown, insulating layer of SiO₂
 - ▶ Use for insulating gates (“thin oxide”)
 - ▶ Also for “field oxide” to isolate devices

Photolithography

- ▶ Oxidation Layer
- ▶ Photoresist (PR) Coating
- ▶ Stepper Exposure
- ▶ PR development and bake
- ▶ Acid Etching
- ▶ Spin, Rinse, Dry
- ▶ Processing step
- ▶ PR removal (ashing)



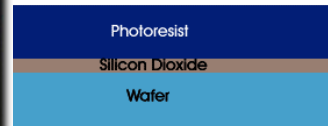
Making the Mask



Adding Photoresist



Photoresist Application
(Ontrak)



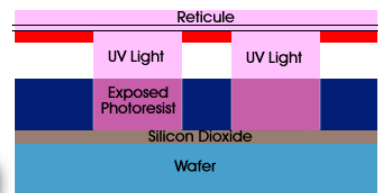
Photoresist Coating

- ▶ Photoresist can be positive or negative
 - ▶ Does the exposed part turn hard, or the unexposed part?

“Steppers” Expose the Mask



Stepper
(ASM Lithography)



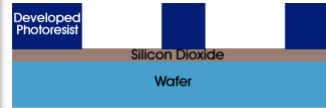
Exposure

- ▶ Use very short wavelength UV light
 - ▶ Single frequency, 436 - 248 nm
- ▶ Expensive! ~\$5,000,000/machine...

Develop and Bake Photoresist



Oxidation Furnace
(Silicon Valley Group - Thermco Systems)



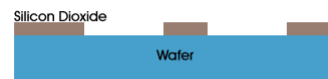
Photoresist Develop & Strip

- ▶ Developed photoresist is soft, unexposed is hardened
 - ▶ So you can etch away the soft (exposed) part

Now Etch the SiO₂



Automated Acid Etch
(SEZ)



Oxide Etch



SRD (Spin, Rinse, Dry)
(SEZ)

- ▶ Etch the SiO₂ to expose the wafer for processing
- ▶ Then Spin Rinse, and Dry

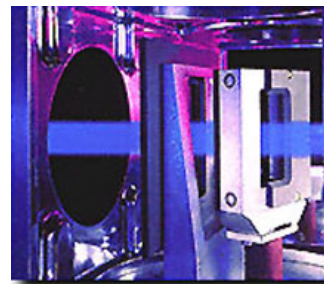
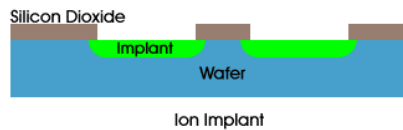
Add a Processing Step

- ▶ Now that we've got a pattern etched to the right level, we can process the silicon
- ▶ Could be:
 - ▶ Ion Implantation (I.e. diffusion)
 - ▶ Chemical Vapor Deposition (silicide, Poly, insulating layers, etc.)
 - ▶ Metal deposition (evaporation or sputtering)
 - ▶ Copper deposition (very tricky)

Ion Implantation



Ion Implanter
(Varian Associates)



Ion Implanter Steering Magnets
(Varian Associates)

- ▶ Implant ions into the silicon
 - ▶ Donor or Acceptor

Chemical Vapor Deposition

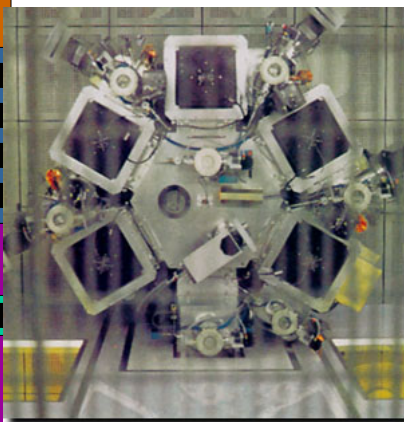


CVD Tool
(Applied Materials)

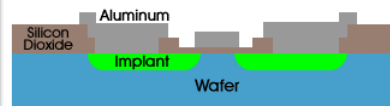


CVD Tool
(Applied Materials)

Metal Deposition



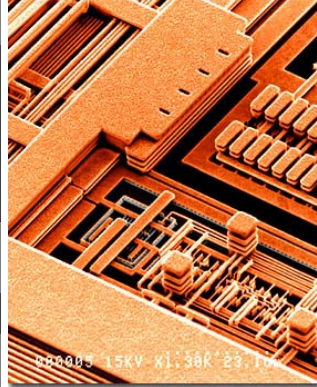
PVD Sputtering Tool
(Sputtered Films Corporation)



Metal Deposition

- ▶ Typically aluminum, gold, tungsten, or alloys

Copper is Tricky



SEM view of Copper Interconnect
(IBM Microelectronics)



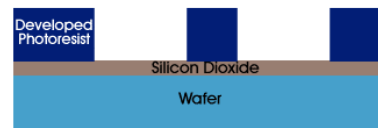
Copper Deposition

- ▶ 40% less resistance than Aluminum
 - ▶ 15% system speed increase
- ▶ But, copper diffuses into Silicon and changes the electrical properties

Ashing - Removing Photoresist

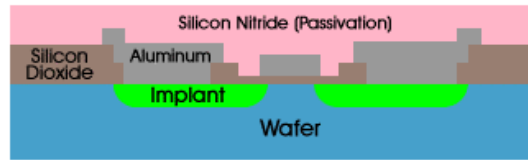


Plasma Asher
(Fusion Systems)



Photoresist Develop & Strip

Final Layer: Passivation



Passivation

- ▶ Basically a final insulating layer (SiO_2 or Si_3N_4) to protect the circuit

CMOS Fabrication

- ▶ Start from single-crystal silicon wafer
- ▶ Use photolithography to pattern device layers
 - ▶ Essentially one mask/photolithographic sequence per layer
 - ▶ Built (roughly) from the bottom up
 - ▶ 6 - Metal 3
 - ▶ 5 - Metal 2
 - ▶ 4 - Metal 1
 - ▶ 2 - Polysilicon
 - ▶ 3 - Diffusions
 - ▶ 1 Tub (N-well)

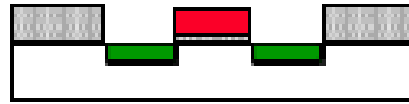
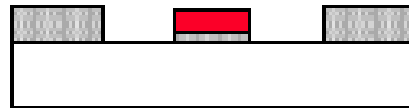
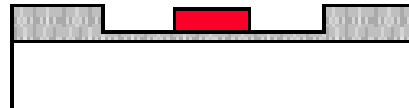
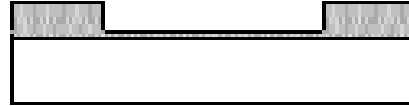
Exception

Via
Via

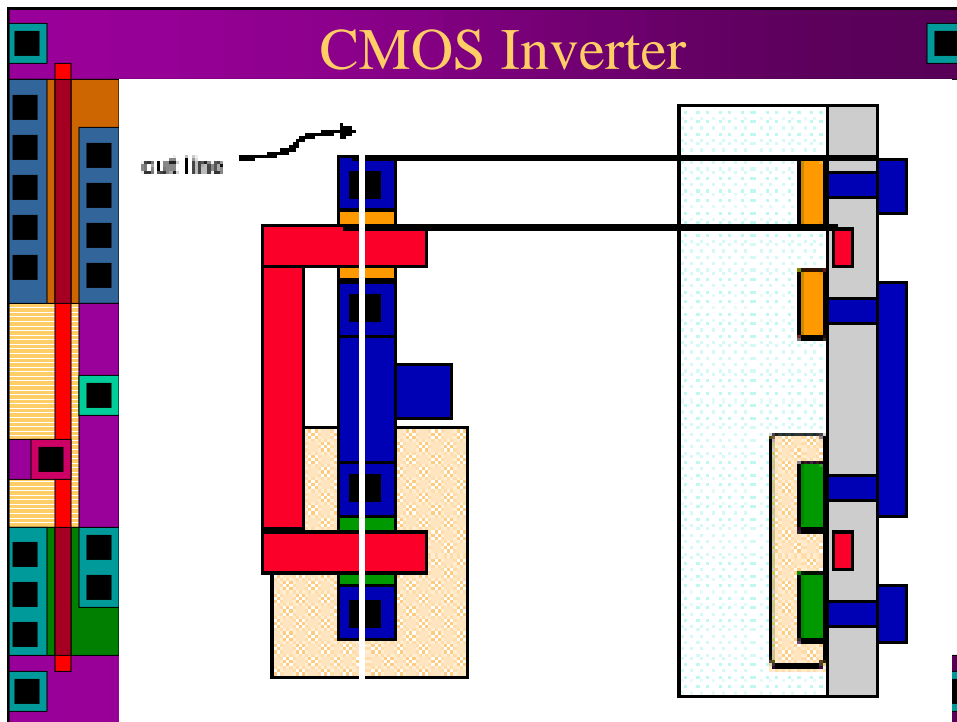
Contact

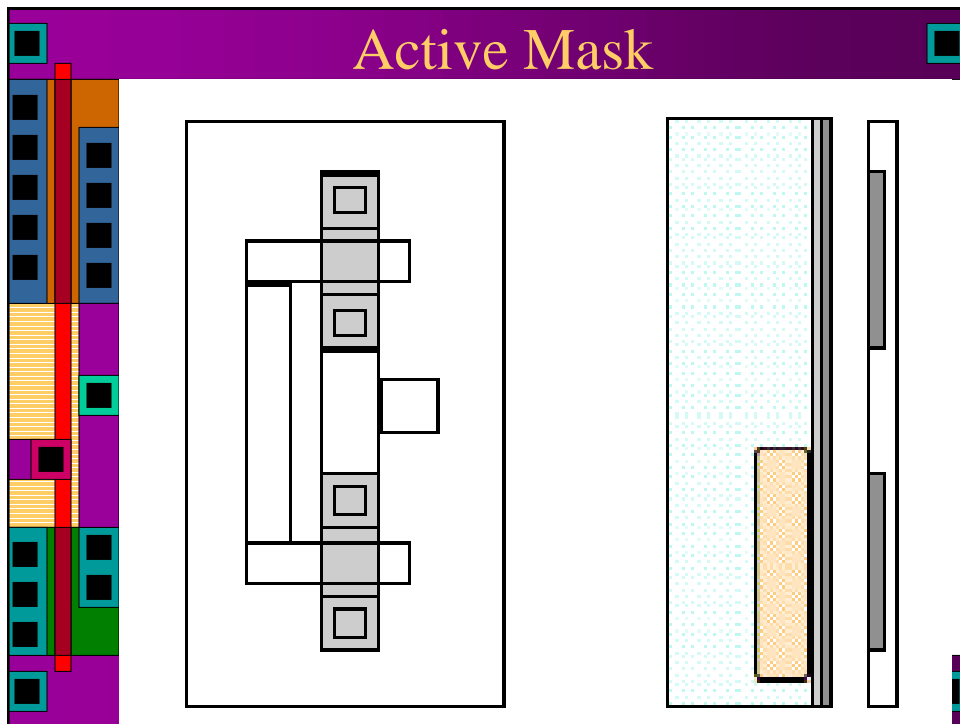
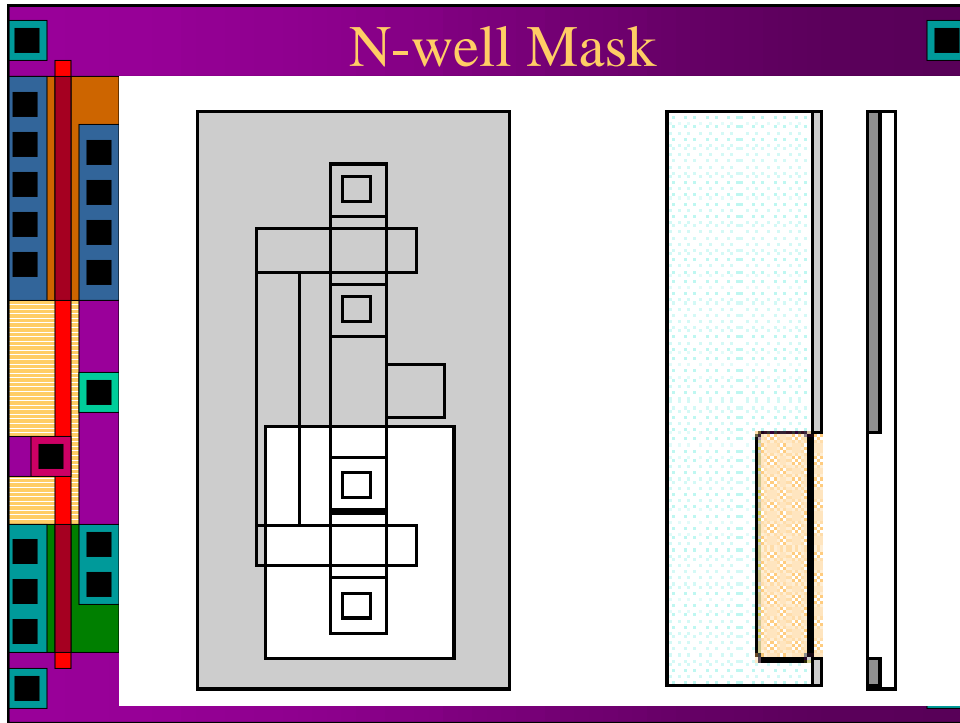
Self-Aligned Gates

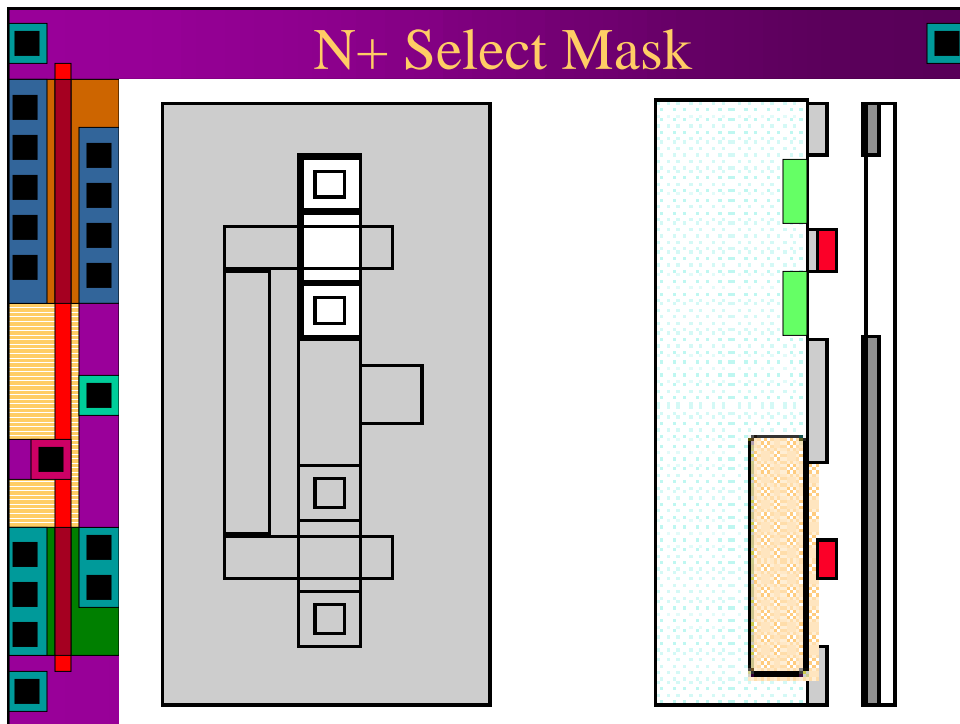
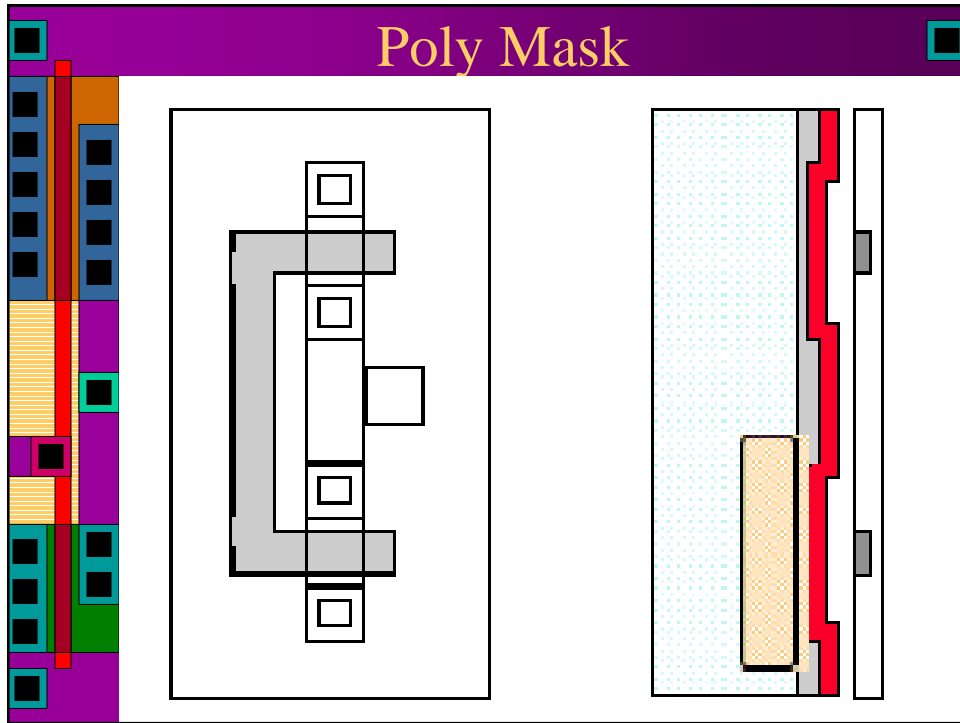
- ▶ Thin ox in active regions, thick elsewhere
- ▶ Deposit Polysilicon
- ▶ Etch thinox from active region (Poly serves as mask for etch/diffusion)
- ▶ Implant dopant

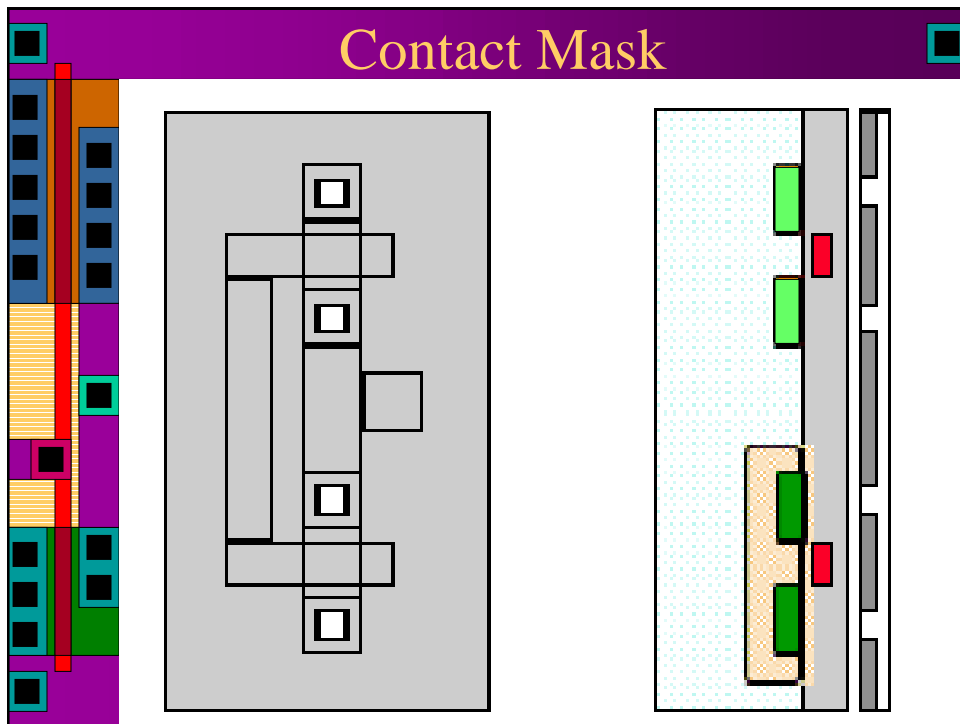
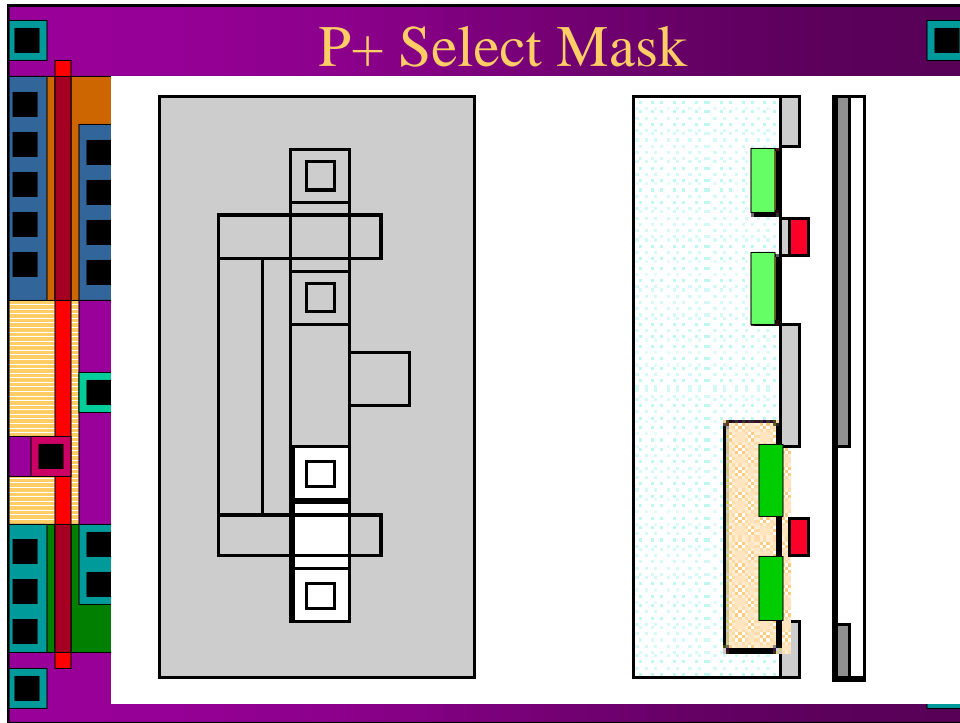


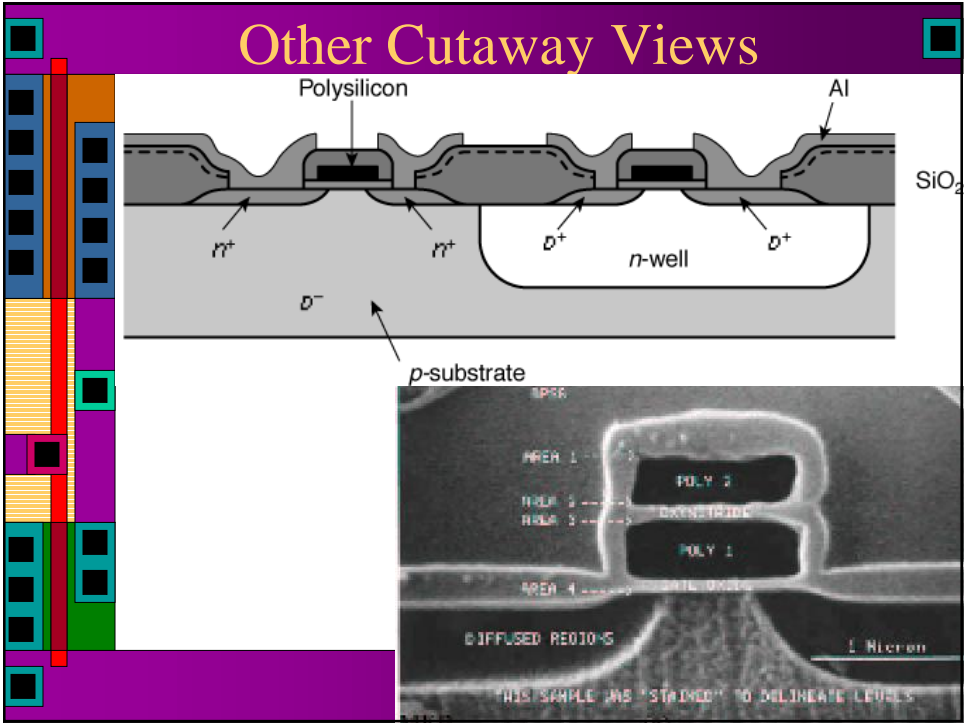
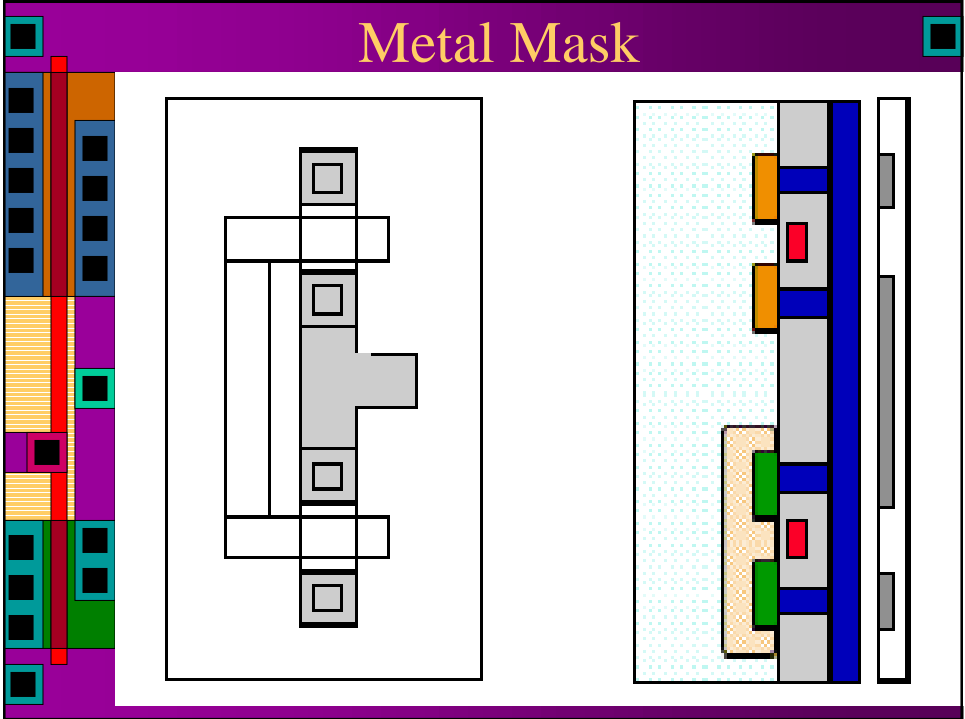
CMOS Inverter





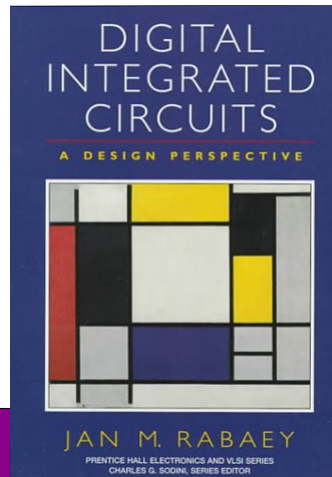




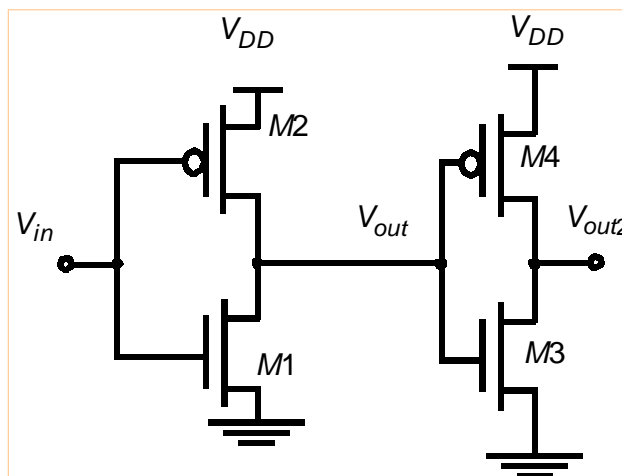


Another View of Fab

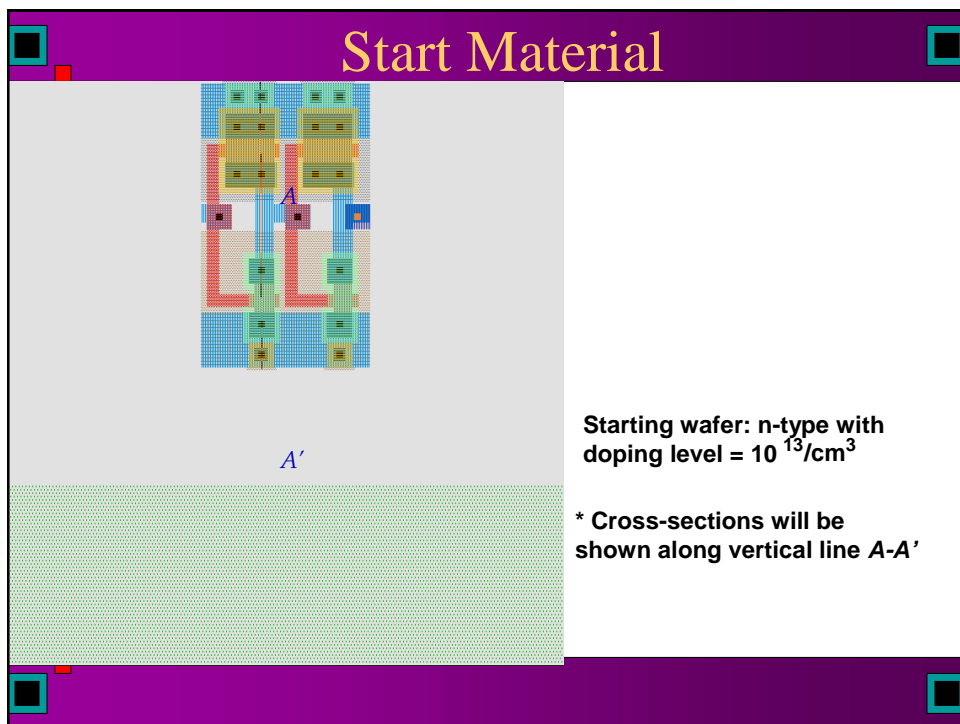
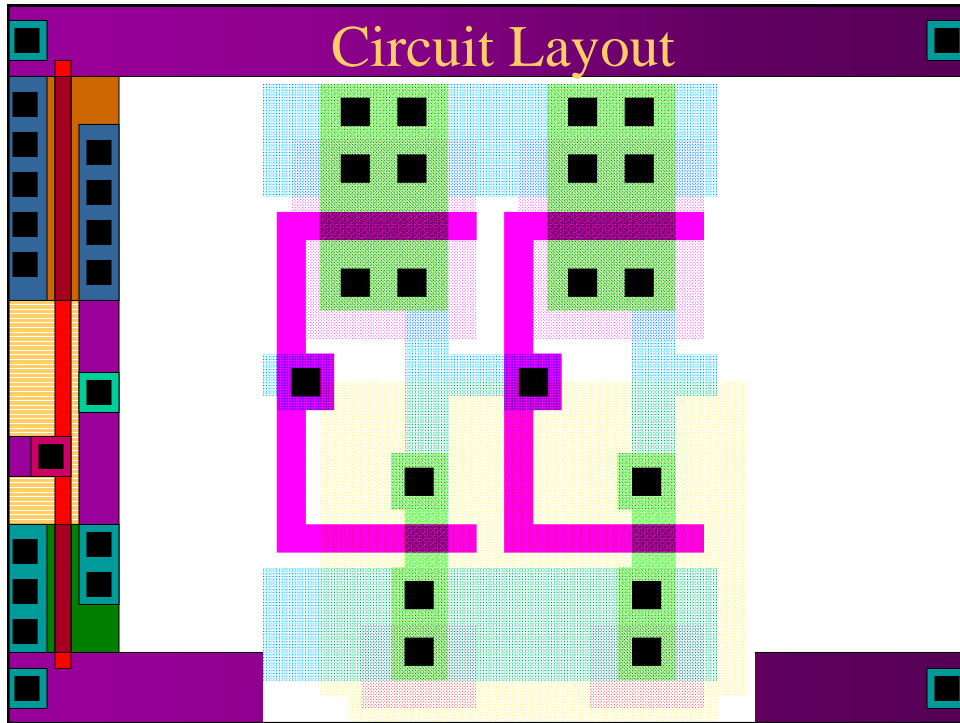
- ▶ Taken from slides by Jan Rabaey
- ▶ From his text “Digital Integrated Circuits”



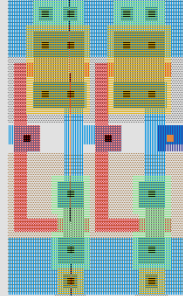
Circuit Under Design



This two-inverter circuit (of Figure 3.25 in Rabaey's text) will be manufactured in a twin-well process.

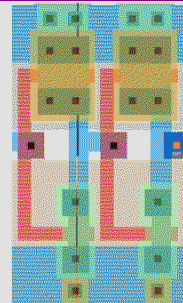


N-well Construction



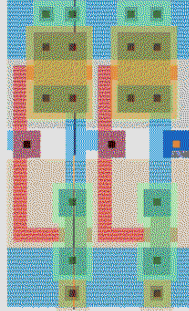
- (1) Oxidize wafer
- (2) Deposit silicon nitride
- (3) Deposit photoresist

N-well Construction



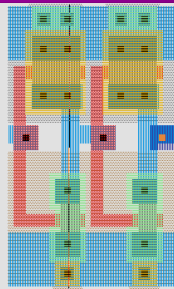
- (4) Expose resist using n-well mask

N-well Construction



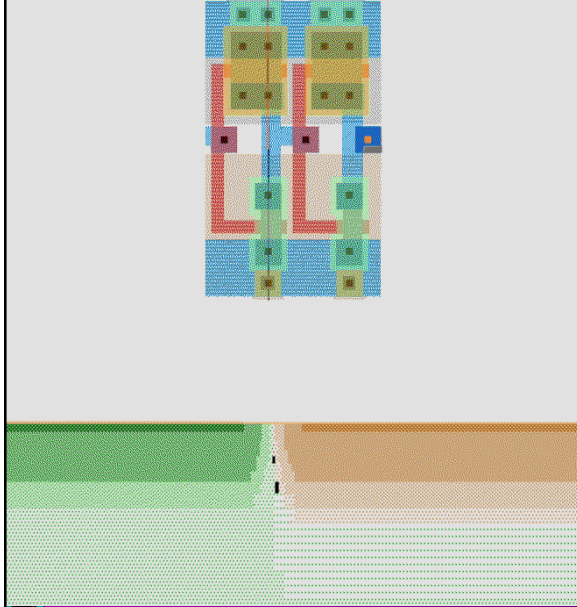
- (5) Develop resist
- (6) Etch nitride and
- (7) Grow thick oxide

N-well Construction



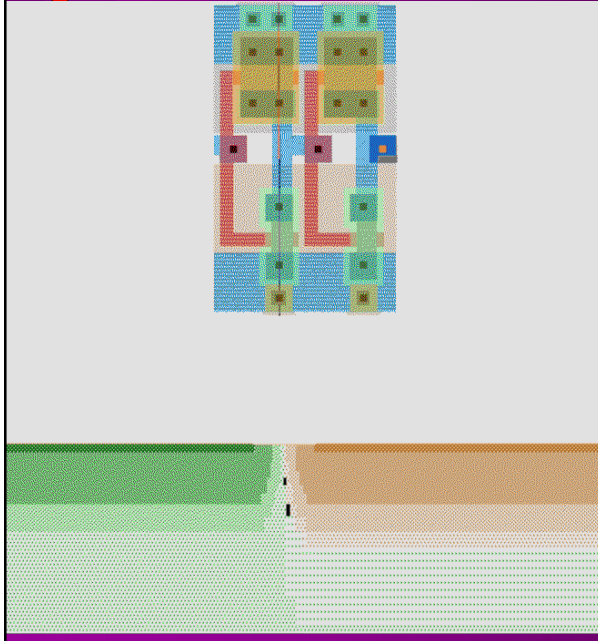
- (8) Implant n-dopants (phosphorus)
(up to 1.5 μm deep)

P-well Construction



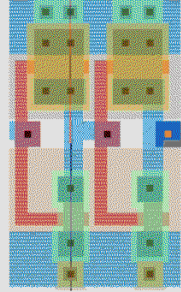
Repeat previous steps

Grow Gate Oxide



0.055 μm thin

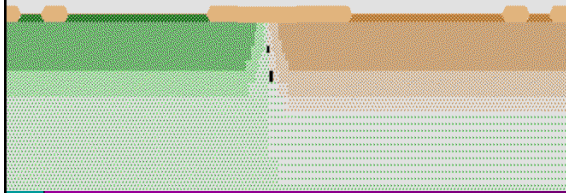
Grow Thick Field Oxide



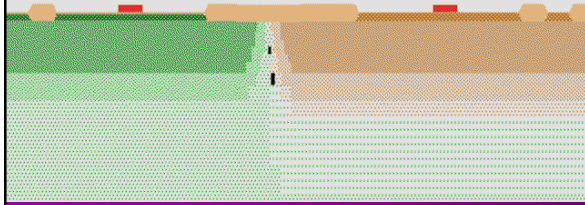
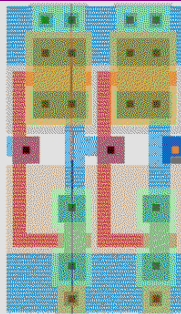
0.9 μm thick

Uses Active Area mask

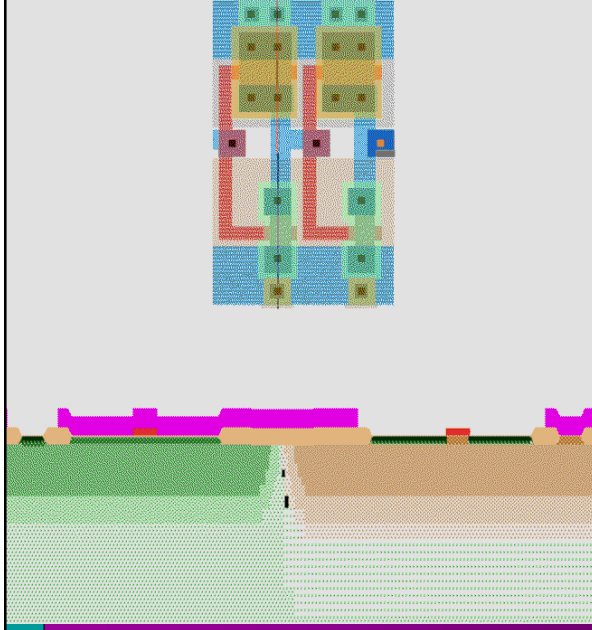
Is followed by
threshold-adjusting implants



Polysilicon layer

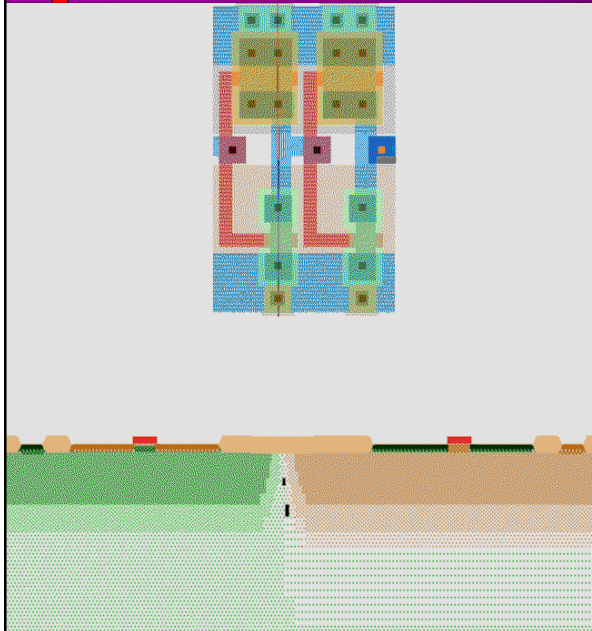


Source-Drain Implants



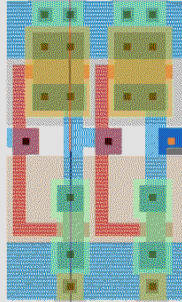
n+ source-drain implant
(using n+ select mask)

Source-Drain Implants

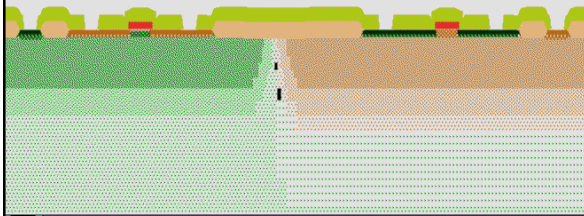


p+ source-drain implant
(using p+ select mask)

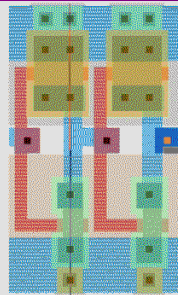
Contact-Hole Definition



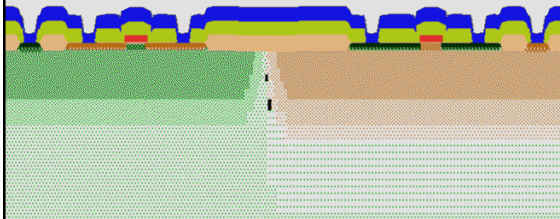
- (1) Deposit inter-level dielectric (SiO_2) — $0.75 \mu\text{m}$
- (2) Define contact opening using contact mask



Aluminum-1 Layer



Aluminum evaporated
($0.8 \mu\text{m}$ thick)
followed by other metal
layers and glass



Advanced Metalization

