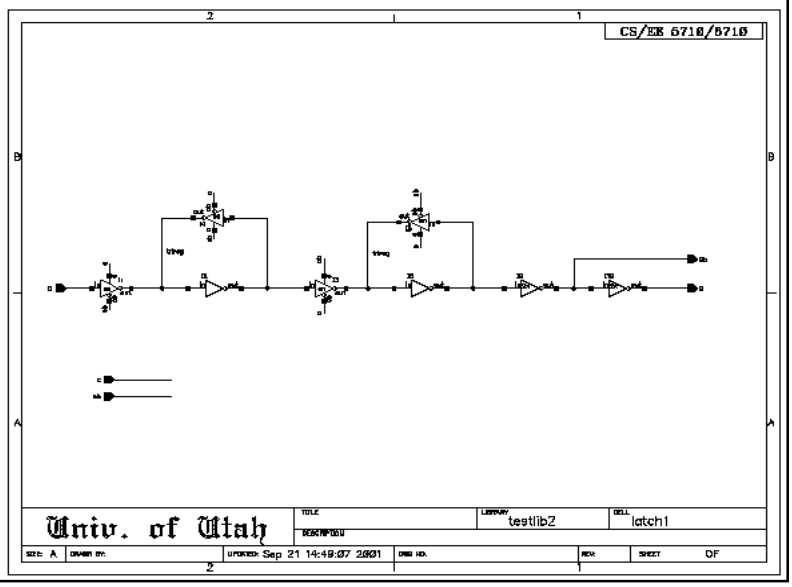
Where are we?

- Lots of Layout issues
  - Line of diffusion style
  - Power pitch
  - Bit-slice pitch
  - Routing strategies
  - Transistor sizing
  - Wire sizing

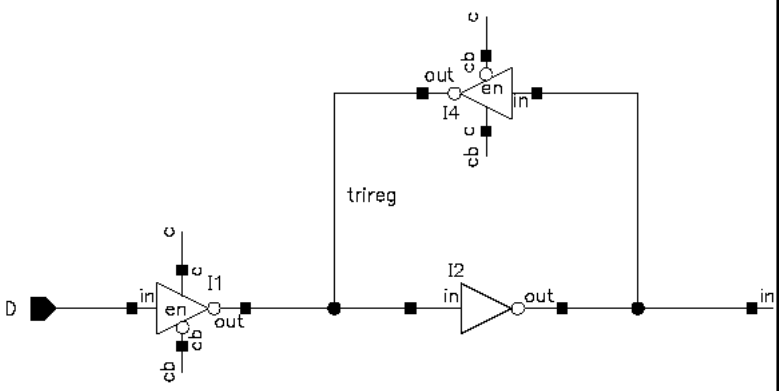
Layout Example: Flip Flop

- Simple D-type edge triggered flip flop



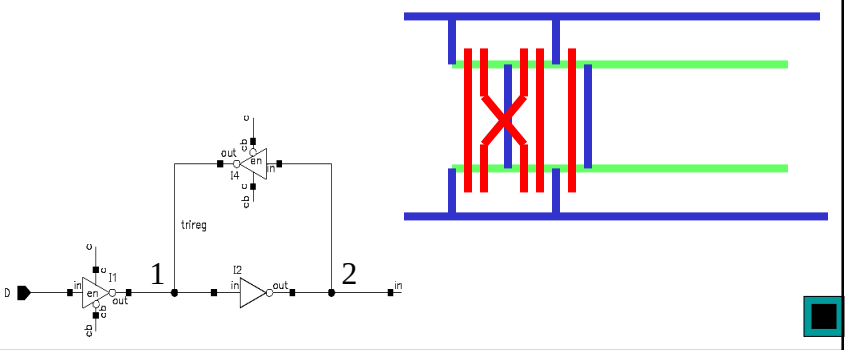
Zoom in on Latch

- Need two copies of this for a full D flip flop



Stick Diagram of Latch

- First add the gates
  - Note where outputs can be shared
  - Ignore details of signal crossings for now…



Stick Diagram of Latch

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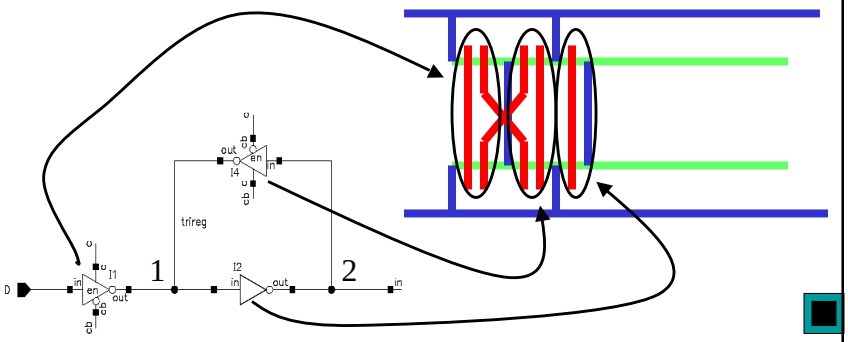
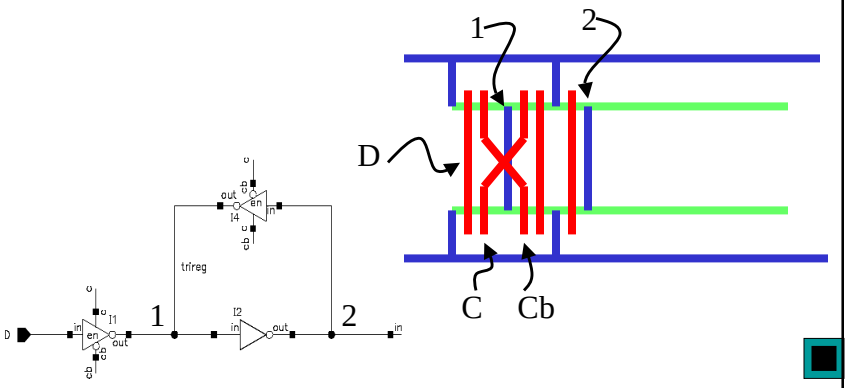


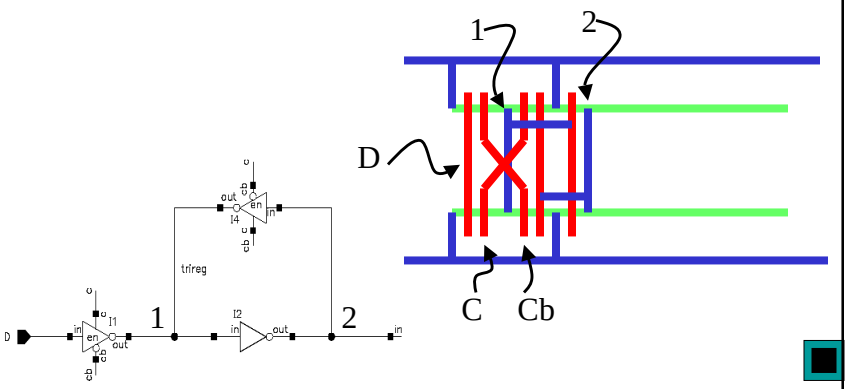
Stick Diagram of Latch

- First add the gates
  - Note where the signals are relative to the schematic



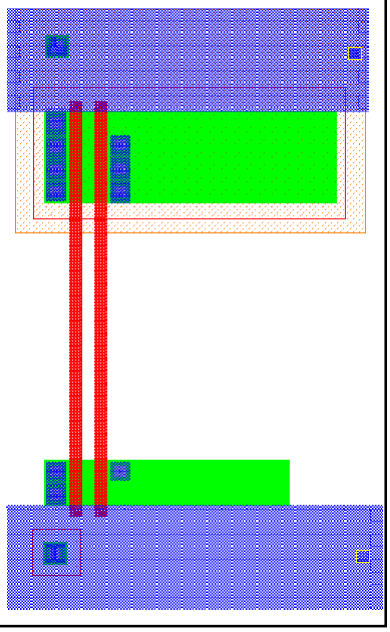
Stick Diagram of Latch

- First add the gates
  - Note where the signals are relative to the schematic
  - Note where additional connections are needed



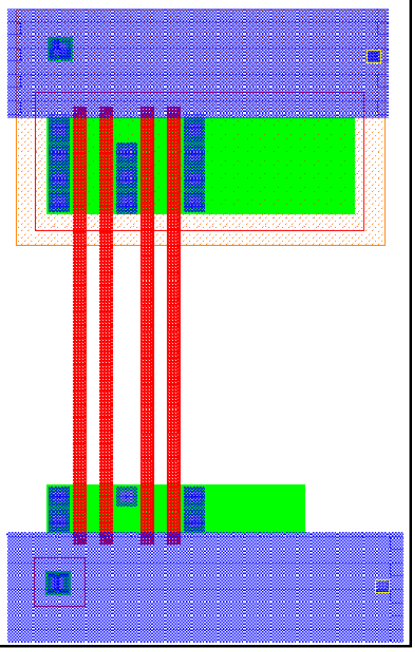
Start With First Enabled Inv

- I'm using 5u power wires, 29u vertical picth based on the C5x standard cell model
  - Probably overkill…
- Add DIF for N- and P-type transistors
  - Note 2x standard size because of serial connection

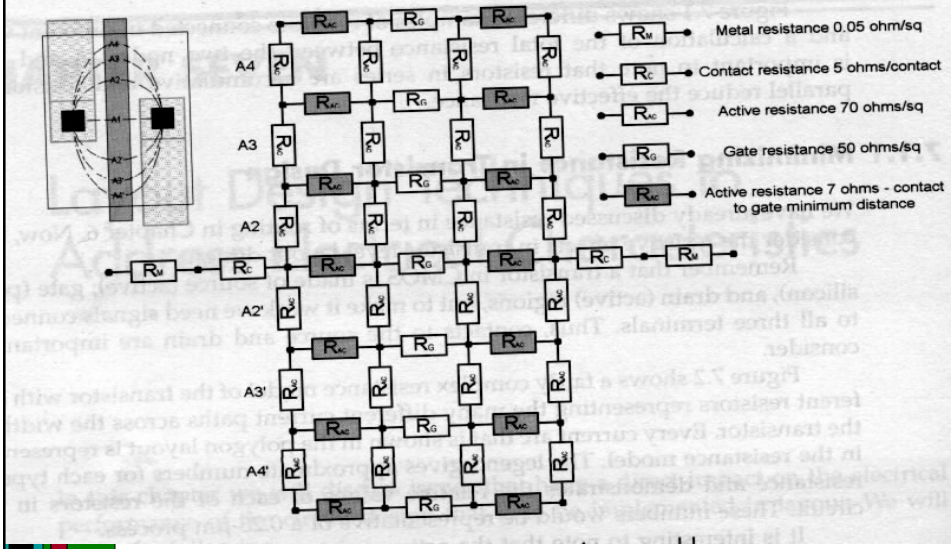


Add Next Enabled Inverter

- Add two more poly gates for second enabled inverter
- Note that the two enabled inverters share an output (not connected yet)
- Note that I've added vdd! and gnd! For DRC
- I'll deal with C-Cb crossover later…

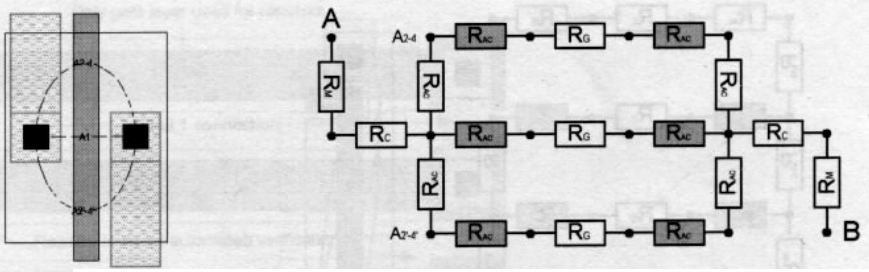


Aside: Multiple Contacts



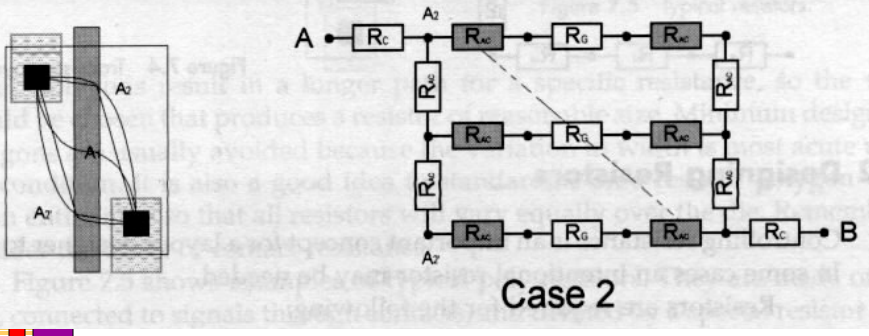
- Look at a model of transistor resistance

Contact Option #1



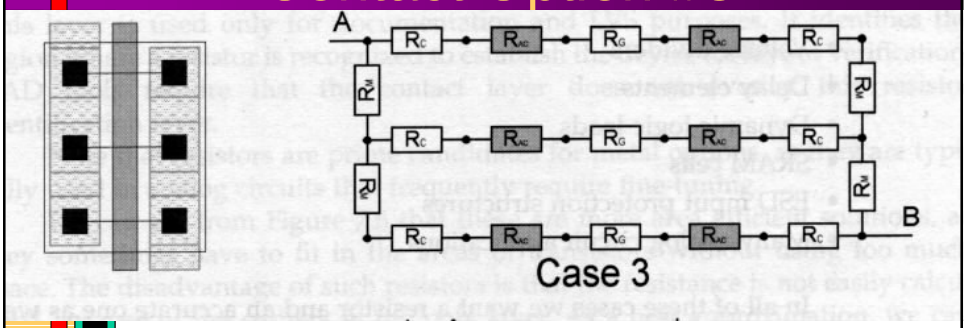
- Total equivalent resistance = 56.1 Ohms
  - Metal resistance = 0.05 O/square
  - Contact resistance = 5 O/contact
  - Active resistance = 70 O/square
  - Gate resistance = 50 O/square
  - Active resistance 7O - contact to gate

Contact Option #2



- Total equivalent resistance = 105.1 Ohms

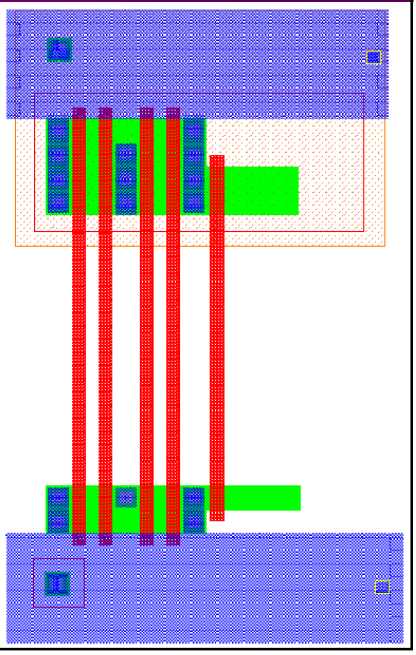
Contact Option #3



- Total equivalent resistance = 24.7 Ohms
- So, put in as many contacts as will fit along side a wide gate…

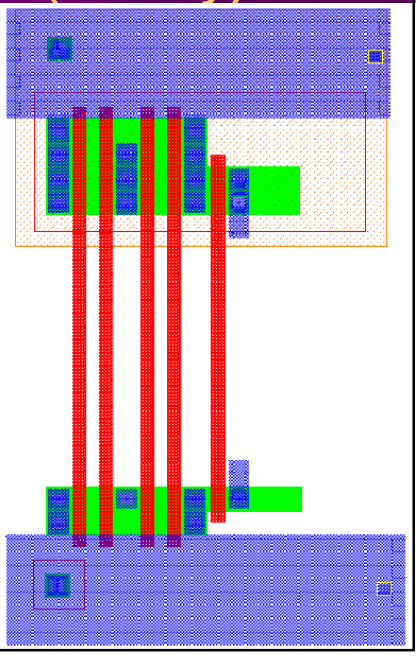
Meanwhile, Add inverter

- Note that it's back to standard size
- Shares vdd/gnd connection with enabled inverter
- Minimum spacing for all transistors so far
  - Incremental DRC at EVERY step!



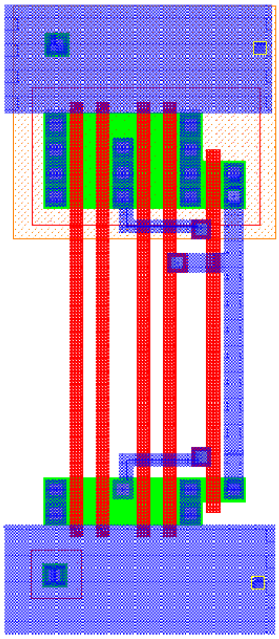
Finish Inverter (mostly)

- Make inverter output connections
  - Don't connect yet
  - I'm going to use M1 as a horizontal layer
  - Which means being careful about vertical use of M1



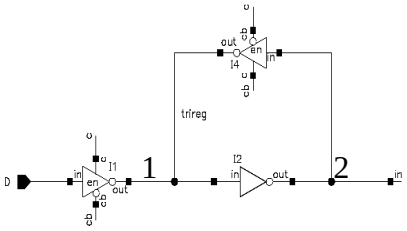
Make Feedback Connections

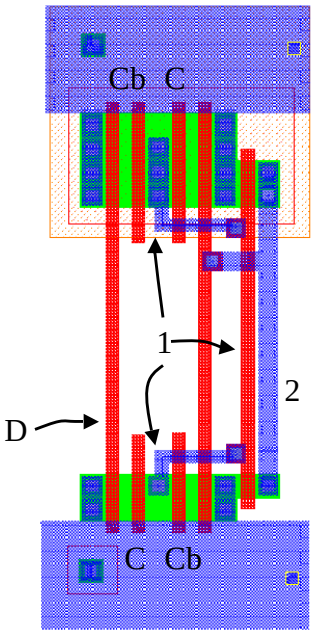
- Output of inverter (connected in M1 for now) goes to input of 2nd enabled inverter
- Output of enabled inverters goes to input of inverter
  - Note that outputs of enabled inverters goes through POLY



Deal With C/Cb Crossover

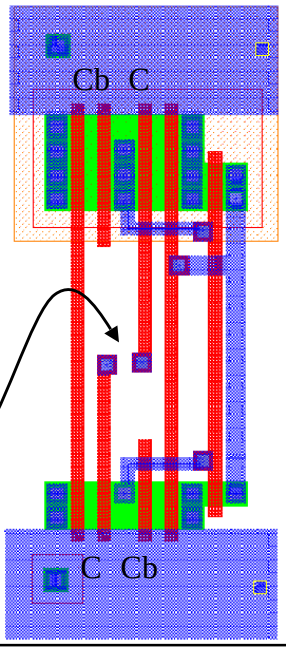
- Start by cutting the "select" gates of the enabled inverters





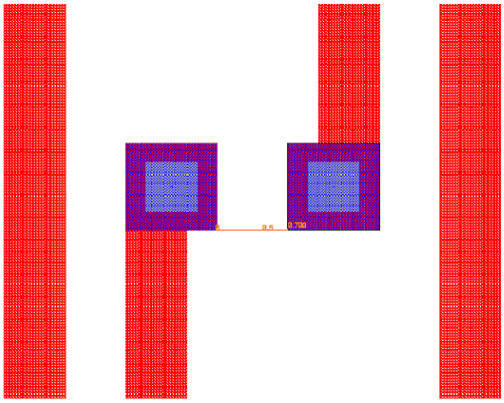
Connect the C Input

- Prepare for M1 crossover in C wire
  - C is N-type in first enabled inverter, P-type in second enabled inverter
  - Use M1PLY contacts
- PROBLEM! We need to squeeze a poly wire inbetween those contacts…
  - Use design rules to plan for space



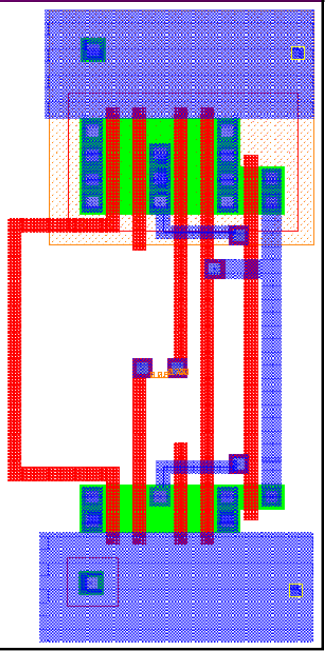
Look at Gap

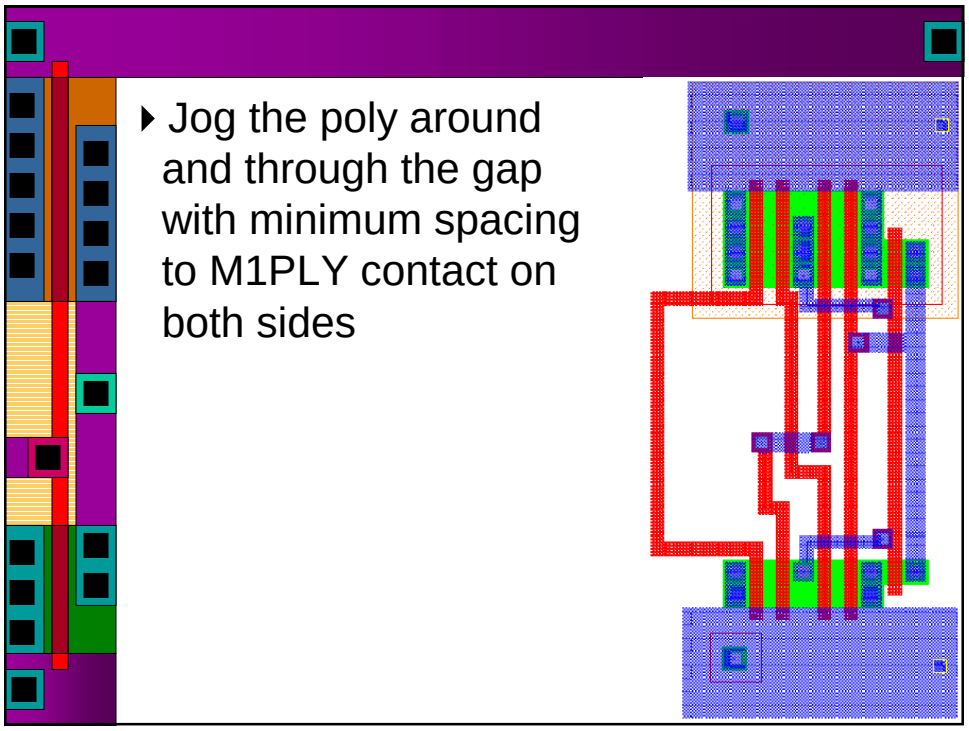
- You need to have enough space for minimum width poly to fit through gap

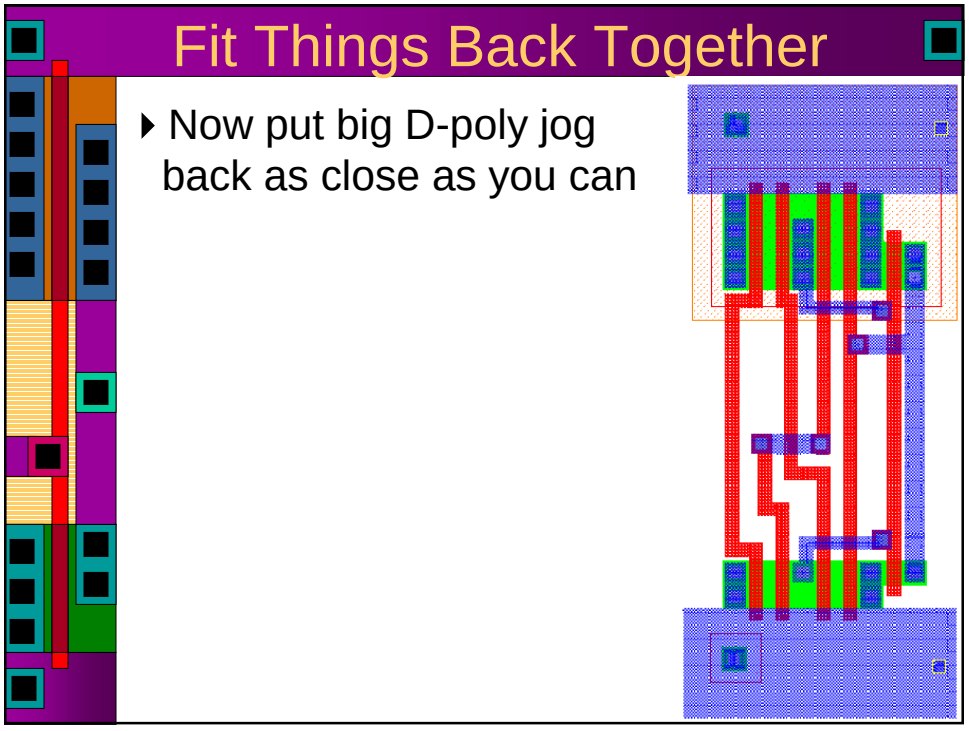


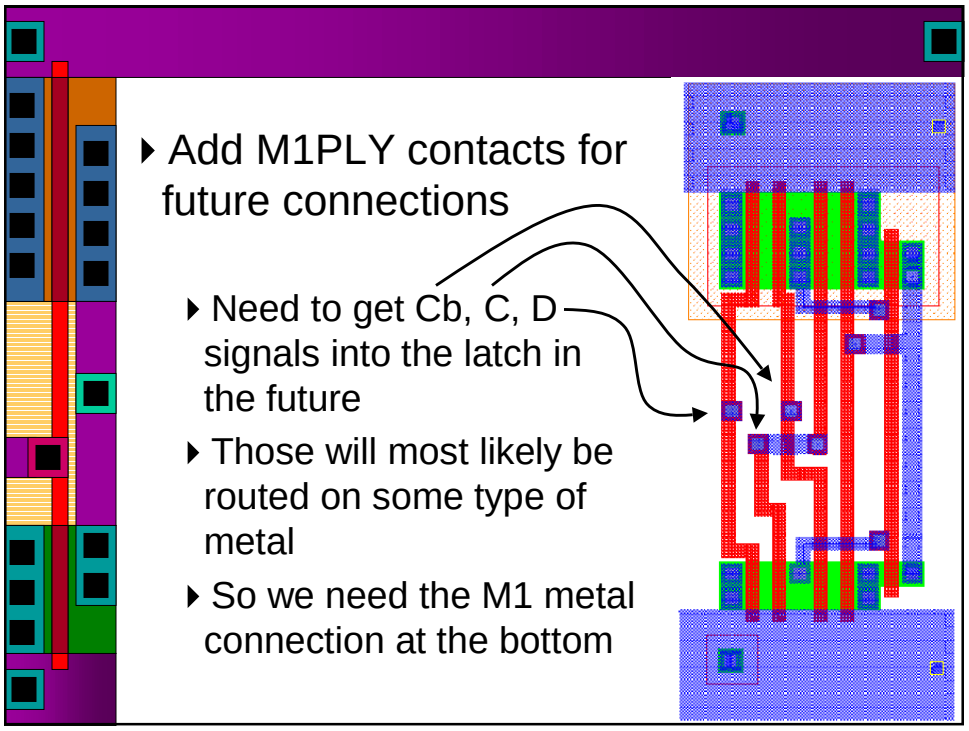
Start Making Room

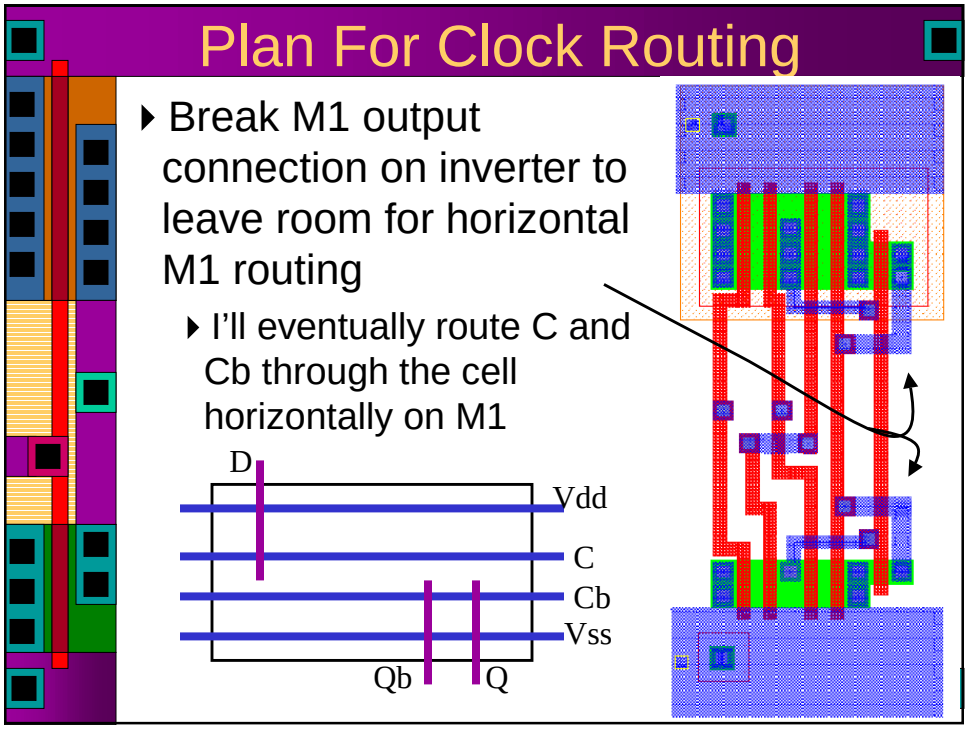
- Push D-signal poly out of the way with minimum spacing to DIF
  - We'll move it back later
- Make sure to continue to DRC at every step!




Jog the poly around and through the gap with minimum spacing to M1PLY contact on both sides

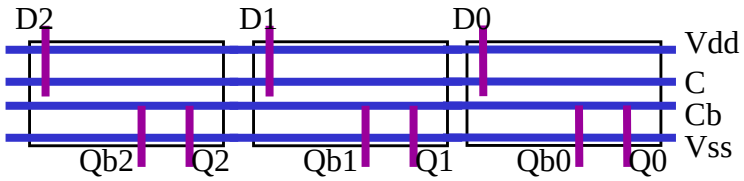

Fit Things Back Together
Now put big D-poly jog back as close as you can


Add M1PLY contacts for future connections
Need to get Cb, C, D signals into the latch in the future
Those will most likely be routed on some type of metal
So we need the M1 metal connection at the bottom


Plan For Clock Routing
Break M1 output connection on inverter to leave room for horizontal M1 routing
I'll eventually route C and Cb through the cell horizontally on M1
D
Vdd
C
Cb
Vss
Qb
Q

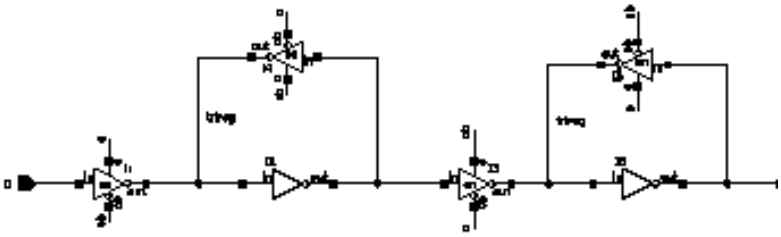
Bit Slice Plan

- Plan is to stitch these together to make a register
  - Inputs on top in M2
  - Outputs on bottom in M2
  - Clock and Clock-bar routed horizontally in M1



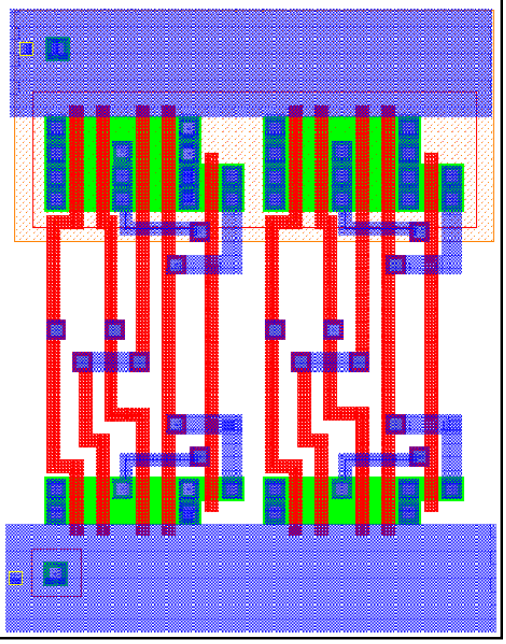
Need Second Latch

- Basically a copy of the first latch
  - But with reversed C and Cb connections
  - Copy the first layout…



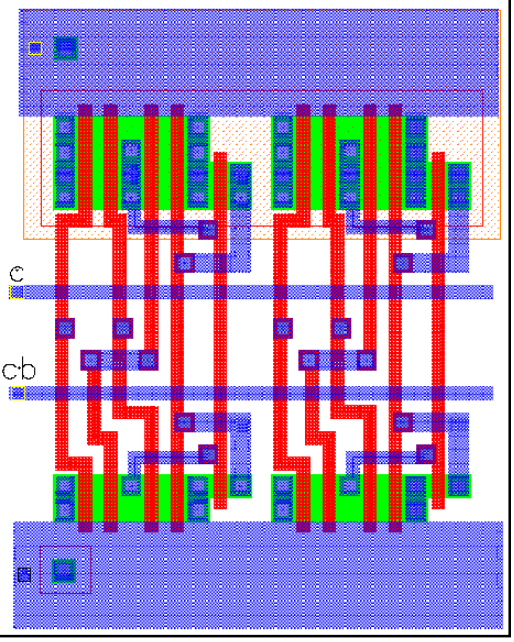
Expand from Latch to F/F

- Select and copy the first latch
- Now I need to reverse the C and Cb connections



C/Cb Routing Plan

- Remember my C/Cb routing plan
  - Plan for where those wires can go



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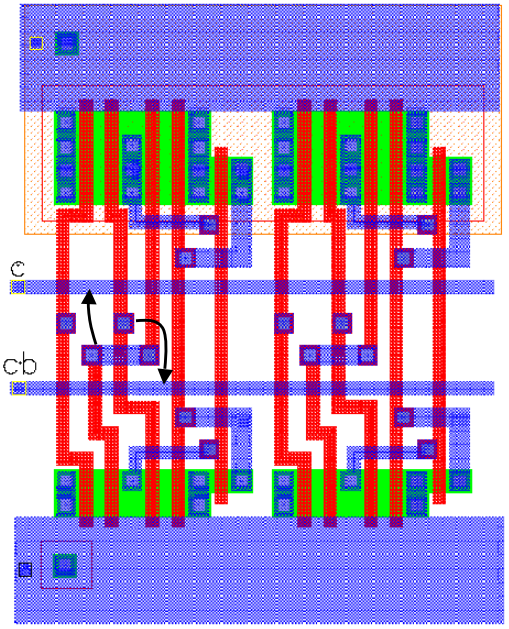
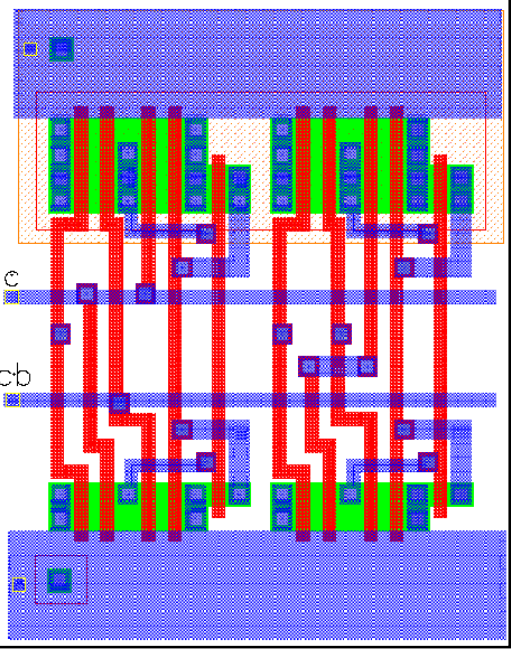


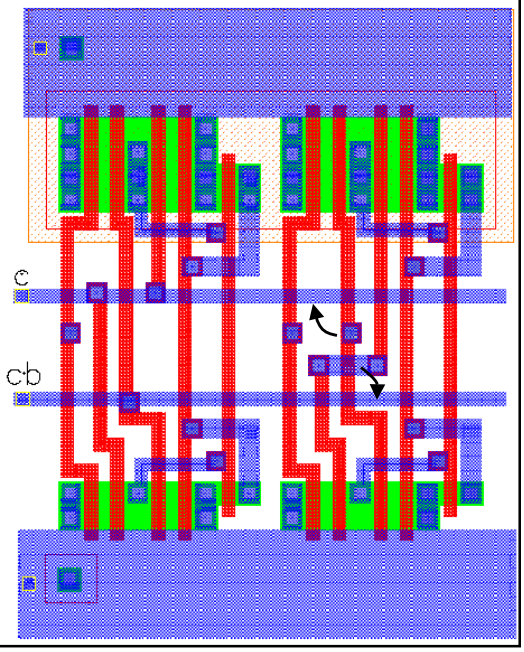
Connect Clocks to 1st Latch

- Adjust contact positions for the first enabled inverter



Connect Clocks to 2nd Latch

- Now shift the contacts the other way for the second latch
  - Makes the complementary C/Cb connection



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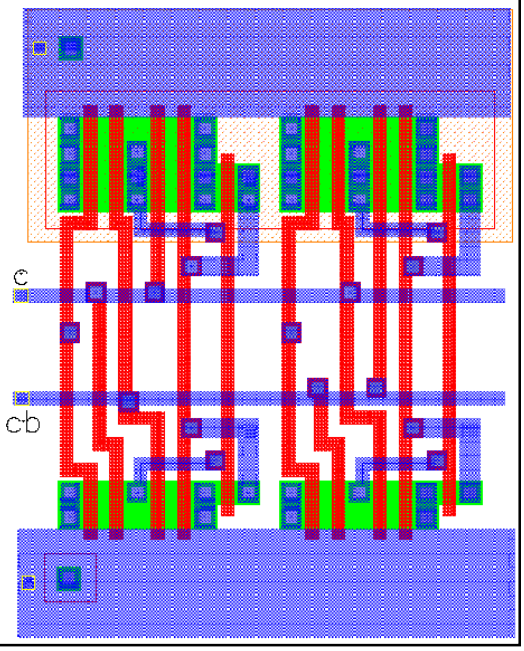
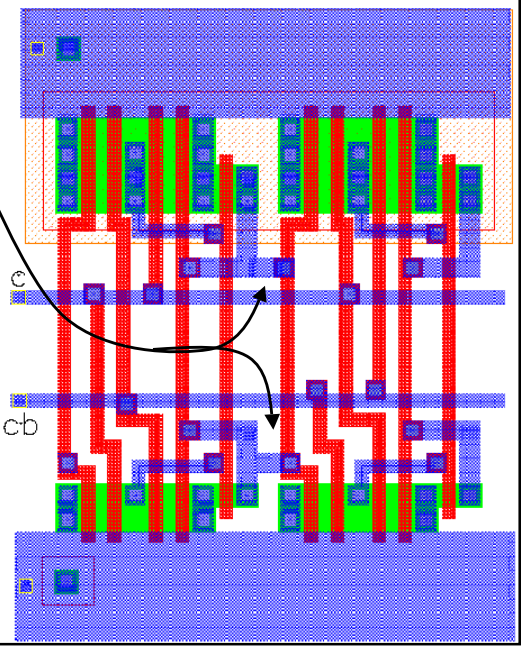


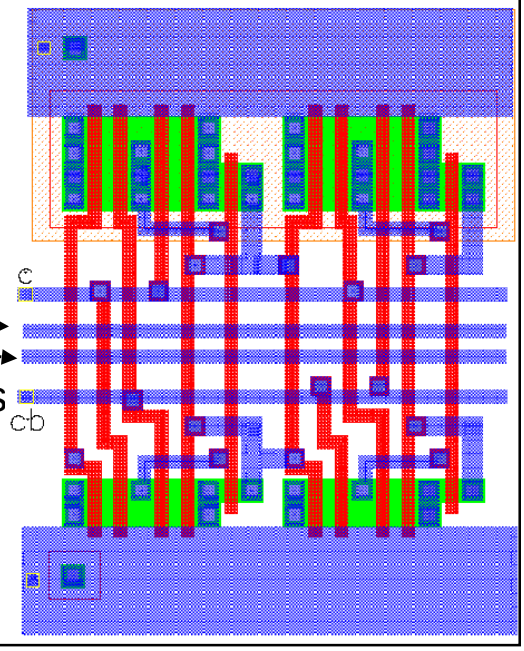
Connect the Two Latches

- Q of first goes to D of second
  - Don't really need both top and bottom connections, but it doesn't hurt
  - Lower resistance paths



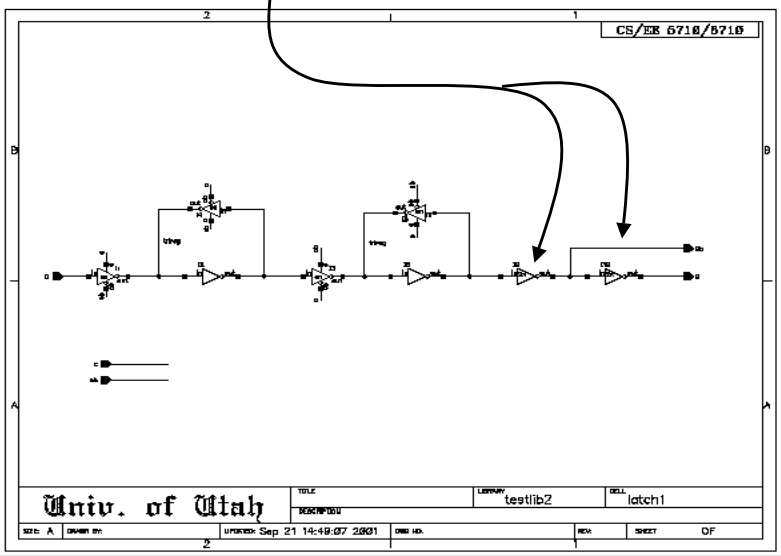
Note Extra Routing Channels

- Note that this vertical pitch, and this cell contents have left two additional M1 horizontal routing channels through the middle of the cell



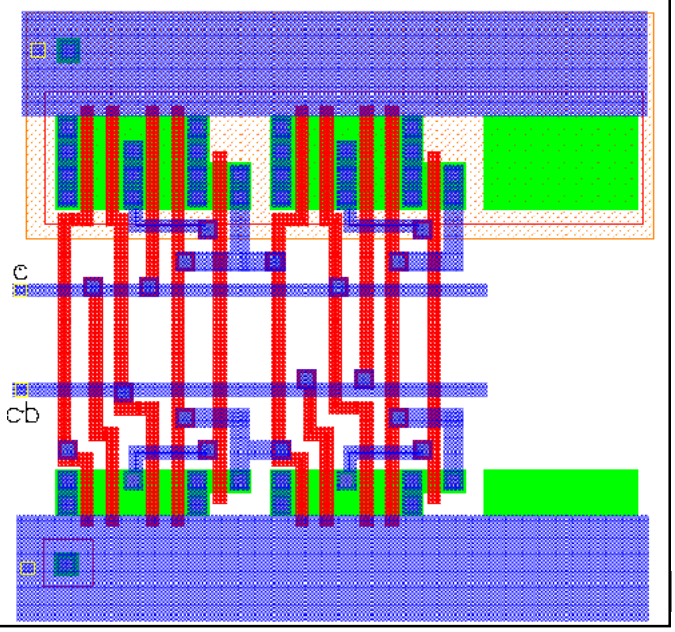
Now Consider Output Inverters

- Two more inverters
  - Make them 2x size for output drive



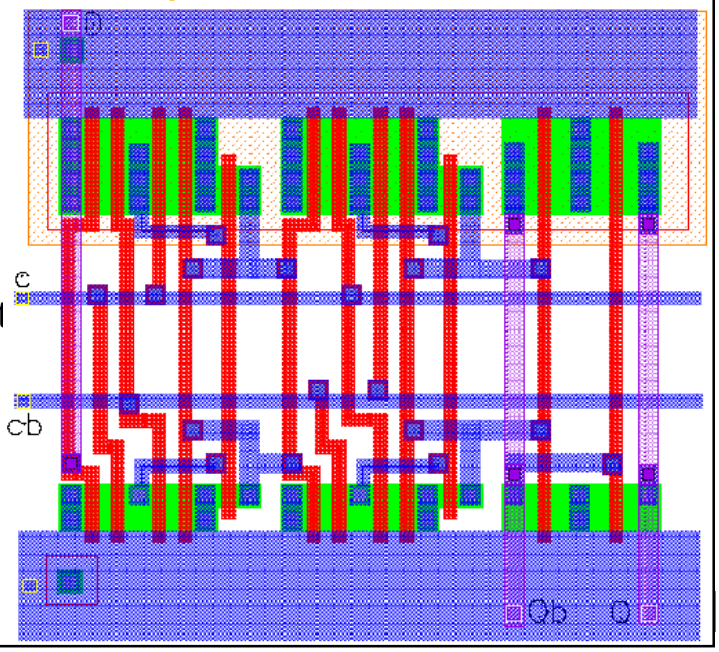
Output Inverters

- Add the DIF for the output inverters
  - Remember I want to make them 2x size



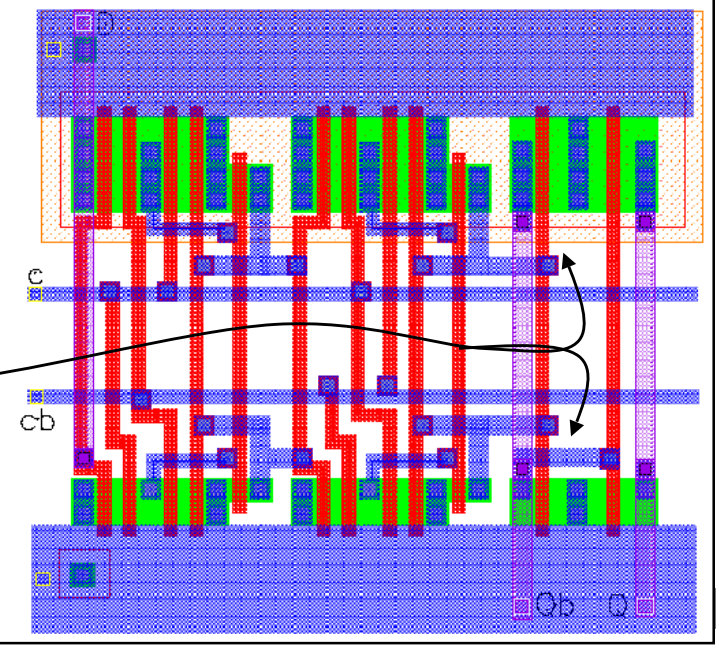
Make Output Connections

- Add vdd, gnd and output contacts
- Add poly gates
- Make output connections in M2
- Connect to 2nd latch and to 2nd inverter



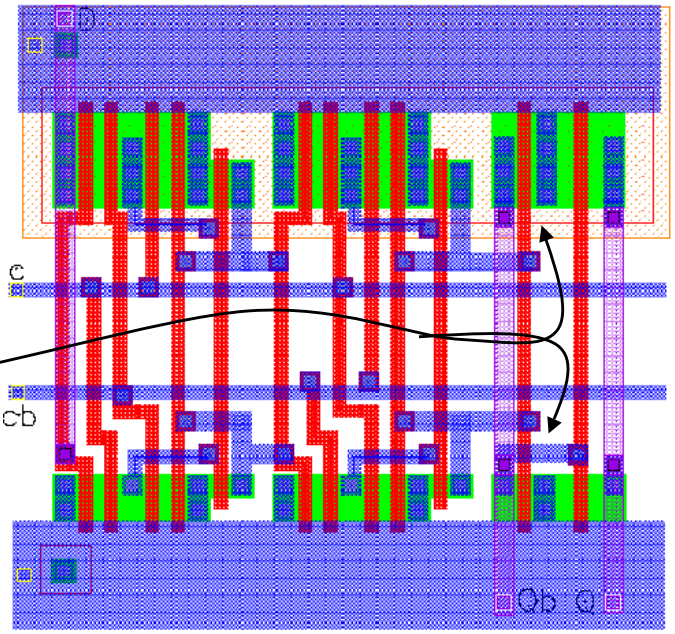
Now Squeeze Inverter

- Select regions of the layout and stretch to move it all to a new spot



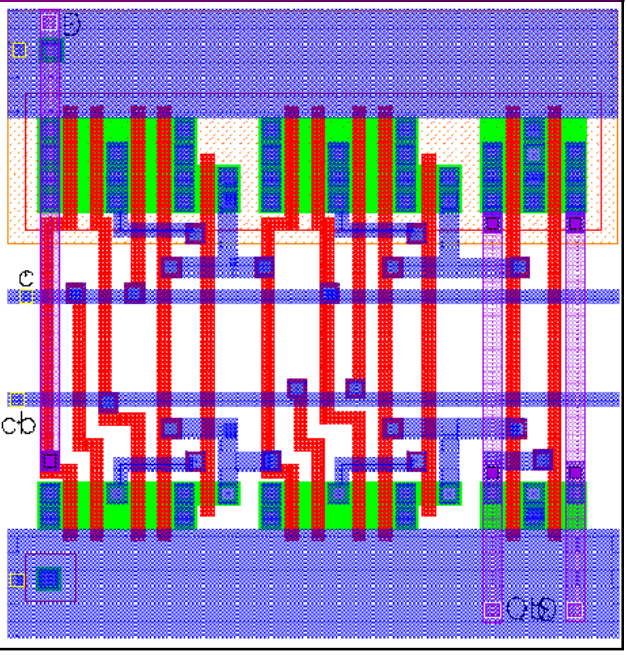
Keep Squeezing

- Now squeeze power supply contacts



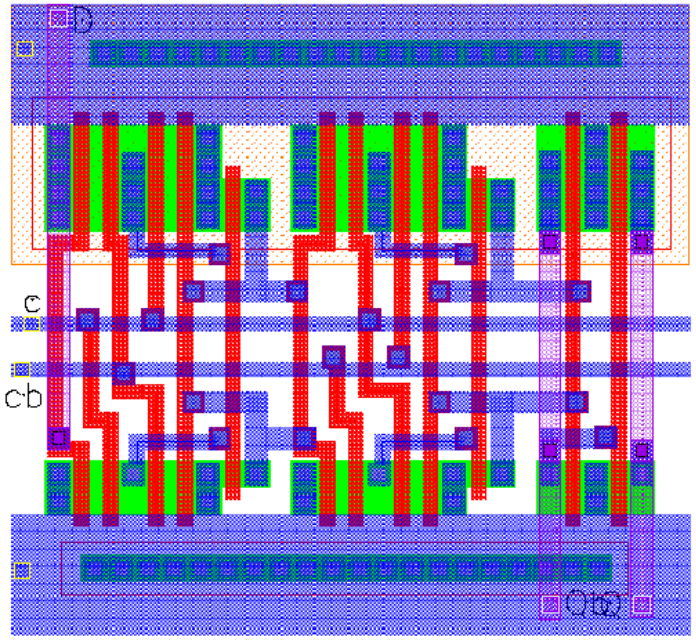
Squeezed Version

- Output inverters squeezed together
- Note that D, Q, And Qb are routed vertically in M2

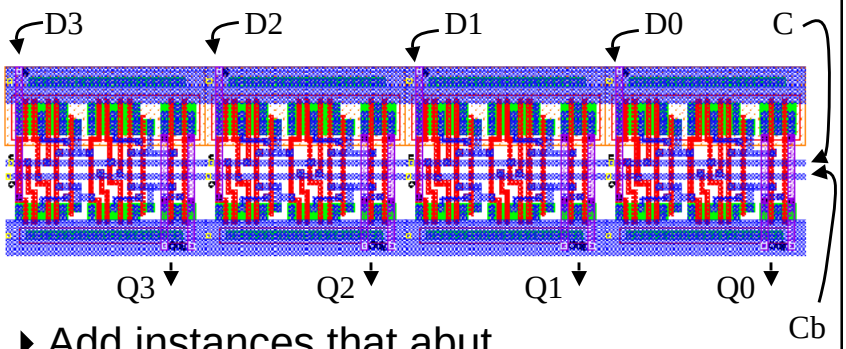


Final D-Type Flip Flop

- Squeeze vertically since I don't need extra routing channels, and I don't need to match with standard cells
- Add long TUB and SUB contacts

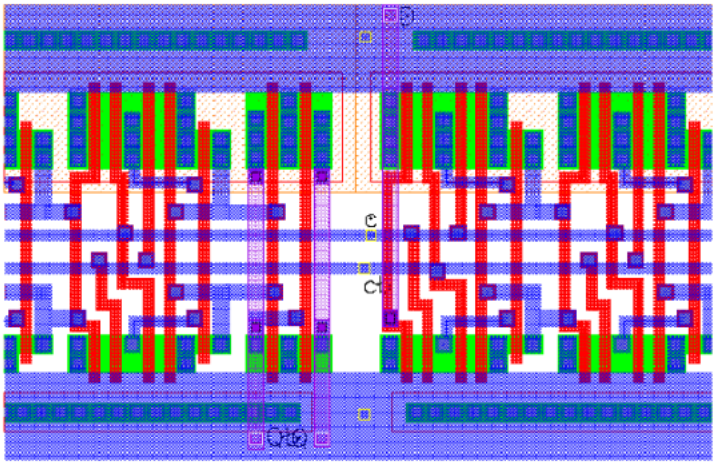


Put Four of them Together



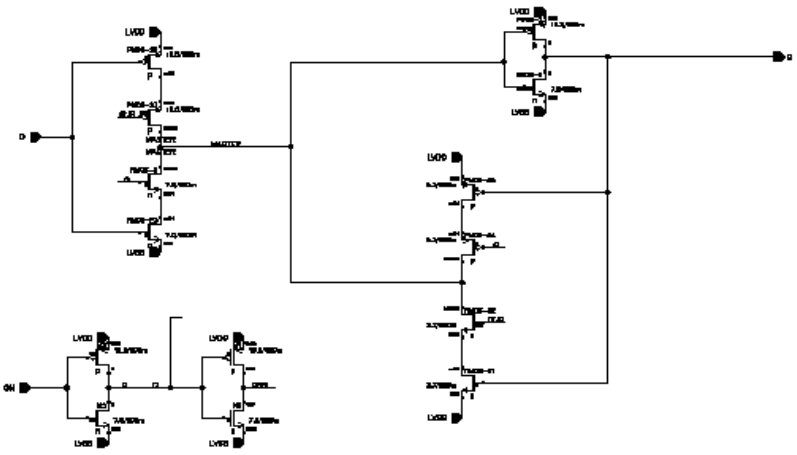
- Add instances that abut
  - Or use the "array" feature of the instance dialog
- Note that C and Cb are routed in horizontal M1

Zoom in to Cell Boundary



- There's a little extra space
  - Cause by wanting each latch to DRC on its own
  - Could close this up by overlapping cells

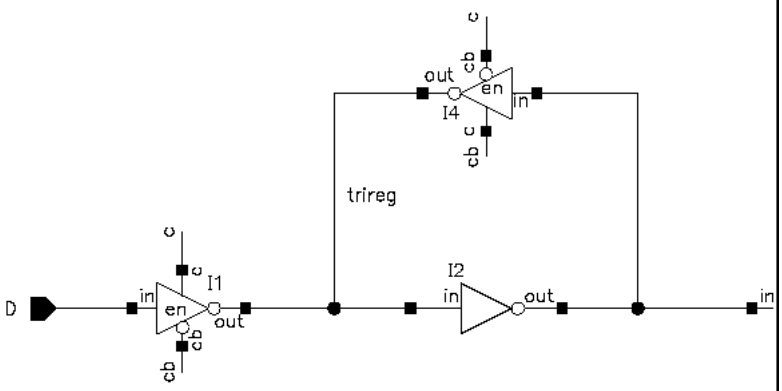
Standard Cell D-latch



- Pretty much the same circuit
  - Without extra Q/Qb driver inverters

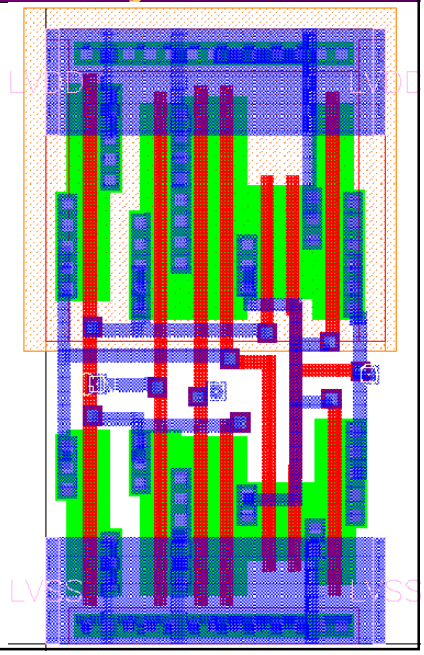
Here's My Latch

- I didn't include the C/Cb inverters
  - Otherwise it's pretty much the same
  - They used very different transistor sizes

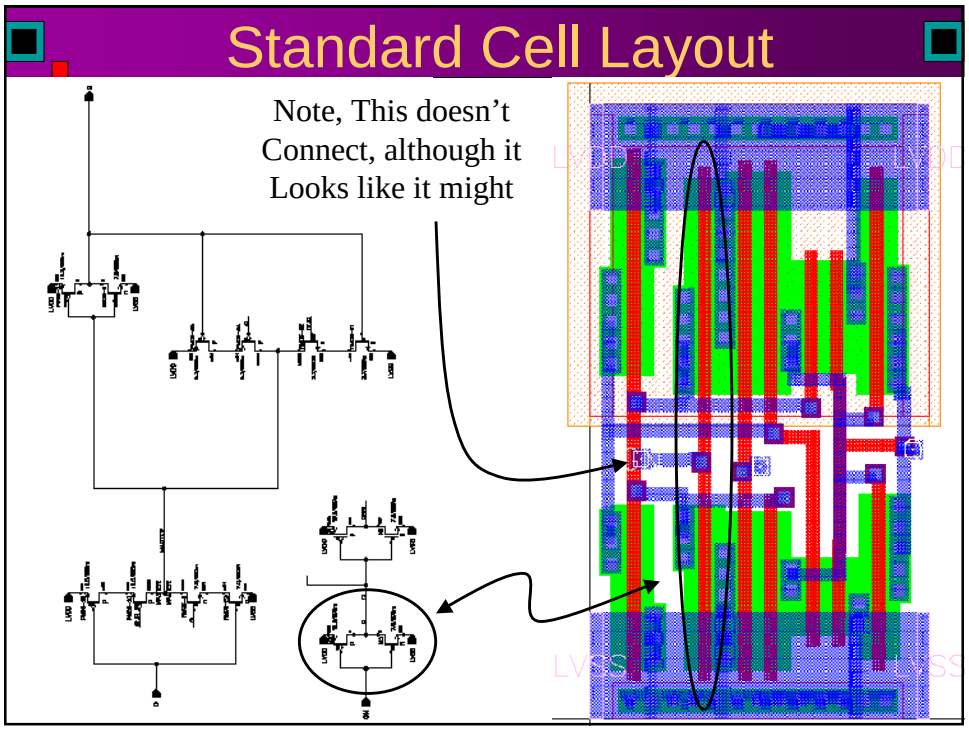


Standard Cell Layout

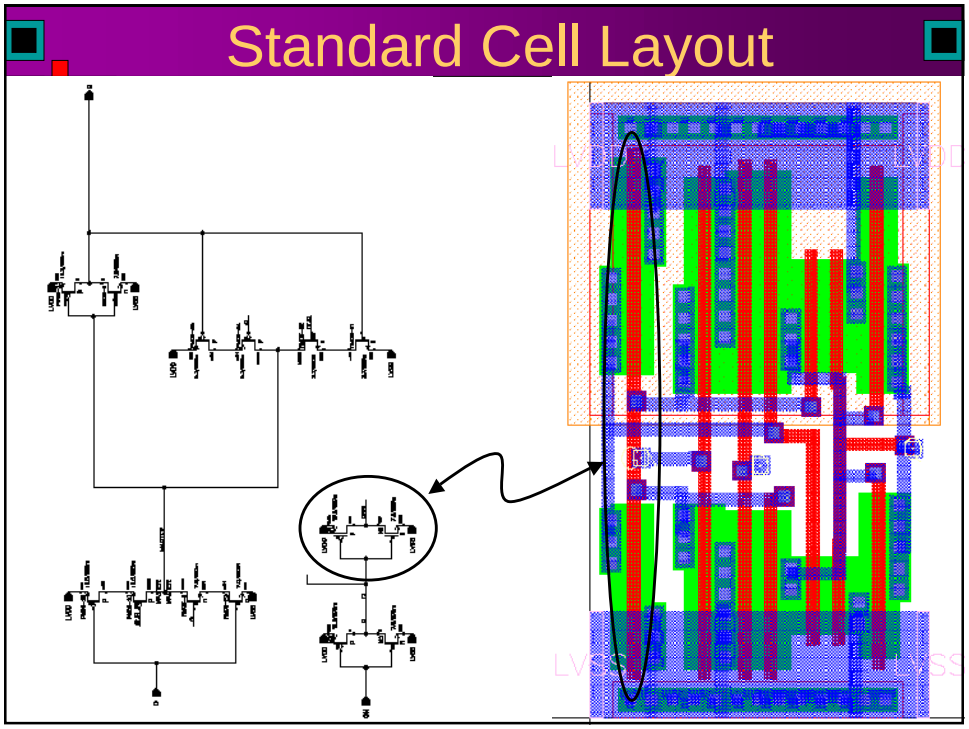
- Because it's a "standard cell," they use much larger transistors
  - They assume you'll be driving large loads
- Also two sizes of EnInv transistors
  - Feedback gate is smaller



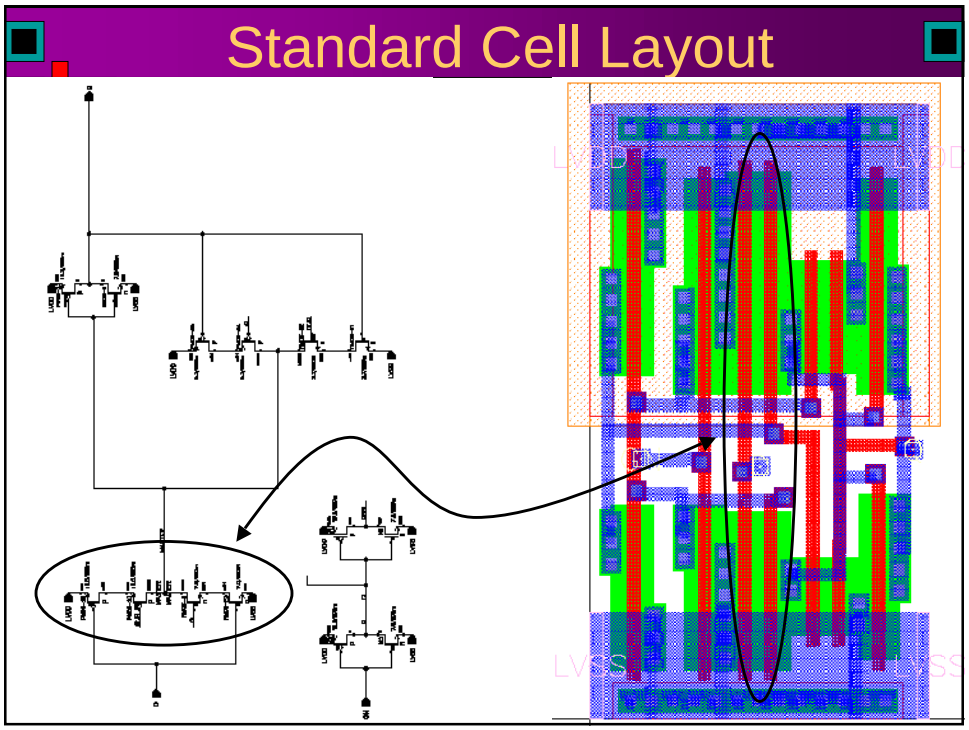
Standard Cell Layout



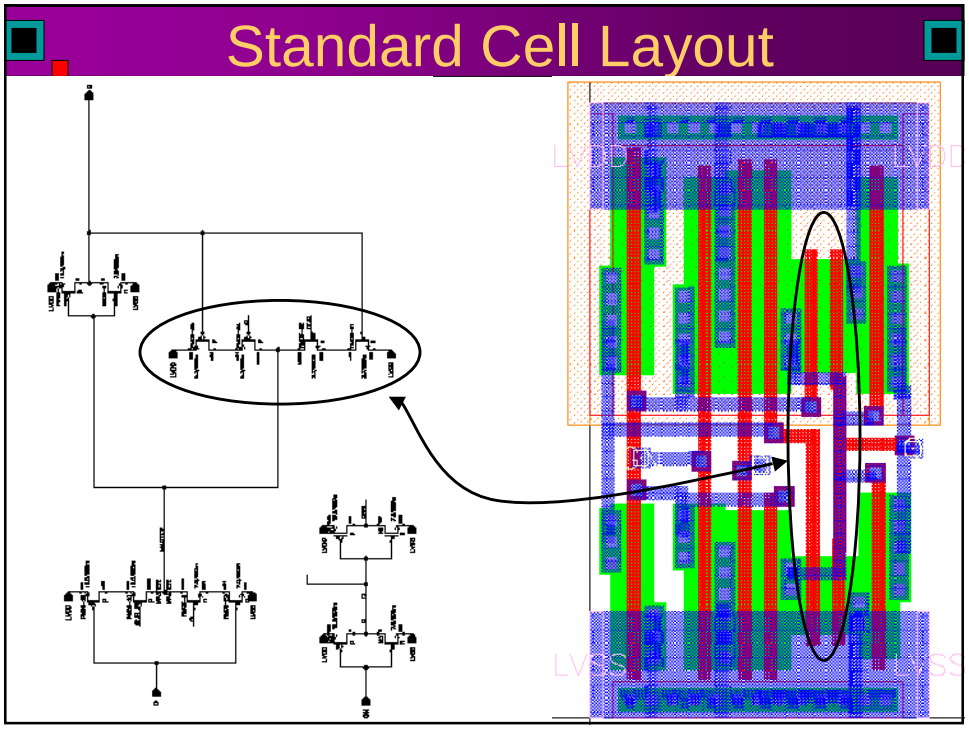
Standard Cell Layout



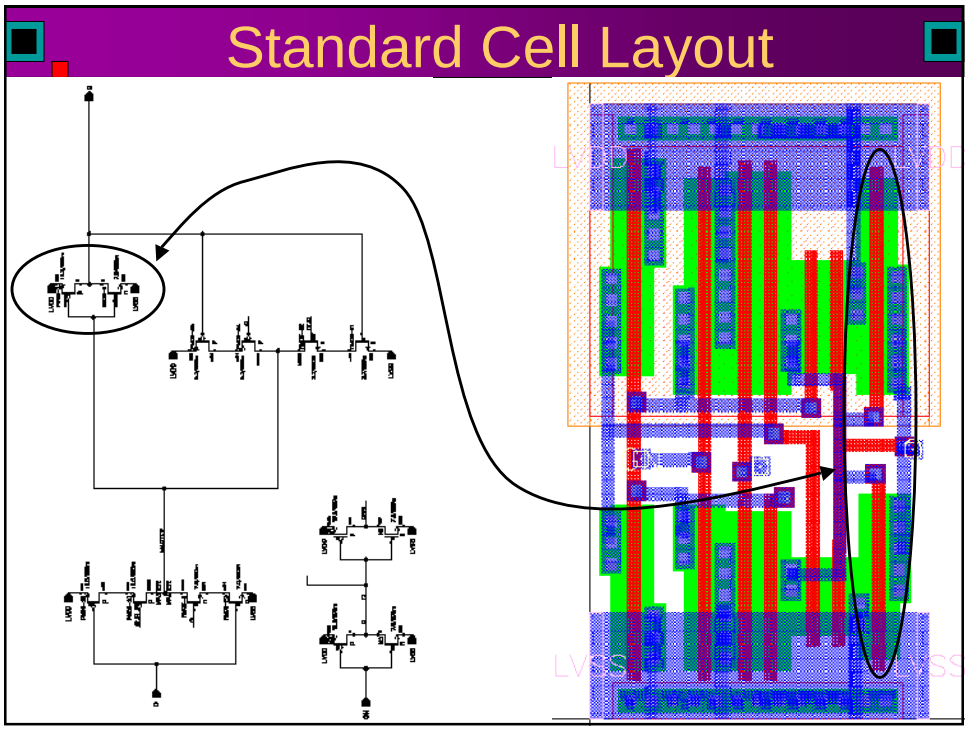
Standard Cell Layout



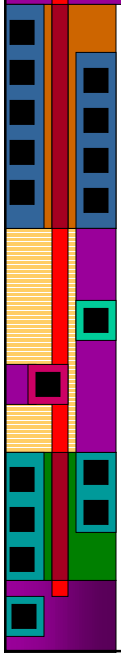
Standard Cell Layout



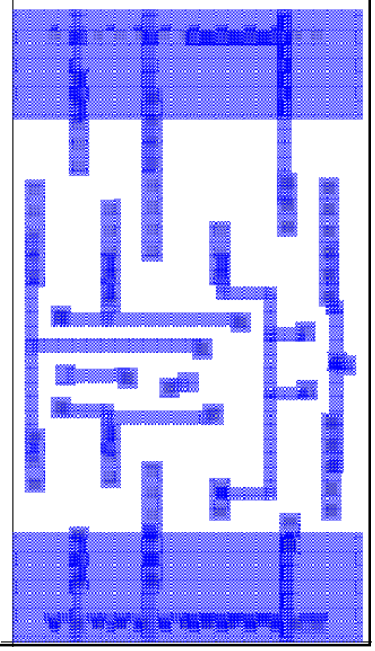
Standard Cell Layout



M1 Layer of Standard Cell

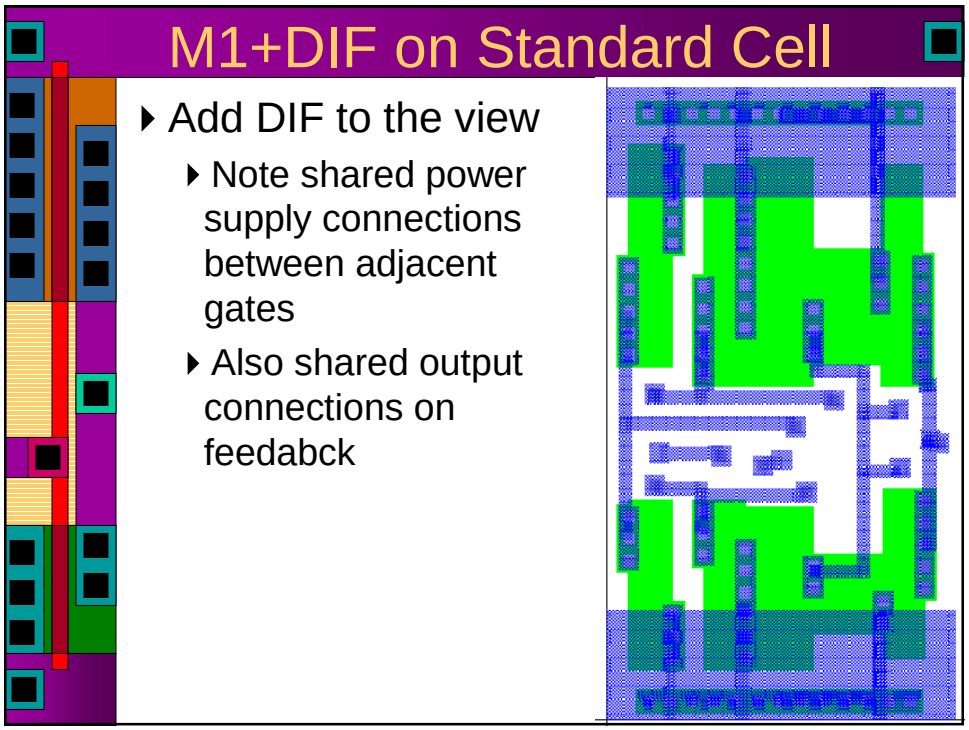


- It's both horizontal and vertical
  - Not designed for routing any signals through the cell on M1
  - Connections are by M2 wires from top or bottom



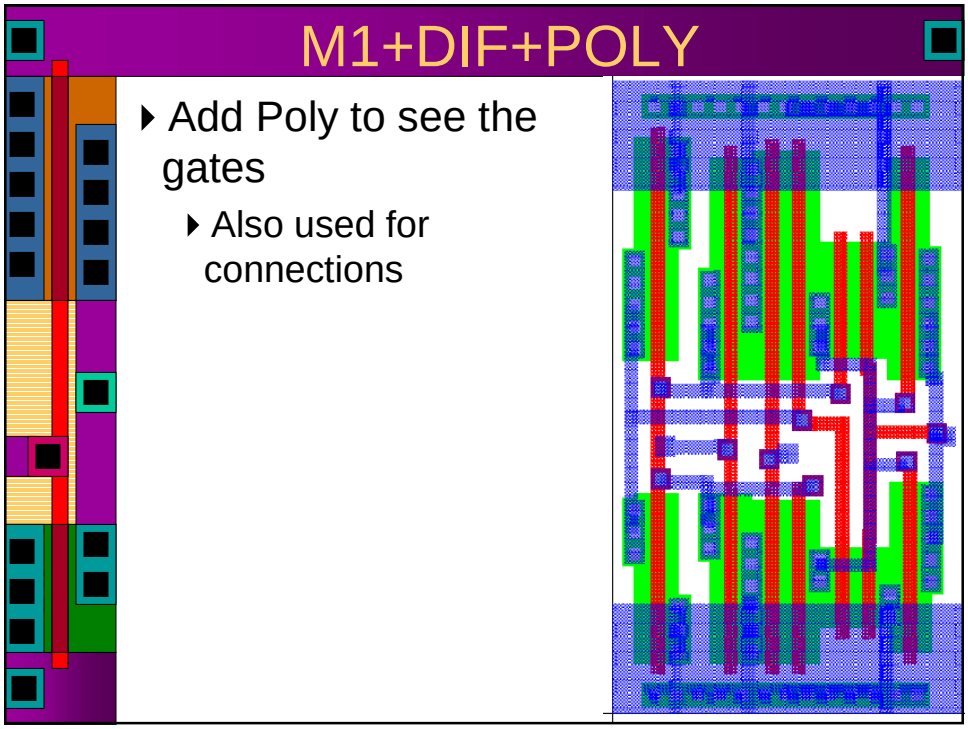
M1+DIF on Standard Cell

- Add DIF to the view
  - Note shared power supply connections between adjacent gates
  - Also shared output connections on feedabck



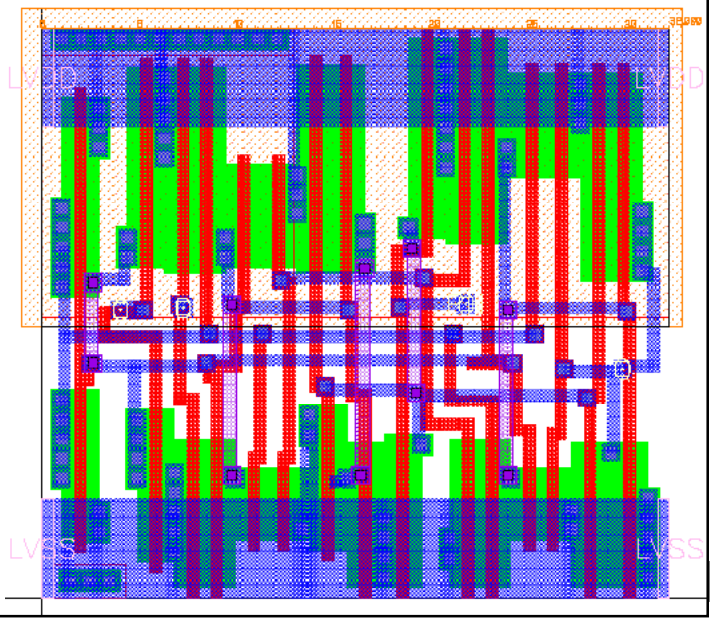
M1+DIF+POLY

- Add Poly to see the gates
  - Also used for connections

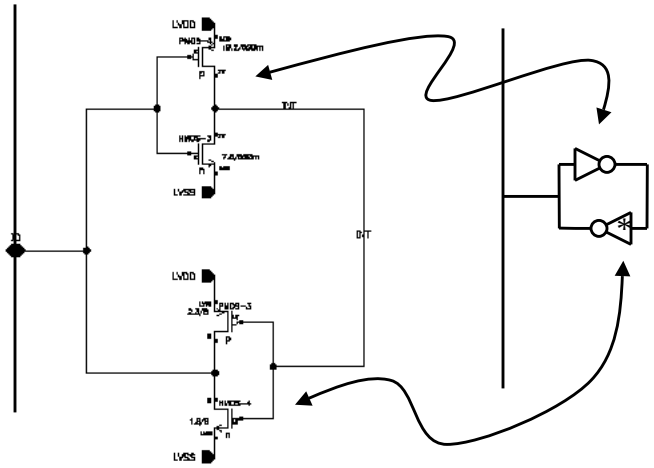


Std Cell D Flip Flop

- Basically 2 latches attached together
- Includes C/Cb inverters



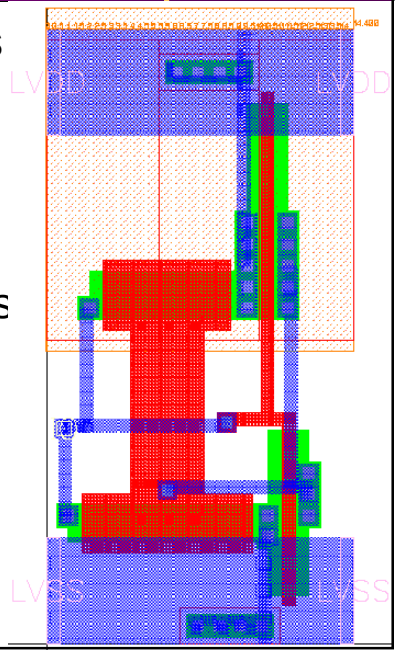
Keeper Latch – Weak Feedback



- Use week feedback to hold a value on a bus when it's undriven
  - Also used for some register/latch cells

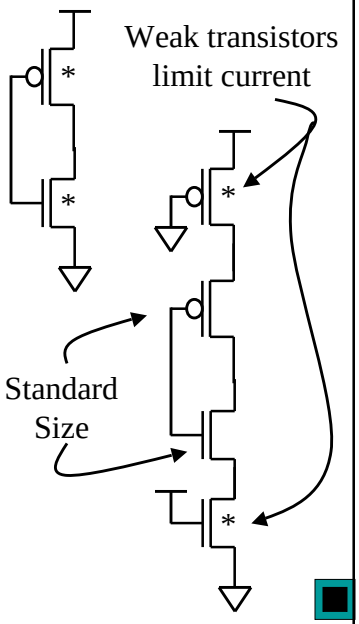
Weak Feedback Keeper

- Regular inverter uses wide transistors
  - Typical of standard cell conventions
- Week inverter uses very LONG transistors
  - Reduces Beta
  - Reduces current
  - Increases resistance



Another Weak Feedback Plan

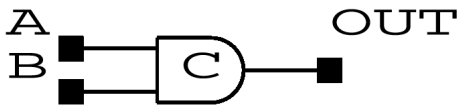
- Problem is that the long transistors in the weak feedback device have a lot of area
  - Thus a lot of capacitance
  - You can reduce the Beta of the inverter by limiting the current in the pullup and pulldown tree, but still drive small transistors



Example: C-Element

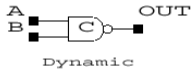
- A type of S/R latch
  - Sets if both inputs are 1
  - Resets if both inputs are 0
  - Holds if inputs are different values

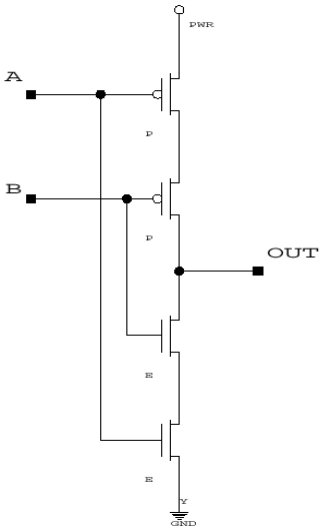
A	B	Out+
0	0	0
0	1	Out
1	0	Out
1	1	1



Inverting Dynamic C-element

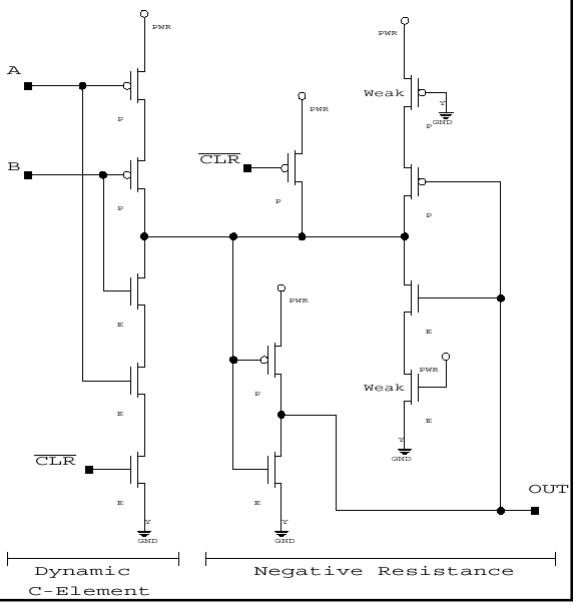
- If both A and B are low, output is pulled high
- If both A and B are high, output is pulled high
- If they are opposite, output is not driven
  - Relies on capacitance of output node for storage



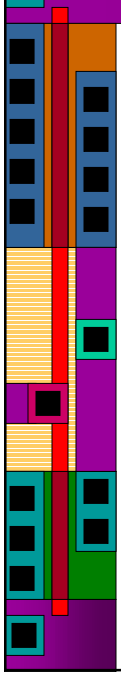


C-element with Weak Feedback

- Dynamic C-element followed by an inverter
  - Uses a weak feedback inverter for storage
  - Clear pulls up internal node
  - Note it also turns off pulldown tree so there's no fighting



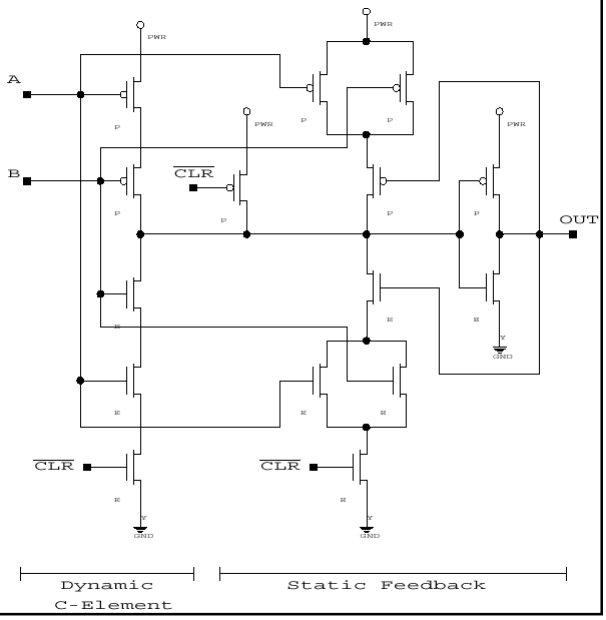
Weak-Feedback C Layout



- I couldn't find it…

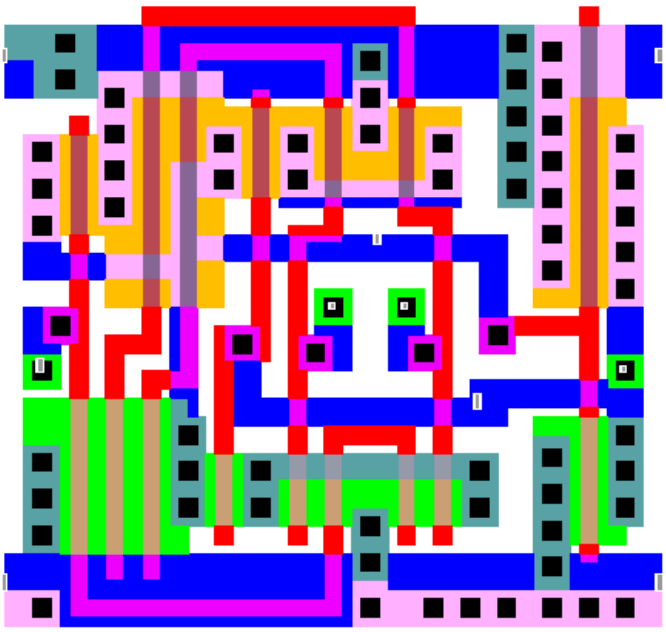
Static Feedback C-element

- Still based on a dynamic C followed by an inverter
- But this time the feedback only pulls the right way
- There's never any fighting as with a weak feedback
- Clearing works the same way



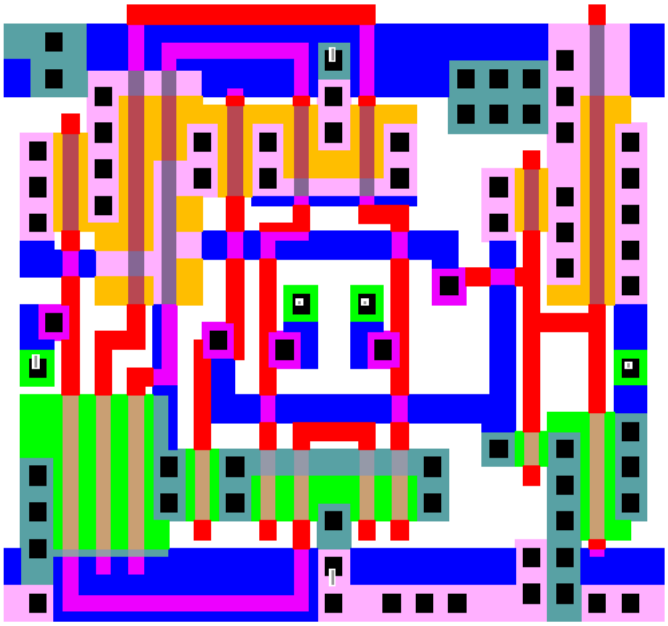
Static Feedback C Layout

- Built for a different standard cell template
  - Only two metal layers
- Note use of Poly for routing



Slightly Different C Layout

- Note extra inverter near output stage
- Output inverter is not used to drive feedback



Another Version, Same Layout

- MCb routing in poly
- Power supply routing in M2
- Smaller transistors in general
- TUB and SUB contacts in contact stacks