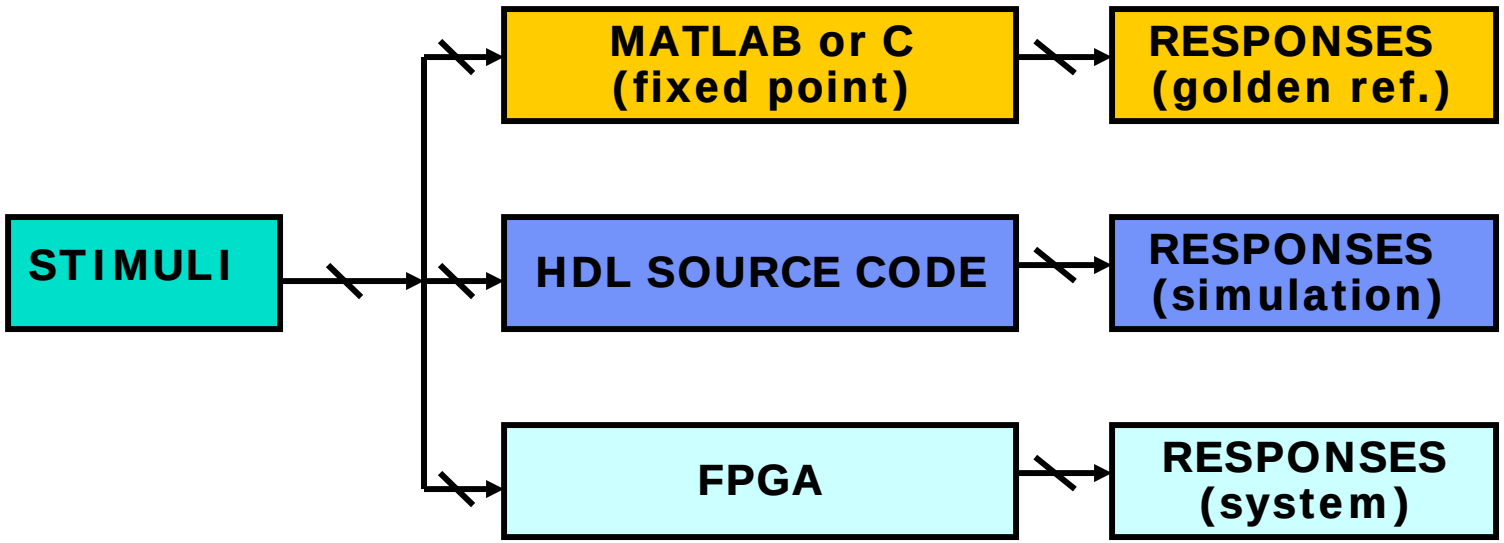
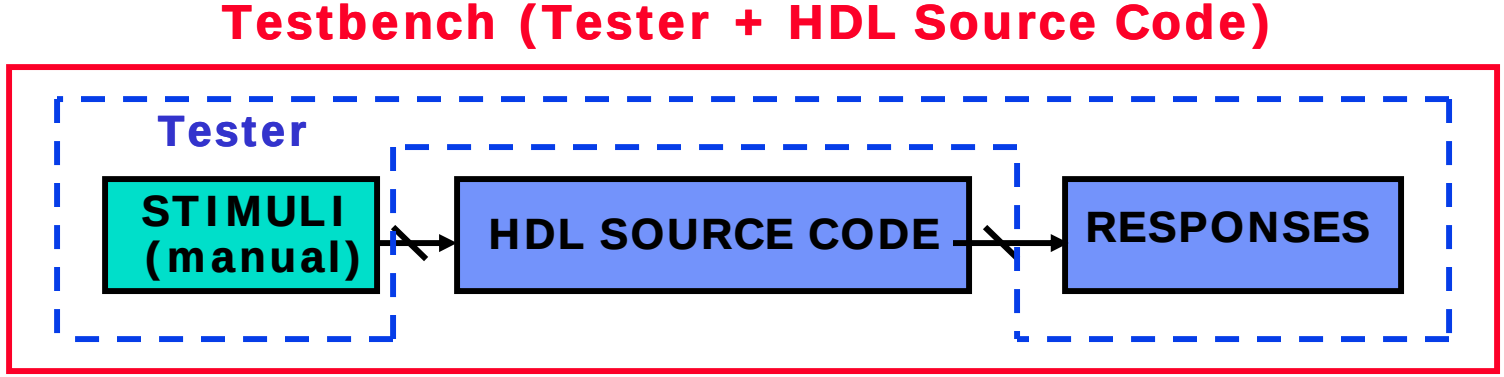
DEVELOPING QUALITY IP

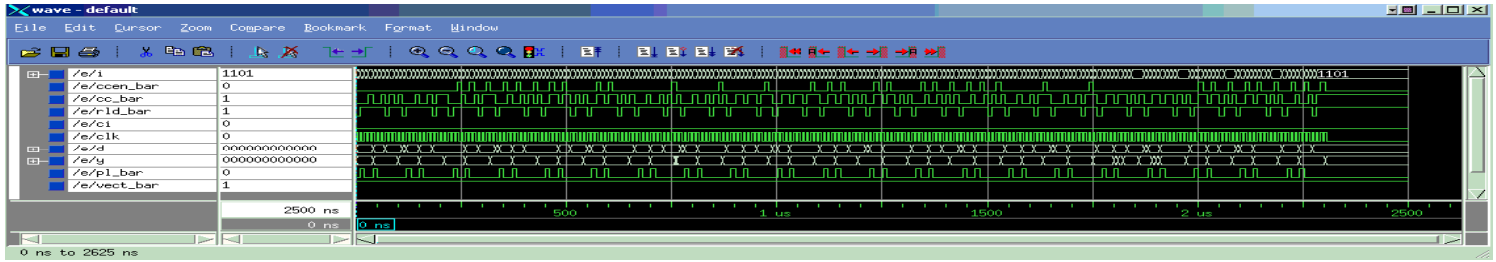
- Requirements should be mapped into an executable specification which produces the desired golden reference responses.
- HDL and FPGA responses must match the golden responses identically.



THE TESTBENCH CONTAINS THE STIMULI, RESPONSES AND UUT

- Functional stimuli are developed by the designer to mimic the system environment.
- The tester is written in HDL but is not synthesized into the FPGA.





RAPID VERIFICATION SAVES TIME

- **Minimizing time-to-market encourages designers to develop only a few tests for simulation and then proceed to testing the design inside the FPGA in its real-world environment. The FPGA executes tests 500x faster than the simulator and the real-world system environment produces the tests automatically.**