Characterization of Surface Channel CCD Image Arrays at Low Light Levels

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Abstract—**The characterization of surface channel charge-coupled device (CCD) line imagers with front-surface imaging, interline transfer, and 2-phase stepped oxide, silicon-gate CCD registers is presented in this paper. The analysis, design, and evaluation of 1 × 64 CCD line arrays are described in terms of their performance at low light levels. The signal-to-noise(S/N) is formulated in terms of charge at the collection diode. A dynamic range of 80 dB and a noise equivalent signal (NES), where S/N = 1, of 135 electrons is achieved with a picture element time of 20 μs and an integration time of 1.32 ms in the absence of a fat zero. A unique CMOS readout circuit, which uses correlated double sampling within a picture element time window, removes the Nyquist noise of the reset switch, eliminates switching transients, and suppresses low-frequency noise to provide low-noise analog signal processing of the video signals. This paper describes the responsivity, resolution, spectral, and noise measurements on silicon-gate CCD sensors and CCD interline shift-registers. The influence of transfer inefficiency and electrical fat-zero insertion on resolution and noise is described at low light levels.**

I. Introduction

CHARGE-COUPLED devices (CCD's), since their invention [1] and experimental investigation [2], have promised low dispersive, analog delay lines with low-noise signal propagation and high dynamic range. The CCD analog delay line may be coupled with a monolithic photosensor, such as a "semitransparent" silicon-gate CCD or diffused photodiode, and a low-noise monolithic preamplifier to provide low light level imaging. The transfer inefficiency ϵ, in practical *surface-channel* CCD structures, is determined by surface-state trapping [3] which limits the free-charge transfer process and introduces dispersion [4] into the analog delay line. The CCD analog delay line should have a $NP\epsilon \leq 0.1$ (N = number of bits, P = number of phases) to prevent loss in image resolution or modulation transfer function (MTF) degradation.

The CCD imager uses the flow of minority carriers to transfer the video signal to a low capacitance collection diode. The collection diode is typically 0.25 pF in the CCD imager, whereas, the readout line capacitance in the x-y addressed image arrays is at least an order of magnitude larger in value. The low capacitance provides a reduction in noise and an increase in voltage swing at the gate electrode of an on-chip MOS electrometer amplifier. Thus, with the CCD principle a photon-generated signal charge may be transported over long distances within the silicon and amplified at low input noise charge levels. Although the clock and video signal levels are noninteracting within the CCD imager, there is an interaction at the collection diode. We have developed a method of signal processing called *correlated double sampling* [5], [6] to remove the switching transients, eliminate the Nyquist noise associated with the reset switch/node capacitance combination, and suppress "1/f" surface-state noise contributions. With this technique we have realized the intrinsic noise equivalent signal (NES) of the CCD imager which is set by the thermal "shot" noise of the leakage current. In the CCD imager the video signal is processed within the array by an analog CCD shift register, whereas, in non-CCD arrays the signal is transferred from the sensor to the video preamplifier by the closure of an address switch with a gate pulse from a digital shift register [7], [8]. Thus, in a CCD imager we require analog characteristics from both the sensor and the shift register, and this dual requirement places limitations on yield due to the presence of nonuniformities within the array.

II. CCD Line Arrays

General Considerations

Fig. 1 illustrates the line array functional block diagram. The *interline transfer* approach requires a transfer pulse ϕ_T, at the start of a line time, to transfer the stored photocharge from the individual sensor locations to a corresponding bit in the parallel-to-serial CCD shift register. In our case, a 2-phase clock system transfers the charge along the shift register to a CMOS readout circuit. The shift register is a 2-phase stepped-oxide geometry with a surface field and potential profile as shown in Fig 2. Fig. 3 is an enlargement of the CCD line array after the definition of the shift register with an aluminum interconnection. The sensors are constructed with transparent, conductive, polycrystalline silicon-gate electrodes with an n^+ stopper diffusion (n-type, ⟨100⟩ substrates) on three sides. This diffusion reduces the interaction between adjacent elements and inhibits blooming in the array. The sensor bias voltage is adjusted such that the maximum collected charge at any sensor location cannot overflow the storage well of the shift register. The fourth side of

Manuscript received May 8, 1973; revised July 23, 1973.
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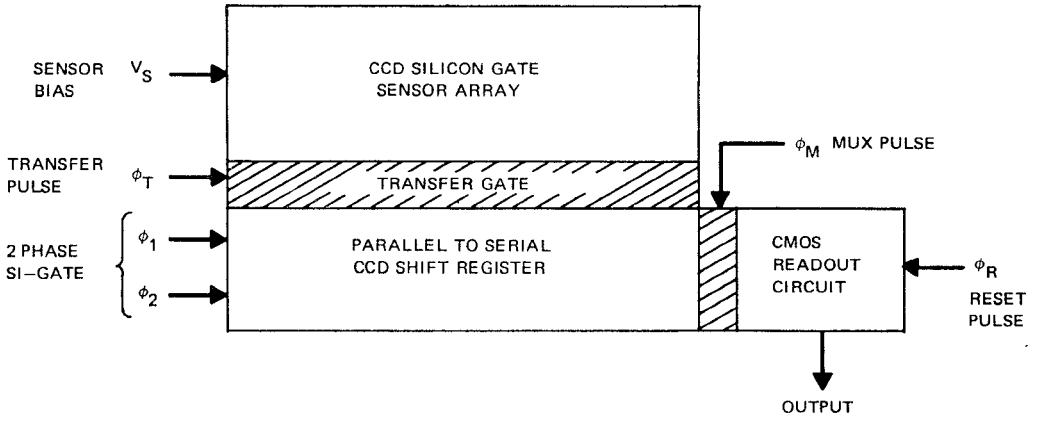

Fig. 1. CCD line array functional block diagram illustrating interline transfer.

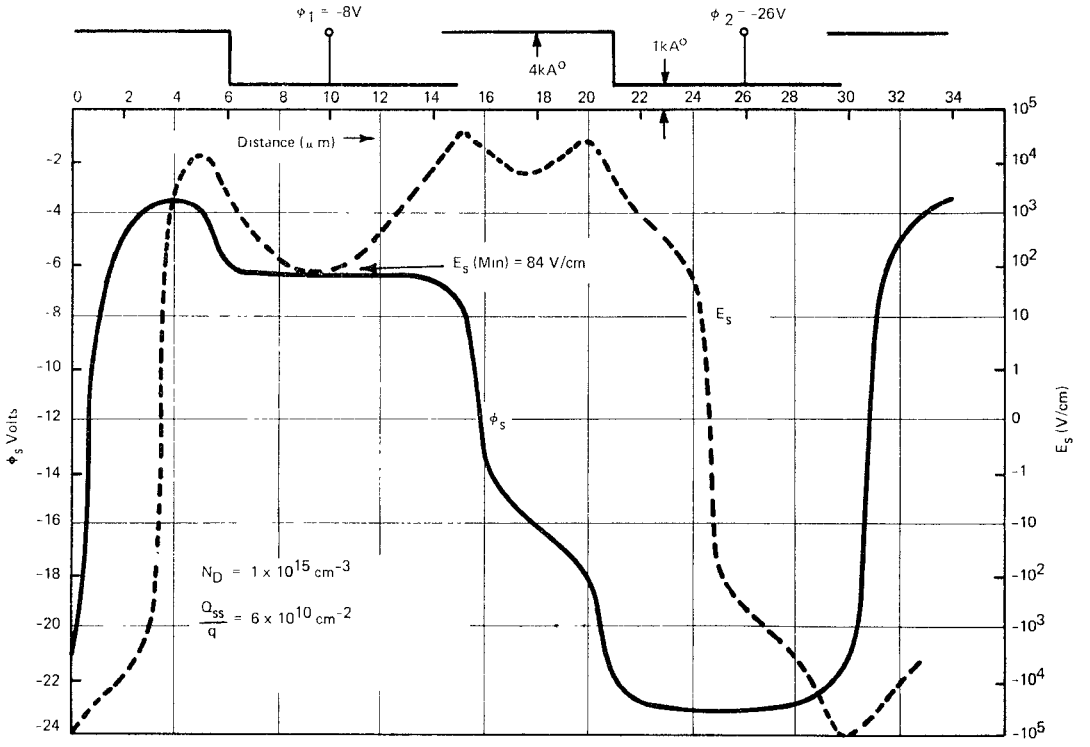

Fig. 2. Two-phase stepped oxide CCD unit cell with curves of periodic surface potential and Longitudinal electric field relative to electrode cross section at top of figure.

the CCD sensor is "stoppered" by holding the transfer gate at a positive potential with respect to the substrate during the integration period to form an n^+ accumulation layer. The sensors are defined by and aluminum light shield which also serves to cover the CCD shift-register and CMOS readout circuits. The CCD line array is constructed of 128 CCD sensors with a $2P$ offset in the along-track direction ($P = 15$ μm, $\Delta x = 22$ μm, $\Delta y = 18$ μm). The dimension Δx is in the across-track electron-scan direction and Δy is in the along-track mechanical-scan direction.

Fig. 4 illustrates the CMOS readout circuit which consists of a multiplex gate (i.e., muxgate ϕ_M), a reverse-biased collection diode, n-channel MOS reset switch (i.e., reset gate ϕ_R), and p-channel MOS electrometer amplifier. The voltage waveform on the gate of the electrometer is also displayed in Fig. 4. Below the waveform four distinct timing intervals are labeled for discussion. These four timing intervals comprise a *pixel* (i.e., picture element) time and form the basis of a signal processing method called *correlated double sampling*. The node capacitance at the collecting diode is 0.25 pF and is not influenced by the parasitic n^+/p^- diode of the reset switch which is reverse-biased to prevent discharge of the collecting node by the reset feedthrough "pedestal" when the reset switch is turned off. The aluminum light shield provides about 0.03 pF of the node capacitance since it rests over 1.3 to 1.5 μm of deposited SiO_2 and forms a ground plane to shield the sensitive output collection circuit from pickup.

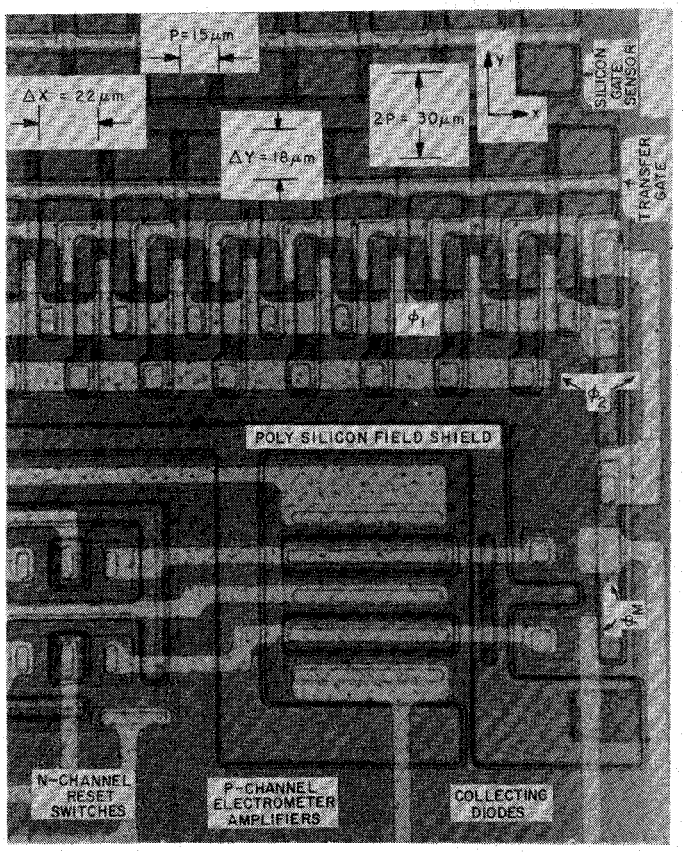

Fig. 3. CCD "interline-transfer" line array with CMOS readout circuit (prior to aluminum light shield).

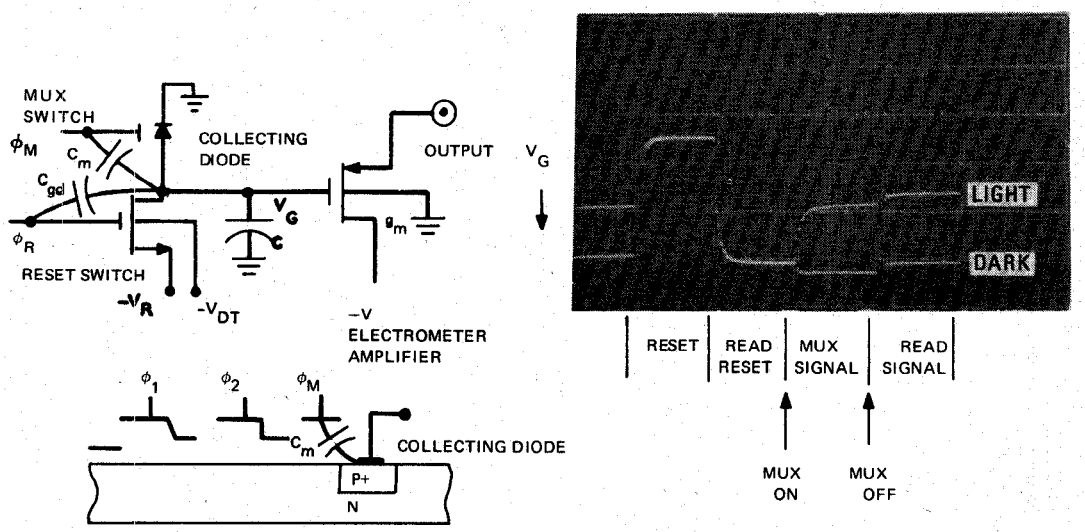

Fig. 4. "On-chip" correlated double sampling (CDS) readout circuit with gate voltage waveform comprised of separate sequential steps.

III. Correlated Double Sampling Analog Signal Processor

In the use of a CCD sensor array the natural output is charge integration, and sampling techniques are advantageous to provide on-chip signal processing and reconstruction. In the introduction we mentioned a major limitation to x-y addressed image arrays was the interaction of the clock pulses with the video signal charge to be detected and amplified. In addition to this problem, the random rise and fall times of the clocks give rise to frequency components which fall in the passband of the video preamplifier. The minimum detectable signal or noise equivalent signal (NES) after preamplification was set by the system noise in these image arrays. It seemed as though all of the effort was placed on sensor development with little emphasis on the problem of signal detection and video processing. With the advent of CCD

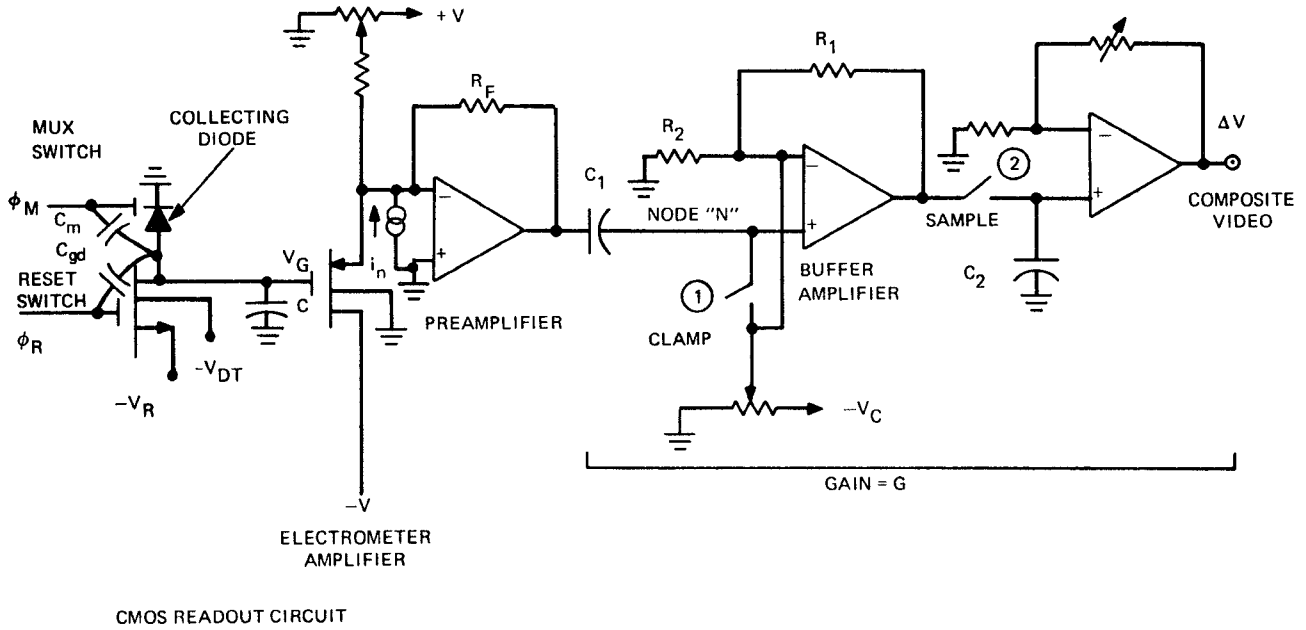

Fig. 5. Schematic diagram of a CDS processor with critical capacitances, noise sources, and signal nodes.

imagers, the integrity of the signal charge is maintained until signal detection occurs at a common collection diode. The importance of this point cannot be emphasized too strongly since the problem of signal and clock interaction is localized at a common readout circuit. All of the pixel information passes through a common collection diode, integrating capacitance, and electrometer amplifier. This is true for the line and area CCD imagers. We also mentioned in the introduction the low output capacitance ($C = 0.25$ pF) at the collection diode. For a well designed 10-MHz video amplifier, as used with a vidicon, the shunt capacitance may be 20–30 pF. For a noise current i_n, which is shown at the input to the preamplifier in Fig. 5, the equivalent noise charge at the collection diode is $C\ i_n/g_m$. Thus, the small C/g_m of the electrometer increases the signal-to-noise charge ratio at the collection diode for such noise currents as shot noise, preamplifier noise, surface-state noise, and supply noise.

Let us examine the four distinct timing intervals employed in the readout circuit of Fig. 4.

1) Reset: The n-channel MOSFET reset switch is turned on and the voltage V_G across the capacitor C is reset to the reference voltage V_R with a noise uncertainty V_n. This noise voltage may be introduced through inadequate filtering of the reference supply voltage and the Nyquist noise contribution of the reset switch, [9], [10] where the latter is given by $V_n = (kT/C)^{1/2}$ or in terms of noise charge $Q_n = (kTC)^{1/2}$. The full Nyquist voltage appears across C when the electrical time constant formed by the series resistance of the reset switch and integration capacitance C is much less than the time the reset switch is on. The p-channel electrometer is connected to an operational amplifier which is the preamplifier in the CCD signal processor circuit shown in Fig. 5.

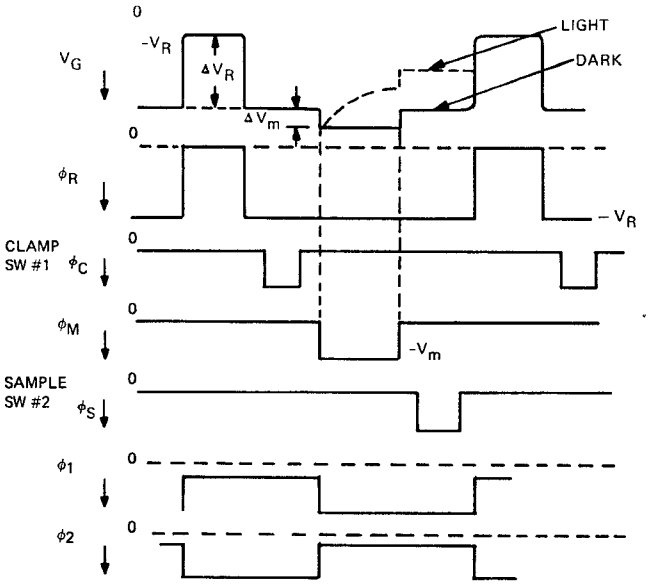

Fig. 6. Timing diagram for CCD line array with CDS analog signal processor. The four steps are separated in sequence to correspond to explanation in the text.

The timing diagram for the signal processing is illustrated in Fig. 6. At the start of the reset interval the pixel charge is in transit to the last well (i.e., see phase ϕ_2 and Fig. 4) of the electrical bit adjacent to the muxgate ϕ_M and the collection diode.

2) Read Reset: After the n-channel reset switch is turned off, the voltage present on the gate of the electrometer consists of a feedthrough pedestal ΔV_R and a noise voltage V_n. With the reset switch off, the gate voltage is holding on a high impedance point with a time constant of seconds. In the read reset interval, the clamp switch 1

is turned on and C_1 is charged to a voltage indicative of the voltage on the gate of the electrometer. Switch 1 is turned off and one side of the capacitor, node N, is *clamped* or dc restored to a reference voltage V_c, while the other side of the capacitor represents the instantaneous sample of the gate voltage. The instantaneous voltage across the clamp switch from this moment on is the differential or incremental charge caused by a change in the on-chip gate or collection diode voltage. With the clamp switch turned off, the measured reset level is holding on the high impedance node N formed by the clamp capacitor C_1, and the noninverting input of the buffer amplifier.

3) Mux Signal: At the start of the mux signal interval the pixel charge is raised in the storage well (ϕ_2 goes high) and ϕ_M goes low to transfer the pixel charge to the collection diode. The collection of pixel charge (minority carriers) discharges the voltage V_G as shown in the signal waveform of Fig. 4. If we assume, for the moment, there is no pixel charge, then the only charge transferred to the gate electrode is the feedthrough pedestal $\Delta V_m = V_m C_m / C$, where V_m is the mux voltage swing and C_m the feedthrough capacitance from the muxgate to the collection diode. The charge is removed, however, when the muxgate is turned off as shown in Fig. 4. A Nyquist noise of $Q_n^2 = 2KTC_m$ is introduced, which may be minimized for $C_m < 0.01$ pF for the case where the muxgate does not overlap the collection diode. Alternatively, an overlapping muxgate ϕ_m may be held at a fixed d-c potential with the clock ϕ_2 transferring charge to the collection diode (see Fig. 4). In the absence of any optical pixel charge we would collect the leakage current from the sensor and the shift register wells.

4) Read Signal: After the mux signal is turned off, the running output voltage on node N is the *time difference* between the previously clamped reset level and the hame reset level plus signal increment introduced by the closure of the mux switch (i.e., there is negligible leakage of the reset level between read reset (clamp) and read signal (sample) intervals). *Thus, the reset noise, which includes Nyquist noist and V_R power supply noise, is correlated within a pixel time window.* The signal increment, which consists of sensor and shift register leakage current added to photocharge, is amplified and passed to the output of the signal processor by the closure of the sample switch 2. The output video stream is a sequence of pixel element responses free from reset noise and proportional to the minority carrier signal increment introduced by closure of the mux switch.

The correlated double sampling (CDS) method removes switching transients similar to an earlier technique [11] which used a gated charge integrator in lieu of storing (clamping) the actual diode reset level for subsequent subtraction from the reset level plus signal increment to give the signal increment without reset noise. The Nyquist noise of the reset switch has been removed

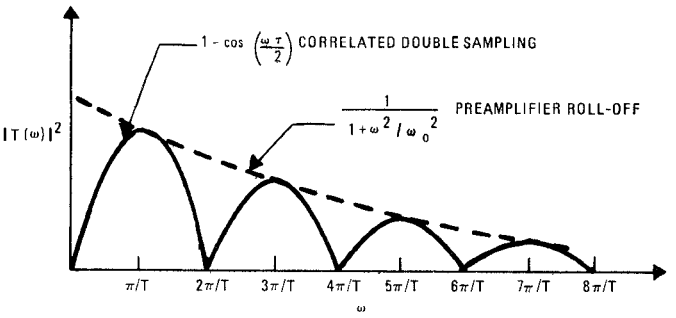

Fig. 7. Filter characteristic of CDS analog processor with $\tau = T/2$.

since it is correlated within a pixel time, and this means a removal of a noise charge

$$Q_n = \frac{(kTC)^{1/2}}{q} = 200e^- \tag{1}$$

for a 0.25 pF capacitor. The "$1/f$" surface-state noise is also suppressed by the filter characteristic of the analog signal processor which is shown as follows.

The transfer function, which acts on any time-varying components of the signal between clamp and sample intervals, may be written as

$$T(s) = T_0 \frac{(1 - e^{-s\tau})}{1 + s/\omega_0} \tag{2}$$

where T_0 is the signal gain and τ is the delay time between the end of the clamp pulse and the end of the sample pulse, and ω_0 is the bandwidth of the front-end preamplifier. Fig. 7 illustrates a plot of the filter characteristic for a value of $\tau = T/2$, where T is the clock period. The important features of this filter are the "double zeros" of $|T(\omega)|^2$ at $\omega = 2N\pi/T$ ($N = 0, 1, 2, \cdots$). The "double zero" at the origin ($\omega = 0$) serves to suppress $1/f$ and low-frequency noise arising from power supplies, pulse jitter, etc., and the double zero at even harmonics of the fundamental clock frequency also suppresses surface-state noise generation in the p-channel MOS electrometer amplifier. Thus, the signal processing does not degrade but enhances the qualities of the sensor element by removing the Nyquist noise and filtering the $1/f$ noise while amplifying the signal. In addition to these features, we have automatic dark level subtraction to increase the dynamic range since the video signal is clamped by the reference voltage V_c. There is no need to filter out the clock fundamental and higher order harmonics; and the video output is already in a format for image display or further data processing (see Fig. 8).

IV. Responsivity and Noise Considerations

Analytical Formulation

We can begin by an examination of what we mean by responsivity. We will define this quantity to be R in pA/

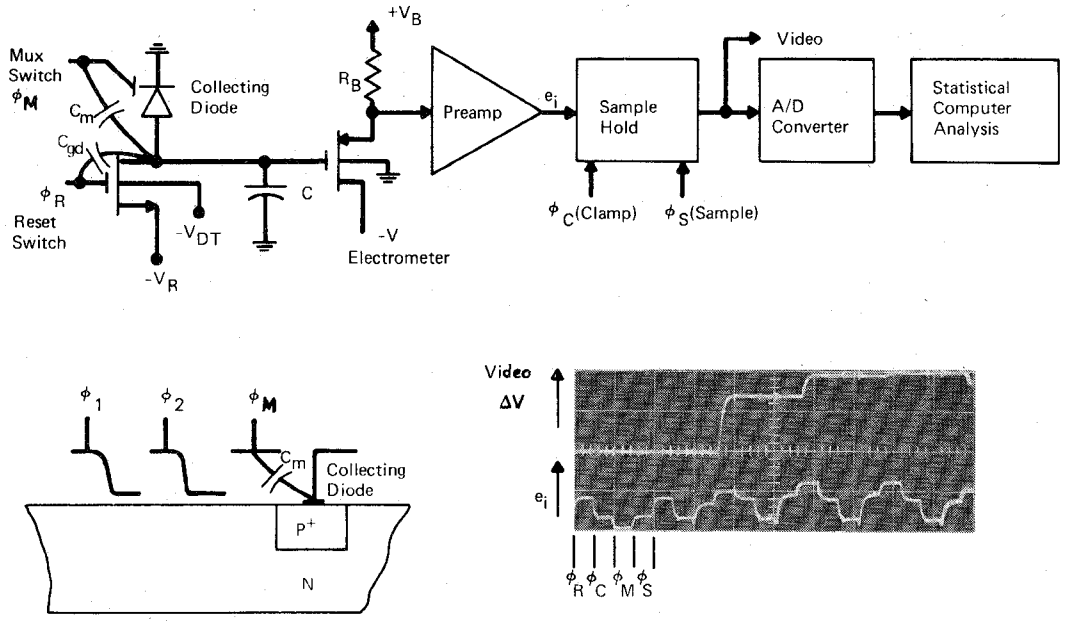

Fig. 8. Test apparatus for measurement of responsivity and noise with typical output waveforms.

mW/m² or current output per input irradiance,[1] which makes the responsivity a function of sensor area. Suppose we attempt to formulate the responsivity by reference to an ideal blackbody source of temperature T_s (e.g., T_s = 6000 K). Thus, we can write

$$R = \frac{\int_{\lambda_1}^{\lambda_2} R_\lambda H_s(\lambda)\, d\lambda}{\int_{\lambda_1}^{\lambda_2} H_s(\lambda)\, d\lambda} = \text{individual sensor responsivity} \quad (3)$$

and

$$R_\lambda = \text{spectral responsivity} = \frac{q\eta(\lambda)A}{hc/\lambda}$$

where H_s is the specified source irradiance, λ_2 and λ_1 the reference spectral band (e.g., λ_1 = 400 nm, λ_2 = 800 nm), A the area of the sensor, and $\eta(\lambda)$ the effective quantum efficiency. Integration of (3) for the specified temperature source and wavelength interval yields

$$R = 0.186\eta\left[\frac{A}{18\ \mu\text{m} \times 22\ \mu\text{m}}\right]\frac{\text{pA}}{\text{mW/m}^2} \quad (4)$$

where η has been assumed to be constant over the wavelength interval. *The experimental responsivity may be referred to the gate capacitance C of the electrometer in Fig. 8 and expressed in terms of quantities in Fig. 5,*

$$R\cdot(1-\epsilon)^{2N} = \frac{C\Delta V}{g_m R_F G \Delta E} = \frac{\Delta Q}{\Delta E}$$

$$= \text{responsivity measured at collection diode} \quad (5)$$

where C is the node capacitance at the gate of the electrometer, g_m the electrometer transconductance, R_F the preamplifier feedback resistance, G the gain of the signal processor following the preamplifier, and ΔV the change in output voltage for a change in input exposure density ΔE. The responsivity of each sensor is degraded by a factor $(1-\epsilon)^{2N}$ where $2N$ is the number of transfers the signal undergoes before it reaches the collection diode. In practice, the integral in the numerator of (3), which represents current output, is obtained with a test source whose spectral irradiance profile is known. The irradiance supplied by the test source, while effective over the entire spectral response of the sensor (i.e., 200 nm to 1200 nm for silicon), is converted to an effective irradiance from a 6000 K blackbody source in the 400 nm to 800 nm window.

The measurement procedure involves the use of a 10-b A/D converter, which provides an accuracy of 1024 b. In practice, the signal output from each sensor element in the array is sampled 1024 times at each irradiance level and recorded in terms of A/D bits. The mean and variance are calculated in A/D bits for each signal. The mean represents the signal while the variance corresponds to the uncertainty or noise as determined over 1024 samples. With these quantities we can determine linearity, streaking, responsivity, noise, etc. The measurement circuit is illustrated in Fig. 8 which shows the timing sequence (discussed in Section III) at the preamplifier output and video output signal. The noise is converted from rms A/D bits to an equivalent input exposure density (microjoules/meter²), called the noise equivalent signal (NES), by multiplying the rms A/D bits by the reciprocal slope of the transfer curve at the particular irradiance level (exposure density). The transfer curve is essentially a plot of signal A/D bits versus input exposure density. The reciprocal slope of the transfer curve is called the quantizing interval and is given as

[1] R may easily be converted to electrons/microjoule/meter².

$$Q_I = \frac{\Delta E}{\Delta(\text{A/D bits})}\left(\frac{\mu\text{J}}{\text{m}^2\cdot\text{bit}}\right). \quad (6)$$

Thus, if we have B_{rms} bits variance at a specified irradiance level, then the NES becomes

$$\text{NES} = Q_I B_{\text{rms}}\ (\mu\text{J/m}^2). \quad (7)$$

The NES, which is measured by the above procedure, consists of 4 principal terms:

1) *System noise* from analog signal processor, power supplies, pulse jitter, mechanical vibrations, etc.
2) *Chip noise* from the CCD sensor array. This noise is determined by geometrical design and fabrication processes for the chip.
3) *Radiation shot noise* from the fluctuation in arriving signal photons and which represents a background limited performance.
4) *Quantization noise* from the uncertainty associated with the finite size of the quantizing interval Q_I.

The measured or total NES is given as

$$\text{NES}_T{}^2(\text{total}) = \text{NES}_{\text{syst}}{}^2 + \text{NES}_{\text{chip}}{}^2 + \frac{qE}{R} + \frac{Q_I^2}{12} \quad (8)$$

where the radiation shot noise term involves the exposure density and the quantization noise assumes an error which varies linearly with time [12]. The system noise can be reduced through painstaking debugging of the voltage logic waveforms, examination of grounding, heavy filtering on supplies, careful layout of the analog signal processor, low noise preamplifier, and high source biasing resistor R_B for a given R_F to reduce Nyquist noise contribution. The quantization interval is determined by the dynamic range requirements and the resolution or accuracy in the measurements. We can determine the system noise by measurement, and see the effect of radiation shot noise through measurements at different exposure densities.

The chip NES is determined by the remaining noise in (8). We can formulate analytically the chip NES at the collection diode in Fig. 4. There are 3 sources of noise on the CCD chip:

1) *Nyquist noise* at the reset switch and output capacitance $Q_n{}^2 = kTC$.
2) *Thermal shot noise* associated with the sensor and shift register $Q_n{}^2 = q[I_{LR} + I_{LS}\ (1 - \epsilon)^{2N}]\tau$, where here τ = line readout time.
3) *Surface state noise* associated with the transfer of charge to and from Si-SiO_2 interface states within the sensor, shift register and electrometer amplifier

$$Q_n{}^2 = kTC_{st}$$

where C_{st} is an effective surface state capacitance determined by the number of transfers, the clock frequency, the effective bandwidth of the signal processor, etc.

We have mentioned that the correlated double sampling removes the *Nyquist noise* of the reset switch; however, to be general we will include this term in the formulation of signal-to-noise which may be written as

$$\frac{\text{S}}{\text{N}} = \frac{\text{signal charge}}{\text{noise charge}} = \frac{R(1-\epsilon)^{2N}E}{(kT(C + C_{st}) + q[I_{LR} + I_{LS}(1-\epsilon)^{2N}]\tau)^{1/2}}. \quad (9)$$

If we set the S/N = 1 in (5)–(7), then the chip NES becomes

$$\text{NES}_{\text{chip}} = \frac{(kT(C + C_{st}) + q[I_{LR} + I_{LS}(1-\epsilon)^{2N}]\tau)^{1/2}}{R(1-\epsilon)^{2N}}. \quad (10)$$

TABLE I
EXPERIMENTAL PARAMETERS OF CCD READOUT CIRCUIT AND ANALOG SIGNAL PROCESSOR

g_m = 250 μmho	G = 2.57	ΔV = 3.56 V
R_F = 75 Ω	ΔE 290 μJ/m²	C = 0.25 pF
A = 18 μm × 22 μm	τ = 1.32 ms	$\epsilon = 10^{-4}$
$2N$ = 5 to 133	V_R = −12 V	

Measurements

Table I lists the experimental measurements of parameters associated with a 1 × 64 element CCD line array. The experimental responsivity calculated from these parameters [see (5)] is

$$R(\text{exp}) = \frac{0.065\ \text{pA}}{\text{mW/m}^2}\left(\frac{406e^-}{\mu\text{J/m}^2}\right) \quad (11)$$

and substitution of (11) into (4) yields

$$\eta(\text{effective}) = 0.35 \quad (12)$$

for the CCD sensor. The effective quantum efficiency for this CCD sensor must be taken with caution since the relative spectral response profile displays interference fringes due to the $2k$ Å polysilicon electrodes over a $1k$ Å gate oxidation. The relative spectral responses of the CCD sensor compared with a diffused $p^+/p^-/n(x_j = 12\ \mu\text{m})$ photodiode are shown in Fig. 9. The photodiode response illustrates a constant quantum efficiency $\eta = 0.65$ between 400 nm and 800 nm and the responsivity for an equivalent area size is 0.124 pA/(mW/m²). Thus, it is clear that a photodiode sensor would have a definite advantage over its CCD sensor counterpart. Both sensors are overcoated with approximately 3 μm of SiO_2.

The response of the CCD sensor array to input irradiance (responsivity) may be determined in another manner through the radiation shot noise. Fig. 10 illustrates the total $(\text{NES})^2$ plotted versus exposure density $E(\mu\text{J/m}^2)$. We notice the straight line obtained which indicates the CCD becomes background limited at exposure densities above 50μJ/m². The quantizing interval for these measurements was $Q_I = 0.30\ \mu\text{J/m}^2 \cdot \text{bit}$, and the re-

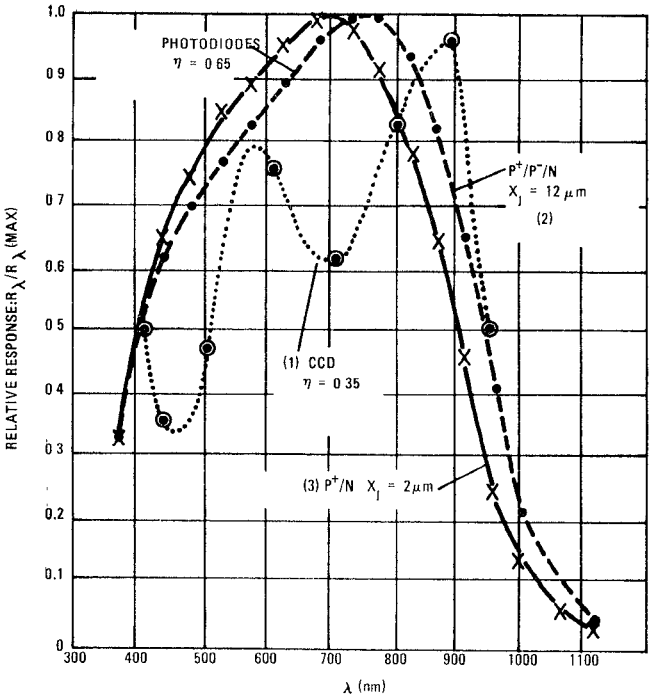

Fig. 9. Relative spectral responses of (1) a CCD sensor with a 0.2 μm silicon gate over a 0.1 μm SiO_2 and of two diffused photodiodes; (2) a $p^+/p^-/n$ diode 12 μm deep; and (3) a p^+/n diode 2 μm deep.

sponsivity obtained from the slope of the curve in Fig. 10 [see (8)] is

$$R = \frac{q\Delta E}{\Delta(\mathrm{NES})^2} = \frac{1.6 \times 10^{-19} \times 140 \times 10^{-6}}{[(0.72)^2 - (0.42)^2] \times 10^{-12}} \cong \frac{0.065\ \mathrm{pA}}{\mathrm{mW/m^2}} \tag{13}$$

in agreement with the responsivity obtained through (5) as calculated in (11).

The dynamic range of a CCD sensor line array (1 × 64 element) is shown in Fig. 11. This particular CCD array had a high quantizing interval $Q_I = 0.80\ \mu\mathrm{J/m^2}$ · bit and a leakage current of 7.0 pA/well as measured by the offset between clamp and sample intervals (see Fig. 4). The leakage current, to a first approximation, is assumed to buildup linearly down the N-b CCD shift register such that the last well in the register carries approximately $2N$ times the leakage charge as the first well. This leakage current is affected severely by the choice of clock voltages which are −8 and −26 V (substrate grounded). A reduction of the clock voltage amplitudes will reduce the leakage current substantially, however, the resolution will be impaired due to inadequate charge transfer. Fig. 11 illustrates the variance or noise measured for the correlated and uncorrelated sampling case. To obtain the uncorrelated noise we reversed the clamp and sample sequence such that they were not performed in the same pixel time window. This is proof of the correlated double sampling technique in action. Measurements had been taken on another CCD line array with a lower leakage current (1.5 pA/well) and the total NES

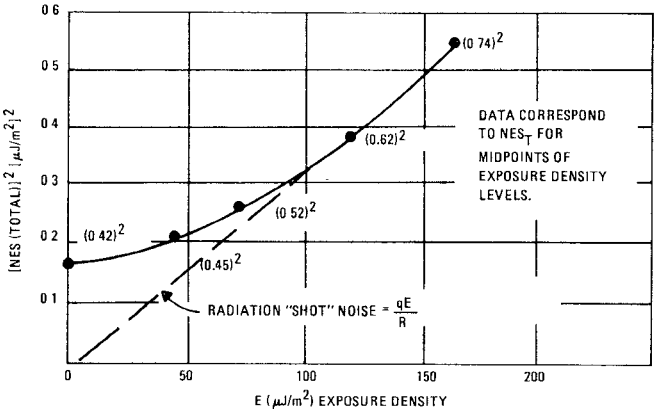

Fig. 10. Effect of radiation shot noise on the total noise-equivalent signal (NES) with a quantizing interval, $Q_I = 0.30\ \mu\mathrm{J/m^2 \cdot bit}$.

measured was 0.40 $\mu\mathrm{J/m^2}$ ($160e^-$) for a quantizing interval of 0.30 μJ. This total NES is less than the Nyquist noise contribution which is

$$\mathrm{NES\ (Nyquist)} = \frac{(2kTC)^{1/2}}{R} = \frac{0.70\ \mu\mathrm{J}}{\mathrm{m}^2}\ (284e^-) \tag{14}$$

where the factor of 2 is used to illustrate the uncorrelated case of 2 independent readings of clamp and sample. The NES values shown in Fig 11 are for the basic sensor chip. The system NES = 0.15 $\mu\mathrm{J/m^2}$ which is referred to the input of the electrometer amplifier. As Fig. 11 illustrates, the dynamic range is about 75 dB for this particular CCD array with a chip NES = $260e^-$; however, measurements on lower leakage devices indicate a chip NES = $135e^-$ and a dynamic range of 80 dB. All of the measurements were performed under uniform irradiance (line time $\tau = 1.32$ ms with the limitation as the "shot" noise associated with the leakage current on the chip. For example, the device measured in Fig. 11 had a leakage current $I_{LR} = 7.0$ pA in the register (the sensor leakage current I_{LS} was negligible compared with the register leakage current because of the low sensor bias voltage $V_S = -8$ V) and the shot noise NES contribution.

$$\mathrm{NES(shot)} = \frac{(qI_{LR}\tau)^{1/2}}{R} = 0.591\,\frac{\mu\mathrm{J}}{\mathrm{m}^2}\ (240e^-) \tag{15}$$

which accounts for most of the noise. In the low leakage devices the measured chip NES = [0.33 $\mu\mathrm{J/m^2}$ ($135e^-$)] can be attributed to the leakage current of 1.5 pA/well or a NES = [0.275 $\mu\mathrm{J/m^2}$ ($112e^-$)]. The remaining noise is attributed to the surface-state noise and in the low leakage device this is a NES = [0.18 $\mu\mathrm{J/m^2}$ ($74e^-$)]. The noise measurements do not appear to change across the 1 × 64 element line array and the values quoted are representative of the average noise along the array. One reason for the noise to remain constant across the array is that the major surface-state noise contribution is from the electrometer amplifier. There is also a suppression of

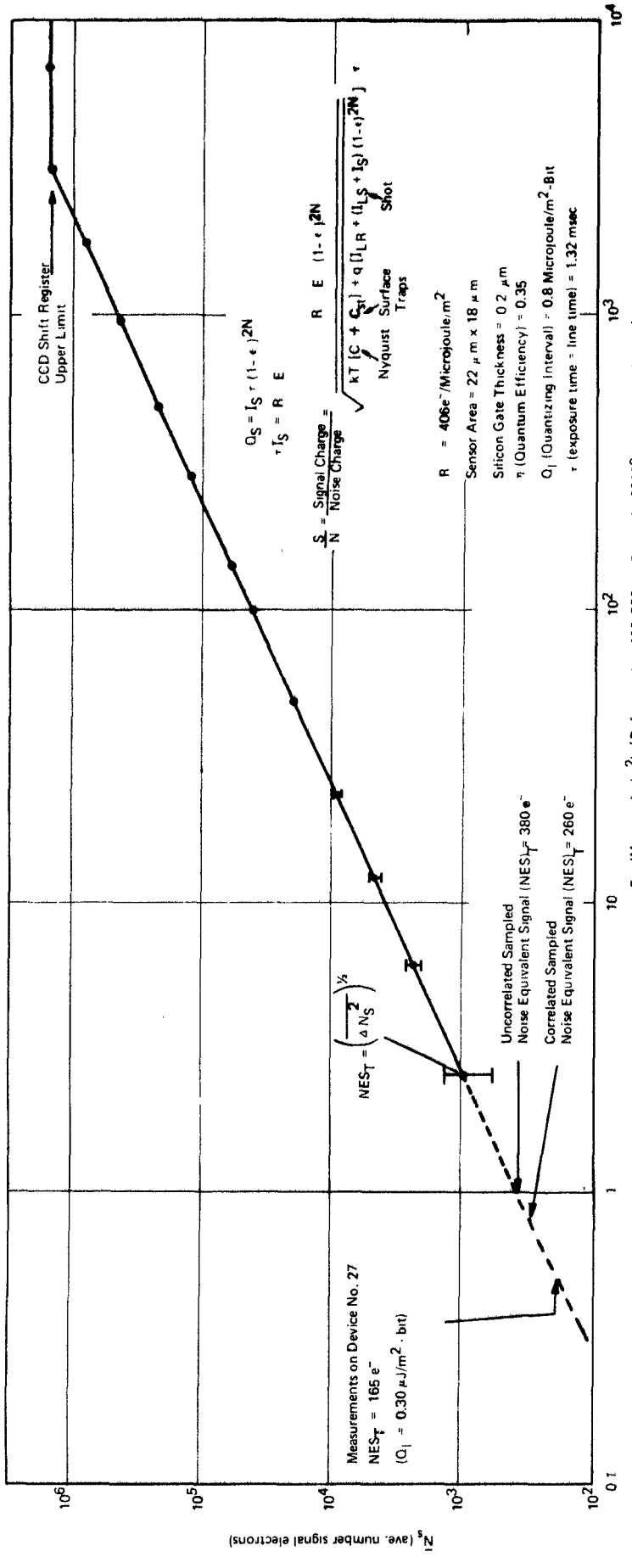

Fig. 11. Dynamic range and noise in a CCD sensor array (1 × 64 elements) with uniform irradiance.

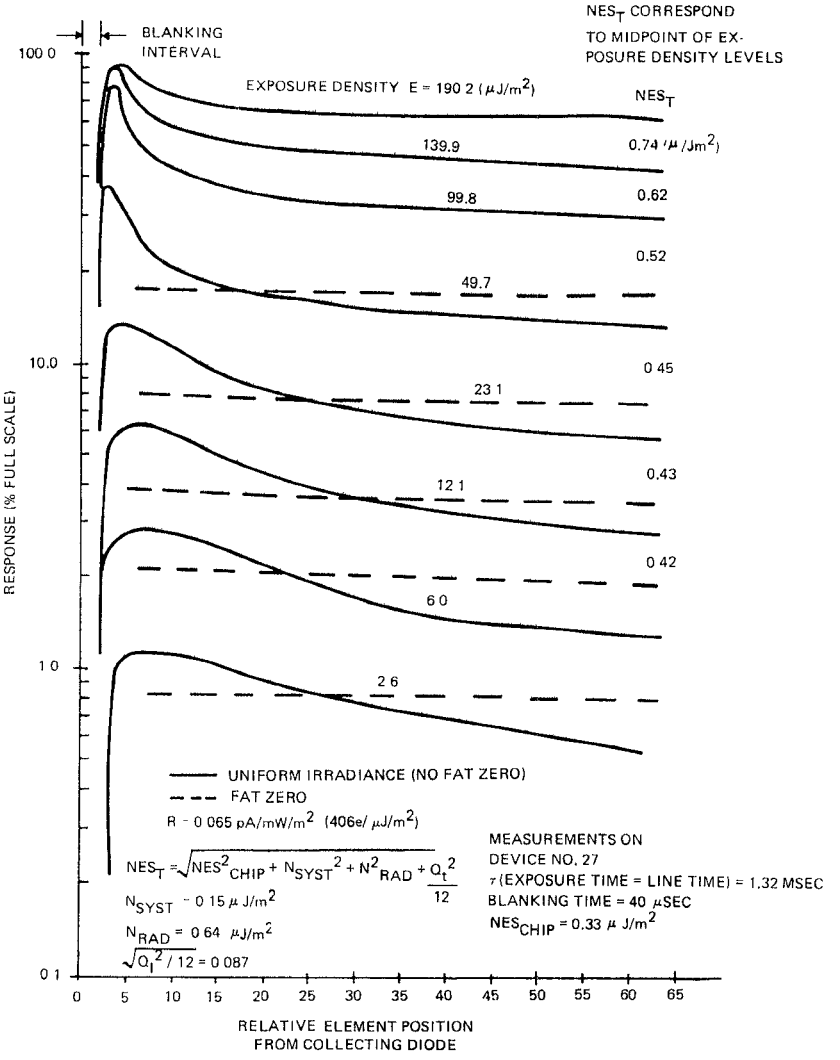

Fig. 12. Low light level response uniformity and noise performance of a 1 × 64 element CCD line array with and without a 20 percent fat zero. (CDS analog signal processing at a clock frequency f_c = 50 kHz.)

the surface-state noise within the array by the correlation of noise between adjacent wells [13]. The surface state capacitance may be written as

$$C_{st} \simeq e^2 N_{st} A \tag{16}$$

where N_{st} is the interface state density[2] (states/cm^2·eV) and A the area of the gate electrode of the MOS electrometer. Typical values of $N_{st} \simeq 4 \times 10^{10}$ cm^{-2} ev^{-1} near the band edge at 50 kHz and $A = 6.2 \times 10^{-6}$ cm^2 yield a $C_{st} = 0.04$ pF and a noise contribution of

$$\text{NES (surface state)} = \frac{(kTC_{st})^{1/2}}{R} = 0.20 \frac{\mu\text{J}}{\text{m}^2} (80e^-) \tag{17}$$

which is close to the observed value.

Fig. 12 illustrates the responsivity and noise performance of the 1 × 64 element CCD line array discussed in the preceding paragraphs. Table II summarizes the noise performance and noise sources which influence the performance of the CCD array. The line array is "blanked" or held still for approximately 2 pixel times between lines. In the absence of a fat zero, the video response (response minus dark) varies across the array: high for the first pixels (i.e., pixels nearest collection diode) after the blanking interval and low for the last pixels. Inefficient transfer of excess charge, which accumulates during the blanking interval in the larger potential wells nearest the collecting diode (see Fig. 3), contributes only to the high response. Inefficient transfer of photocharge along the CCD register causes the video output from the last pixels to be diminished by residual charge which is added to the first pixels in the next video line. If we inject an electrical fat zero (20 percent full CCD well) into the shift register, the output is uniform [see dashed lines in Fig. (12)] because of improved transfer efficiency. An electrical fat zero injected over the entire pixel time window produced a high, nonuniform noise at the output. The output noise for a 10 percent full CCD well under these conditions was approximately [4.0 μJ/m^2

[2] N_{st} is an effective surface-state density modified by the transfer function of the signal processor and the distribution of surface states.

TABLE II
SUMMARY OF NOISE PERFORMANCE OF CCD IMAGING ARRAY
(NO ELECTRICAL FAT ZERO)

$R = 406e^-/\mu J/m^2$	
Total NES (measured) at 166 $\frac{\mu J}{m^2}$ =	0.74 $\frac{\mu J}{m^2}$
Calculated radiation shot noise $\left(\frac{qE}{R}\right)^{1/2}$ =	0.64 $\frac{\mu J}{m^2}$
Signal processor noise (measured system noise) =	0.15 $\frac{\mu J}{m^2}$
Quantizing noise $\left(\frac{QI^2}{12}\right)^{1/2}$ =	0.087 $\frac{\mu J}{m^2}$
NES (chip) = $((0.74)^2 - (0.64)^2 - (0.15)^2 - (0.087)^2)^{1/2}$ =	0.33 $\frac{\mu J}{m^2}$
$= (kTC_{st} + qI_{LR}\tau)^{1/2}$ (theoretical)	0.34 $\frac{\mu J}{m^2}$
NES (shot) = $\frac{(qI_{LR}\tau)^{1/2}}{R}$ =	0.275 $\frac{\mu J}{m^2}$
NES (surface) = $\frac{(kTC_{st})^{1/2}}{R}$ =	0.20 $\frac{\mu J}{m^2}$

($1600e^-$)] and consisted of irregular "burst" noise. When the time window for electrical injections was narrowed to about 1 percent of the pixel window, the output noise for a 20 percent full CCD well was reduced to approximately [3.0 $\mu J/m^2$ ($1200e^-$)] with no evidence of irregular noise. The method of electrical fat zero injection requires further investigation to produce a truly low noise injection process.

V. LOW LIGHT LEVEL IMAGING

Transfer Inefficiency at Low Light Levels in Surface-Channel CCD Imagers

The *modulation transfer function* (MTF) [4] is determined by the charge transfer inefficiency ϵ. The ability of the CCD to transfer charge from one potential well to another is described by the transfer inefficiency ϵ, which in a practical CCD is limited by surface-state trapping [3]

$$\epsilon = \frac{kTN_{st}}{N_{sig}} \ln (f/f_0) \tag{18}$$

where N_{st} is the interface state density (typically $\simeq 1 \times 10^{10}/cm^2 \cdot eV$), N_{sig} the signal charge in the CCD shift register well (charges/cm^2), and f_0 the characteristic surface-state escape frequency (typically $f_0 \simeq 1 - 10$ kHz). A small amount of background charge or *fat zero* is required to fill the interface states permanently and reduce the transfer inefficiency. Our transfer inefficiency measurements, with a 10 μm optical profile slit placed in the center of the various sensor elements, indicate a variable transfer inefficiency across the CCD line array. The transfer efficiency improves as leakage accumulates to fill the surface states along the shift register. With an

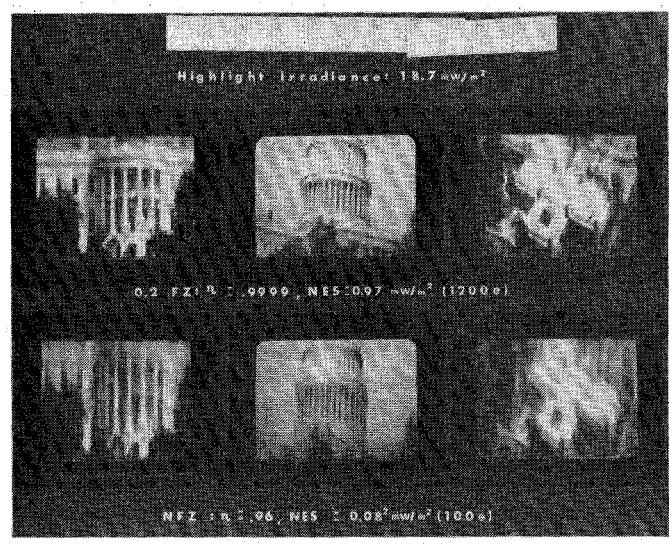

Fig. 13. Low light level imaging with and without a 20 percent fat zero. (Collection diode at photo-bottom for end pictures, at photo-top for middle pictures.)

electrical fat zero the transfer inefficiency $\epsilon \simeq 1 \times 10^{-4}$ from low frequencies to 2 MHz, which is suffiicient to operate both line and area CCD imagers. We have made measurements on the response uniformity with a fat-zero injection and there is less than $\pm$ 5 percent variation in response across a 1 $\times$ 64 element array with $\pm$ 5 percent variation in NES across the array. The deviation from straight line linearity over the entire dynamic range ($>$ 60 dB with an electrical fat zero) is within $\pm$ 2 percent.

Imaging Evaluation

In order to evaluate the CCD line arrays we employed a rotating drum to provide the along track image motion while the line array was scanned electronically in the across track direction. A transparency was mounted on the drum and irradiated by a calibrated source with all irradiance levels referenced to a blackbody source at 6000 K in the 400 nm to 800 nm band. Fig. 13 illustrates the low light level performance of the CCD 1 $\times$ 64 element line array with 3 ms exposure time (0.75 ms line readout time) and a highlight irradiance of 18.7 mW/m^2, which is about 120 pA of signal current. Our minimum detectable signal with a 20 percent fat zero is 0.97 mW/m^2 or about 6 pA. The minimum detectable signal, if we could introduce the fat zero with negligible noise,[3] is 0.08 mW/m^2 or about 0.4 pA. Notice the loss in resolution if we remove the electrical fat zero. In the scene of the White House the elements furthest from the collecting diode are at the top of the picture. It is apparent that the long number of empty CCD wells (as denoted by the black "tree" area), affects the resolution severely since these wells do not have a background "radiation fat zero" to provide low transfer inefficiencies.

[3] A method for low-noise, electrical injection of a fat zero [14] can give a NES less than the simple shot noise associated with the fat zero.

Since a CCD imager uses an analog shift register we must have low leakage register elements in addition to the requirements of low leakage sensor elements. With the interline transfer method we can separate the causes of leakage in an imager by simply turning on and off the transfer gate. In general, we encounter more leakage in the shift register than the sensor elements. One advantage of the interline transfer approach is that the shift register can be operated "free-running" to distribute the leakage throughout the register. If the register is "blanked" or held stationary for a period of time, then the local dark-current spots will begin to saturate the analog signal processor. The pictures illustrated in Fig. 13 illustrate the high quality imaging that is possible with CCD imagers.

VI. Conclusions

We have developed a method of signal processing called *correlated double sampling* which removes the switching transients at the output collection diode, eliminates, the Nyquist noise of the reset switch-output capacitance combination, provides dc restoration and increases dynamic range, and suppresses surface state and $1/f$ noise contributions. The analog signal processor, which uses this technique has been operated with clock frequencies from 800 Hz to over 3 MHz. We have measured the intrinsic noise-equivalent-signal (NES) or minimum detectable input exposure density of the CCD imager with this technique. The primary limitation to the NES is the shot noise associated with thermal leakage current generated in the sensor and shift register. The surface channel CCD imager requires a 20 percent fat zero for transfer inefficiency $\epsilon \leq 10^{-4}$ to obtain geometrical resolution. The excess noise associated with the electrical fat zero limits the sensitivity of the surface channel CCD and attention must be directed toward a method of low noise electrical injection. For an electrical fat zero introduced by a gated diode, our measurements indicate a noise charge of 1000 to 1200 electrons; however, a redesign of the input electrical injection circuit [14] should enable surface channel CCD's to operate with an NES limited by thermal leakage shot noise and a dynamic range in excess of 80 dB. For our simple gated diode injection circuit with a 20 percent fat zero, we have achieved greater than 60 dB dynamic range with less than $\pm$ 2 percent deviation from linearity over this range and less than $\pm$ 3 percent variation in responsivity and NES across a 1 $\times$ 64 element line array. The dark current variation was less than $\pm$ 3.4 percent across the array. We have made measurements without an electrical fat zero and under uniform exposure to indicate a noise charge of 135 electrons at an integration time of 1.32 ms. The noise was associated primarily with the thermal leakage current in the CCD shift register. The thermal leakage current on the better arrays was about 50 nA/cm^2.

Spectral response and responsivity measurements indicate a nonuniform spectral response due to interference fringes caused by this silicon gate thickness and the underlying SiO_2. The effective quantum efficiency of the silicon gate CCD sensor in the range from 400 nm to 800 nm was $\eta = 0.35$, compared with a photodiode $\eta = 0.65$, which is constant. Consideration should be given to the design of the CCD imaging array with the use of a diffused photodiode for the sensor. The g_m/C ratio should be increased at the output collection diode to overcome system noise limitations; and the quantizing interval Q_I, if digital signal processing is used, should be decreased in accordance with dynamic range and data rate limitations.

Acknowledgment

The authors wish to express their appreciation to R. M. McLouski for the diffusions and oxidations, P. R. Reid for the polysilicon depositions, J. Grossman for the chemical processing, C. J. Taylor for the photolithography, and D. S. Herman for the special aluminum/silicon evaporations. They would also like to thank D. H. McCann for his valuable assistance and technical discussions, and to express appreciation to W. S. Corak (Manager), M. N. Giuliano and R. C. Gallagher (Supervisors), of the Solid State Systems Technology Laboratory, and to G. Strull, Manager of the Advanced Technology Laboratories, for their encouragement and support. A special thanks is accorded to C. Lesniewski and S. Viscomi for preparation of the manuscript.

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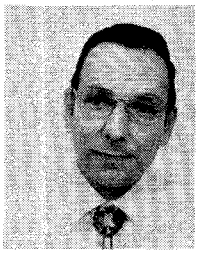

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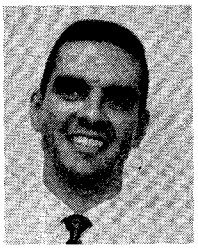

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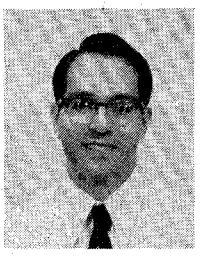

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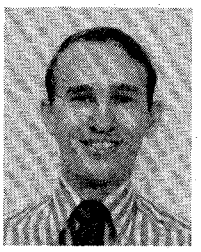

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