Lecture 10: Isolated Converters II & DCM Introduction

ECE 481: Power Electronics Prof. Daniel Costinett

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Announcements

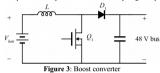
- Midterm exam due Thursday, start of class
- Hw #3 returned today
- Missing HW assignments

3. [30 pts] Design of a Boost Converter

The boost converter in Fig. 3 connects a lead-acid battery to a 48 V DC bus. The converter input is the battery voltage, which has characteristics:

Maximum V_{batt} : 15 V Minimum V_{batt} : 10 V

The maximum output power is 100 W, and the switching frequency is 100 kHz. The inductance L is chosen to be $10~\mu\text{H}$, and the capacitance may be assumed to be very large for parts (a)-(c).



a) [10 pts] A number of parts are available for both the MOSFET and diode. Important characteristics of each device are shown in Tables I and II. The rated maximum currents and voltages are the maximum instantaneous values which the devices can handle.

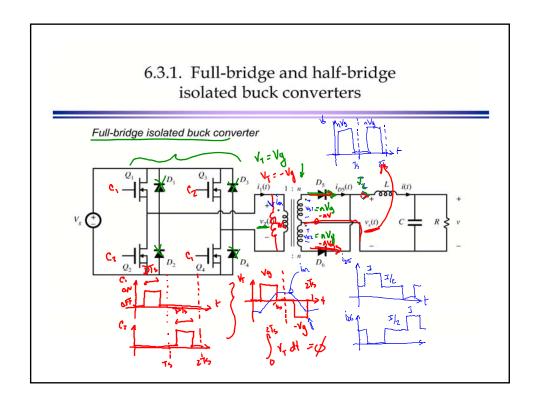
TABLE I: MOSFET DEVICES

Device	Rated max V_{DS}	Rated max I _{DS}	R_{on}
I	40 V	30 A	5 mΩ
II	100 V	15 A	$15 \text{ m}\Omega$
III	100 V	20 A	$50 \text{ m}\Omega$
IV	150 V	15 A	$30 \text{ m}\Omega$
V	150 V	20 A	75 mΩ

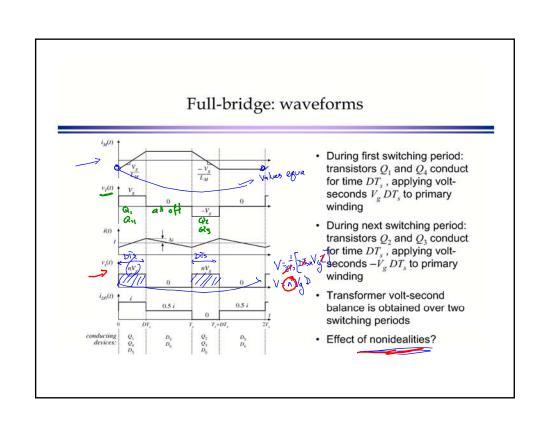
TABLE II: DIODE DEVICES

Device	Rated max V_R	Rated max I_F	V_F
VI	40 V	20 A	0.5 V
VII	100 V	15 A	1.0 V
VIII	150 V	5 A	0.7 V
IX	200 V	20 A	1.5 V

Select one MOSFET and one diode which will work best in this converter. Explain why you



Full Bridge Switch Structure | Interpretation of Mosfer | Property | Propert



Effect of nonidealities on transformer volt-second balance

Volt-seconds applied to primary winding during first switching period:

 $(V_g - (Q_1 \text{ and } Q_4 \text{ forward voltage drops}))(Q_1 \text{ and } Q_4 \text{ conduction time})$

Volt-seconds applied to primary winding during next switching period:

 $-(V_g - (Q_2 \text{ and } Q_3 \text{ forward voltage drops)})(Q_2 \text{ and } Q_3 \text{ conduction time})$

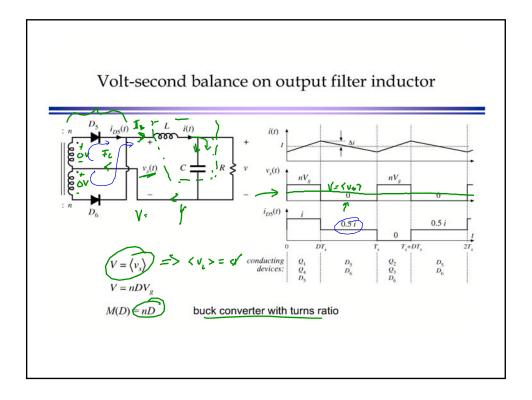
These volt-seconds never add to exactly zero.

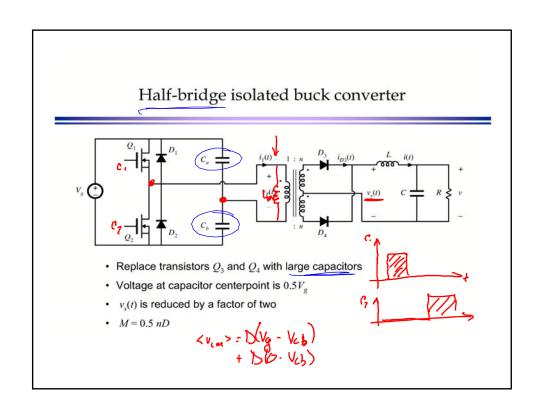
Net volt-seconds are applied to primary winding

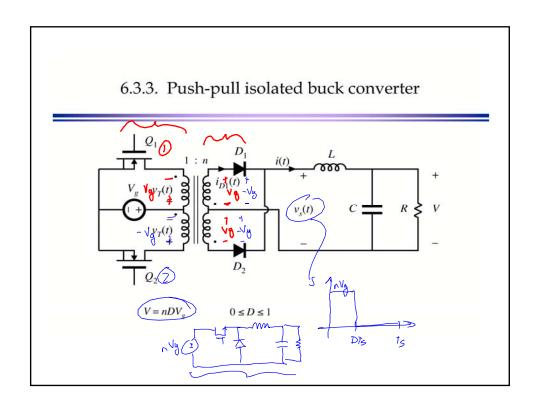
Magnetizing current slowly increases in magnitude

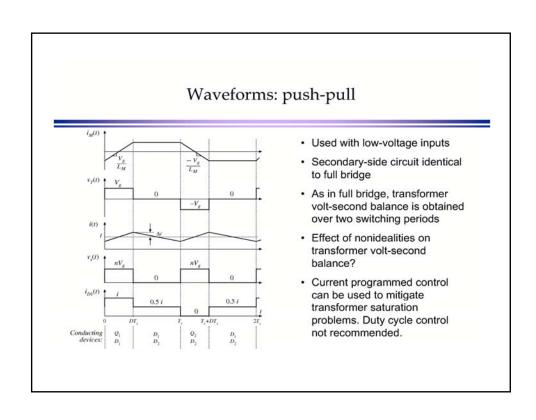
Saturation can be prevented by placing a capacitor in series with primary, or by use of current programmed mode (Chapter 12)

Operation of secondary-side diodes L $i_{D5}(t)$ i(t) During second (D') subinterval, both secondary-side diodes $v_s(t)$ conduct · Output filter inductor current divides D_6 approximately equally $v_s(t)$ between diodes Secondary amp-turns add 0 to approximately zero $i_{D5}(t)$ 0.5iEssentially no net magnetization of $T_s + DT_s$ transformer core by D_{5} conducting secondary winding currents

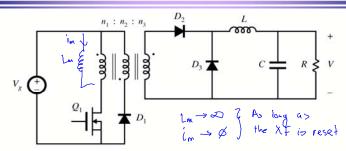






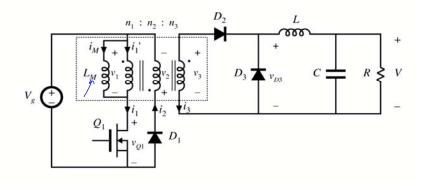


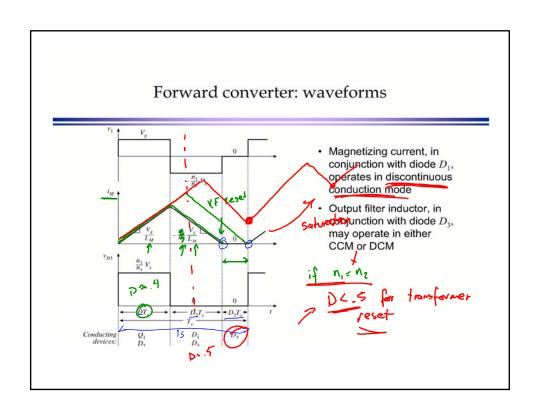
6.3.2. Forward converter

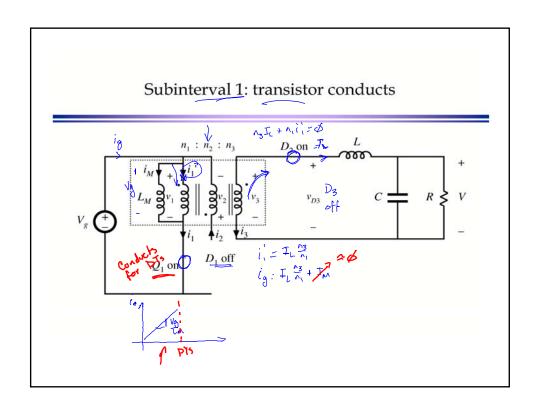


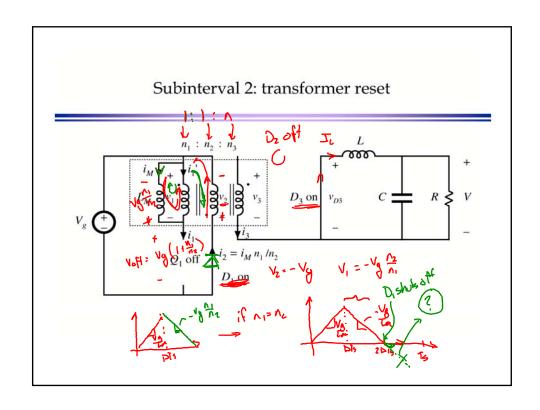
- · Buck-derived transformer-isolated converter
- · Single-transistor and two-transistor versions
- · Maximum duty cycle is limited
- · Transformer is reset while transistor is off

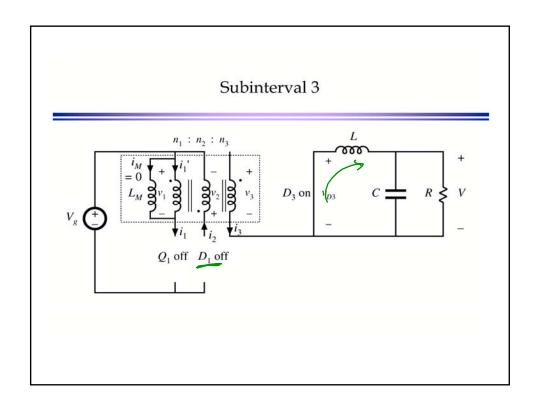
Forward converter with transformer equivalent circuit

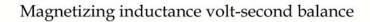


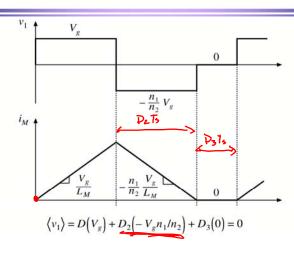












Transformer reset

From magnetizing current volt-second balance:

$$\left\langle v_1 \right\rangle = D \left(V_g \right) + D_2 \left(-V_g n_1 / n_2 \right) + D_3 \left(0 \right) = 0$$

Solve for
$$D_2$$
:

$$D_2 = \frac{n_2}{n_+} D$$

 D_3 cannot be negative. But $D_3 = 1 - D - D_2$. Hence

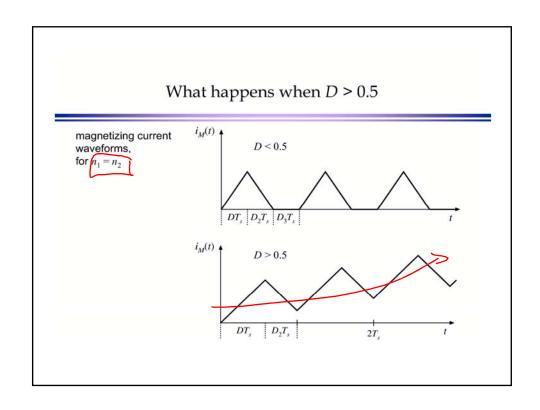
$$D_3=1-D-D_2\geq 0$$

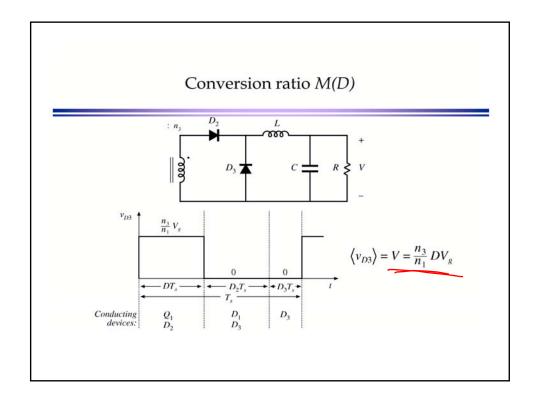
$$D_3 = 1 - D\left(1 + \frac{n_2}{n_1}\right) \ge 0$$

Solve for D

$$D \le \frac{1}{1 + \frac{n_2}{n_1}}$$

for
$$n_1 = n_2$$
: $D \le -1$





Maximum duty cycle vs. transistor voltage stress

Maximum duty cycle limited to

$$D \le \frac{1}{1 + \frac{n_2}{n_1}}$$

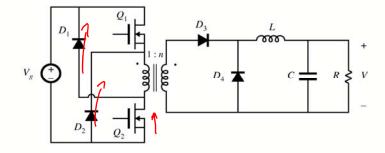
which can be increased by increasing the turns ratio n_2/n_l . But this increases the peak transistor voltage:

$$\max\left(v_{Q1}\right) = V_g\left(1 + \frac{n_1}{n_2}\right)$$

For $n_1 = n_2$

$$D \le \frac{1}{2}$$
 and $\max(v_{Q1}) = 2V_g$

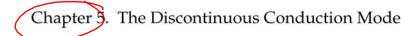
The two-transistor forward converter



$$V = nDV_g$$

$$D \le \frac{1}{2}$$

$$\max(v_{Q1}) = \max(v_{Q2}) = V_g$$



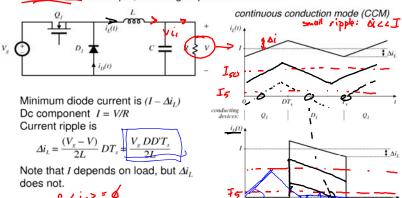
- Origin of the discontinuous conduction mode, and mode boundary
- 5.2. Analysis of the conversion ratio M(D,K)
- 5.3. Boost converter example
- 5.4. Summary of results and key points

Introduction to Discontinuous Conduction Mode (DCM)

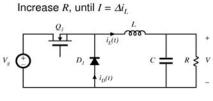
- Occurs because switching ripple in inductor current or capacitor voltage causes polarity of applied switch current or voltage to reverse, such that the current- or voltage-unidirectional assumptions made in realizing the switch are violated.
- Commonly occurs in dc-dc converters and rectifiers, having singlequadrant switches. May also occur in converters having two-quadrant switches.
- Typical example: dc-dc converter operating at light load (small load current). Sometimes, dc-dc converters and rectifiers are purposely designed to operate in DCM at all loads.
- Properties of converters change radically when DCM is entered:
 - M becomes load-dependent
 - Output impedance is increased
 - Dynamics are altered
 - Control of output voltage may be lost when load is removed

5.1. Origin of the discontinuous conduction mode, and mode boundary

Buck converter example, with single-quadrant switches



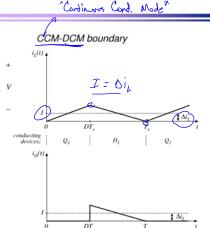
Reduction of load current



Minimum diode current is $(I-\Delta i_L)$ Dc component $I=V\!/\!R$ Current ripple is

$$\Delta i_L = \frac{(V_g - V)}{2L} DT_s = \frac{V_g DD'T_s}{2L}$$

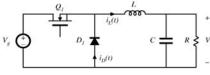
Note that I depends on load, but $\varDelta i_L$ does not.



Further reduce load current

Increase R some more, such that $I < \Delta i_L$

Discontinuous conduction mode

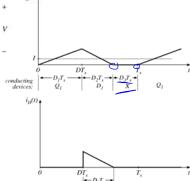


Minimum diode current is $(I - \Delta i_L)$ Dc component I = V/RCurrent ripple is

$$\Delta i_L = \frac{(V_g - V)}{2L} DT_s = \frac{V_g DD'T_s}{2L}$$

Note that I depends on load, but Δi_L does not.

The load current continues to be positive and non-zero.



Mode boundary

Bourdary
$$I > \Delta i_L$$
 for CCM $I < \Delta i_L$ for DCM

Insert buck converter expressions for
$$I$$
 and Δi_L : $V = DV_S$

$$\frac{DV_S}{R} < \frac{DD'T_SV_S}{2L} < \qquad \qquad J_C = \frac{DV_S}{R} < \frac{DV_S}{R}$$
Simplify:

Simplify:

Simplify:
$$\frac{2L}{RT_{\star}} < D' \qquad \text{for buck}$$

$$K_{en}(D) = D'$$

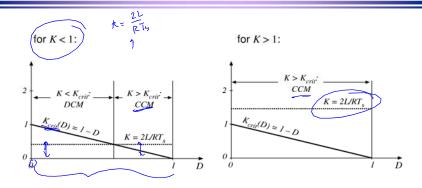
$$K < K_{en}(D) \qquad \text{for DCM}$$

$$K = \frac{2L}{RT_{\star}} \qquad \text{and} \qquad K_{en}(D) = D' \qquad \text{as } T_{e} L \qquad Dir L$$

$$Where \qquad K = \frac{2L}{RT_{\star}} \qquad \text{and} \qquad K_{en}(D) = D' \qquad \text{as } T_{e} L \qquad Dir L$$

$$Where \qquad Where \qquad Whe$$





Critical load resistance R_{crit}

Solve K_{crit} equation for load resistance R:

where
$$R < R_{crit}(D)$$
 for CCM
 $R > R_{crit}(D)$ for DCM
 $R_{crit}(D) = \frac{2L}{DT_s}$

Summary: mode boundary

$$K > K_{crit}(D)$$
 or $R < R_{crit}(D)$ for CCM
 $K < K_{crit}(D)$ or $R > R_{crit}(D)$ for DCM

Table 5.1. CCM-DCM mode boundaries for the buck, boost, and buck-boost converters

Converter	$K_{crit}(D)$	$\max_{0 \le D \le 1} (K_{crit})$	$R_{crit}(D)$	$\min_{0 \le D \le 1} (R_{crit})$
Buck	(I - D)	1	$\frac{2L}{(1-D)T_s}$	$2\frac{L}{T_s}$
Boost	$D(1-D)^2$	$\frac{4}{27}$	$\frac{2L}{D(1-D)^2 T_s}$	$\frac{27}{2}\frac{L}{T_s}$
Buck-boost	$(I-D)^2$	1	$\frac{2L}{(1-D)^2T}$	$2\frac{L}{T_s}$

Analysis of the conversion ratio M(D,K)5.2.

Analysis techniques for the discontinuous conduction mode:

Inductor volt-second balance

$$\langle v_L \rangle = \frac{1}{T_s} \int_0^{T_s} v_L(t) dt = 0$$

Capacitor charge balance

$$\langle i_C \rangle = \frac{1}{T_s} \int_0^{T_s} i_C(t) dt = 0$$

Small ripple approximation sometimes applies: $v(t) \approx V$ because $\Delta v \ll V$ Assuming aperating as regulator $i(t) \approx I$ is a poor approximation when $\Delta i > I$

Converter steady-state equations obtained via charge balance on each capacitor and volt-second balance on each inductor. Use care in applying small ripple approximation.

Example: Analysis of DCM buck converter M(D,K)subinterval 1 v_s v_s