Lecture 25: Transformer Design; Further Topics

ECE 481: Power Electronics

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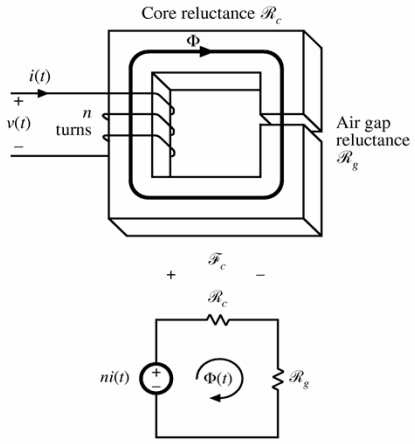
Announcements

- ECE 482: Power Electronic Circuits
- http://oira.tennessee.edu/sais/ (7 students missing)
- Midterm exam:
  - Available after class today
  - Due anytime before 12:15pm on Wednesday, Dec 11th in MK 502

Filter inductor, cont.

- Negligible core loss, negligible proximity loss
- Loss dominated by dc copper loss
- Flux density chosen simply to avoid saturation
- Air gap is employed
- Could use core materials having high saturation flux density (and relatively high core loss), even though converter switching frequency is high



Chapter 14 Inductor Design

14.1 Filter inductor design constraints

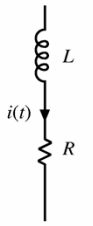
14.2 A step-by-step design procedure

14.3 Multiple-winding magnetics design using the K_g method

14.4 Examples

14.5 Summary of key points

14.1 Filter inductor design constraints



Objective:

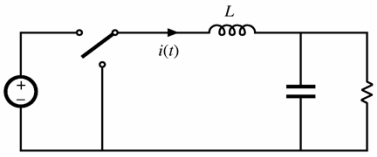
Design inductor having a given inductance L,

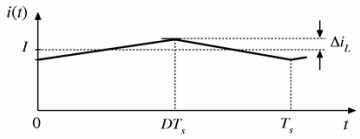
which carries worst-case current I_{max} without saturating,

and which has a given winding resistance R, or, equivalently, exhibits a worst-case copper loss of

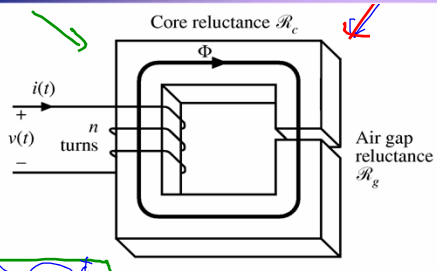
$$P_{cu} = I_{rms}^{\ 2} R$$

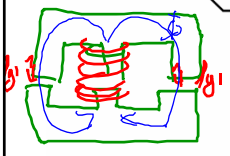
Example: filter inductor in CCM buck converter





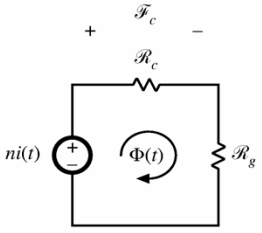
Assumed filter inductor geometry





$$\mathcal{R}_c = \frac{\ell_c}{\mu_c A_c}$$

$$\mathcal{R}_g = \frac{\ell_g}{\mu_0 A_c}$$



Solve magnetic circuit:

$$ni = \Phi\left(\mathcal{R}_c + \mathcal{R}_g\right)$$

Usually $\mathcal{R}_c \ll \mathcal{R}_g$ and hence

$$ni \approx \Phi \mathcal{R}_g$$

14.2 A step-by-step procedure

The following quantities are specified, using the units noted:

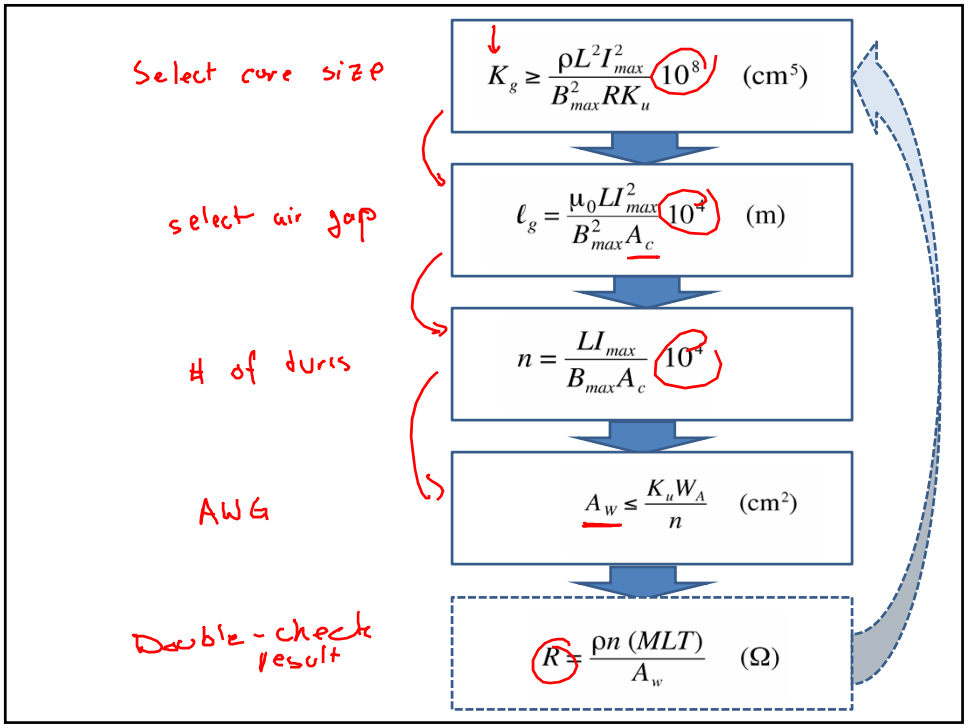
Wire resistivity	ρ	(Ω-cm)
Peak winding current	I_{max}	(A)
Inductance	L	(H)
Winding resistance	R	(Ω)
Winding fill factor	K_u	
Core maximum flux density	B_{max}	(T)

K_g method

The core dimensions are expressed in cm:

Core cross-sectional area	A_c	(cm^2)
Core window area	W_A	(cm^2)
Mean length per turn	MLT	(cm)

The use of centimeters rather than meters requires that appropriate factors be added to the design equations.



Calculation of ac flux density and core loss

Solve for ΔB:

$$\Delta B = \left(\frac{V_g}{n_1 A_c}\right)(DT_s)$$

Plug in values for flyback example:

$$\Delta B = \frac{(200\ \text{V})(0.4)(6.67\ \mu\text{s})}{2(59)(1.09\ \text{cm}^2)}\ 10^4$$

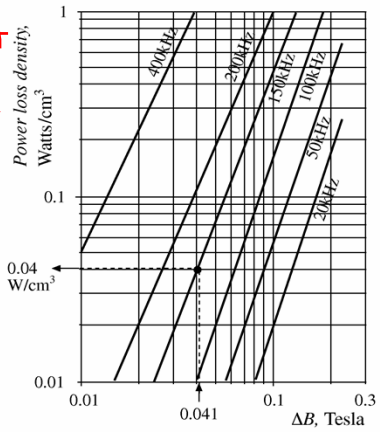
$$= 0.041\ \text{T}$$

From manufacturer's plot of core loss (at left), the power loss density is 0.04 W/cm³. Hence core loss is

$$P_{fe} = (0.04\ \text{W/cm}^3)(A_c \ell_m)$$

$$= (0.04\ \text{W/cm}^3)(1.09\ \text{cm}^2)(5.77\ \text{cm})$$

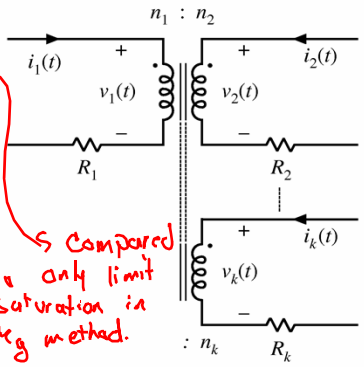
$$= 0.25\ \text{W}$$



Chapter 15 Transformer Design

Some more advanced design issues, not considered in previous chapter:

- Inclusion of core loss
- Selection of operating flux density to optimize total loss
- Multiple winding design: as in the coupled-inductor case, allocate the available window area among several windings
- A transformer design procedure
- How switching frequency affects transformer size



15.1 Transformer Design:
Basic Constraints

Core loss

$$P_{fe} = K_{fe}(\Delta B)^{\beta} A_c \ell_m$$

Typical value of β for ferrite materials: 2.6 or 2.7

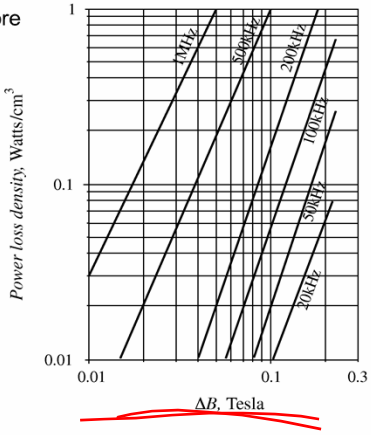
ΔB is the peak value of the ac component of $B(t)$, *i.e.*, the peak ac flux density

So increasing ΔB causes core loss to increase rapidly

This is the first constraint

Total core loss: manufacturer's data

Ferrite core material



Empirical equation, at a fixed frequency:

$$P_{fe} = K_{fe}(\Delta B)^{\beta} A_c \ell_m$$

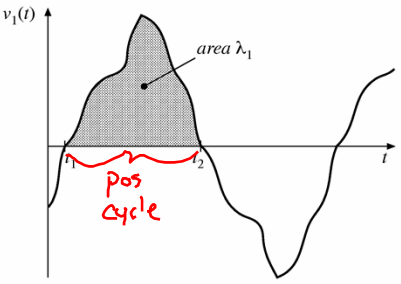
Flux density
Constraint #2

Flux density $B(t)$ is related to the applied winding voltage according to Faraday's Law. Denote the volt-seconds applied to the primary winding during the positive portion of $v_1(t)$ as λ_1:

$$\lambda_1 = \int_{t_1}^{t_2} v_1(t)\,dt$$

This causes the flux to change from its negative peak to its positive peak. From Faraday's law, the peak value of the ac component of flux density is

$$\Delta B = \frac{\lambda_1}{2 n_1 A_c}$$



To attain a given flux density, the primary turns should be chosen according to

$$n_1 = \frac{\lambda_1}{2 \Delta B A_c}$$

Copper loss
Constraint #3

- Allocate window area between windings in optimum manner, as described in previous section
- Total copper loss is then equal to

$$P_{cu} = \frac{\rho (MLT) n_1^2 I_{tot}^2}{W_A K_u}$$

with

$$I_{tot} = \sum_{j=1}^{k} \frac{n_j}{n_1} I_j$$

Eliminate n_1, using result of previous slide:

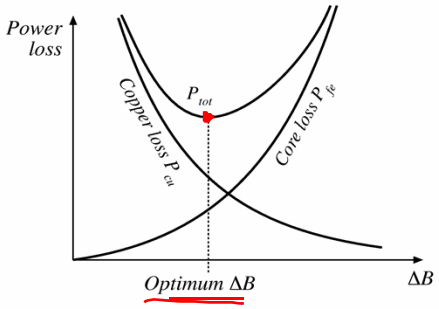
$$P_{cu} = \left(\frac{\rho \lambda_1^2 I_{tot}^2}{4 K_u} \right) \left(\frac{(MLT)}{W_A A_c^2} \right) \left(\frac{1}{\Delta B} \right)^2$$

Note that copper loss decreases rapidly as ΔB is increased

Total power loss

4. $P_{tot} = P_{cu} + P_{fe}$

There is a value of ΔB that minimizes the total power loss



$$P_{tot} = P_{fe} + P_{cu}$$

$$P_{fe} = K_{fe}(\Delta B)^{\beta} A_c \ell_m$$

$$P_{cu} = \left(\frac{\rho \lambda_1^2 I_{tot}^2}{4K_u}\right)\left(\frac{(MLT)}{W_A A_c^2}\right)\left(\frac{1}{\Delta B}\right)^2$$

Total loss

Substitute optimum ΔB into expressions for P_{cu} and P_{fe}. The total loss is:

$$P_{tot} = \left[A_c \ell_m K_{fe}\right]^{\left(\frac{2}{\beta+2}\right)} \left[\frac{\rho\lambda_1^2 I_{tot}^2}{4K_u} \frac{(MLT)}{W_A A_c^2}\right]^{\left(\frac{\beta}{\beta+2}\right)} \left[\left(\frac{\beta}{2}\right)^{-\left(\frac{\beta}{\beta+2}\right)} + \left(\frac{\beta}{2}\right)^{\left(\frac{2}{\beta+2}\right)}\right]$$

Rearrange as follows:

$$\frac{W_A (A_c)^{(2(\beta-1)/\beta)}}{(MLT)\ell_m^{(2/\beta)}} \left[\left(\frac{\beta}{2}\right)^{-\left(\frac{\beta}{\beta+2}\right)} + \left(\frac{\beta}{2}\right)^{\left(\frac{2}{\beta+2}\right)}\right]^{-\left(\frac{\beta+2}{\beta}\right)} = \frac{\rho\lambda_1^2 I_{tot}^2 K_{fe}^{(2/\beta)}}{4K_u (P_{tot})^{((\beta+2)/\beta)}}$$

Left side: terms depend on core geometry

Right side: terms depend on specifications of the application

The core geometrical constant K_{gfe}

Define $$K_{gfe} = \frac{W_A \left(A_c\right)^{\left(2(\beta-1)/\beta\right)}}{(MLT)\ell_m^{(2/\beta)}} \left[\left(\frac{\beta}{2}\right)^{-\left(\frac{\beta}{\beta+2}\right)} + \left(\frac{\beta}{2}\right)^{\left(\frac{2}{\beta+2}\right)} \right]^{-\left(\frac{\beta+2}{\beta}\right)}$$

Design procedure: select a core that satisfies

$$K_{gfe} \geq \frac{\rho \lambda_1^2 I_{tot}^2 K_{fe}^{(2/\beta)}}{4 K_u \left(P_{tot}\right)^{\left((\beta+2)/\beta\right)}}$$

Appendix D lists the values of K_{gfe} for common ferrite cores

K_{gfe} is similar to the K_g geometrical constant used in Chapter 14:

- K_g is used when B_{max} is specified
- K_{gfe} is used when ΔB is to be chosen to minimize total loss

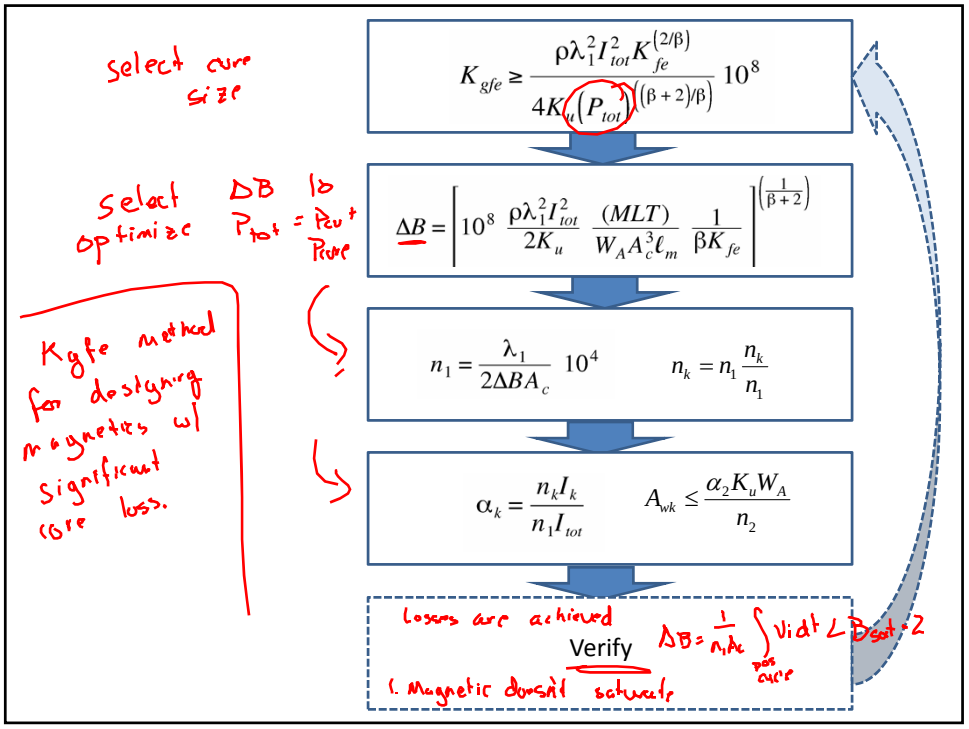
15.2 Step-by-step transformer design procedure

The following quantities are specified, using the units noted:

Wire effective resistivity	ρ	(Ω-cm)
Total rms winding current, ref to pri	I_{tot}	(A)
Desired turns ratios	n_2/n_1, n_3/n_1, etc.	
Applied pri volt-sec	λ_1	(V-sec)
Allowed total power dissipation	P_{tot}	(W)
Winding fill factor	K_u	
Core loss exponent	β	
Core loss coefficient	K_{fe}	(W/cm^3T^β)

Other quantities and their dimensions:

Core cross-sectional area	A_c	(cm^2)
Core window area	W_A	(cm^2)
Mean length per turn	MLT	(cm)
Magnetic path length	ℓ_e	(cm)
Wire areas	A_{w1}, …	(cm^2)
Peak ac flux density	ΔB	(T)



Check: computed transformer model

Predicted magnetizing inductance, referred to primary:

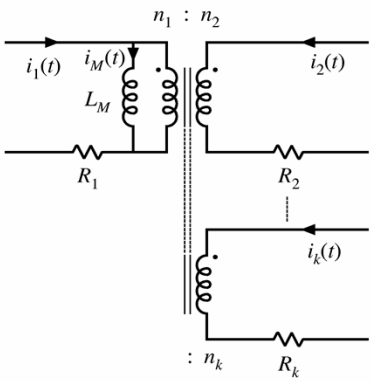
$$L_M = \frac{\mu n_1^2 A_c}{\ell_m}$$

Peak magnetizing current:

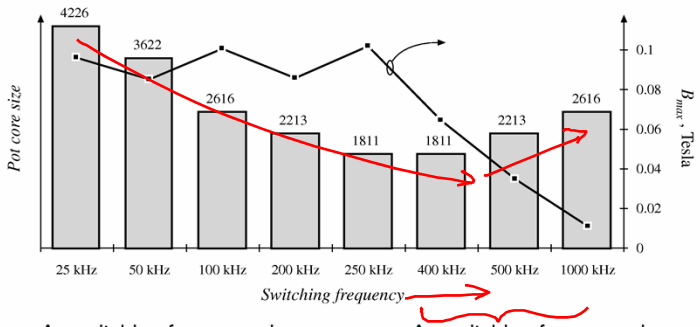
$$i_{M,pk} = \frac{\lambda_1}{2L_M}$$

Predicted winding resistances:

$$R_1 = \frac{\rho n_1 (MLT)}{A_{w1}}$$
$$R_2 = \frac{\rho n_2 (MLT)}{A_{w2}}$$
$$\vdots$$



Effect of switching frequency on transformer size
for this P-material Cuk converter example



- As switching frequency is increased from 25 kHz to 250 kHz, core size is dramatically reduced
- As switching frequency is increased from 400 kHz to 1 MHz, core size increases

Application of ECE481 Theory

Example: Low-Power AC Adapters

Apple "Ultracompact USB Power Adapter"

Goals:

- Produce regulated DC Voltage from universal input (85 to 276 Vrms, 47-63 Hz)
- Maintain high power factor / Low EMI
- High efficiency to allow small size

Design Constraints:

- Single converter needs power stage which can operate over wide input voltage range
- For V_{dc} = +5 V (USB output) need very large step-down capability (M = 0.018)
- Isolation may be necessary for safety

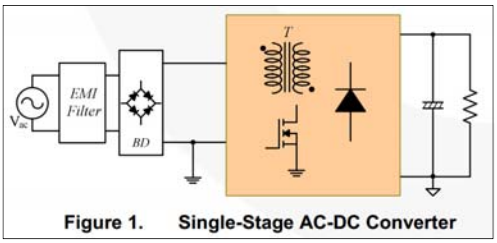
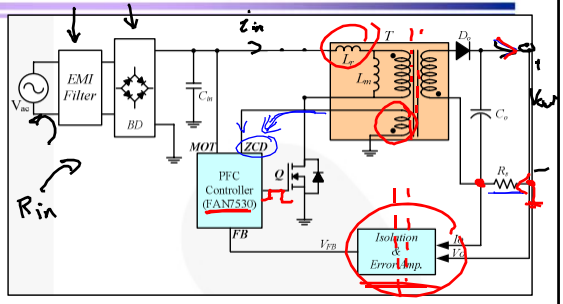


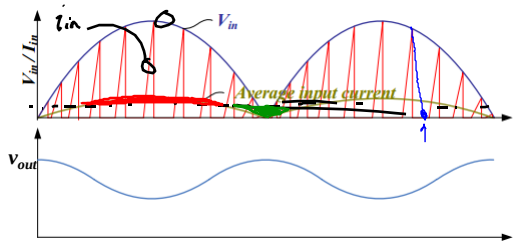
Figure 1. Single-Stage AC-DC Converter

Fairchild Semi, "Design Guideline of Single-Stage Flyback AC-DC Converter Using FAN7530 for LED Lighting"

Flyback Implementation

- Flyback selected as a simple, low part-count topology
- Used almost exclusively in Ac-to-LVDC applications at power levels less than 100W
- DCM may be used for reduced diode RR and increased f_s

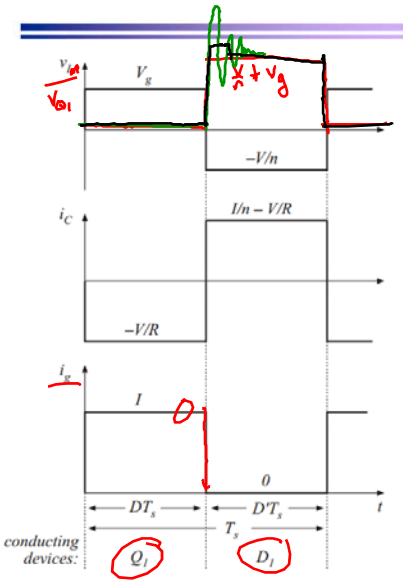


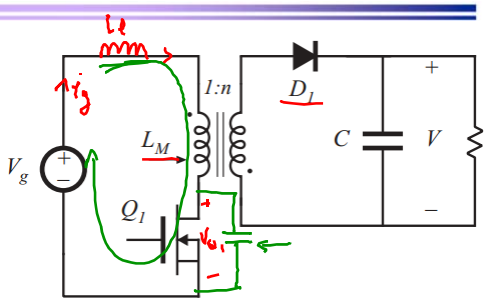


- Pulsating input current requires filtering
- If unity power factor is obtained, significant output ripple results

Fairchild Semi, "Design Guideline of Single-Stage Flyback AC-DC Converter Using FAN7530 for LED Lighting"

Practical Issue: Ringing in Flyback





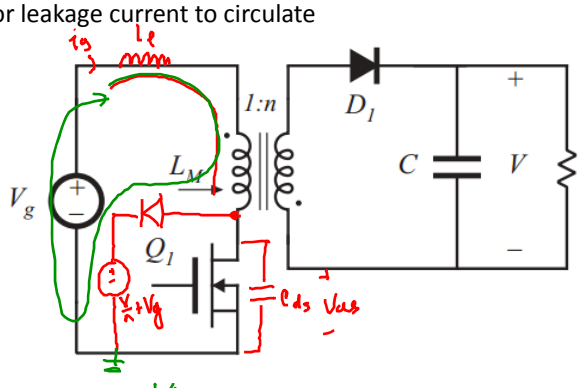
- Practical transformer implementation has nonzero leakage inductance
- When MOSFET switches off, it interrupts leakage current
- Inductor energy dumped into MOSFET output capacitance
- Lossy, high EMI, Potentially can over-voltage MOSFET Q_1

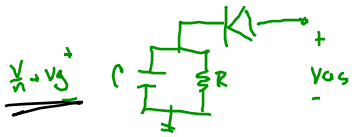
Snubber Design

- Goal is to provide a path for leakage current to circulate

$P_{diss} = \frac{(\frac{V}{n}+v_g)^2}{R}$

$P_{supp} = f_s \frac{1}{2} L_g I_g^2$





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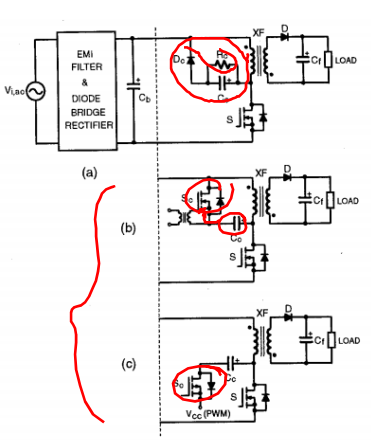


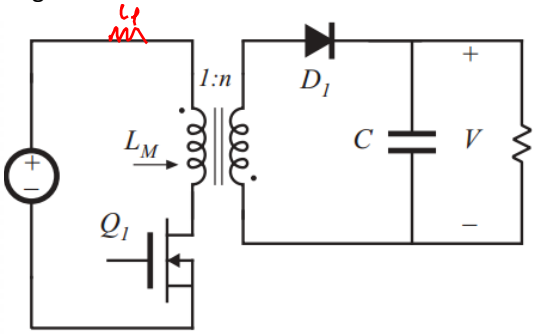


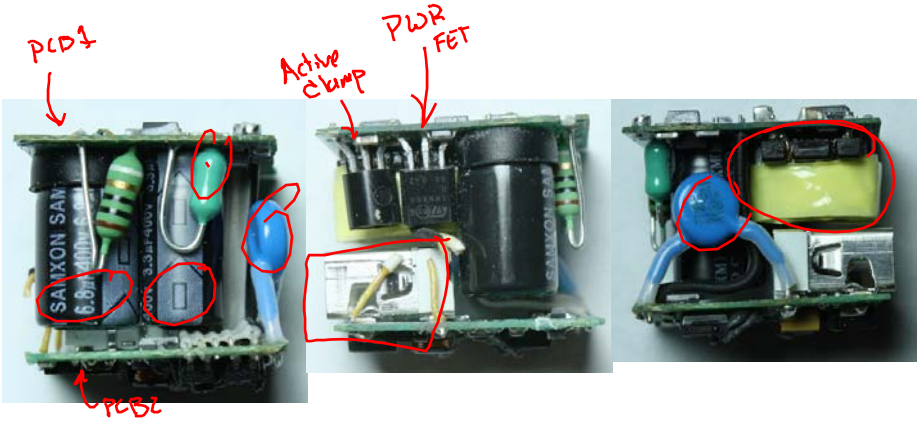
Fig. 1 Simplified circuit diagram of (a) RCD-clamp, (b) NMOS active-clamp, and (c) PMOS active-clamp flyback adapter/charger

L Huber and M Jovanovic, "Evaluation of Flyback Topologies for Notebook AC/DC Adapter/Charger Applications

Apple Power Adapter Implementation

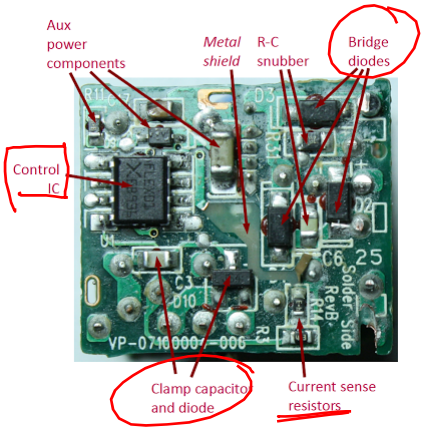
Example:

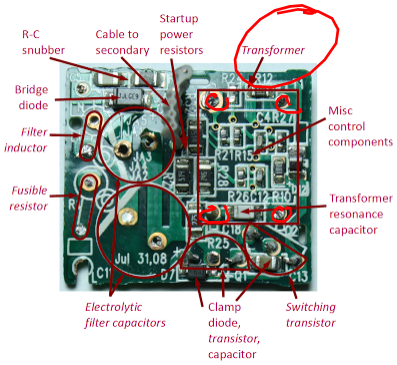
- 5 Watt AC-to-5V adapter



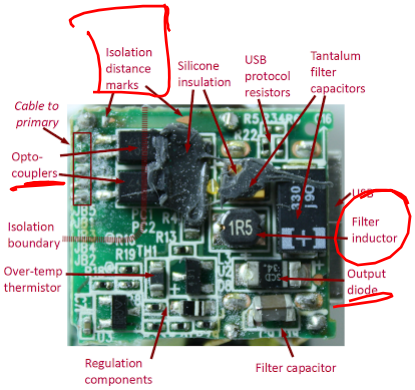
K Shirriff, "Apple iPhone charger teardown: quality in a tiny expensive package"

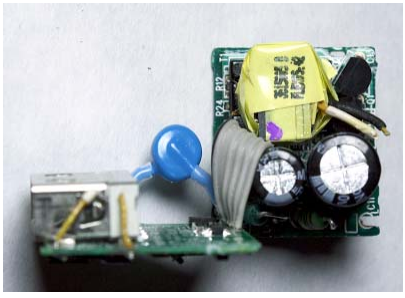
Apple Circuit Primary



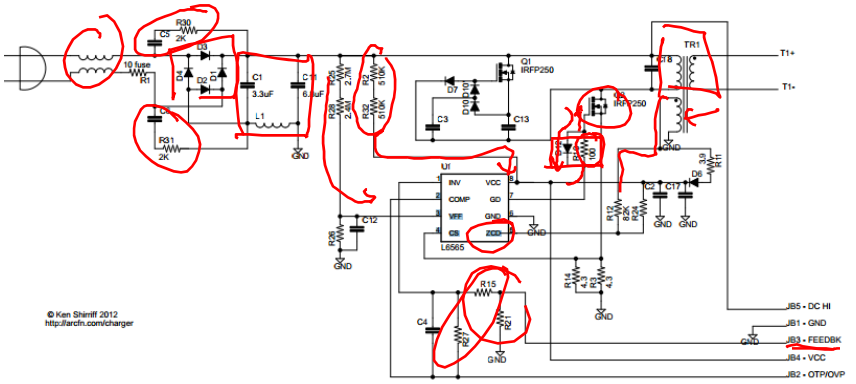


Apple Circuit Secondary





Apple Adapter Schematic



Example Waveforms

(a) at 110 V_{ac} Input (b) at 220 V_{ac} Input

Figure 12. Switching Voltage and Current

L Huber and M Jovanovic, "Evaluation of Flyback Topologies for Notebook AC/DC Adapter/Charger Applications

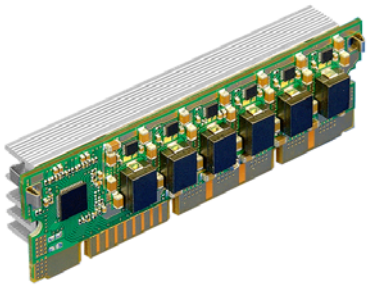
Example 2: VRM Design

Goals:

- Produce tightly regulated 0.8-1.4 V output voltage from 12 V +5%/-8%
- Maintain very strict regulation

Design Constraints:

- < 10mV ripple (pk-to-pk)
- < 50mV deviation at full load current step
- 120 A/ns output current slew rate
- 150 A peak output current
- Regulation down to 500mA
- Voltage variation in 6.25 mV steps



Intel, "VRM and EVRD Design Guidelines", Sept 2009

Traditional Approach: High-Current Buck Converter

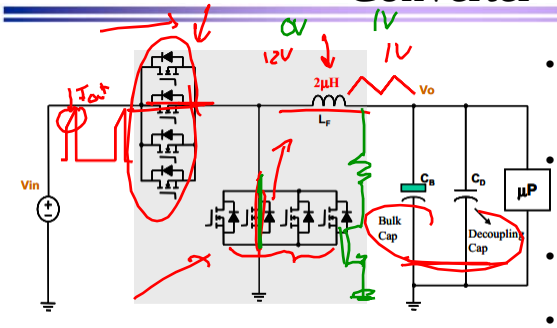


Fig. 1.6. A single-phase buck converter for a Pentium III processor.

- Buck is simplest topology which can meet required step-down
- Multiple devices in parallel used to reduce (dominant) conduction losses
- Large inductor needed to reduce ripple
- Large output cap needed for ripple; transient hold-up
- Switching frequency increased to reduce ripple; still well-below processor speed

K Yao, "High-Frequency and High-Performance VRM Design for the Next Generations of Processors", 2004

Today's Approach: Multiphase Buck

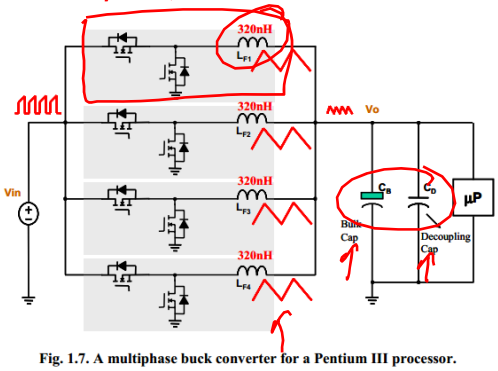


Fig. 1.7. A multiphase buck converter for a Pentium III processor.

- Multiphase to distribute the large output current
- Interleaving to cancel current ripple and to improve transient response
- 12V-input voltage bus to reduce the input bus conduction loss
- Multiphase controller with switching frequency up to 1 MHz
- Commonly, 300KHz to 500KHz switching frequency to achieve reasonable efficiency with 30V vertical trench MOSFETs
- Several electrolytic bulk capacitors in parallel to limit the transient voltage spikes; ceramics in parallel for HF

K Yao, "High-Frequency and High-Performance VRM Design for the Next Generations of Processors", 2004

2-Phase Interleaving

Figure 4. Cancellation of inductor ripple current with D = 25%

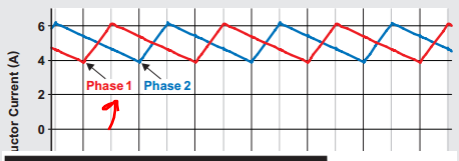


Figure 2. Node waveforms of phases 1 and 2

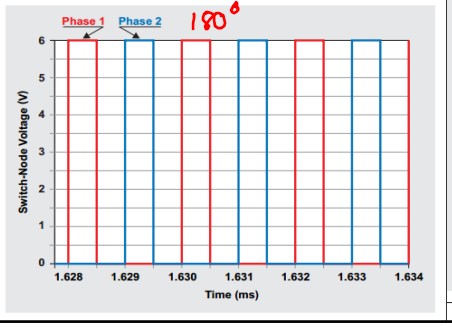
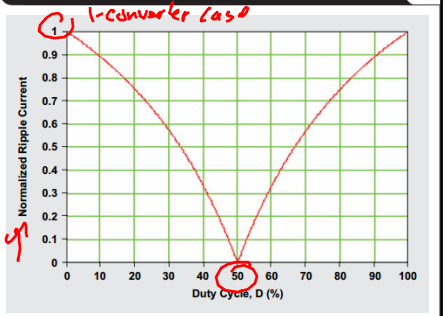


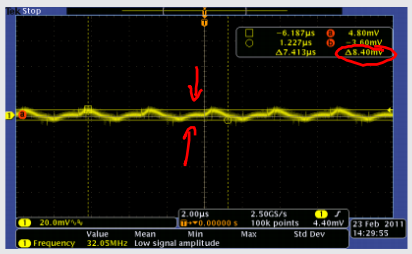
Figure 3. Normalized capacitor ripple current as a function of duty cycle



TI, "Benefits of a multiphase buck converter", 2012

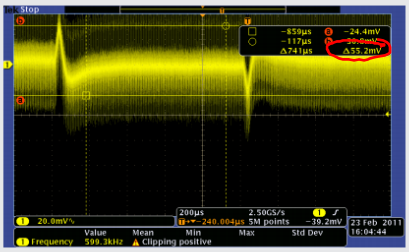
2-phase VRM Operating Waveforms

Figure 9. Output voltage ripple



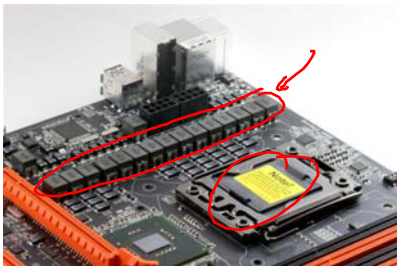
V_{IN} = 12 V, V_{OUT} = 1.2 V at 40 A

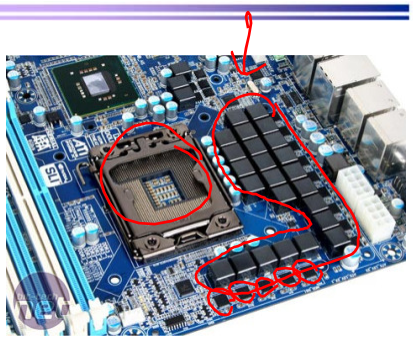
Figure 10. Transient response: 20 µs with 10-A load step (undershoot/overshoot ~ 27 mV)



TI, "Benefits of a multiphase buck converter", 2012

Commercial Motherboard VRMs





Issues:

- Small duty cycles (D ~ 1/12) cause poor device utilization
- Large size due to many phases despite high switching frequency
- C_{out} limited by holdup times (large signal); further increase in f_s not beneficial
- Noneven slew rates:

$$\Delta I_{\max} = \frac{12 - V_{out}}{L} \qquad \Delta I_{\min} = \frac{-V_{out}}{L}$$

- Balancing between phases needs to be enforced via control

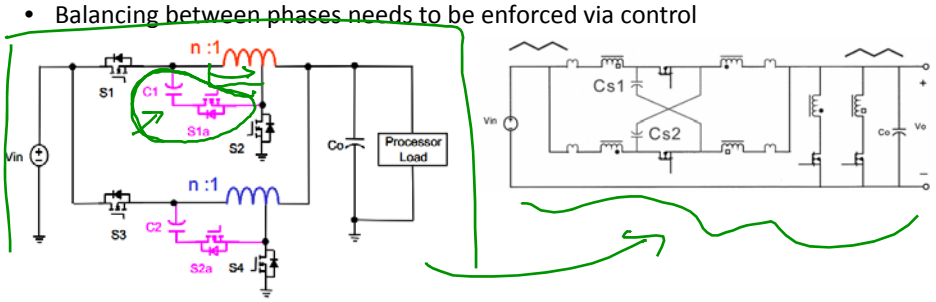
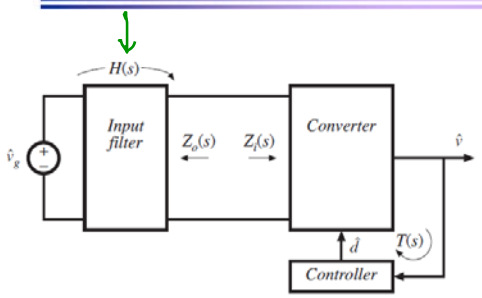


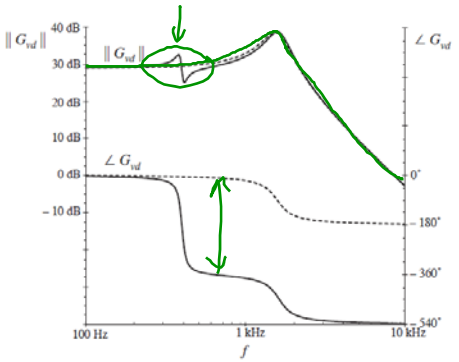
Fig. 9. Multiphase tapped-inductor buck converter with an additional active clamping circuit for each channel.

P Xu, J Wei, and F Lee, "Multiphase Coupled-Buck Converter—A Novel High Efficient 12 V Voltage Regulator Module"

Further Topics In Power Electronics

Input Filter Design

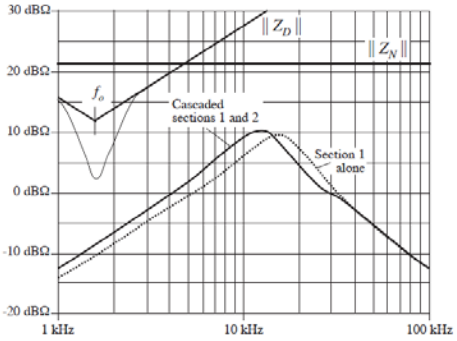




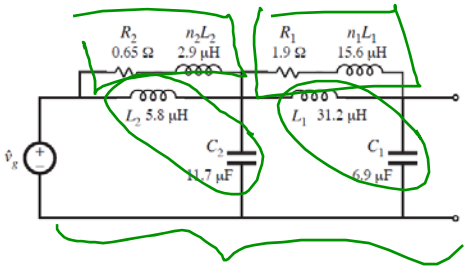
- Filter can seriously degrade converter control system behavior
- Use extra element theorem to derive conditions which ensure that converter dynamics are not affected by input filter
- Must design input filter having adequate damping

Damped Input Filters

Design criteria derived via Extra Element theorem:

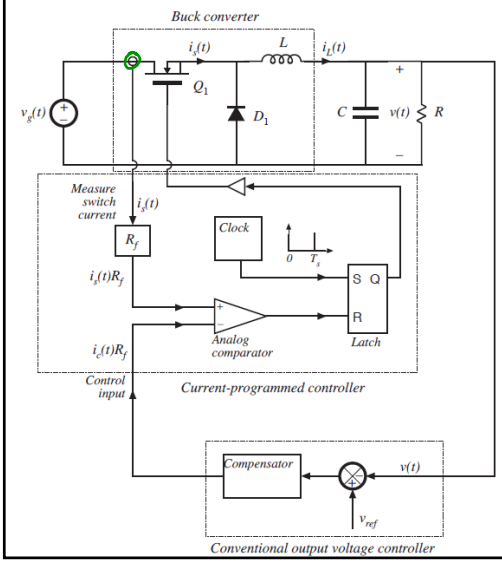


Two-section damped input filter design:

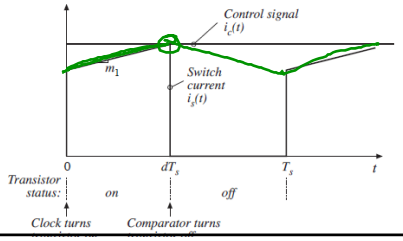


$$|Z(j\omega)| \gg |Z_N(j\omega)|$$
$$|Z(j\omega)| \gg |Z_D(j\omega)|$$

Current Programmed Control

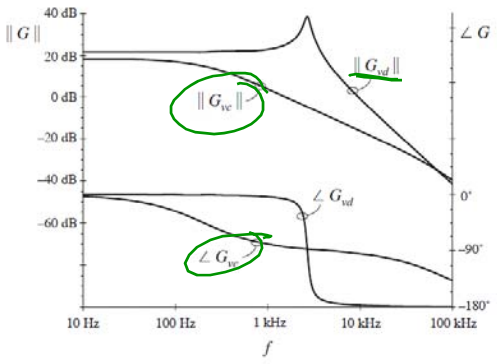


- Chapter 12
- A very popular method for controlling PWM converters
- Transistor turns off when its current $i_s(t)$ is equal to the control input $i_c(t)$
- Simpler dynamics, more robust compensator

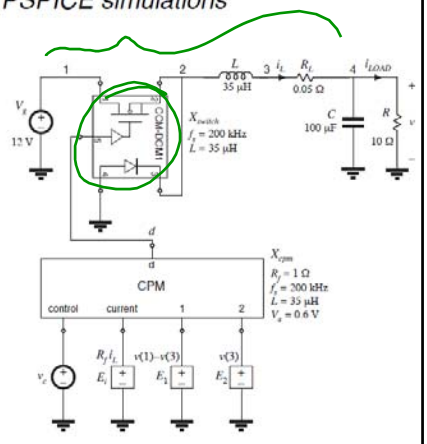


Buck Converter With CPM

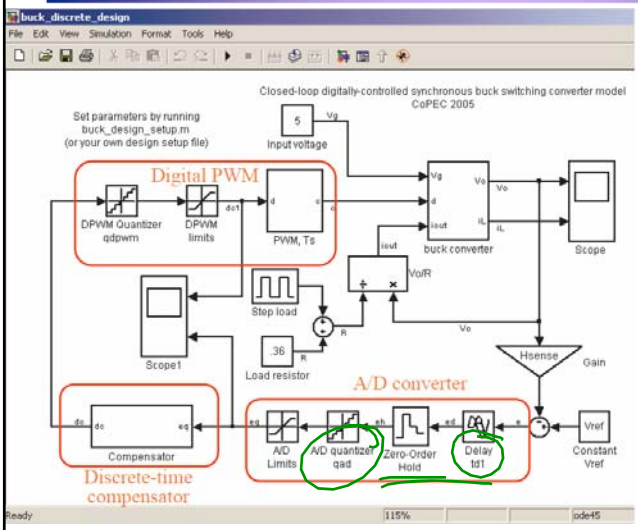
Comparison of control-to-output transfer functions



Averaged switch model used in PSPICE simulations



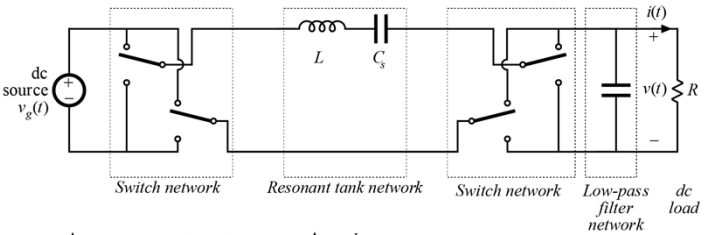
Digital Control of SMPS

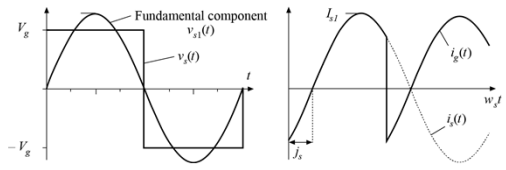


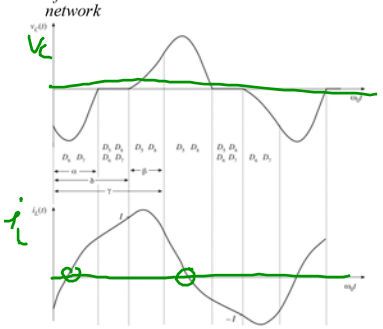
- Digital Control can improve noise immunity, element variation, size/cost
- Advanced tuning algorithms can be included to change compensator dynamically or over lifetime
- Can model power stage without averaging assumptions

- Need to include sampling, delay, saturation, and quantization effects

Resonant and Soft-Switching Topologies

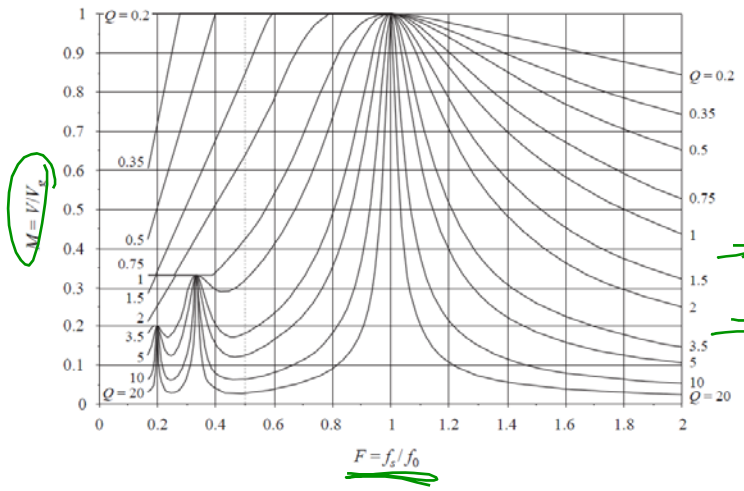






Resonant Converters: Frequency Modulation

Series resonant dc-dc converter example

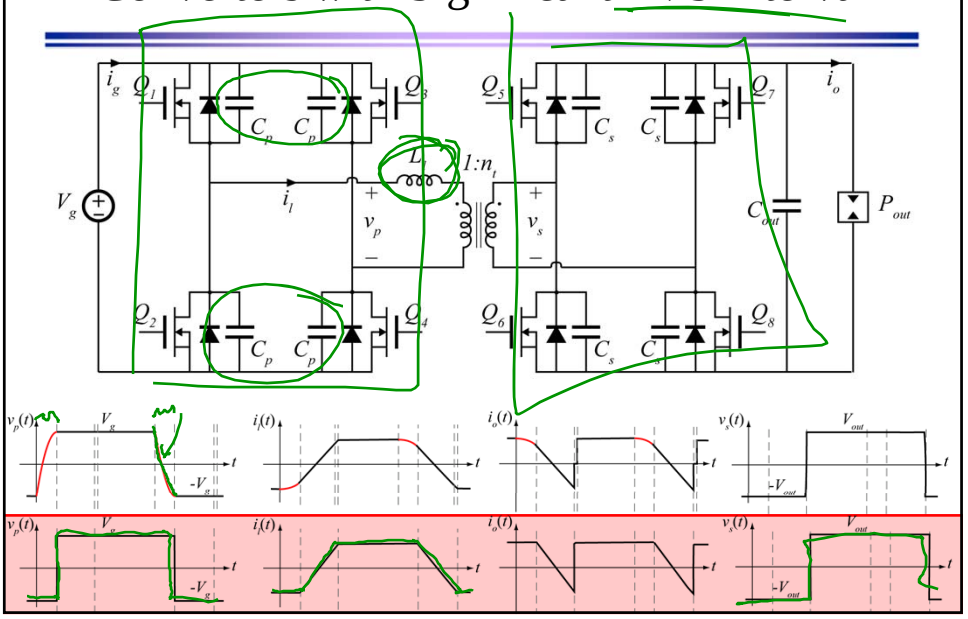


- Complex!
- Small ripple approximation is not valid

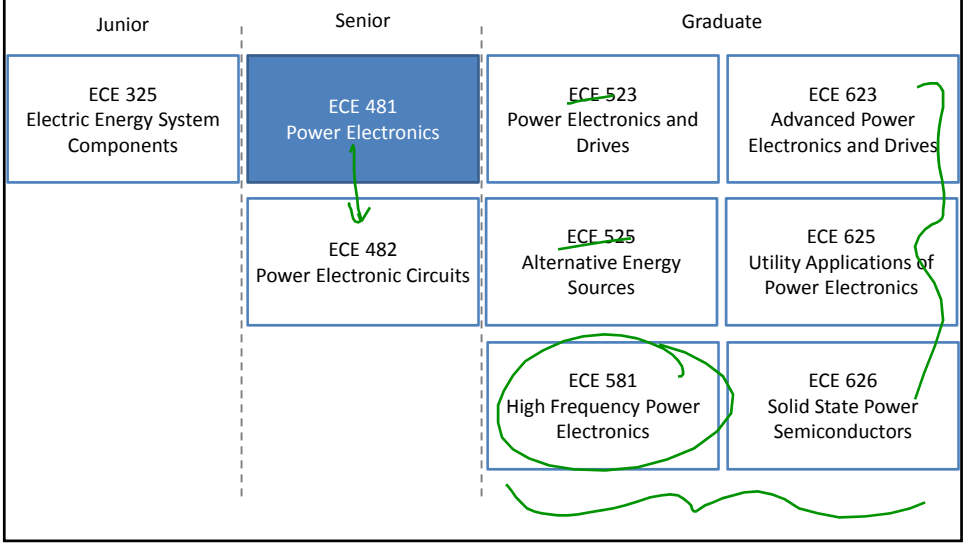
Need new approaches:

- Sinusoidal approximation
- State plane analysis

Converters with Significant ZVS Interval



Power Electronics Courses at UTK



Thank you for a Great Semester

Good Luck with Finals!