Lecture 9: Isolated Converters

ECE 481: Power Electronics

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Fall 2013

Announcements

- Midterm exam begins at the end of class today
  - Turn in Thursday, 10/3
  - You may use extra sheets

Midterm Exam #1

Fall 2013
ECE 481: Power Electronics

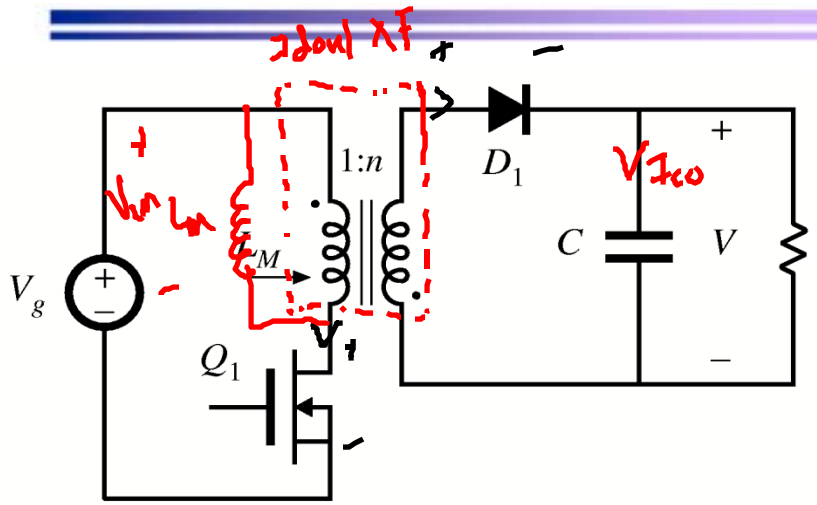
Instructions: This is a one-week take-home exam. It is an open-book, open-note, but ***absolutely no collaboration is allowed***. You may not use internet resources other than the course website and contained materials. Show all work, partial credit will be given. When you have completed the exam, sign the University of Tennessee Knoxville Honor Statement below:

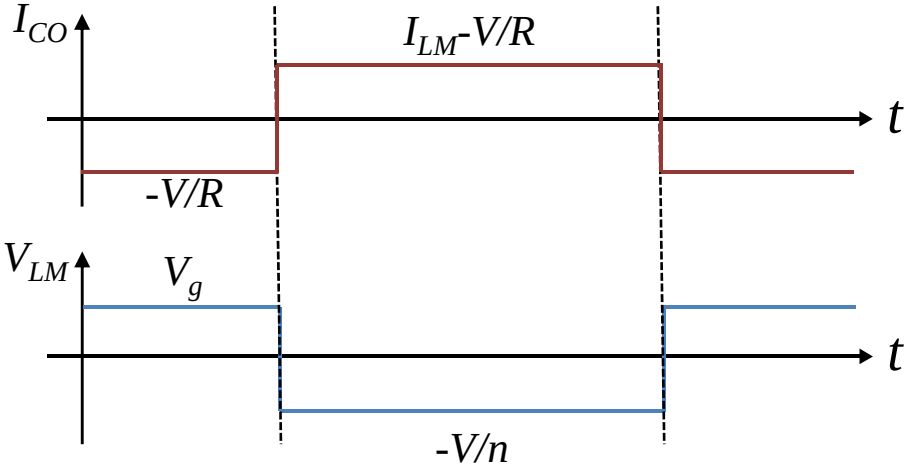
> *As a student of the University, I pledge that I have neither knowingly given nor received any inappropriate assistance in this academic work, thus affirming my own personal commitment to honor and integrity*

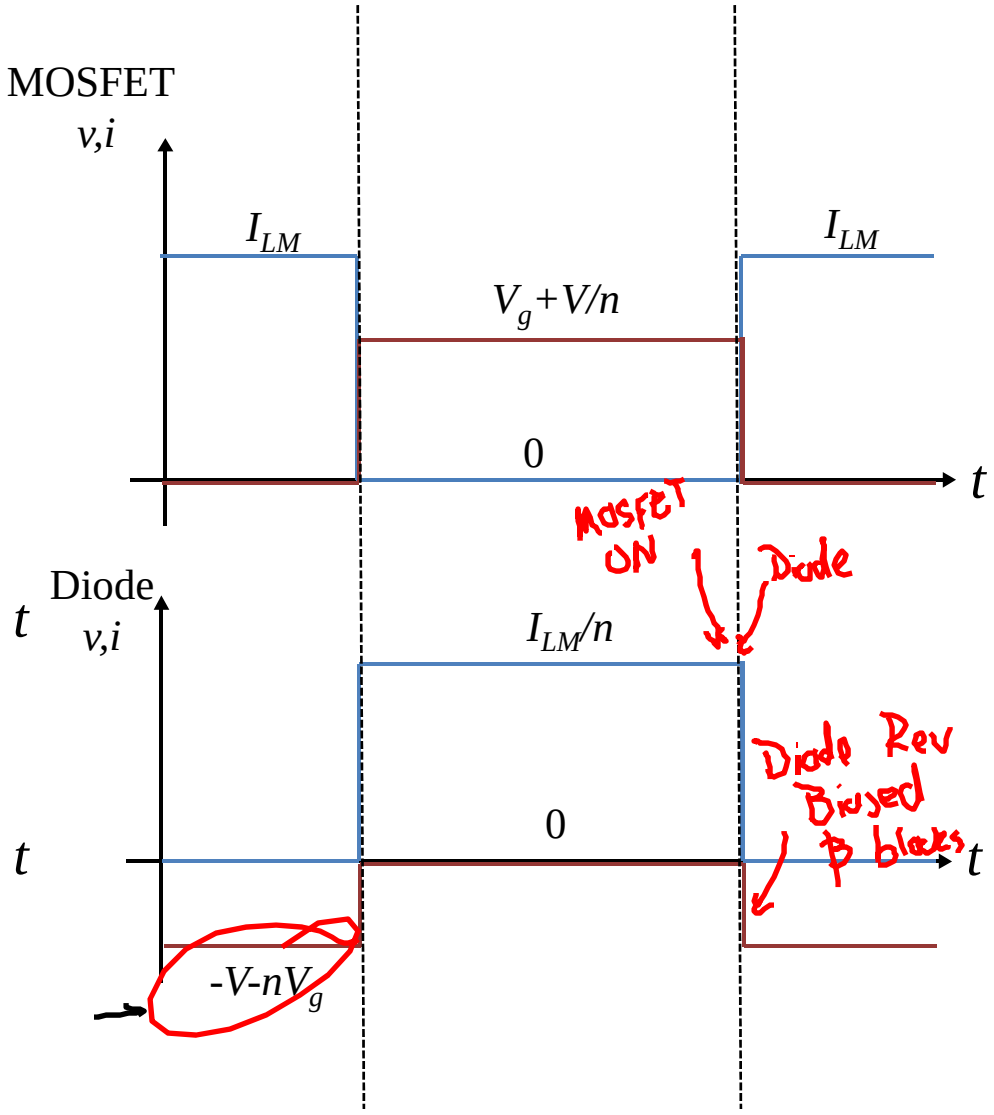
Signature: _____

This exam is due at the beginning of class, 11:10am, Thursday October 3rd. The exam contains three problems.

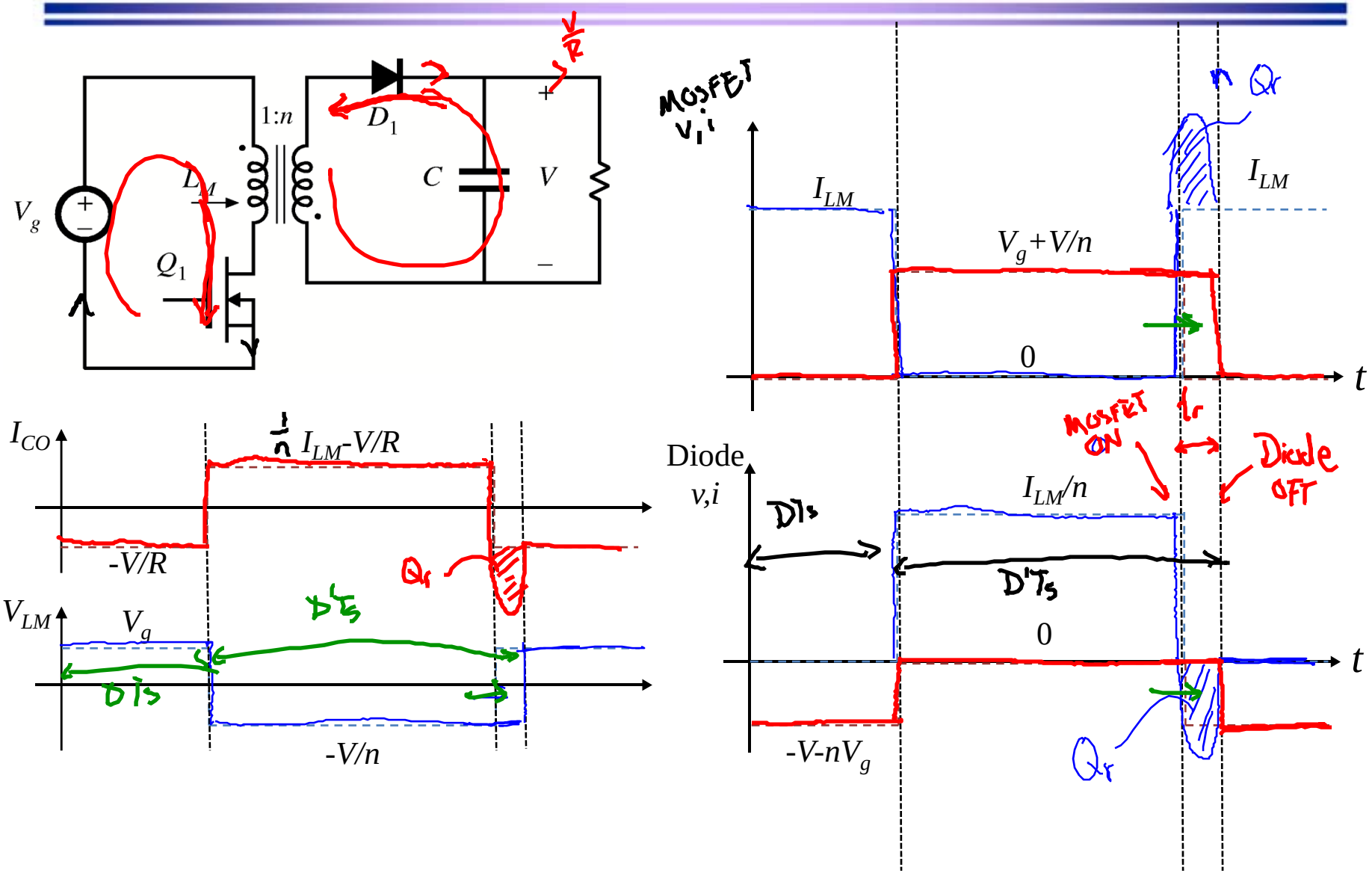
Flyback Ideal Waveforms







Flyback Reverse Recovery

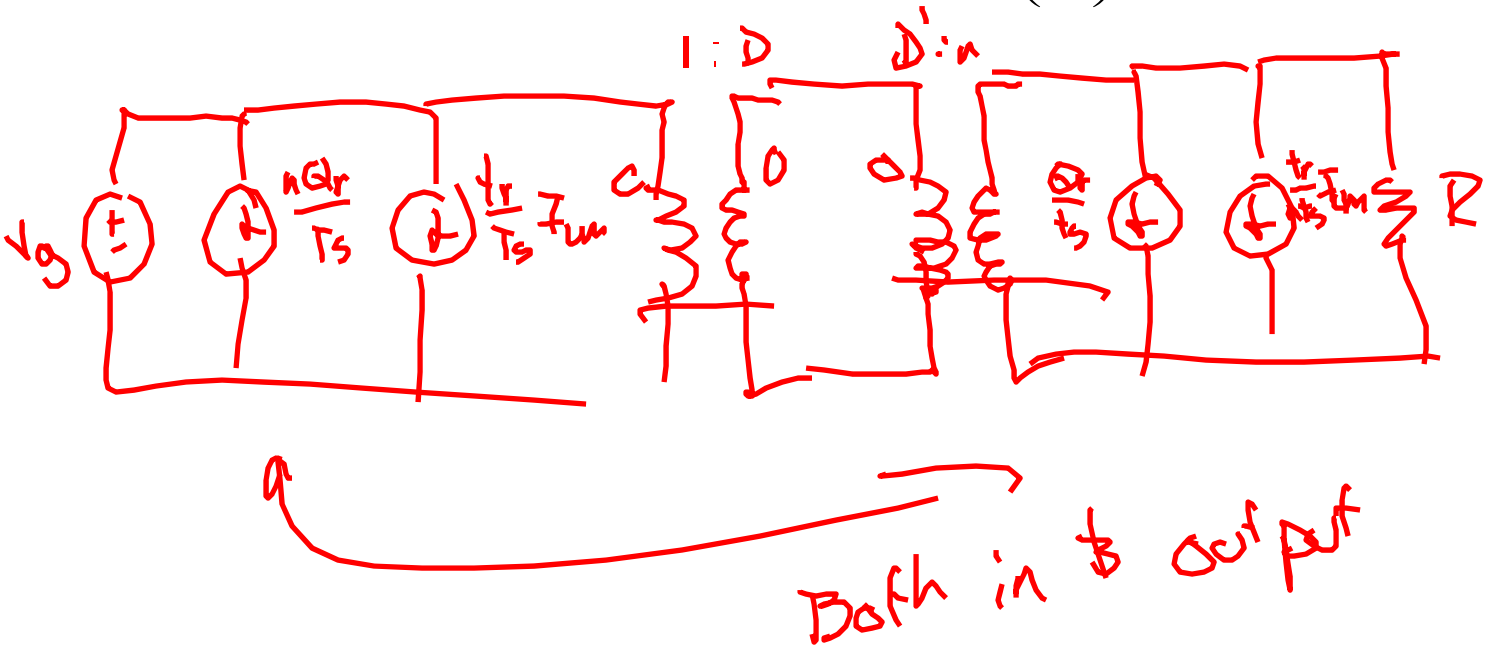


Flyback Reverse Recovery

$$\langle i_g \rangle = DI_{lm} + \frac{t_r}{T_s} I_{lm} + \frac{Q_r}{T_s}$$

$$\langle i_{co} \rangle = 0 = D' \frac{I_{lm}}{n} - \frac{V}{R} - \frac{t_r}{nT_s} I_{lm} - \frac{Q_r}{nT_s}$$

$$\langle v_{lm} \rangle = 0 = DV_g - D'\left(\frac{V}{n}\right)$$

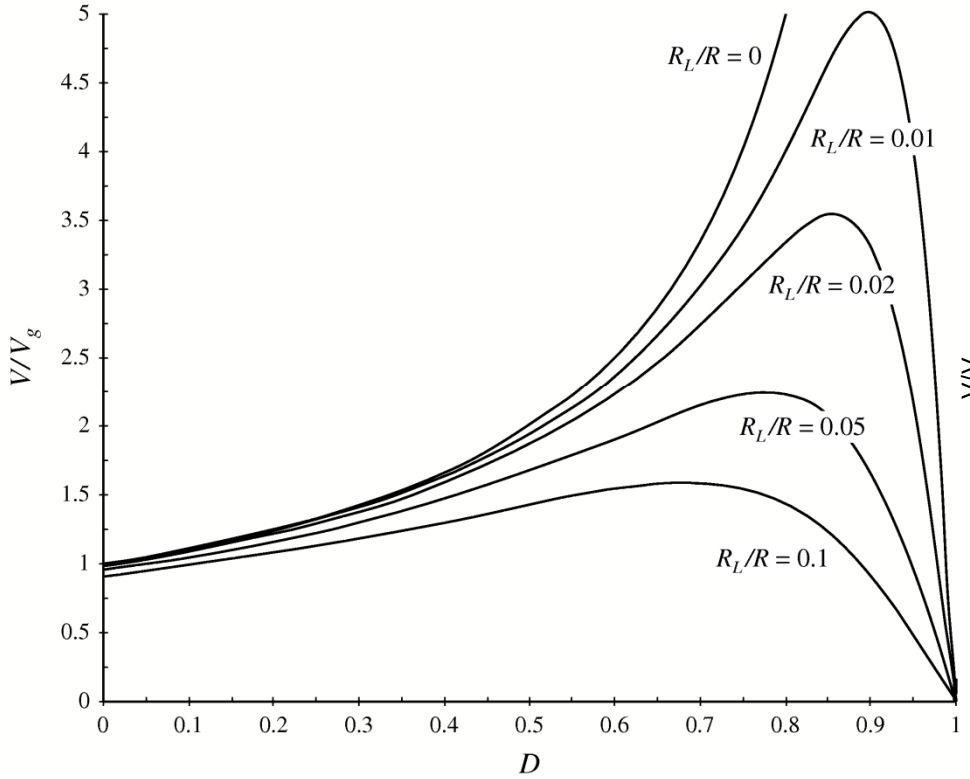


Discussion: Flyback converter

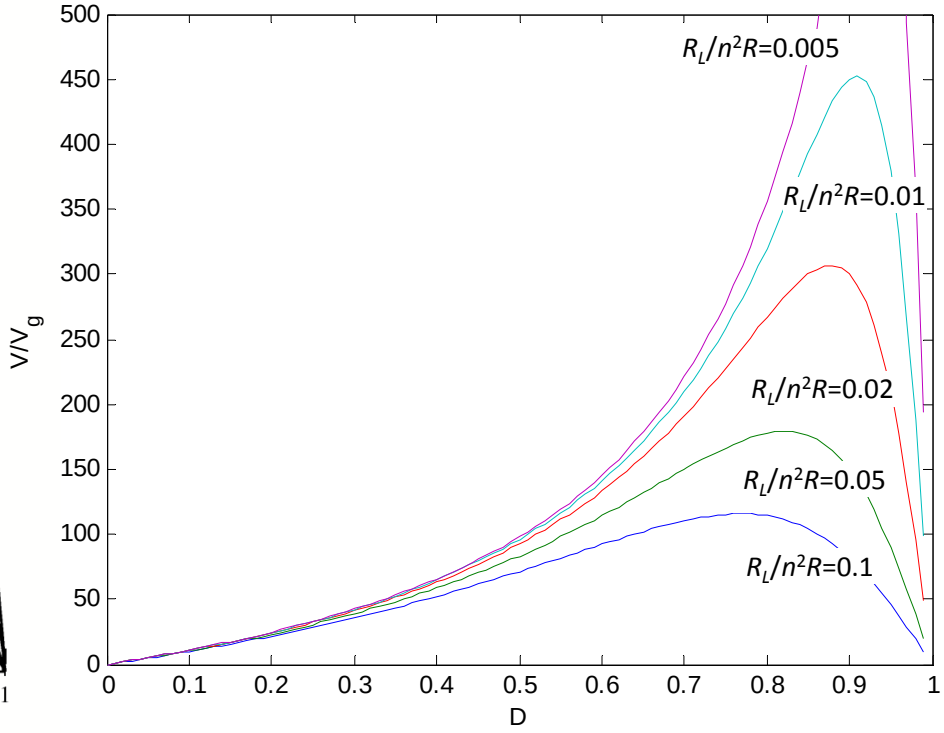
- Widely used in low power and/or high voltage applications
- Low parts count
- Multiple outputs are easily obtained, with minimum additional parts
- Cross regulation is inferior to buck-derived isolated converters
- Often operated in discontinuous conduction mode
- DCM analysis: DCM buck-boost with turns ratio

Large Step Conversion Ratio

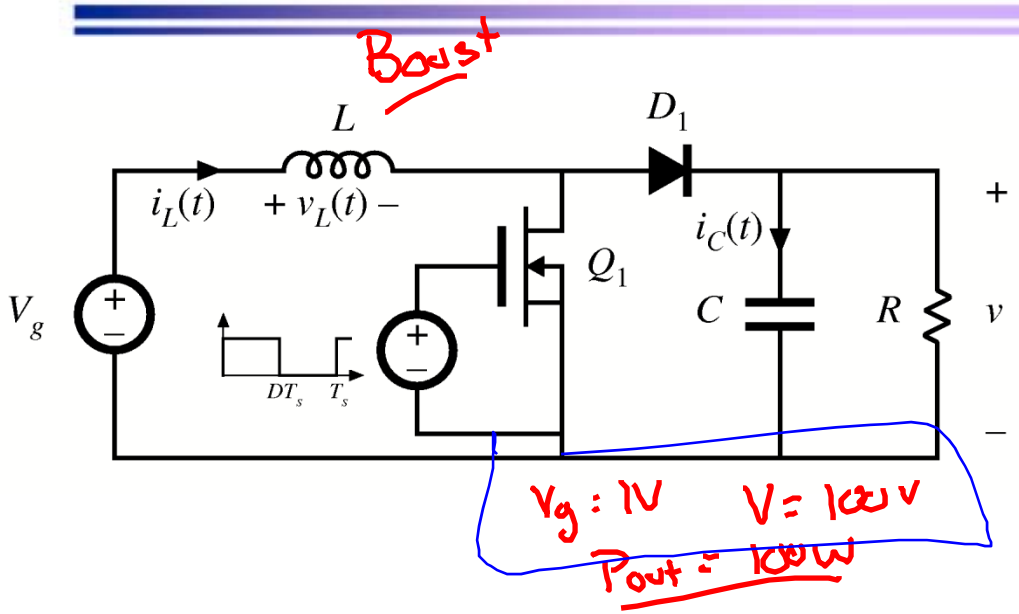
Boost Converter

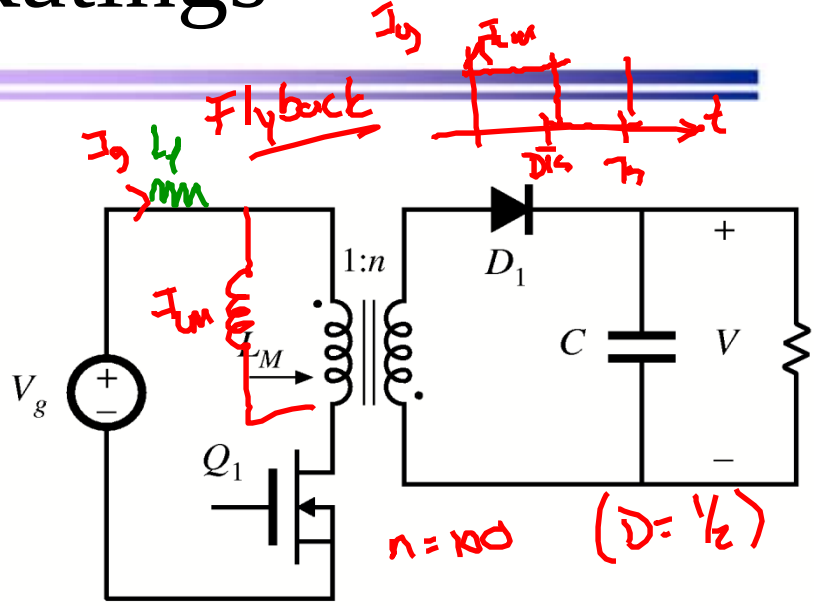


Flyback, n=100



Transistor Ratings





transistor

$V_{off\text{-}pk} = V = 100V$

$I_{on\text{-}pk} = I_L = I_g = 100A$

"Switch Stress"

$S = V_{off\text{-}pk} I_{on\text{-}pk}$

$= 10kVA$

"Switch Utilization" $U = \frac{P_{out}}{S} = \frac{100W}{10kVA} = \frac{1}{100}$

$V_{off\text{-}pk} = V_g + \frac{V}{n} = 2V$

$I_{on\text{-}pk} = I_{LM} = \frac{I_g}{D} = 200A$

$S = 400\ VA$

$U = \frac{1}{4}$

6.4. Converter evaluation and design

For a given application, which converter topology is best?

There is no ultimate converter, perfectly suited for all possible applications

Trade studies

- Rough designs of several converter topologies to meet the given specifications
- An unbiased quantitative comparison of worst-case transistor currents and voltages, transformer size, etc.

Comparison via switch stress, switch utilization, and semiconductor cost

Spreadsheet design

6.4.1. Switch stress and switch utilization

- Largest single cost in a converter is usually the cost of the active semiconductor devices
- Conduction and switching losses associated with the active semiconductor devices often dominate the other sources of loss

This suggests evaluating candidate converter approaches by comparing the voltage and current stresses imposed on the active semiconductor devices.

Minimization of total switch stresses leads to reduced loss, and to minimization of the total silicon area required to realize the power devices of the converter.

Total active switch stress S

In a converter having k active semiconductor devices, the total active switch stress S is defined as

$$S = \sum_{j=1}^{k} V_j I_j$$

where

V_j is the peak voltage applied to switch j,

I_j is the rms current applied to switch j (peak current is also sometimes used).

In a good design, the total active switch stress is minimized.

Active switch utilization U

It is desired to minimize the total active switch stress, while maximizing the output power P_{load}.

The active switch utilization U is defined as

$$U = \frac{P_{load}}{S}$$

The active switch utilization is the converter output power obtained per unit of active switch stress. It is a converter figure-of-merit, which measures how well a converter utilizes its semiconductor devices.

Active switch utilization is less than 1 in transformer-isolated converters, and is a quantity to be maximized.

Converters having low switch utilizations require extra active silicon area, and operate with relatively low efficiency.

Active switch utilization is a function of converter operating point.

CCM flyback example: Determination of S

During subinterval 2, the transistor blocks voltage $V_{Q1,pk}$ equal to V_g plus the reflected load voltage:

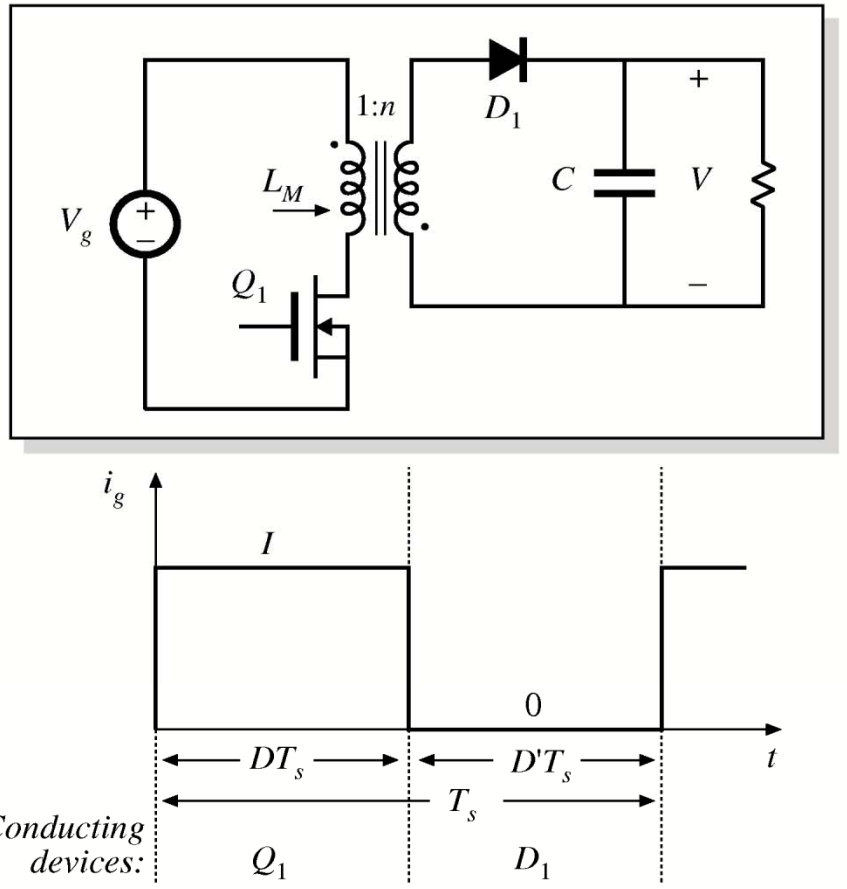
$$V_{Q1,pk} = V_g + \frac{V}{n} = \frac{V_g}{D'}$$

Transistor current coincides with $i_g(t)$. RMS value is

$$I_{Q1,rms} = I\sqrt{D} = \frac{P_{load}}{V_g\sqrt{D}}$$

Switch stress S is

$$S = V_{Q1,pk}\, I_{Q1,rms} = \left(V_g + \frac{V}{n}\right)\left(I\sqrt{D}\right)$$



CCM flyback example: Determination of U

Express load power P_{load} in terms of V and I:

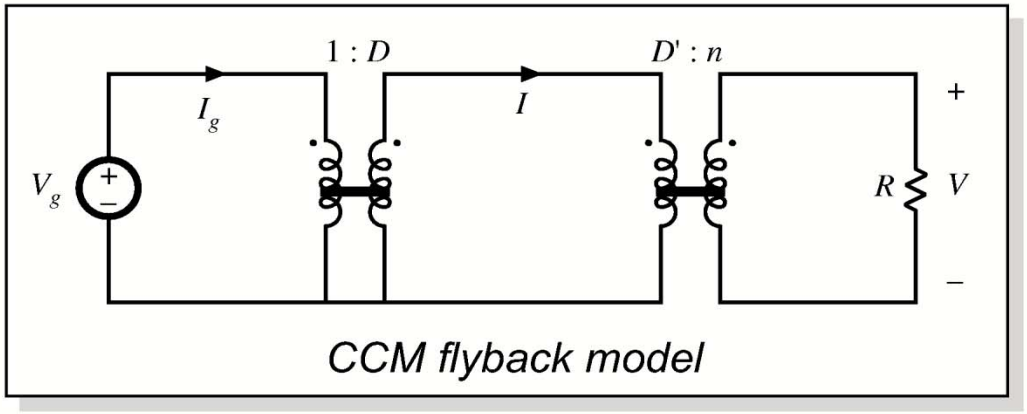
$$P_{load} = D' V \frac{I}{n}$$

Previously-derived expression for S:

$$S = V_{Q1,pk}\, I_{Q1,rms} = \left(V_g + \frac{V}{n}\right)\left(I\sqrt{D}\right)$$

Hence switch utilization U is

$$U = \frac{P_{load}}{S} = D'\sqrt{D}$$



CCM flyback model

Flyback example: switch utilization $U(D)$

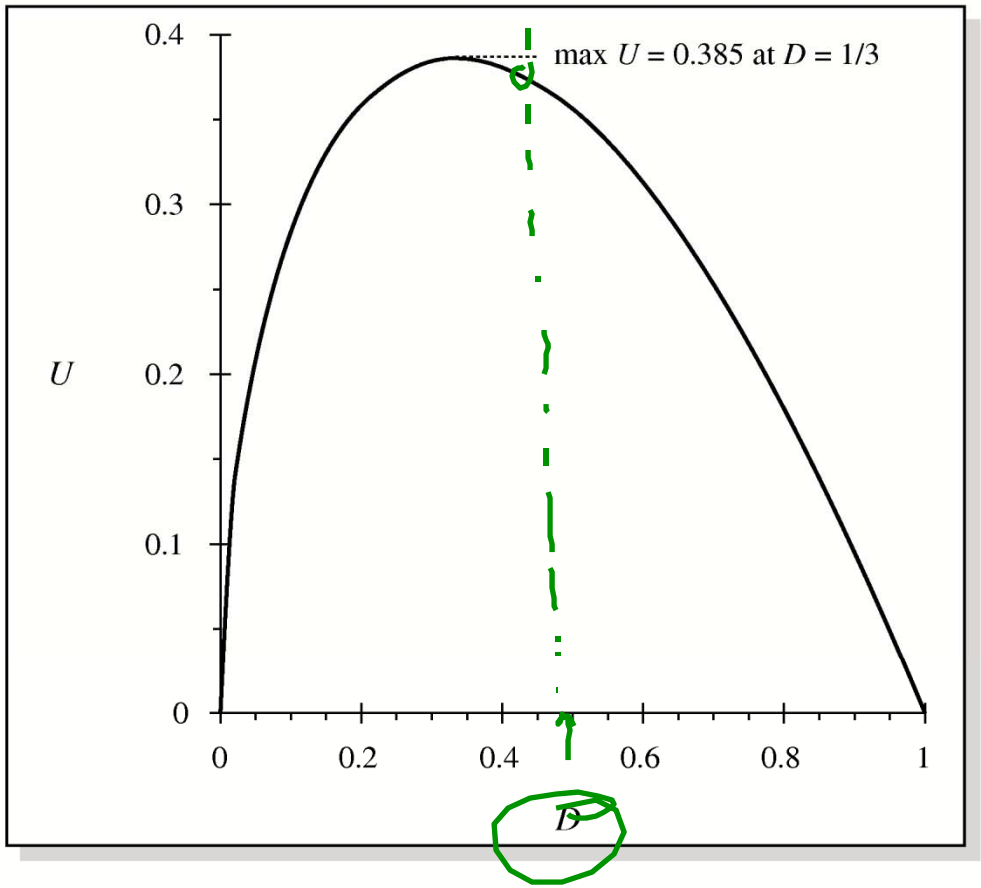
For given V, V_g, P_{load}, the designer can arbitrarily choose D. The turns ratio n must then be chosen according to

$$n = \frac{V}{V_g}\frac{D'}{D}$$

Single operating point design: choose $D = 1/3$.

small D leads to large transistor current

large D leads to large transistor voltage



Comparison of switch utilizations of some common converters

Table 6.1. Active switch utilizations of some common dc-dc converters, single operating point.

Converter	*U(D)*	max *U(D)*	max *U(D)* *occurs at D =*
Buck	$\sqrt{D}$	1	1
Boost	$\frac{D'}{\sqrt{D}}$	∞	0
Buck-boost, flyback, nonisolated SEPIC, isolated SEPIC, nonisolated Cuk, isolated Cuk	$D'\sqrt{D}$	$\frac{2}{3\sqrt{3}} = 0.385$	$\frac{1}{3}$
Forward, $n_1 = n_2$	$\frac{1}{2}\sqrt{D}$	$\frac{1}{2\sqrt{2}} = 0.353$	$\frac{1}{2}$
Other isolated buck-derived converters (full-bridge, half-bridge, push-pull)	$\frac{\sqrt{D}}{2\sqrt{2}}$	$\frac{1}{2\sqrt{2}} = 0.353$	1
Isolated boost-derived converters (full bridge, push-pull)	$\frac{D'}{2\sqrt{1+D}}$	$\frac{1}{2}$	0

Active semiconductor cost vs. switch utilization

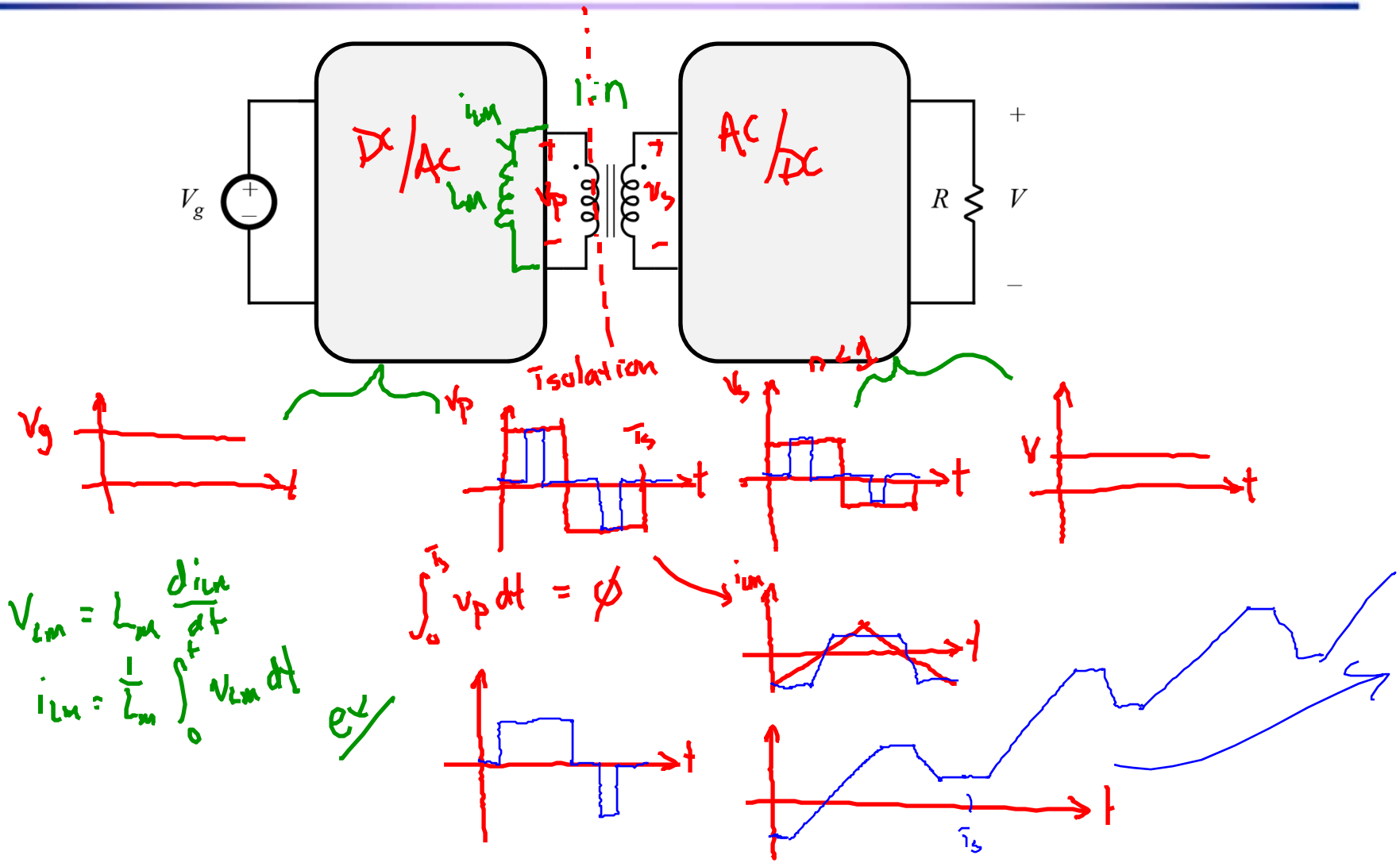
$$\left(\begin{array}{c}\text{semiconductor cost}\\ \text{per kW output power}\end{array}\right) = \frac{\left(\begin{array}{c}\text{semiconductor device cost}\\ \text{per rated kVA}\end{array}\right)}{\left(\begin{array}{c}\text{voltage}\\ \text{derating}\\ \text{factor}\end{array}\right)\left(\begin{array}{c}\text{current}\\ \text{derating}\\ \text{factor}\end{array}\right)\left(\begin{array}{c}\text{converter}\\ \text{switch}\\ \text{utilization}\end{array}\right)}$$

(semiconductor device cost per rated kVA) = cost of device, divided by product of rated blocking voltage and rms current, in \$/kVA. Typical values are less than \$1/kVA

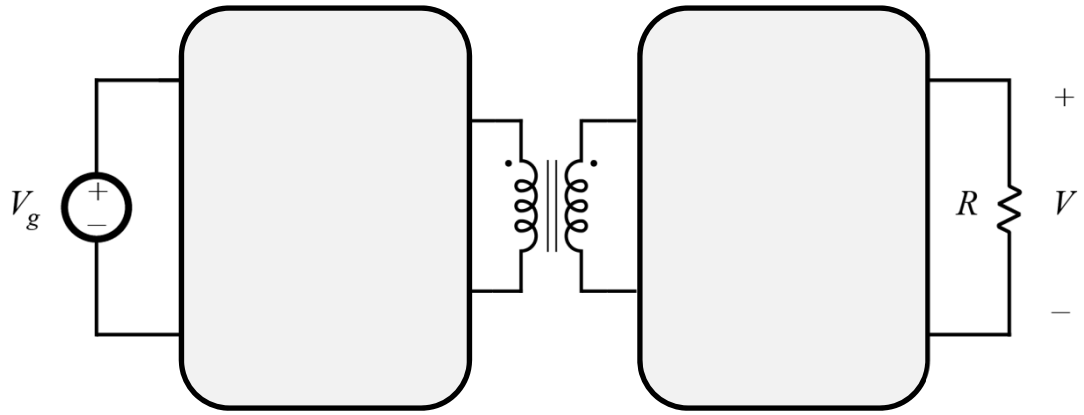
(voltage derating factor) and (current derating factor) are required to obtain reliable operation. Typical derating factors are 0.5 - 0.75

Typical cost of active semiconductor devices in an isolated dc-dc converter: \$1 - \$10 per kW of output power.

Isolated Converters



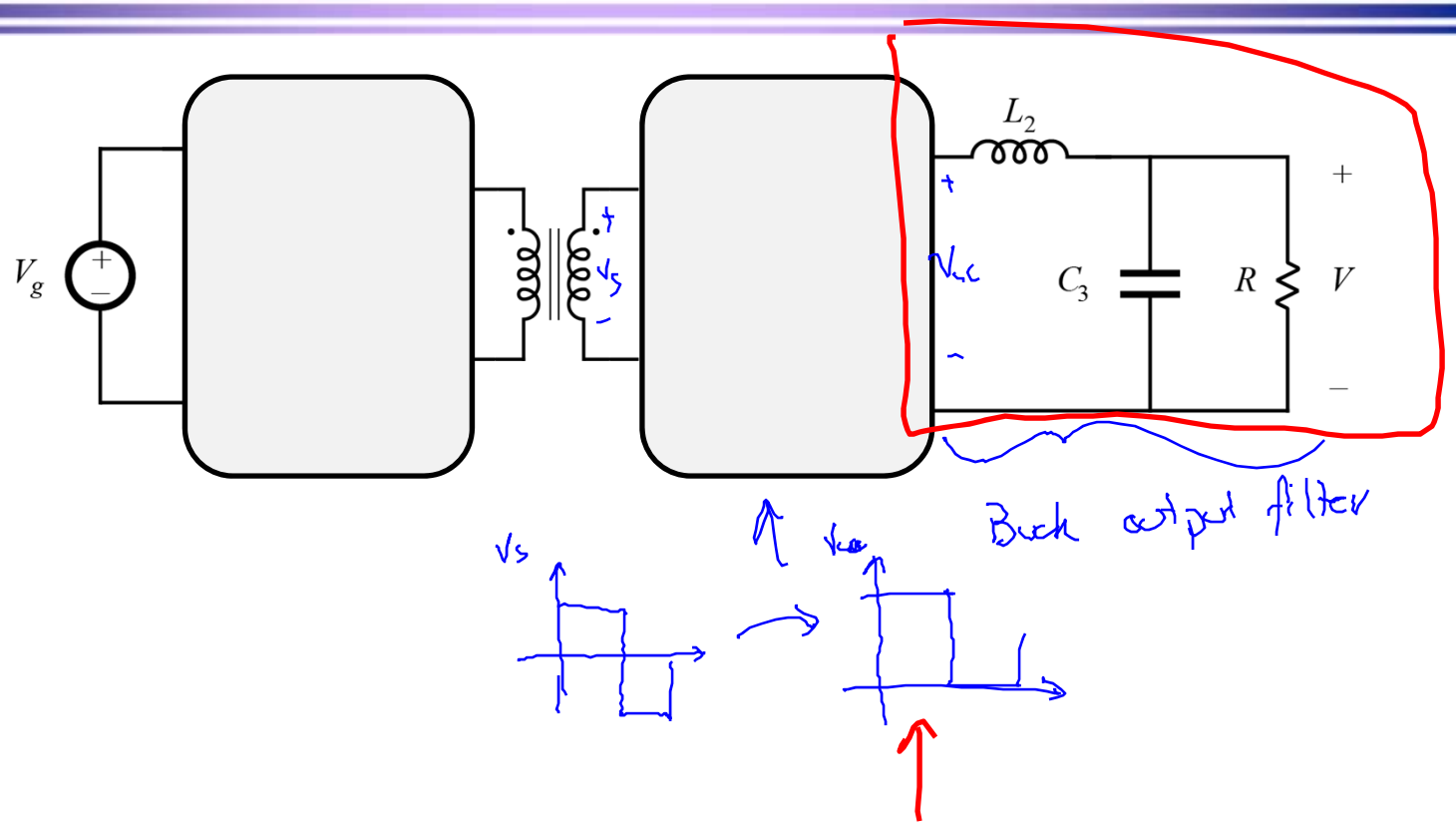
Transformer Saturation



Transformer reset

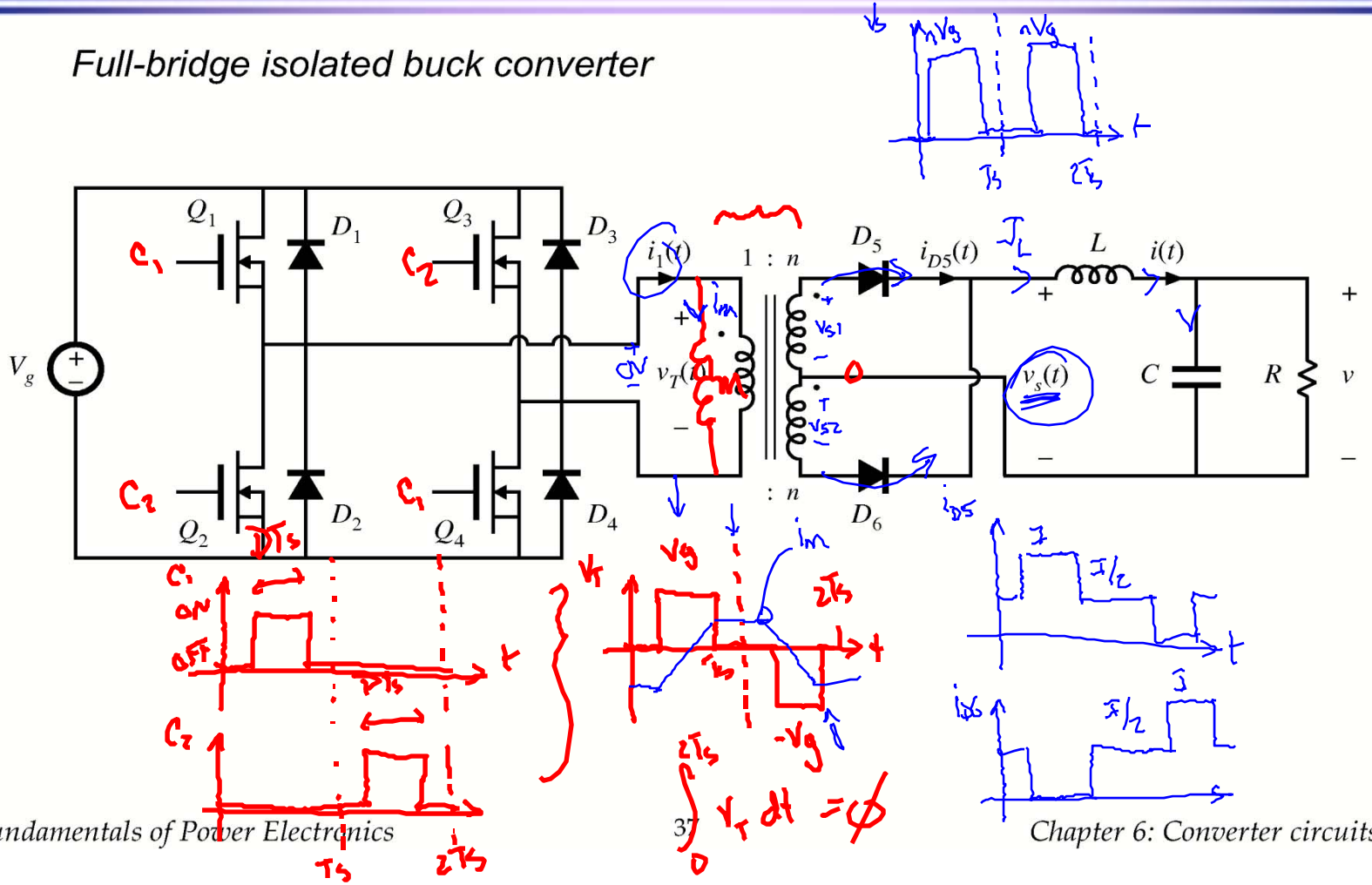
- "Transformer reset" is the mechanism by which magnetizing inductance volt-second balance is obtained
- The need to reset the transformer volt-seconds to zero by the end of each switching period adds considerable complexity to converters
- To understand operation of transformer-isolated converters:
  - replace transformer by equivalent circuit model containing magnetizing inductance
  - analyze converter as usual, treating magnetizing inductance as any other inductor
  - apply volt-second balance to all converter inductors, including magnetizing inductance

Buck-Derived Isolated Converters

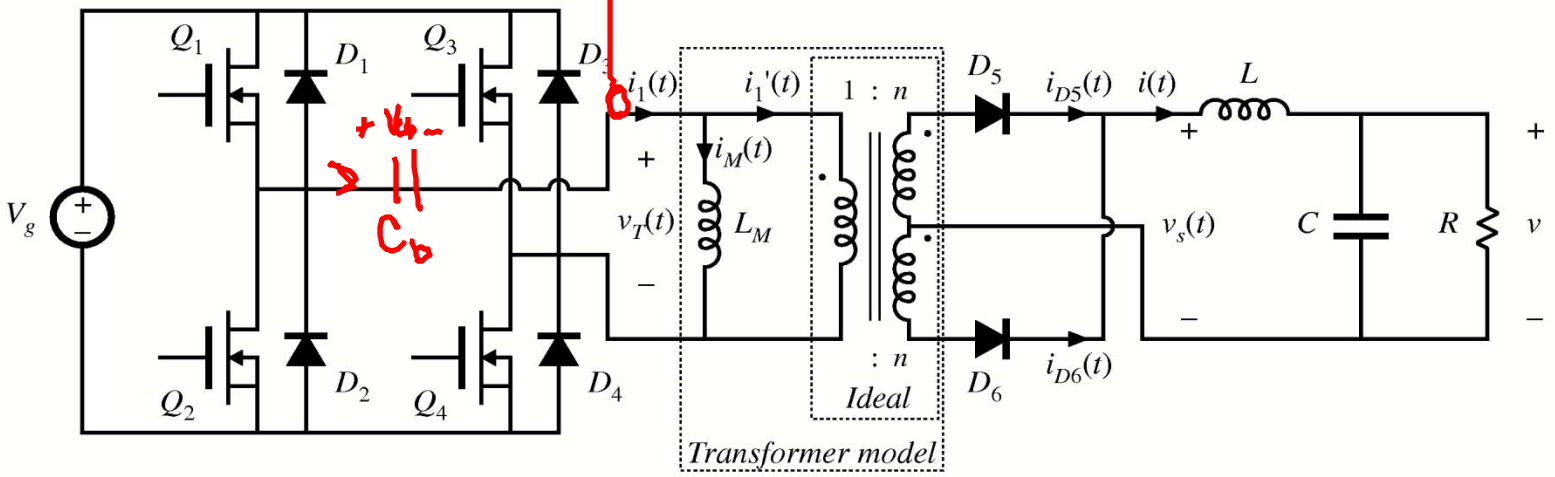


6.3.1. Full-bridge and half-bridge isolated buck converters

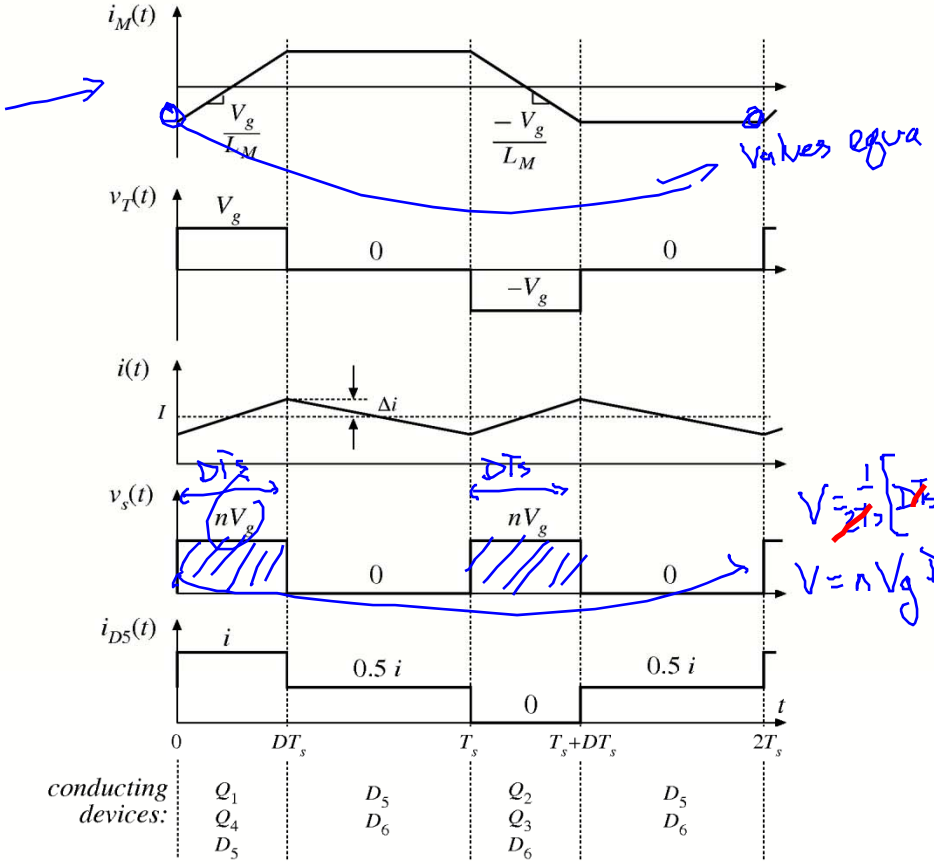
Full-bridge isolated buck converter



Full-bridge, with transformer equivalent circuit



Full-bridge: waveforms



- During first switching period: transistors Q_1 and Q_4 conduct for time DT_s , applying volt-seconds $V_g DT_s$ to primary winding
- During next switching period: transistors Q_2 and Q_3 conduct for time DT_s , applying volt-seconds $-V_g DT_s$ to primary winding
- Transformer volt-second balance is obtained over two switching periods
- Effect of nonidealities?