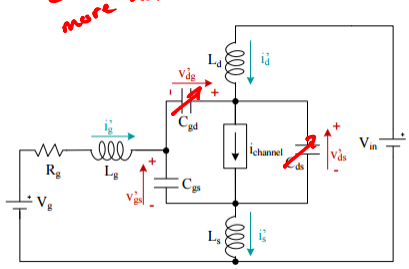
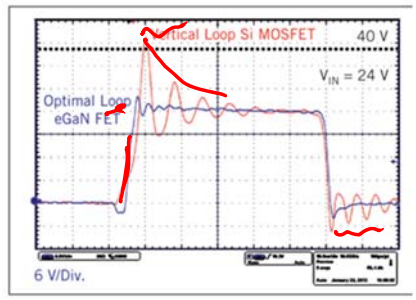
Experimental Switching Waveforms

ex. more detailed switching model





Approaches to reduce ringing:
(1) Select new device
(2) Improve layout

D Reusch, "eGaN® FET-Silicon Power Shoot-Out Vol. 13, Part 2: Optimal PCB Layout"
M Rodriguez et al, "Analysis of the switching process of power MOSFETs using a new analytical losses model"

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The Double Pulse Test

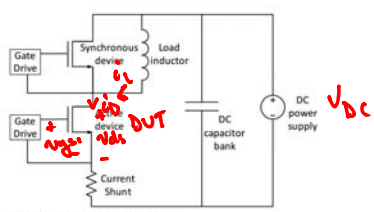
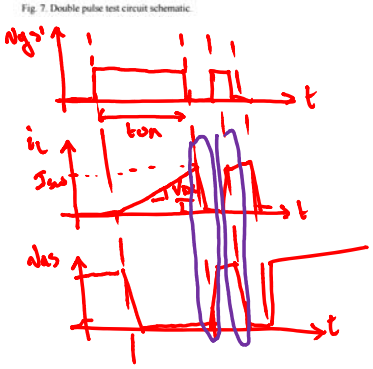


Fig. 7. Double pulse test circuit schematic.



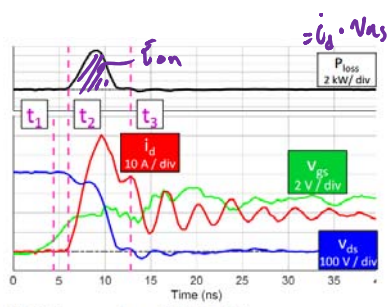


Fig. 11. Turn-on waveform at 400 V, 10 A, 25 °C.

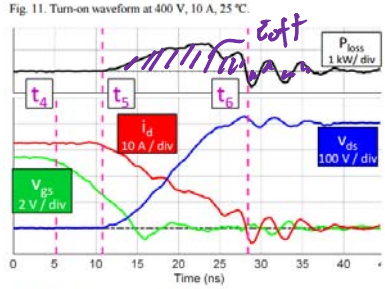


Fig. 12. Turn-off waveform at 400 V, 10 A, 25 °C.

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The Double Pulse Test

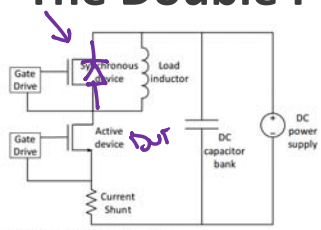


Fig. 7. Double pulse test circuit schematic.

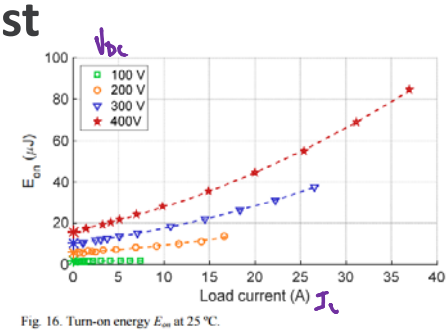
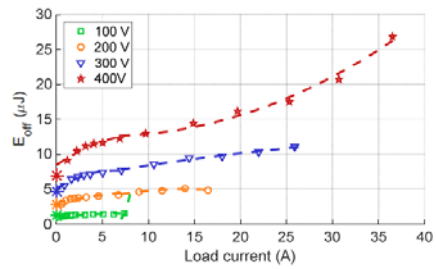


Fig. 16. Turn-on energy E_{on} at 25 °C.



- Purely empirical approach
- occasionally provided in a datasheet
- E_{on} & E_{off} vary significantly w/ Layout & Gate Drive circuit

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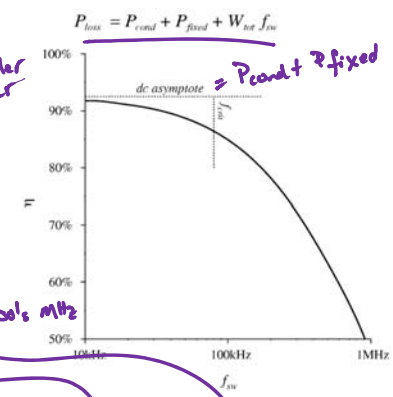
Converter Efficiency Vs. f_s

$P_{loss} = P_{cond} + P_{sw} + P_{fixed}$

$f(P_{out})$ $f(f_s)$ e.g. controller power

- Less P_{sw}
- Lower EMI/noise at HF

- Less ripple or
- Smaller passives
- faster control



0Hz — f_s — 100's MHz

60Hz — 1kHz — 10kHz — 100kHz — 1MHz

High power Line-commutated rectifier

High power IGBT-based e.g. EV traction drives

General power supplies

VRM

Research

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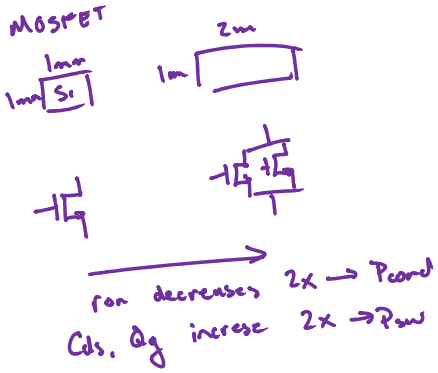
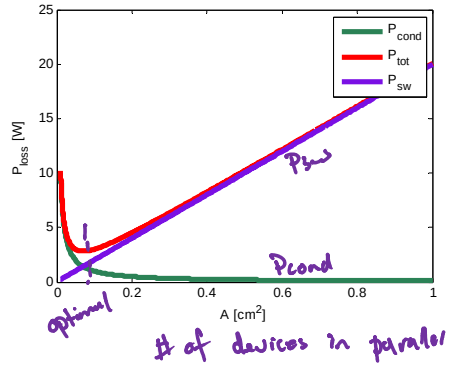
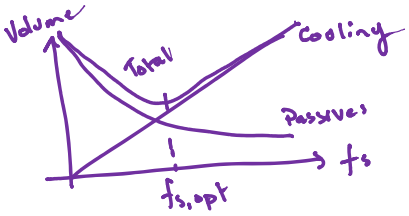
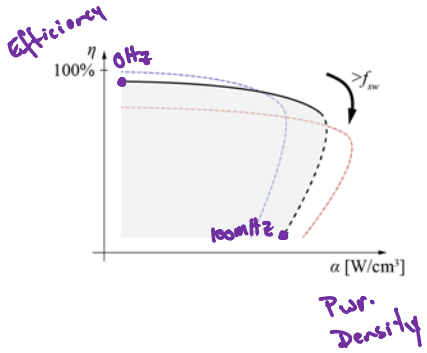
Die Size Selection



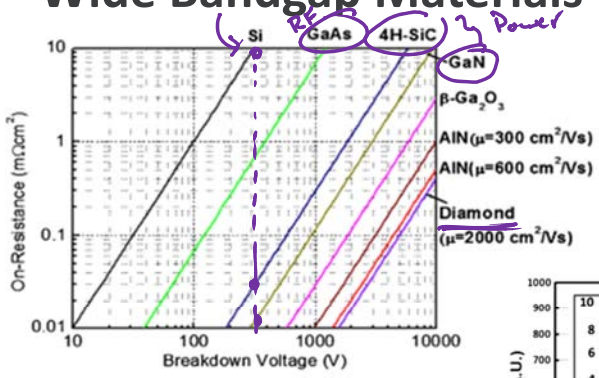


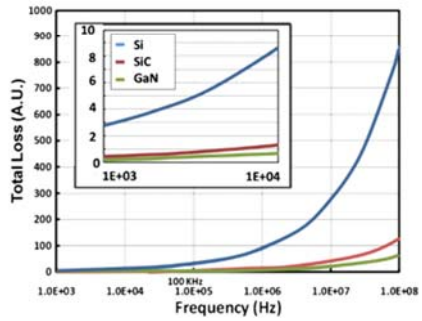
Converter Optimization





Wide Bandgap Materials





Srabanti Chowdhury *et al* "Current status and scope of gallium nitride-based vertical transistors for high-power electronics application" 2013 *Semicond. Sci. Technol.* 28, 074014

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