Active Switch Stress

Active Switch Utilization

Semiconductor Proportional Cost

$$\left(\begin{array}{c}\text{semiconductor cost}\\ \text{per kW output power}\end{array}\right) = \frac{\left(\begin{array}{c}\text{semiconductor device cost}\\ \text{per rated kVA}\end{array}\right)}{\left(\begin{array}{c}\text{voltage}\\ \text{derating}\\ \text{factor}\end{array}\right)\left(\begin{array}{c}\text{current}\\ \text{derating}\\ \text{factor}\end{array}\right)\left(\begin{array}{c}\text{converter}\\ \text{switch}\\ \text{utilization}\end{array}\right)}$$

(semiconductor device cost per rated kVA) = cost of device, divided by product of rated blocking voltage and rms current, in \$/kVA. Typical values are less than \$1/kVA

(voltage derating factor) and (current derating factor) are required to obtain reliable operation. Typical derating factors are 0.5 - 0.75

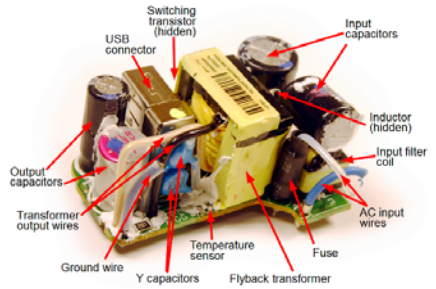
Typical cost of active semiconductor devices in an isolated dc-dc converter: \$1 - \$10 per kW of output power.

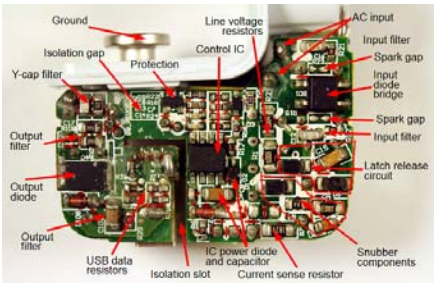
Switch Utilization Table

Table 6.1. Active switch utilizations of some common dc-dc converters, single operating point.

Converter	*U(D)*	max *U(D)*	max *U(D)* *occurs at D =*
Buck	$\sqrt{D}$	1	1
Boost	$\frac{D'}{\sqrt{D}}$	∞	0
Buck-boost, flyback, nonisolated SEPIC, isolated SEPIC, nonisolated Cuk, isolated Cuk	$D'\sqrt{D}$	$\frac{2}{3\sqrt{3}} = 0.385$	$\frac{1}{3}$
Forward, $n_1 = n_2$	$\frac{1}{2}\sqrt{D}$	$\frac{1}{2\sqrt{2}} = 0.353$	$\frac{1}{2}$
Other isolated buck-derived converters (full-bridge, half-bridge, push-pull)	$\frac{\sqrt{D}}{2\sqrt{2}}$	$\frac{1}{2\sqrt{2}} = 0.353$	1
Isolated boost-derived converters (full bridge, push-pull)	$\frac{D'}{2\sqrt{1+D}}$	$\frac{1}{2}$	0

Flyback Application: iPad Charger





http://www.righto.com/2014/05/a-look-inside-ipad-chargers-pricey.html

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Flyback Off-Line Charger Application Circuit

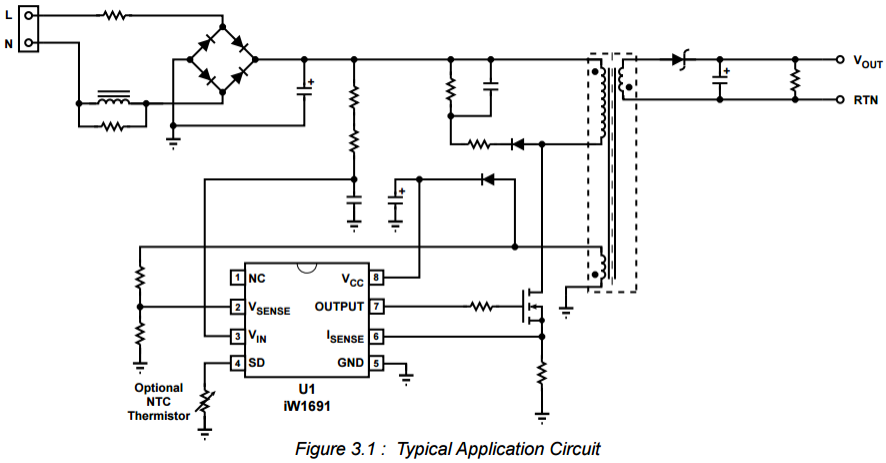

Figure 3.1 : Typical Application Circuit

http://www.dialog-semiconductor.com/sites/default/files/iw1691-datasheet.pdf

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Converter Design

- No definitive way to determine best converter topology for a given application
- Performance in power electronics depends heavily on details of implementation
  - Circuit layout
  - Gate driver design
  - Cooling system
  - Materials
- Switch stress/utilization give some direction on candidate topologies
  - Active switches often dominate loss and cost of converter

Parameterized Design

- To design converter independent of device implementation, consider voltage and current stresses of all elements
- In transformer isolated converters, the turns ratio is a degree of freedom for the design
- Use design equations in e.g. Excel or Matlab to examine effects of design on resulting stresses

Spreadsheet Design Example

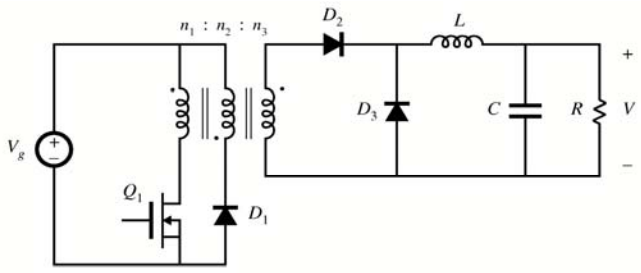
Specifications	
Maximum input voltage V_g	390 V
Minimum input voltage V_g	260 V
Output voltage V	15 V
Maximum load power P_{load}	200 W
Minimum load power P_{load}	20 W
Switching frequency f_s	100 kHz
Maximum output ripple Δv	0.1 V

- Input voltage: rectified 230 Vrms ±20%
- Regulated output of 15 V
- Rated load power 200 W
- Must operate at 10% load
- Select switching frequency of 100 kHz
- Output voltage ripple ≤ 0.1V

Compare single-transistor forward and flyback converters in this application

Specifications are entered at top of spreadsheet

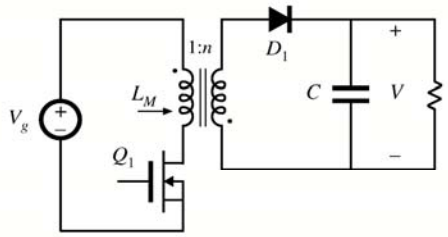
Forward Converter in CCM



Design variables	
Reset winding turns ratio n_2/n_1	1
Turns ratio n_3/n_1	0.125
Inductor current ripple Δi	2A ref to sec

- Design for CCM at full load; may operate in DCM at light load

Flyback Converter in CCM



Design variables

Turns ratio n_2/n_1	0.125
Inductor current ripple Δi	3 A ref to sec

- Design for CCM at full load; may operate in DCM at light load

Forward Converter Analysis

Maximum duty cycle occurs at minimum V_g and maximum P_{load}. Converter then operates in CCM, with

$$D = \frac{n_1}{n_3}\frac{V}{V_g}$$

Inductor current ripple is

$$\Delta i = \frac{D'VT_s}{2L}$$

Solve for L:

$$L = \frac{D'VT_s}{2\Delta i}$$

Δi is a design variable. For a given Δi, the equation above can be used to determine L. To ensure CCM operation at full load, Δi should be less than the full-load output current. C can be found in a similar manner.

Forward Converter DCM Bound

Check for DCM at light load. The solution of the buck converter operating in DCM is

$$V = \frac{n_3}{n_1} V_g \frac{2}{\sqrt{1 + \frac{4K}{D^2}}}$$

with $K = 2L / R T_s$, and $R = V^2 / P_{load}$

These equations apply equally well to the forward converter, provided that all quantities are referred to the transformer secondary side.

Solve for D:

$$D = \frac{2\sqrt{K}}{\sqrt{\left(\frac{2n_3 V_g}{n_1 V} - 1\right)^2 - 1}} \quad \text{in DCM} \qquad D = \frac{n_1}{n_3}\frac{V}{V_g} \quad \text{in CCM}$$

at a given operating point, the actual duty cycle is the small of the values calculated by the CCM and DCM equations above. Minimum D occurs at minimum P_{load} and maximum V_g.

Forward Converter Stress

Worst-case component stresses can now be evaluated.

Peak transistor voltage is

$$\max\left(v_{Q1}\right) = V_g\left(1 + \frac{n_1}{n_2}\right)$$

RMS transistor current is

$$I_{Q1,rms} = \frac{n_3}{n_1}\sqrt{D}\sqrt{I^2 + \frac{\left(\Delta i\right)^2}{3}} \approx \frac{n_3}{n_1}\sqrt{D}\, I$$

(this neglects transformer magnetizing current)

Other component stresses can be found in a similar manner. Magnetics design is left for a later chapter.

Spreadsheet Design Results

Forward converter design, CCM		*Flyback converter design, CCM*	
Design variables		*Design variables*	
Reset winding turns ratio n_2/n_1	1	Turns ratio n_2/n_1	0.125
Turns ratio n_3/n_1	0.125	Inductor current ripple Δi	3 A ref to sec
Inductor current ripple Δi	2 A ref to sec		
Results		*Results*	
Maximum duty cycle D	0.462	Maximum duty cycle D	0.316
Minimum D, at full load	0.308	Minimum D, at full load	0.235
Minimum D, at minimum load	0.251	Minimum D, at minimum load	0.179
Worst-case stresses		*Worst-case stresses*	
Peak transistor voltage v_{Q1}	780 V	Peak transistor voltage v_{Q1}	510 V
Rms transistor current i_{Q1}	1.13 A	Rms transistor current i_{Q1}	1.38 A
Transistor utilization U	0.226	Transistor utilization U	0.284
Peak diode voltage v_{D2}	49 V	Peak diode voltage v_{D1}	64 V
Rms diode current i_{D2}	9.1 A	Rms diode current i_{D1}	16.3 A
Peak diode voltage v_{D3}	49 V	Peak diode current i_{D1}	22.2 A
Rms diode current i_{D3}	11.1 A		
Rms output capacitor current i_C	1.15 A	Rms output capacitor current i_C	9.1 A

Design Comparison

Flyback converter

- Ideal peak transistor voltage: 510V
- Actual peak voltage will be higher, due to ringing causes by transformer leakage inductance
- An 800V or 1000V MOSFET would have an adequate design margin

Forward converter

- Ideal peak transistor voltage: 780V, 53% greater than flyback
- Few MOSFETs having voltage rating of over 1000 V are available —when ringing due to transformer leakage inductance is accounted for, this design will have an inadequate design margin
- Fix: use two-transistor forward converter, or change reset winding turns ratio

A conclusion: reset mechanism of flyback is superior to forward

Converter Current Stresses

Forward

1.13A worst-case

transistor utilization 0.226

Flyback

1.38A worst case, 22% higher than forward

transistor utilization 0.284

CCM flyback exhibits higher peak and rms currents. Currents in DCM flyback are even higher

Secondary Device Stresses

Forward

peak diode voltage 49V

rms diode current 9.1A / 11.1A

rms capacitor current 1.15A

Flyback

peak diode voltage 64V

rms diode current 16.3A

peak diode current 22.2A

rms capacitor current 9.1A

Secondary-side currents, especially capacitor currents, limit the practical application of the flyback converter to situations where the load current is not too great.

Chapter 6: Summary

- Transformer-based converters often useful when extreme conversion ratios or galvanic isolation are required
- Isolated converters can be analyzed using conventional approaches, first replacing transformer by ideal transformer with magnetizing inductance
- Must ensure transformer volt-second balance, even in converters where it is not used as an energy storage element
- Selecting the best topology for a given application is an imprecise science, but active switch stress and utilization are figures-of-merit that give some insight
- Full comparison requires detailed analysis of candidate topologies