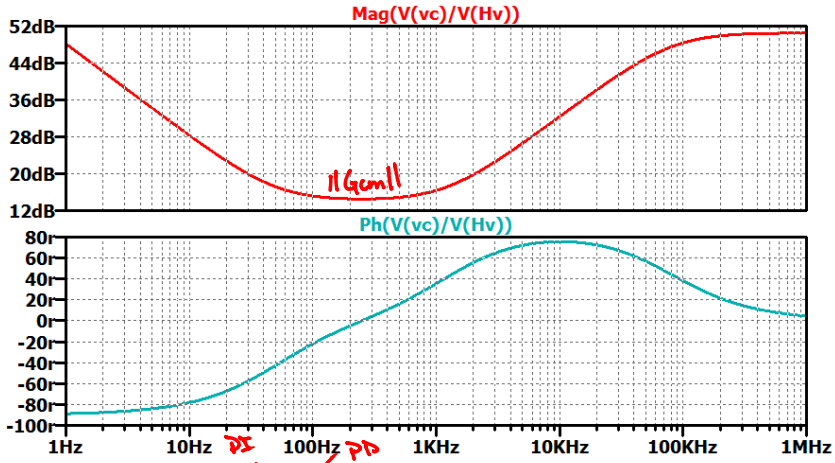
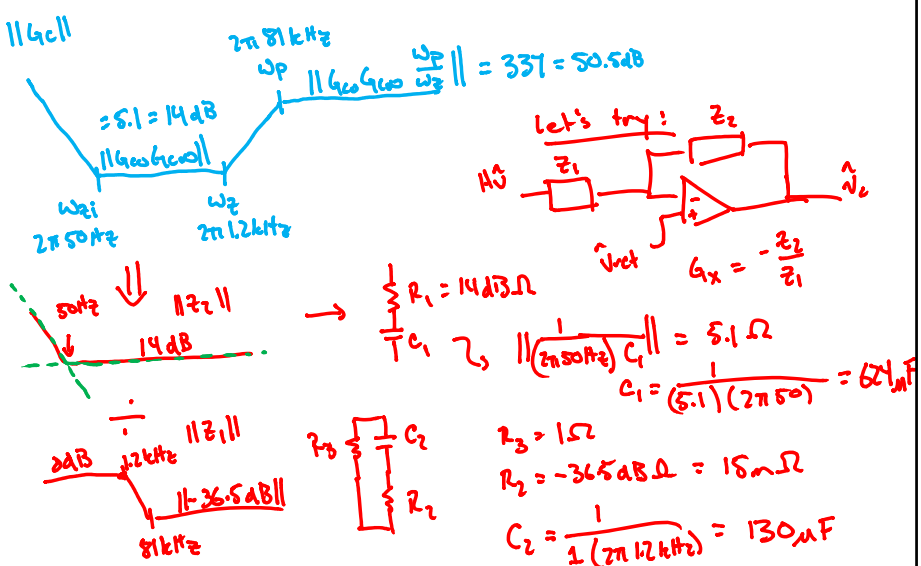
Complete Compensator

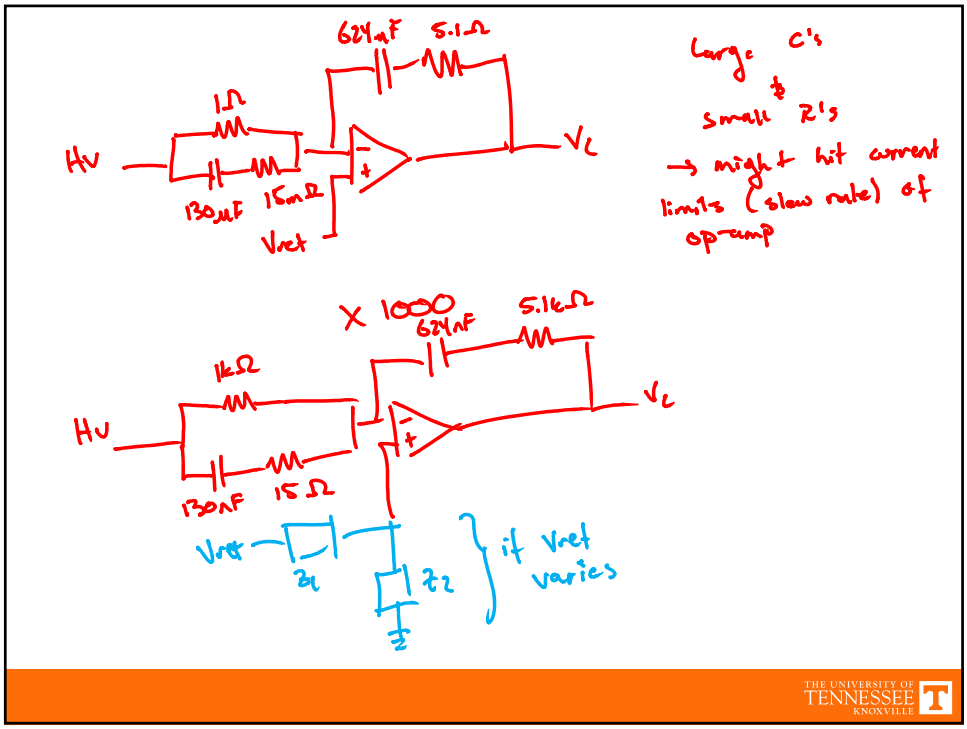


G_{cm} G_{cm}

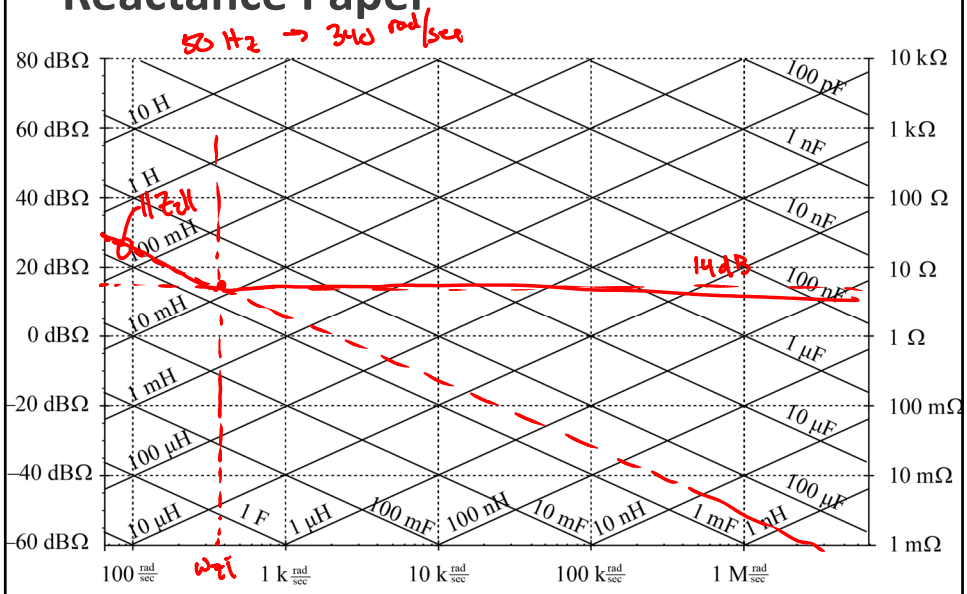
$$G_c = G_{cm}\left(1 + \frac{2\pi(50\text{Hz})}{s}\right)\frac{\left(1 + \frac{s}{2\pi(1.2\text{kHz})}\right)}{\left(1 + \frac{s}{2\pi(81k\text{Hz})}\right)}$$

Compensator Realization

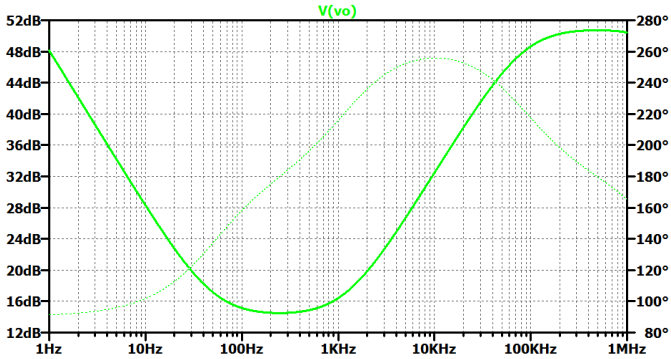




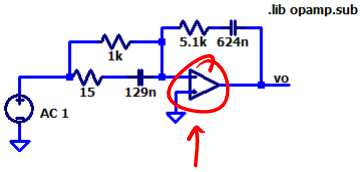
Reactance Paper



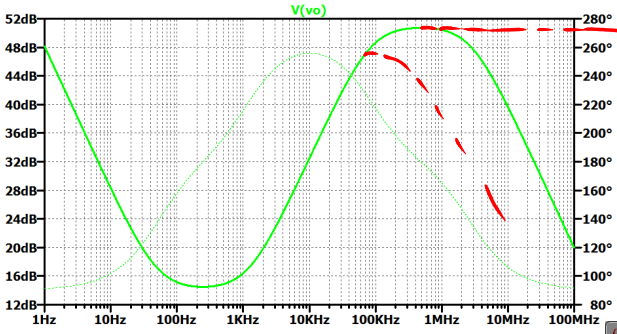
Compensator TF

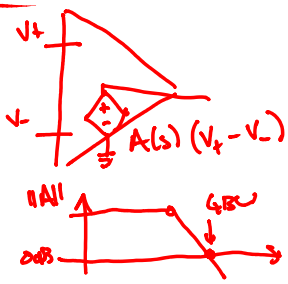


.ac dec 1000 1 1Meg

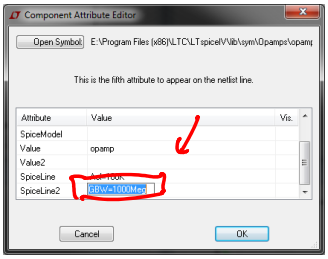


Op-amp GBW



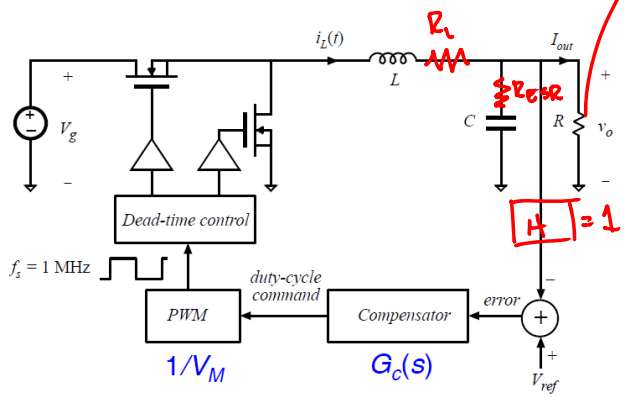


Additional HF pole due to op-amp GBW product



Another Example

$R \in [\infty, 360\,m\Omega]$



Point-of-Load Synchronous Buck Regulator

Power stage parameters

- Switching frequency: $f_s = 1$MHz
- $V_{ref} = 1.8$ V
- $I_{out} = 0$ to 5 A
- $V_g = 5$ V
- $L = 1$ µH
- $R_L = 30$ mΩ
- $C = 200$ µF
- $R_{esr} = 0.8$ mΩ
- $V_M = 1$ V
- $H = 1$

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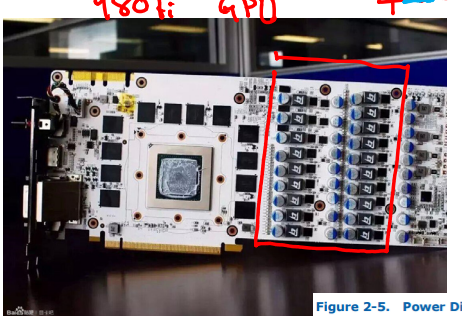
POL Converters

980ti GPU



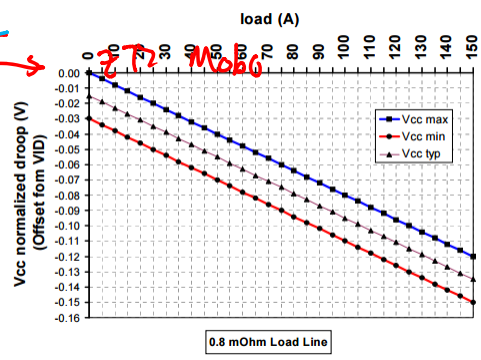


Table 2-1. Icc Guidelines

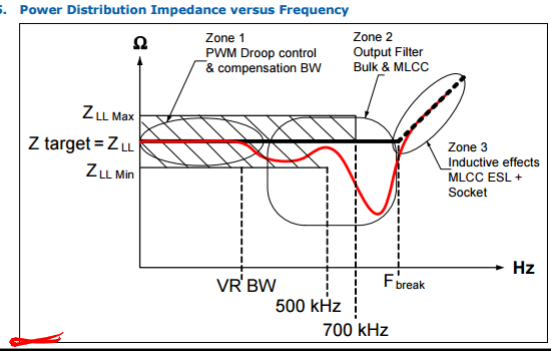
Processor (Vcore)	ICC (At
Intel Xeon Processor 5500 Series	11
Intel Xeon Processor 5500 Series 95W SKU	8
Intel Xeon Processor 5500 Series	7
Intel Xeon Processor 5500 Series	6
Intel Xeon Processor 5500 Series	2

Table 2-2. Vcc Load Step Size vs. Rep Rate

Rep Rate (RR)	Step Size
≤ 50 kHz	100%
50 kHz < RR < 200 kHz	(50kHz/RR)*
≥ 200 kHz	25%

The 100% Load Step Size corresponds to the

Figure 2-5. Power Distribution Impedance versus Frequency

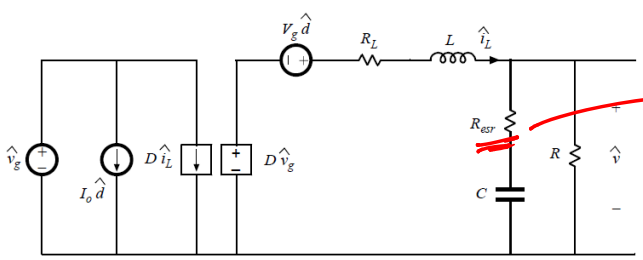


Intel, "VRM and EVRD Design Guidelines,"

Design Goals

- Set f_c = 100 kHz = $f_s/10$
- Set $\phi_m > 52°$ (Q_{CL}=1)
- Obtain $\|T_0\| \rightarrow \infty$

AC Modeling



$$G_{vd}(s) = \frac{\hat{v}_o}{\hat{d}}$$

$$G_{vd}(s) = V_g \frac{1 + \frac{s}{\omega_{esr}}}{1 + \frac{1}{Q}\frac{s}{\omega_o} + \left(\frac{s}{\omega_o}\right)^2}$$

Pair of poles:

$$f_o = \frac{1}{2\pi\sqrt{CL}} = 11\,\text{kHz}$$

$$Q_{loss} = \frac{\sqrt{L/C}}{R_{esr} + R_L} = 2.3 \rightarrow 7.2\,\text{dB} \qquad Q_{load} = \frac{R}{\sqrt{L/C}} > 5$$

$$Q = Q_{loss} \,\|\, Q_{load} = \frac{Q_{loss} Q_{load}}{Q_{loss} + Q_{load}} < 2.3 \rightarrow 7.2\,\text{dB}$$

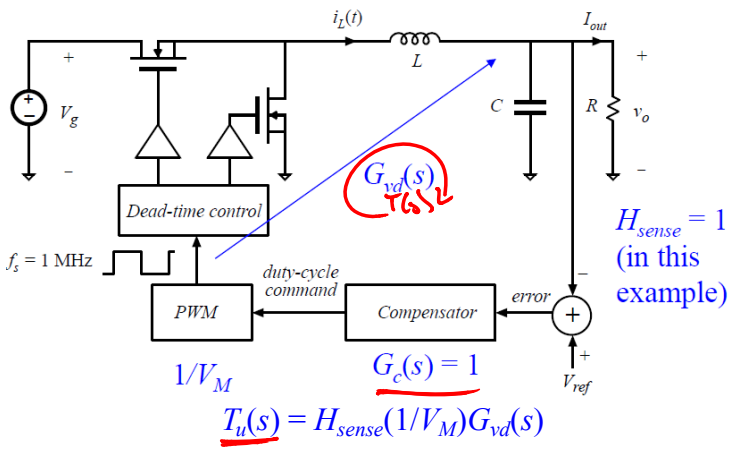
Low-frequency gain (including PWM gain):

$$G_{vdo} \frac{1}{V_M} = 5 \rightarrow 14\text{dB}$$

ESR zero:

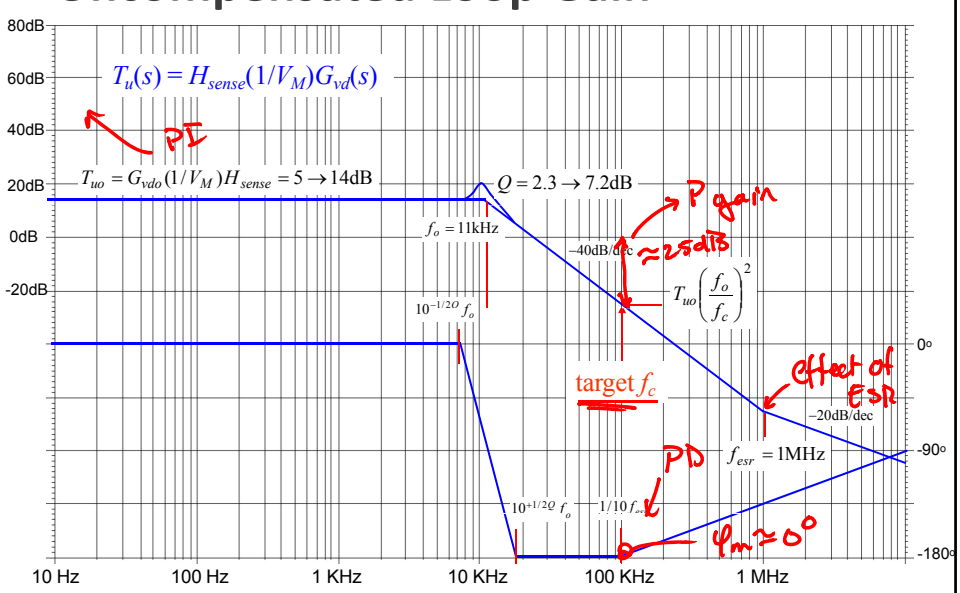
$$f_{esr} = \frac{1}{2\pi C R_{esr}} = 1\,\text{MHz}$$

Loop Gain

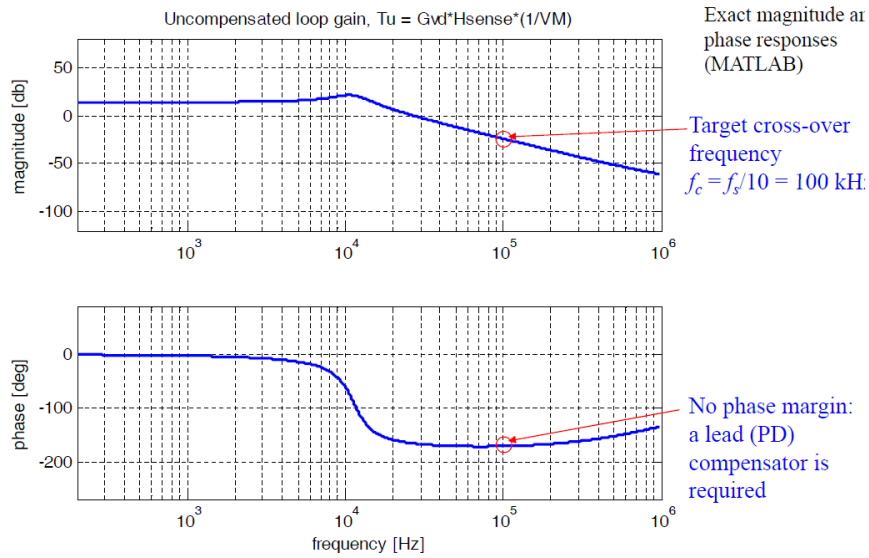


Plot magnitude and phase responses of $T_u(s)$ to plan how to design $G_c(s)$

Uncompensated Loop Gain



Exact Bode Plot of T_u



Exact magnitude ar
phase responses
(MATLAB)

Target cross-over frequency
$f_c = f_s/10 = 100$ kH

No phase margin: a lead (PD) compensator is required

Lead Compensator Design

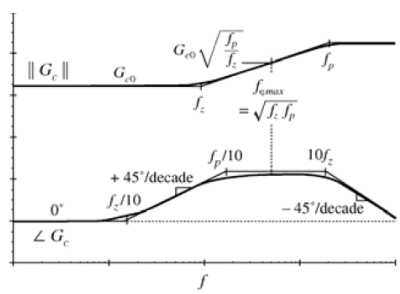
1. Choose: $f_c = 100$ kHz

$\theta = \varphi_m = 53^o$

2. Compute:

$$f_z = f_c \sqrt{\frac{1-\sin(\theta)}{1+\sin(\theta)}} = 33\text{ kHz}$$

$$f_p = f_c \sqrt{\frac{1+\sin(\theta)}{1-\sin(\theta)}} = 300\text{ kHz}$$



3. Find G_{co} to position the crossover frequency:

$$\underbrace{T_{uo}\left(\frac{f_o}{f_c}\right)^2}_{\text{Magnitude of } T_u \text{ at } f_c} \underbrace{G_{co}\sqrt{\frac{f_p}{f_z}}}_{\text{Magnitude of } G_c \text{ at } f_c} = 1 \quad \rightarrow \quad G_{co} = \frac{1}{T_{uo}}\left(\frac{f_c}{f_o}\right)^2 \sqrt{\frac{f_z}{f_p}} = 5.45 \rightarrow 15\text{ dB}$$

Lead Compensator Summary

Added to attenuate f_s & above

$$G_c(s) = G_{co}\underbrace{\frac{\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)}}_{\text{Lead compensator}}\underbrace{\frac{1}{\left(1+\frac{s}{\omega_{p2}}\right)}}_{\text{HF pole}}$$

$G_{co} = 5.45 \rightarrow 15\,\text{dB}$

$f_z = 33\,\text{kHz}$

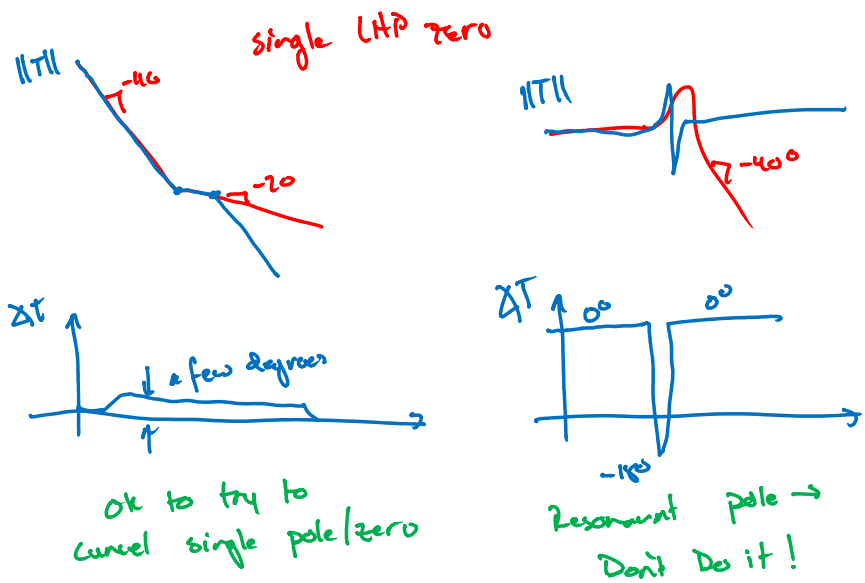
$f_{p1} = 300\,\text{kHz}$

$f_c = 100\,\text{kHz}$ (=1/10 of f_s)

High-frequency gain of the lead compensator: $G_{co}f_{p1}/f_z = 49$ (34 dB)

Added high-frequency pole: $f_{p2} = 1\,\text{MHz}$ ($= f_{esr} = f_s$ in this example)

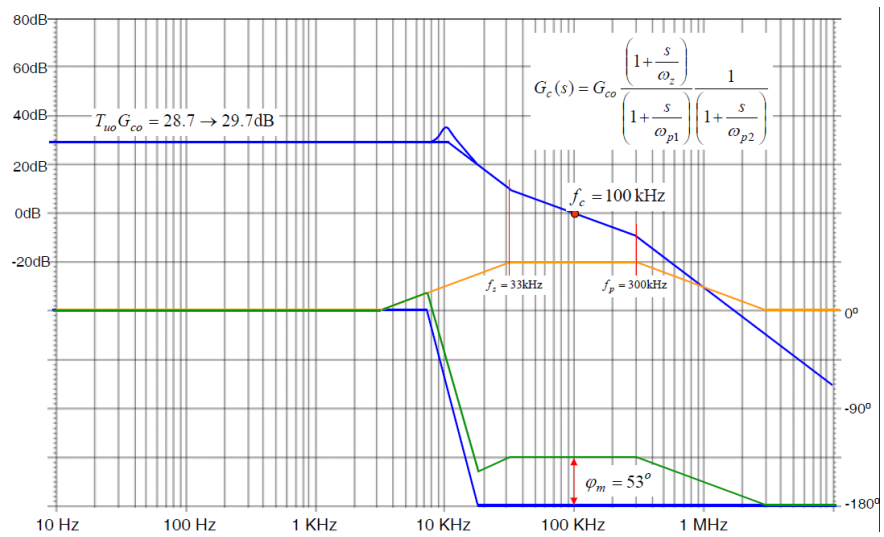
Practical implementation would require an op-amp with a gain bandwidth product of at least $49 * f_{p2} = 49$ MHz



ok to try to cancel single pole/zero

Resonant pole → Don't Do it!

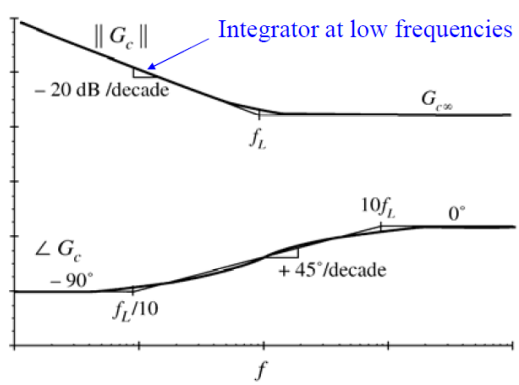
Loop Gain With Lead Compensator



Lag Compensator Design

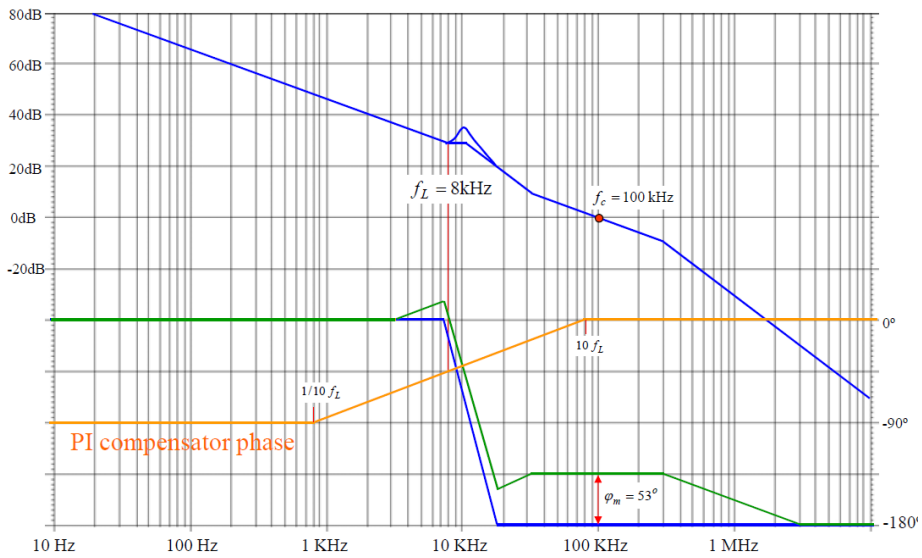
$$G_c(s) = G_{c\infty}\left(1 + \frac{\omega_L}{s}\right)$$

Improves low-frequency loop gain and regulation

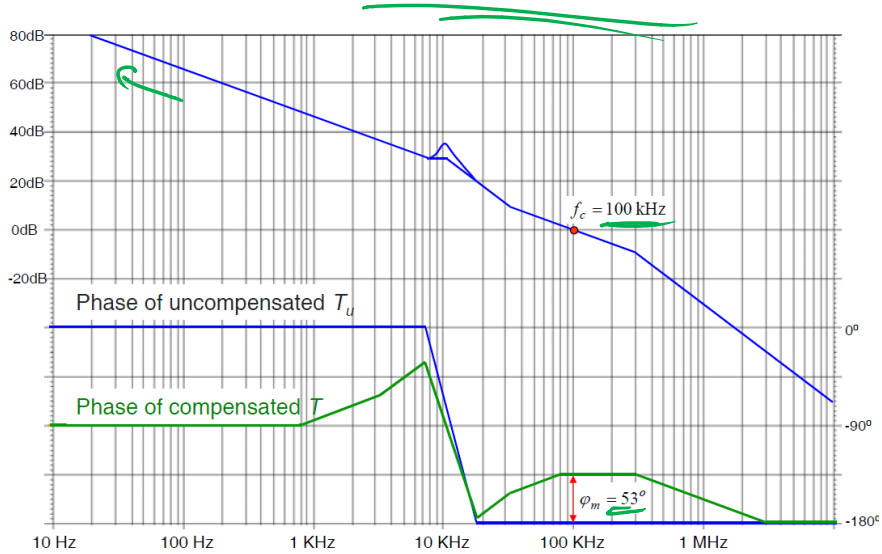


Choose $10f_L < f_c$ so that phase margin stays approximately the same: $f_L = 8$ kHz

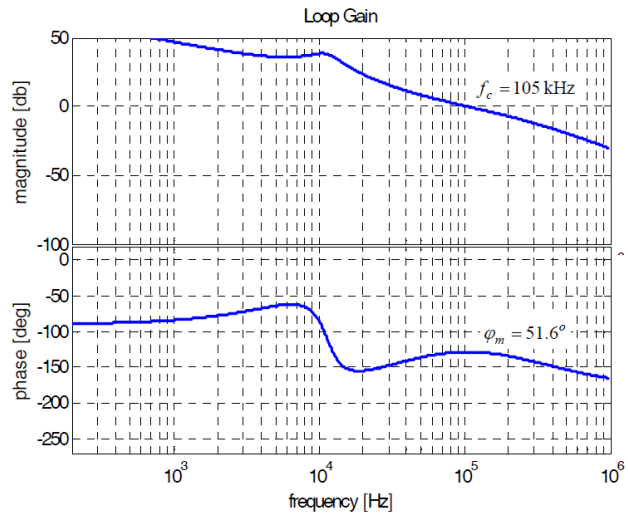
Keep the same cross-over frequency: $G_{c\infty} = G_{co} = G_{cm} = 5.45 \rightarrow 15\text{ dB}$



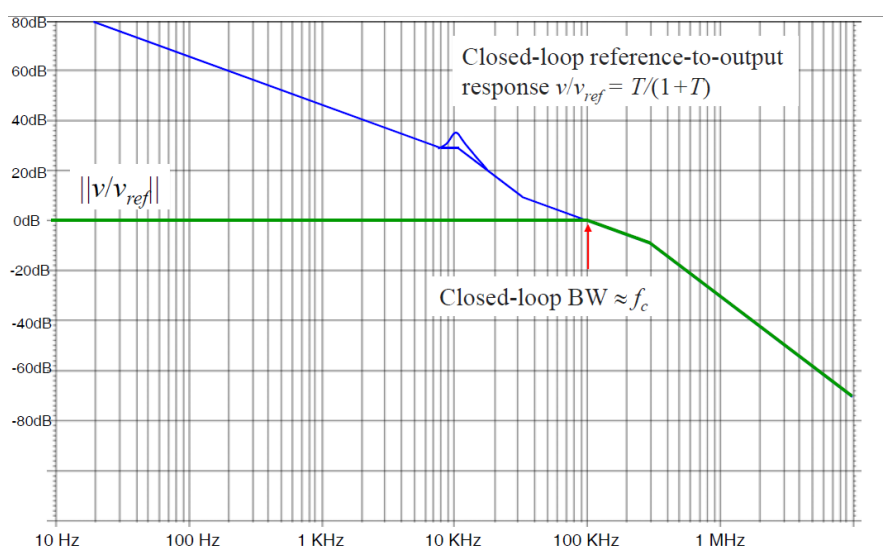
Loop Gain with PID Compensator



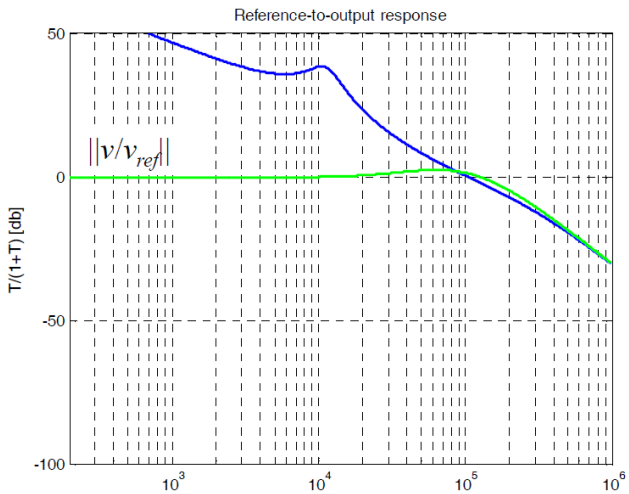
Exact Compensated Loop Gain



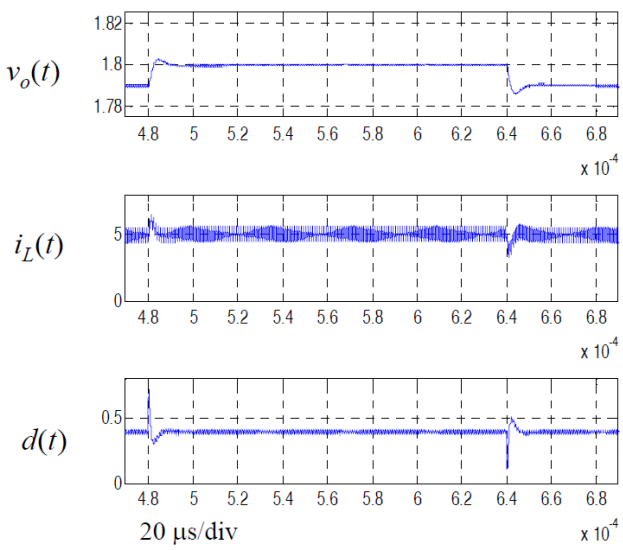
Construction of T/(1+T)



Closed-Loop Reference-to-Output

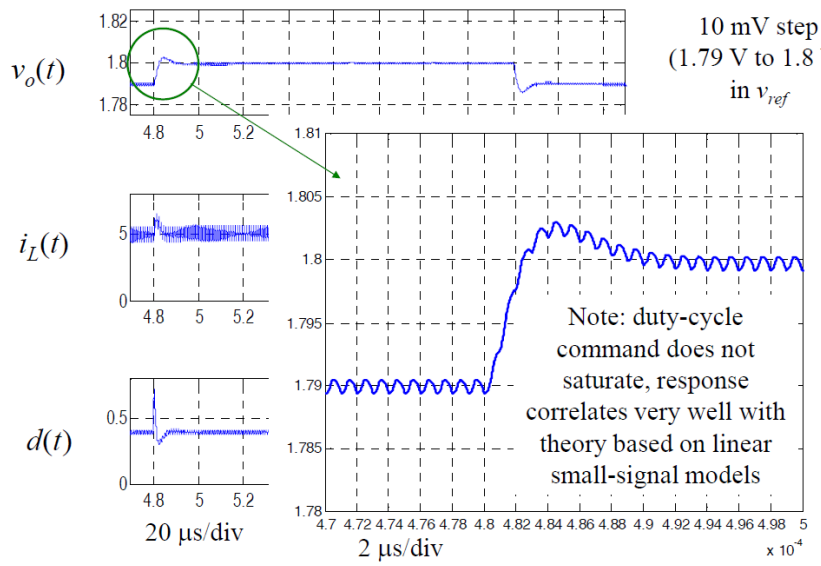


Reference Step Response



10 mV step
(1.79 V to 1.8 V)
in v_{ref}

Reference Step Response

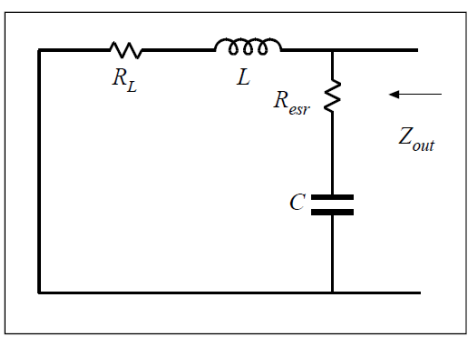


10 mV step (1.79 V to 1.8 V) in v_{ref}

Note: duty-cycle command does not saturate, response correlates very well with theory based on linear small-signal models

Output Impedance

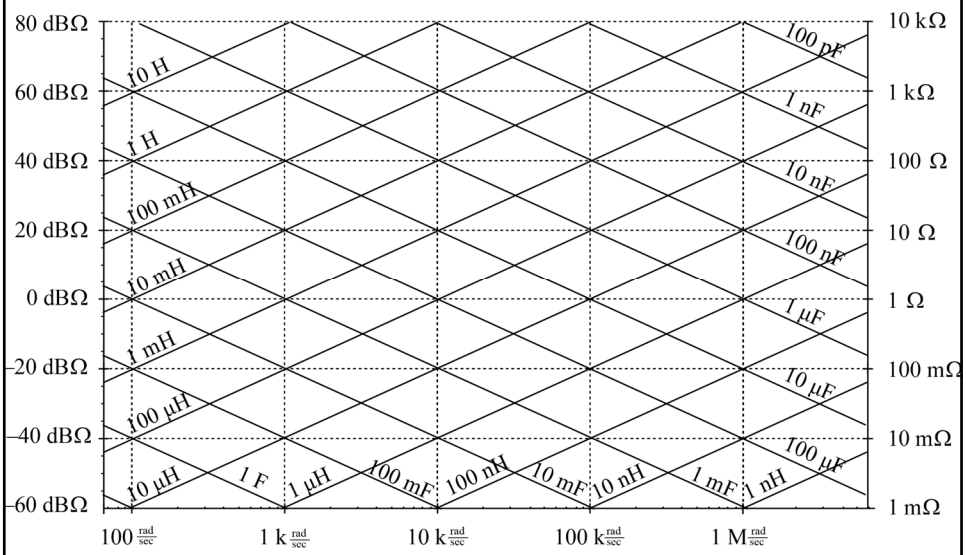
Synchronous buck open-loop output impedance



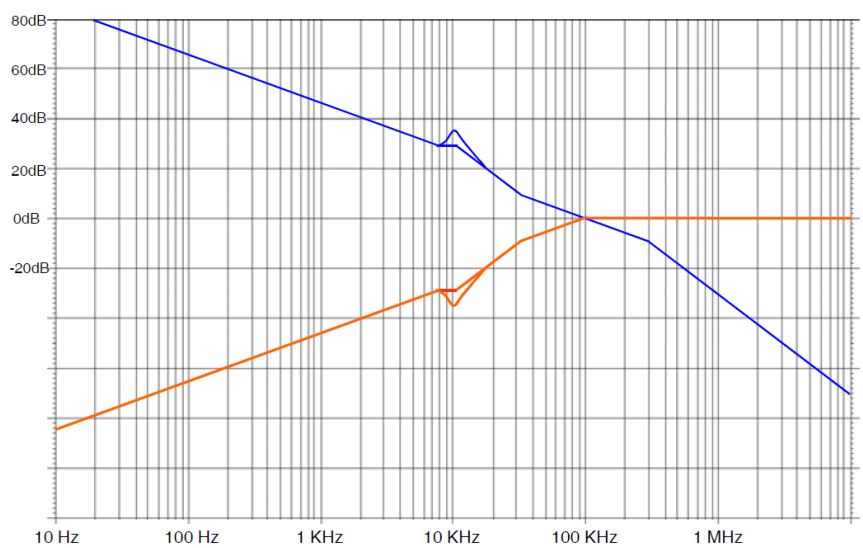
$$Z_{out}(s) = \left(R_{esr} + \frac{1}{sC}\right) \| \left(R_L + sL\right)$$

- L = 1 μH
- R_L = 30 mΩ
- C = 200 μF
- R_{esr} = 0.8 mΩ

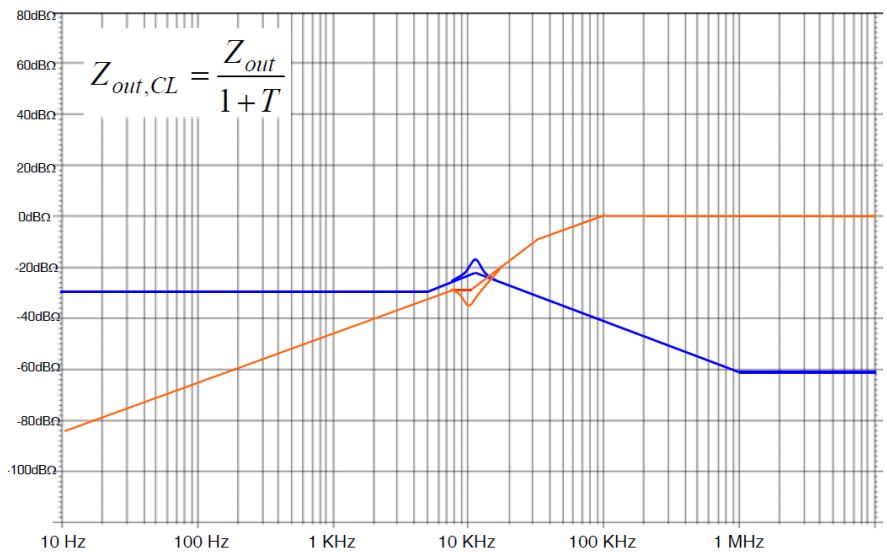
Reactance Paper



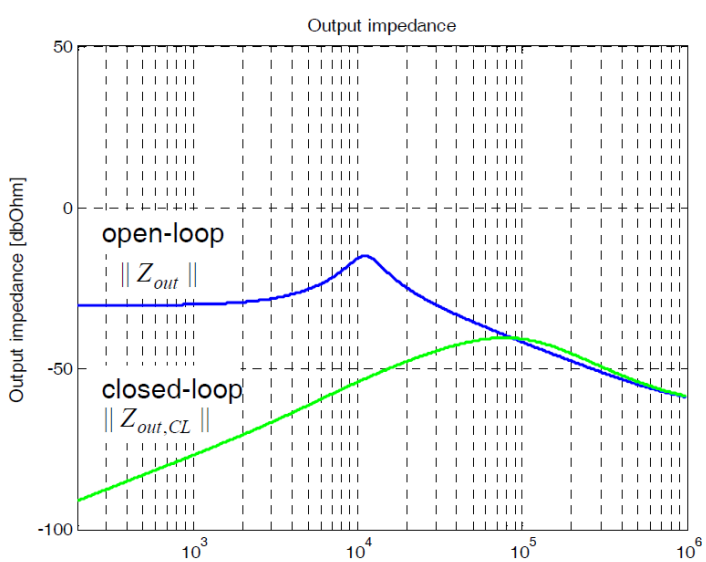
Construction of 1/(1+T)



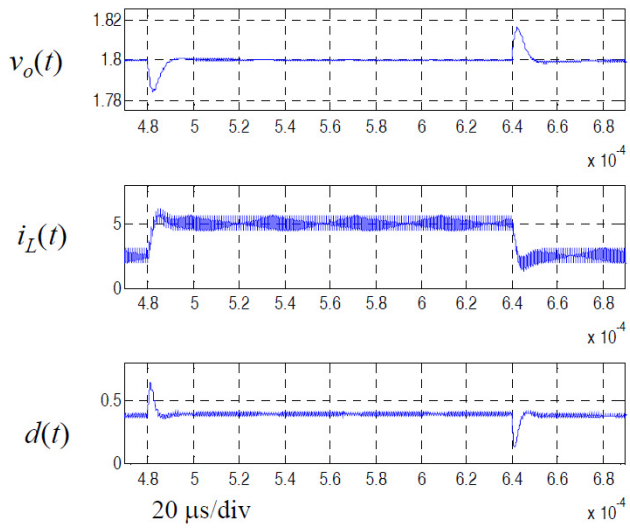
Closed-Loop Z_{out}



Exact Z_{out}

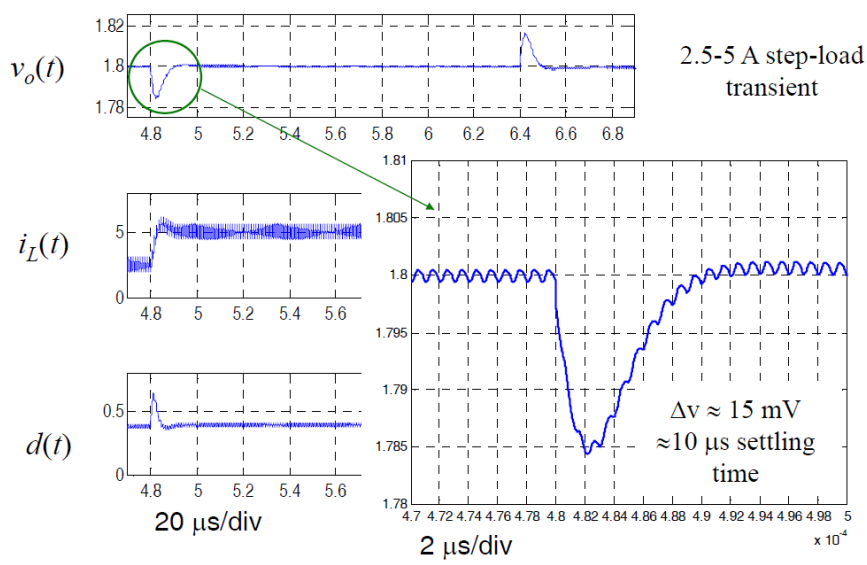


Load Step Response



2.5-5 A step-load transient

Load Step Response



2.5-5 A step-load transient

Chapter 9: Summary

1. Negative feedback causes the system output to closely follow the reference input, according to the gain $1/H(s)$. The influence on the output of disturbances and variation of gains in the forward path is reduced.
2. The loop gain $T(s)$ is equal to the products of the gains in the forward and feedback paths. The loop gain is a measure of how well the feedback system works: a large loop gain leads to better regulation of the output. The crossover frequency f_c is the frequency at which the loop gain T has unity magnitude, and is a measure of the bandwidth of the control system.

Chapter 9: Summary

3. The introduction of feedback causes the transfer functions from disturbances to the output to be multiplied by the factor $1/(1+T(s))$. At frequencies where T is large in magnitude (i.e., below the crossover frequency), this factor is approximately equal to $1/T(s)$. Hence, the influence of low-frequency disturbances on the output is reduced by a factor of $1/T(s)$. At frequencies where T is small in magnitude (i.e., above the crossover frequency), the factor is approximately equal to 1. The feedback loop then has no effect. Closed-loop disturbance-to-output transfer functions, such as the line-to-output transfer function or the output impedance, can easily be constructed using the algebra-on-the-graph method.
4. Stability can be assessed using the phase margin test. The phase of T is evaluated at the crossover frequency, and the stability of the important closed-loop quantities $T/(1+T)$ and $1/(1+T)$ is then deduced. Inadequate phase margin leads to ringing and overshoot in the system transient response, and peaking in the closed-loop transfer functions.

Chapter 9: Summary

5. Compensators are added in the forward paths of feedback loops to shape the loop gain, such that desired performance is obtained. Lead compensators, or *PD* controllers, are added to improve the phase margin and extend the control system bandwidth. *PI* controllers are used to increase the low-frequency loop gain, to improve the rejection of low-frequency disturbances and reduce the steady-state error.
6. Loop gains can be experimentally measured by use of voltage or current injection. This approach avoids the problem of establishing the correct quiescent operating conditions in the system, a common difficulty in systems having a large dc loop gain. An injection point must be found where interstage loading is not significant. Unstable loop gains can also be measured.