ECE481

GaN Boost Converter Design

A 10-to-50 V boost converter is shown in Fig. 1. The output power is 50 W. The boost converter design constraints at this operating point are as follows:

- Power stage efficiency $\eta \geq 95\%$
- Inductor current ripple $\Delta i_l \leq 10\%$
- Output voltage ripple $\Delta v_c \leq 2\%$

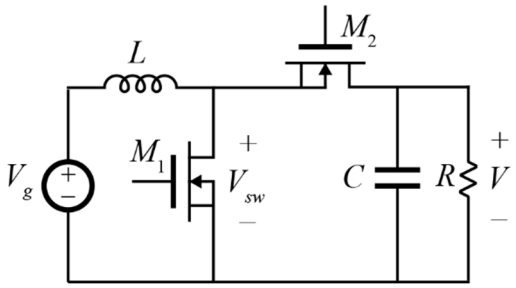

Figure. 1: Boost converter

Both M_1 and M_2 are implemented as the following device, made from Gallium Nitride on silicon:

http://epc-co.com/epc/documents/datasheets/EPC2007_datasheet.pdf

Other than the devices' resistance R_{on}, and output capacitance C_{oss}, the circuit is lossless. When calculating losses due to the device output capacitance, you may assume C_{oss}, is linear (i.e. doesn't vary with voltage). Using the above datasheet, report and explain what values you use for R_{on} and C_{oss}.

You may assume that, regardless of f_s, the switching transitions occupy a negligibly small portion of the switching period. Small ripple approximations do apply.

Assume that the size of the converter is proportional to the sum of the capacitance C and inductance L. Find the switching frequency f_s of the converter, such that the sum $L + C$ is minimized, while still meeting the constraints on efficiency and voltage/current ripple.

Report the inductance L and capacitance C, and the switching frequency of the converter f_s.