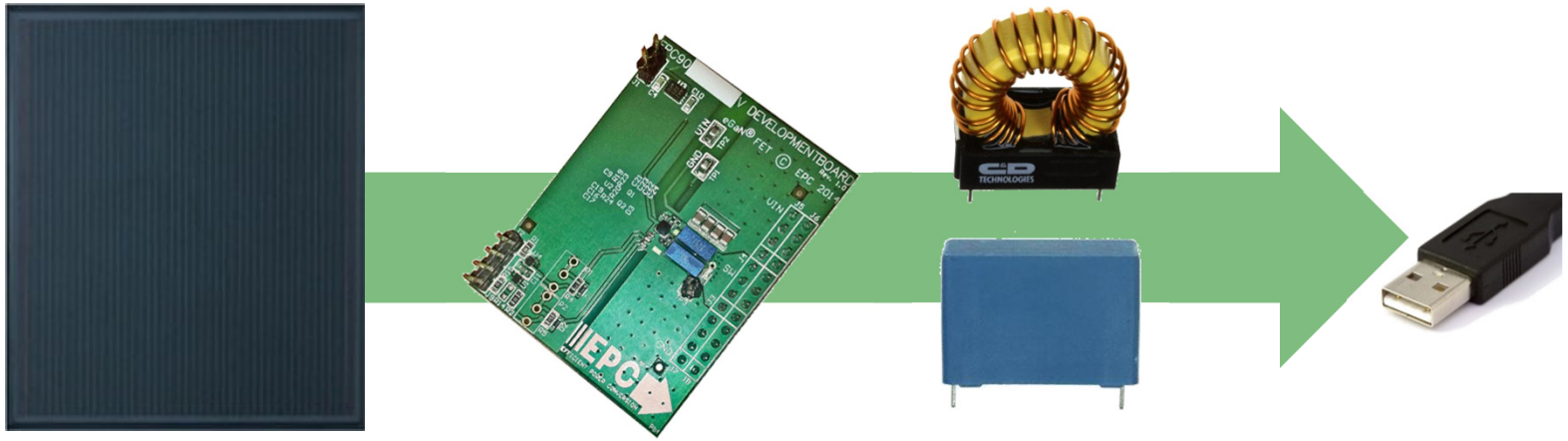
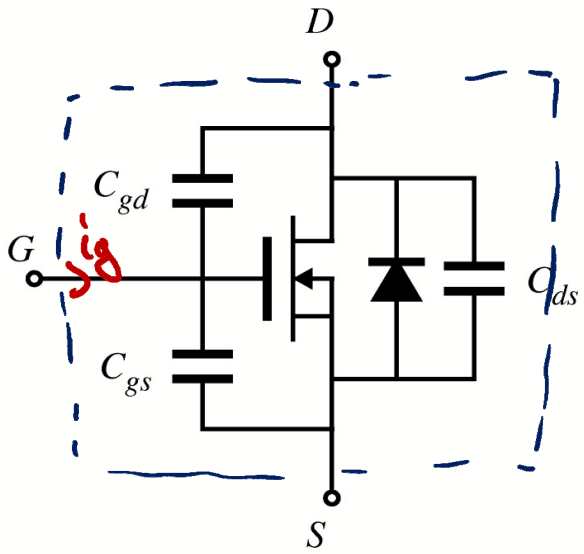
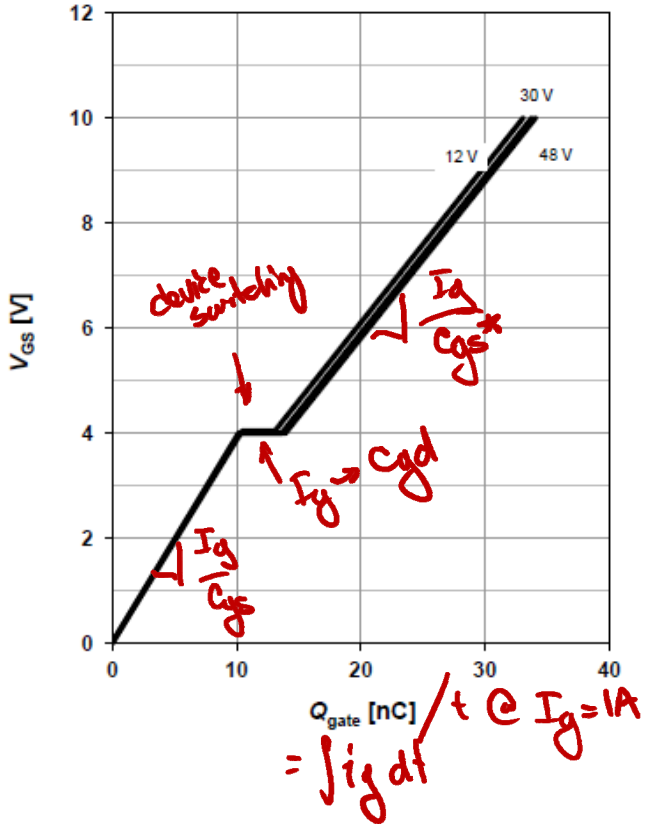
Announcements

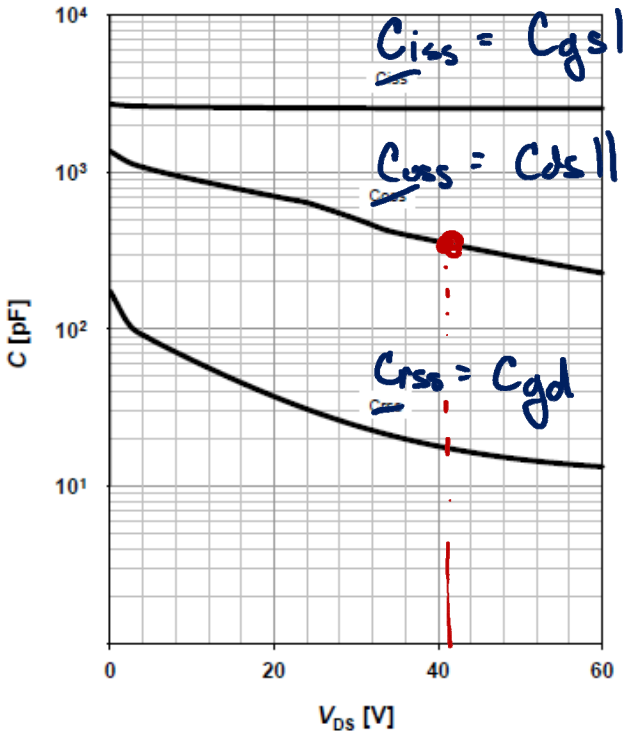
- Experiment 1 assigned
  - Model PV panel for future converter design/analysis
  - Self-assign lab groups of 3 in canvas **this week**
  - Complete experiment next week 9/23-9/27
  - Report due 10/4



MOSFET Equivalent Circuit



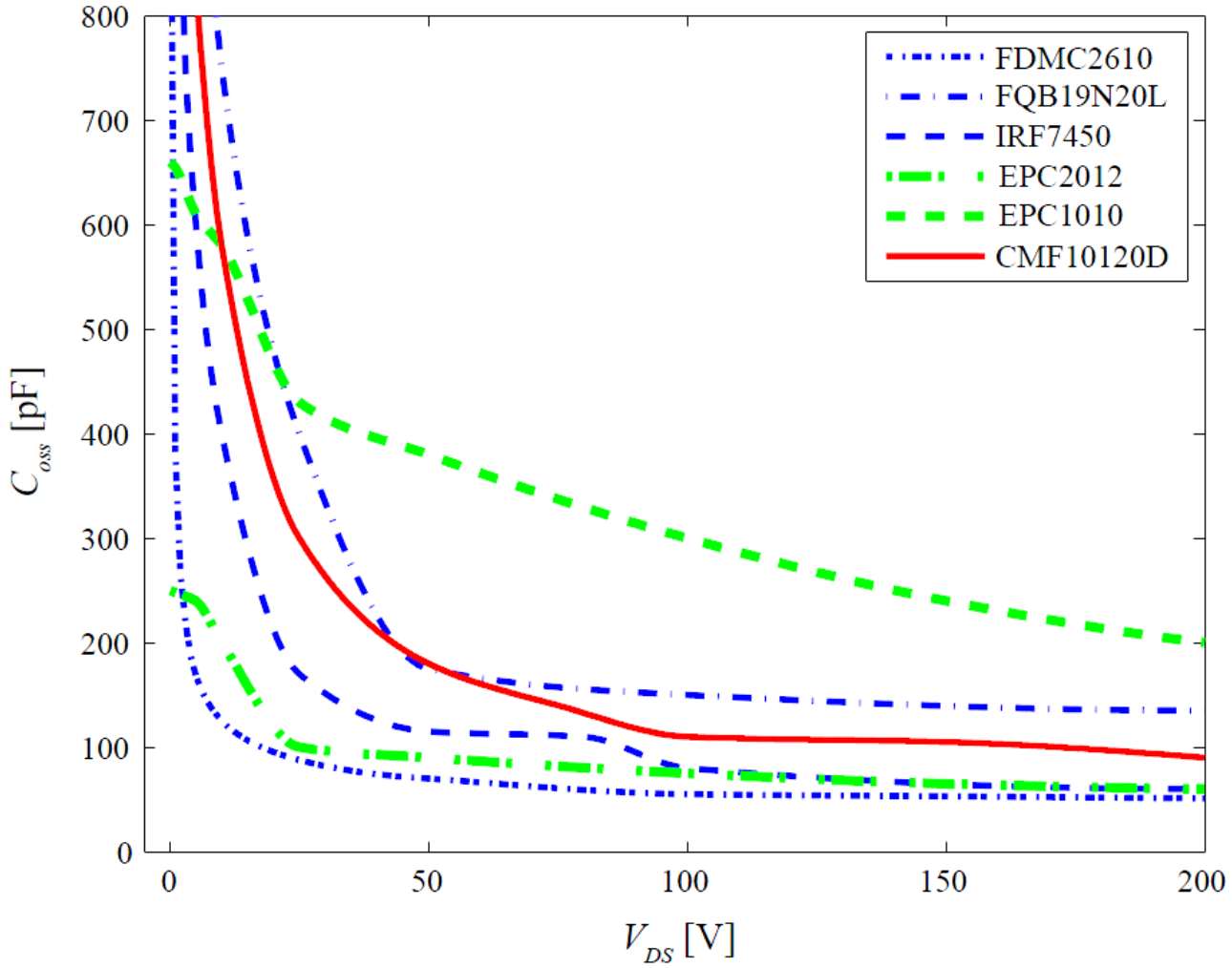




"overlap loss" during time to get from $V_{gs} = V_{th}$ to $V_{gs} = V_{gs,max}$

↳ analysis w/ nonlinear caps ECE 581

Example C_{oss} Curves



$$C_{ds}(V_{ds}) \approx \frac{C_0}{\sqrt{1 + \left(\frac{V_{ds}}{V_0}\right)^m}}$$

Device Figures-of-Merit

for a given material: set N_D in n^- material & height of drift region so that we hit designed V_{BV} @ E_{crit}

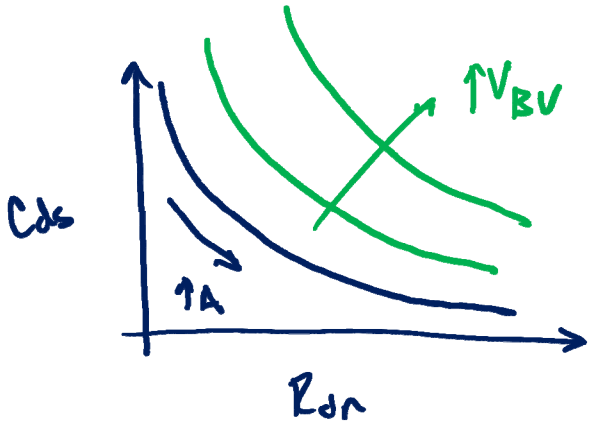
model only drift region resistance

$$R_{sp} = R_{on} \cdot A = \frac{4 V_{BV}^2}{\mu_n \varepsilon E_{crit}^3}$$

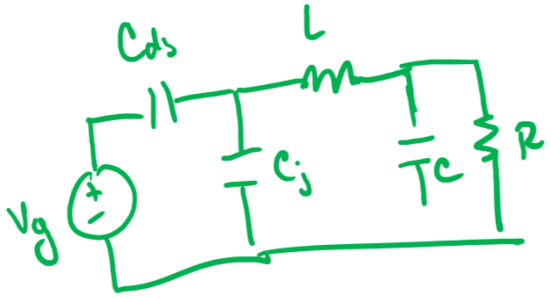
($4 V_{BV}^2$: design; $\mu_n \varepsilon E_{crit}^3$: material properties) → "Baliga's Figure of Merit"

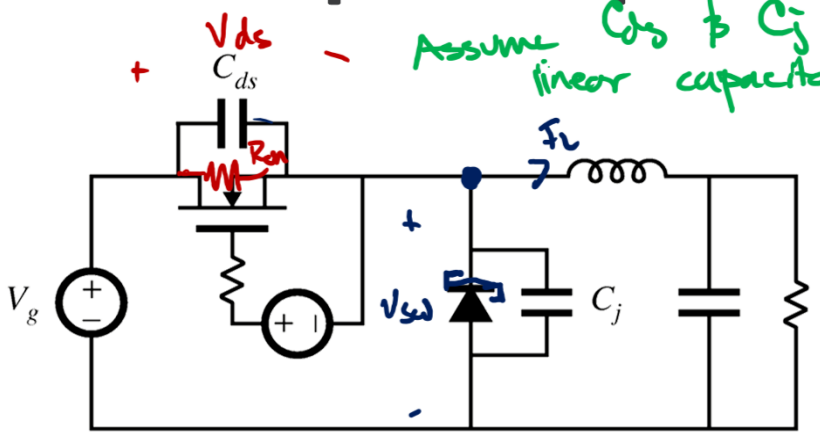
$$C_{sp} = \frac{C_{ds}(V_{BV})}{A} \approx \frac{\varepsilon E_{crit}}{2 V_{BV}}$$

$$R_{sp} \cdot C_{sp} = R_{on} \cdot C_{ds}(V_{BV}) = \frac{2 V_{BV}}{\mu_n E_{crit}^2}$$

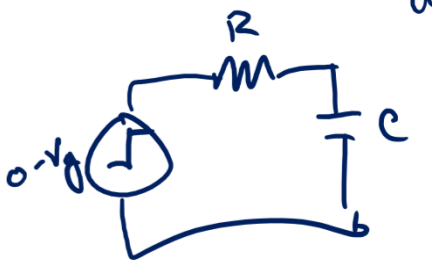


Switching Losses: Output Capacitance

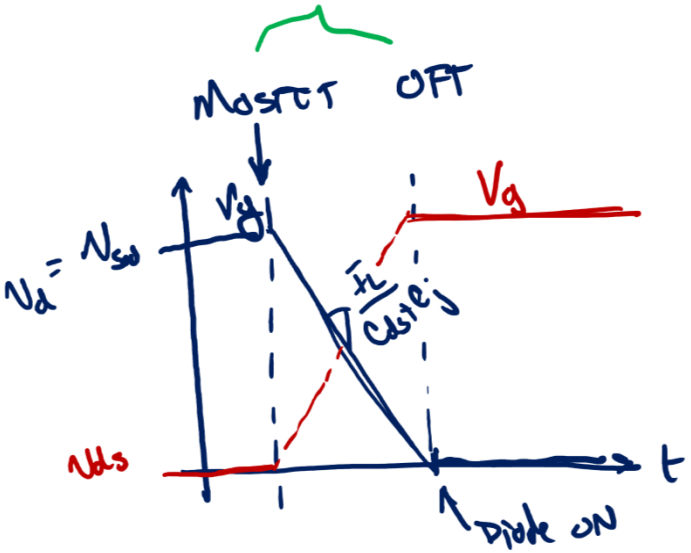




Assume Cds & Cj are linear capacitors

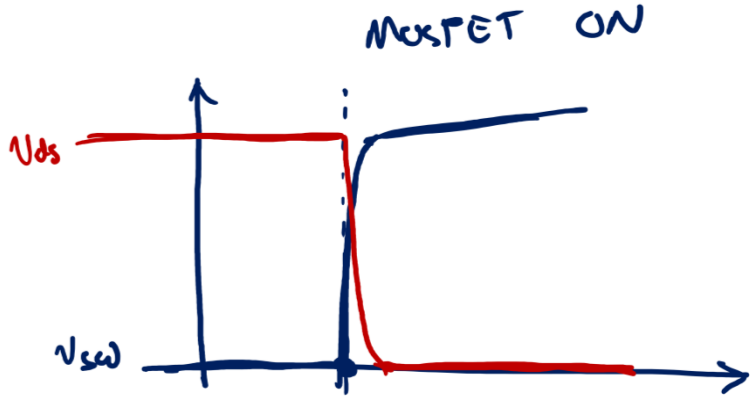


dissipation in R?



$E_{ds} = \frac{1}{2} C_{ds} V_g^2$ → stored in Cds

$E_j = -\frac{1}{2} C_j V_g^2$ → removed from Cj & supplied back to circuit



$E_{ds} = \frac{1}{2} C_{ds} V_g^2$ → Lost in Ron

$E_j = \frac{1}{2} C_j V_g^2$ → Lost in Ron from resistive charging of Cj

Over the period $P_{sw,c} = (E_{ds} + E_j) f_s = \frac{1}{2} (C_{ds} + C_j) V_g^2 f_s$