Exp. 4, Part 2

Converter Transfer Functions

The engineering design process is comprised of several major steps:

1. *Specifications and other design goals* are defined.
2. *A circuit is proposed*. This is a creative process that draws on the physical insight and experience of the engineer.
3. *The circuit is modeled*. The converter power stage is modeled as described in Chapter 7. Components and other portions of the system are modeled as appropriate, often with vendor-supplied data.
4. *Design-oriented analysis* of the circuit is performed. This involves development of equations that allow element values to be chosen such that specifications and design goals are met. In addition, it may be necessary for the engineer to gain additional understanding and physical insight into the circuit behavior, so that the design can be improved by adding elements to the circuit or by changing circuit connections.
5. *Model verification*. Predictions of the model are compared to a laboratory prototype, under nominal operating conditions. The model is refined as necessary, so that the model predictions agree with laboratory measurements.
6. *Worst-case analysis* (or other reliability and production yield analysis) of the circuit is performed. This involves quantitative evaluation of the model performance, to judge whether specifications are met under all conditions. Computer simulation is well-suited to this task.
7. *Iteration*. The above steps are repeated to improve the design until the worst-case behavior meets specifications, or until the reliability and production yield are acceptably high.

Part 3 of this experiment is concerned with the modeling, simulation, and verification steps that are required to design the feedback system of a switched-mode converter.

2.1 INTRODUCTION

Converter systems invariably require feedback. For example, in a typical dc–dc converter application, the output voltage $v(t)$ must be kept constant, regardless of changes in the input voltage $v_g(t)$ or in the effective load resistance R. This is accomplished by building a circuit that varies the converter control input [i.e., the duty cycle $d(t)$] in such a way that the output voltage $v(t)$ is regulated to be equal to a desired reference value v_{ref}. In inverter systems, a feedback loop causes the output voltage to follow a sinusoidal reference voltage. In modern low-harmonic rectifier systems, a control system causes the converter input current to be proportional to the input voltage, such that the input port presents a resistive load to the ac source. So feedback is commonly employed.

A typical dc–dc system incorporating a buck converter and feedback loop block diagram is illustrated in Fig. 2.1. It is desired to design this feedback system in such a way that the output voltage is accurately regulated, and is insensitive to disturbances in $v_g(t)$ or in the load current. In addition, the feedback system should be stable, and properties such as transient overshoot, settling time, and steady-state regulation should meet specifications.

To design the system of Fig. 2.1, we need a dynamic model of the switching converter. How do variations in the power input voltage, the load current, or the duty cycle affect the output voltage? What are the small-signal transfer functions? To answer these questions, we will derive an equivalent circuit model of the converter, which predicts the dynamics introduced by the inductors and capacitors of the converter.

Modeling is the representation of physical phenomena by mathematical means. In engineering, it is desired to model the important dominant behavior of a system, while neglecting other insignificant phenomena. Simplified terminal equations of the component elements are used, and many aspects of the system response are neglected altogether, that is, they are "unmodeled." The resulting simplified model yields physical insight into the system behavior, which aids the engineer in designing the system to operate in a given specified manner. Thus, the modeling process involves use of approximations to neglect small but complicating phenomena, in an attempt to understand what is most important. Once this basic insight is gained, it may be desirable to carefully refine the model, by accounting for some of the previously ignored phenomena. It is a fact of life that real, physical systems are complex, and their detailed analysis can easily lead to an intractable and useless mathematical mess. Approximate models are an important tool for gaining understanding and physical insight.

The switching ripple is small in a well-designed converter operating in continuous conduction mode (CCM). Hence, we should ignore the switching ripple, and model only the underlying ac variations in the converter waveforms. For example, suppose that some ac variation is introduced into the converter duty cycle $d(t)$, such that

$$d(t) = D + D_m \cos \omega_m t \tag{2.1}$$

where D and D_m are constants, $| D_m | \ll D$, and the modulation frequency ω_m is much smaller than the converter switching frequency $\omega_s = 2\pi f_s$. The resulting transistor gate drive signal is illustrated in Fig. 2.2(a), and a typical converter output voltage waveform $v(t)$ is illustrated in Fig. 2.2(b). The spectrum of $v(t)$ is illustrated in Fig. 2.3. This spectrum contains components at the switching frequency as well as its harmonics and sidebands; these components are small in magnitude if the switching ripple is small. In addition, the spectrum contains a low-frequency component at the modulation frequency ω_m. The magnitude and phase of this component depend not only on the duty cycle variation, but also on the frequency response of the converter. If we neglect the switching ripple, then this low-frequency compo-

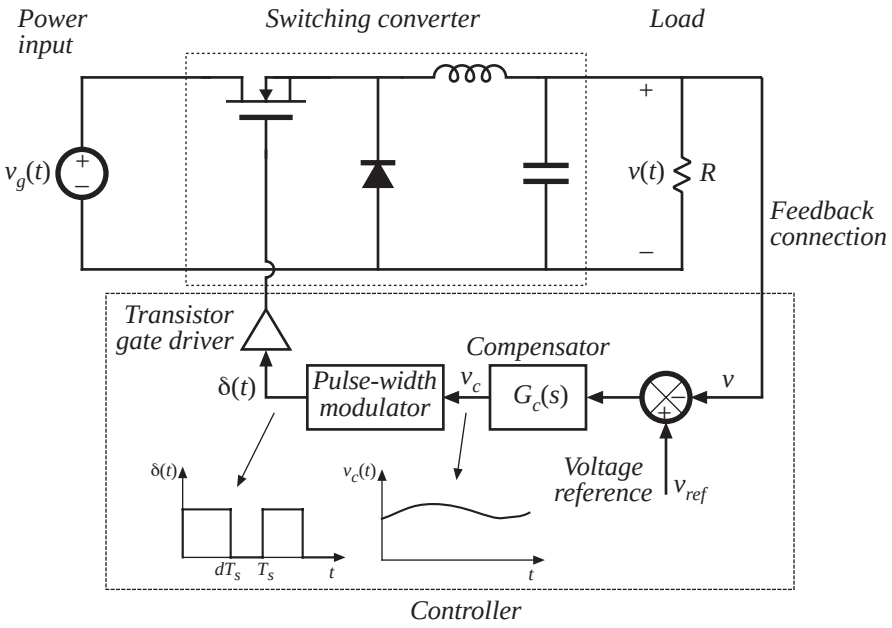


Fig. 2.1 A simple dc–dc regulator system, including a buck converter power stage and a feedback network.

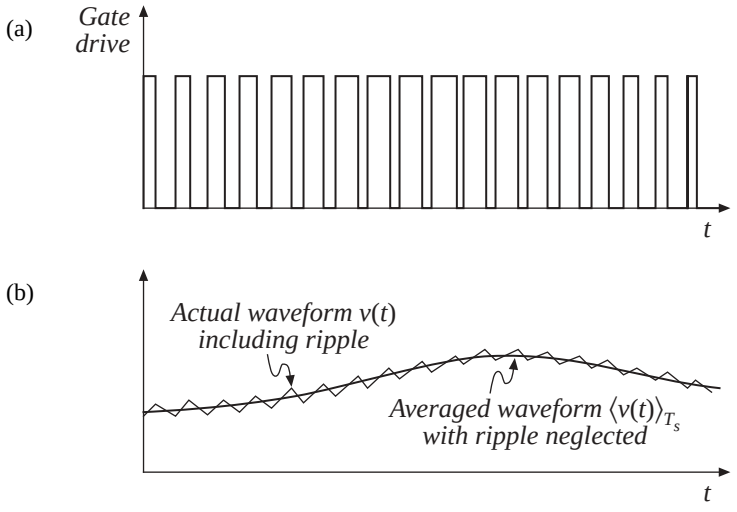


Fig. 2.2 Ac variation of the converter signals: (a) transistor gate drive signal, in which the duty cycle varies slowly, and (b) the resulting converter output voltage waveform. Both the actual waveform $v(t)$ (including high frequency switching ripple) and its averaged, low-frequency component, $\langle v(t) \rangle_{T_s}$, are illustrated.

nent remains [also illustrated in Fig. 2.2(b)]. The objective of our ac modeling efforts is to predict this low-frequency component.

A simple method for deriving the small-signal model of CCM converters is explained here. The switching ripples in the inductor current and capacitor voltage waveforms are removed by averaging over

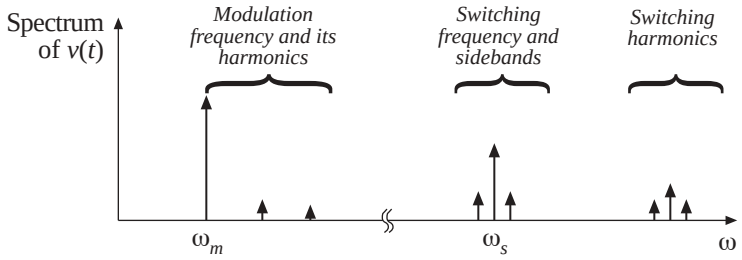


Fig. 2.3 Spectrum of the output voltage waveform $v(t)$ of Fig. 2.2.

one switching period. Hence, the low-frequency components of the inductor and capacitor waveforms are modeled by equations of the form

$$\begin{aligned} L\frac{d\langle i_L(t)\rangle_{T_s}}{dt} &= \langle v_L(t)\rangle_{T_s} \\ C\frac{d\langle v_C(t)\rangle_{T_s}}{dt} &= \langle i_C(t)\rangle_{T_s} \end{aligned} \tag{2.2}$$

where $\langle x(t)\rangle_{T_s}$ denotes the average of $x(t)$ over an interval of length T_s:

$$\langle x(t)\rangle_{T_s} = \frac{1}{T_s}\int_t^{t+T_s} x(\tau)d\tau \tag{2.3}$$

So we will employ the basic approximation of removing the high-frequency switching ripple by averaging over one switching period. Yet the average value is allowed to vary from one switching period to the next, such that low-frequency variations are modeled. In effect, the "moving average" of Eq. (2.3) constitutes low-pass filtering of the waveform.

Note that the principles of inductor volt-second balance and capacitor charge balance predict that the right-hand sides of Eqs. (2.2) are zero when the converter operates in equilibrium. Equations (2.2) describe how the inductor currents and capacitor voltages change when nonzero average inductor voltage and capacitor current are applied over a switching period.

The averaged inductor voltage and capacitor currents of Eq. (2.2) are, in general, nonlinear functions of the signals in the converter, and hence Eqs. (2.2) constitute a set of nonlinear differential equations. Indeed, the spectrum in Fig. 2.3 also contains harmonics of the modulation frequency ω_m. In most converters, these harmonics become significant in magnitude as the modulation frequency ω_m approaches the switching frequency ω_s, or as the modulation amplitude D_m approaches the quiescent duty cycle D. Nonlinear elements are not uncommon in electrical engineering; indeed, all semiconductor devices exhibit nonlinear behavior. To obtain a linear model that is easier to analyze, we usually construct a small-signal model that has been linearized about a quiescent operating point, in which the harmonics of the modulation or excitation frequency are neglected. As an example, Fig. 2.4 illustrates linearization of the familiar diode i–v characteristic shown in Fig. 2.4(b). Suppose that the diode current $i(t)$ has a quiescent (dc) value I and a signal component $\hat{i}(t)$. As a result, the voltage $v(t)$ across the diode has a quiescent value V and a signal component $\hat{v}(t)$. If the signal components are small compared to the quiescent values,

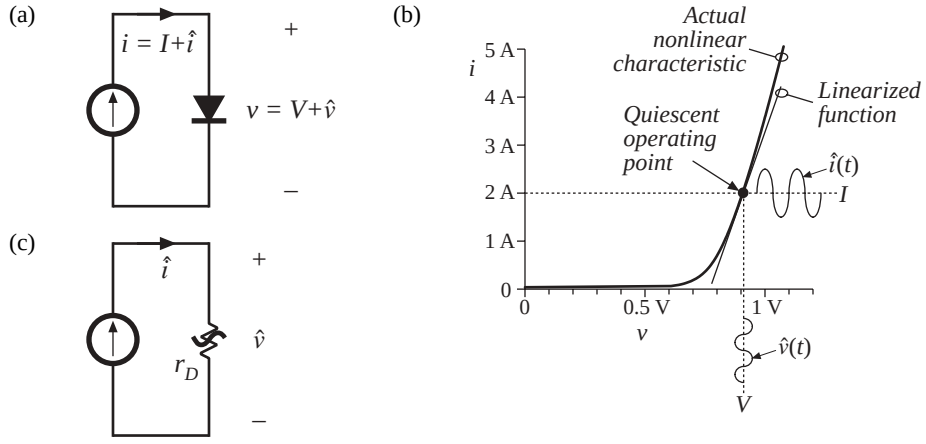


Fig. 2.4 Small-signal equivalent circuit modeling of the diode: (a) a nonlinear diode conducting current i; (b) linearization of the diode characteristic around a quiescent operating point; (c) a linearized small-signal model.

$$|\hat{v}| \ll |V|, \quad |\hat{i}| \ll |I| \tag{2.4}$$

then the relationship between $\hat{v}(t)$ and $\hat{i}(t)$ is approximately linear, $\hat{v}(t) = r_D\hat{i}(t)$. The conductance $1/r_D$ represents the slope of the diode characteristic, evaluated at the quiescent operating point. The small-signal equivalent circuit model of Fig. 2.4(c) describes the diode behavior for small variations around the quiescent operating point.

An example of a nonlinear converter characteristic is the dependence of the steady-state output voltage V of the buck-boost converter on the duty cycle D, illustrated in Fig. 2.5. Suppose that the converter operates with some dc output voltage, say, $V = -V_g$, corresponding to a quiescent duty cycle of $D = 0.5$. Duty cycle variations $\hat{d}$ about this quiescent value will excite variations $\hat{v}$ in the output voltage. If the magnitude of the duty cycle variation is sufficiently small, then we can compute the resulting output voltage variations by linearizing the curve. The slope of the linearized characteristic in Fig. 2.5 is chosen to be equal to the slope of the actual nonlinear characteristic at the quiescent operating point; this slope is the dc control-to-output gain of the converter. The linearized and nonlinear characteristics are

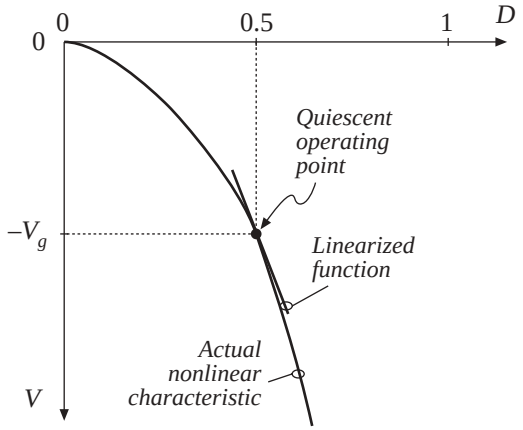


Fig. 2.5 Linearization of the static control-to-output characteristic of the buck-boost converter about the quiescent operating point $D = 0.5$.

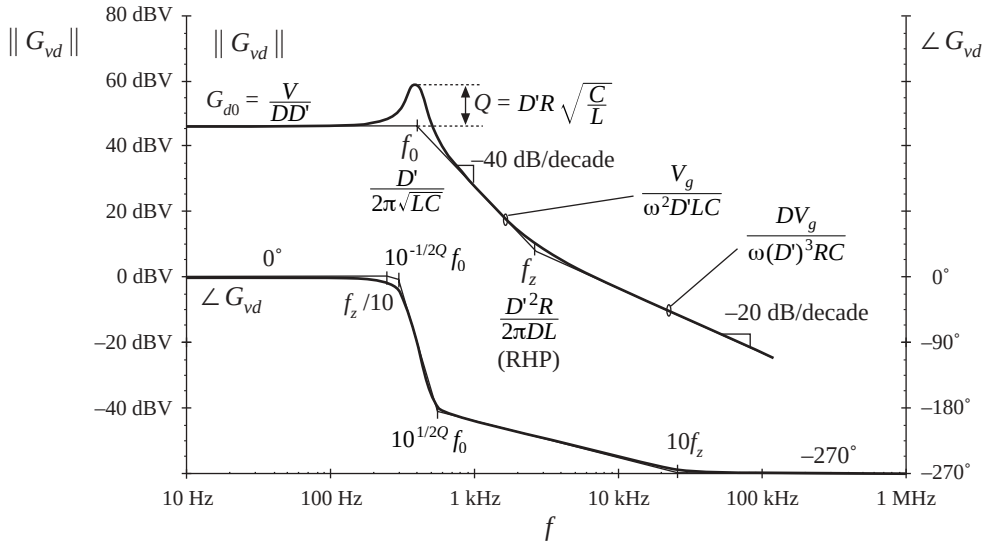


Fig. 2.6 Bode plot of control-to-output transfer function of the buck-boost converter as predicted by the small-signal averaged-switch model, with analytical expressions for the important features labeled.

approximately equal in value provided that the duty cycle variations $\hat{d}$ are sufficiently small.

Although it illustrates the process of small-signal linearization, the buck-boost example of Fig. 2.5 is oversimplified. The inductors and capacitors of the converter cause the gain to exhibit a frequency response. To correctly predict the poles and zeroes of the small-signal transfer functions, we must linearize the converter averaged differential equations, Eqs. (2.2). This is done here, using the averaged switch modeling technique. The resulting small-signal model can be solved using conventional circuit analysis techniques, to find the small-signal transfer functions, output impedance, and other frequency-dependent properties. In systems such as Fig. 2.1, the equivalent circuit model of the switch network can be inserted in place of the transistor and diode elements. When small-signal models of the other system elements (such as the pulse-width modulator) are inserted, then a complete linearized system model is obtained. This model can be analyzed using standard linear techniques, such as the Laplace transform, to gain insight into the behavior and properties of the system.

The line-to-output transfer function $G_{vg}(s)$ is found by setting duty cycle variations $\hat{d}(s)$ to zero, and then solving the model for the transfer function from $\hat{v}_g(s)$ to $\hat{v}(s)$:

$$G_{vg}(s) = \left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\hat{d}(s)=0} \tag{2.5}$$

This transfer function describes how variations or disturbances in the applied input voltage $v_g(t)$ lead to disturbances in the output voltage $v(t)$. It is important in design of an output voltage regulator. For example, in an off-line power supply, the converter input voltage $v_g(t)$ contains undesired even harmonics of the ac power line voltage. The transfer function $G_{vg}(s)$ is used to determine the effect of these harmonics on the converter output voltage $v(t)$.

The control-to-output transfer function $G_{vd}(s)$ is found by setting the input voltage variations $\hat{v}_g(s)$ to zero, and then solving the equivalent circuit model for $\hat{v}(s)$ as a function of $\hat{d}(s)$:

$$G_{vd}(s) = \left.\frac{\hat{v}(s)}{\hat{d}(s)}\right|_{\hat{v}_g(s) = 0} \tag{2.6}$$

This transfer function describes how control input variations $\hat{d}(s)$ influence the output voltage $\hat{v}(s)$. In an output voltage regulator system, $G_{vd}(s)$ is a key component of the loop gain and has a significant effect on regulator performance.

The output impedance $Z_{out}(s)$ is found under the conditions that $\hat{v}_g(s)$ and $\hat{d}(s)$ variations are set to zero. $Z_{out}(s)$ describes how variations in the load current affect the output voltage. This quantity is also important in voltage regulator design. It may be appropriate to define $Z_{out}(s)$ either including or not including the load resistance R.

The objectives of this part of the experiment are the modeling, simulation, and measurement of Bode plots of the important transfer functions of switching converters. For example, Fig. 2.6 illustrates the magnitude and phase plots of $G_{vd}(s)$ for the buck-boost converter. Experimental measurement of transfer functions and impedances (needed in step 4, model verification) is discussed in Section 2.5. Use of computer simulation to plot converter transfer functions (as needed in step 6, worst-case analysis) is covered in Appendix B.

2.2 AVERAGED SWITCH MODELING

The central idea of the *averaged switch modeling* approach is to find an averaged circuit model for the switch network. The resulting averaged switch model can then be inserted into the converter circuit to obtain a complete averaged circuit model of the converter. An important advantage of the averaged switch modeling approach is that the same model can be used in many different converter configurations. It is not necessary to rederive an averaged circuit model for each particular converter. Furthermore, in many cases, the averaged switch model simplifies converter analysis and yields good intuitive understanding of the converter steady-state and dynamic properties.

2.2.1 Switch Networks

We first define a *switch network*, containing the switching devices (*i.e.*, the transistor and diode) and no other elements. The switch network contains two ports, where the switching elements are connected to the remainder of the converter. No connections are assumed between the switches within the switch network itself. As a result, this switch network and its averaged model can be used to easily construct averaged circuit models of many two-switch converters. It is important to note, however, that the definition of the switch network ports is not unique. Different definitions of the switch network lead to equivalent, but not identical, averaged switch models. The alternative forms of the averaged switch model may result in simpler circuit models, or models that provide better physical insight. Two alternative averaged switch models, better suited for analyses of boost and buck converters, are described in this section.

Consider the ideal boost converter of Fig. 2.7(a). The switch network contains the transistor and the diode, with input and output ports 1 and 2. To derive the averaged switch model, we first write the waveforms of the voltages and currents at ports 1 and 2. These switch network terminal waveforms are shown in Fig. 2.7(b). Since $i_1(t)$ and $v_2(t)$ coincide with the converter inductor current and capacitor voltage, it is convenient to choose these waveforms as the "independent inputs" to the switch network. We then treat the remaining terminal waveforms $i_2(t)$ and $v_1(t)$ as dependent quantities, to be solved for and

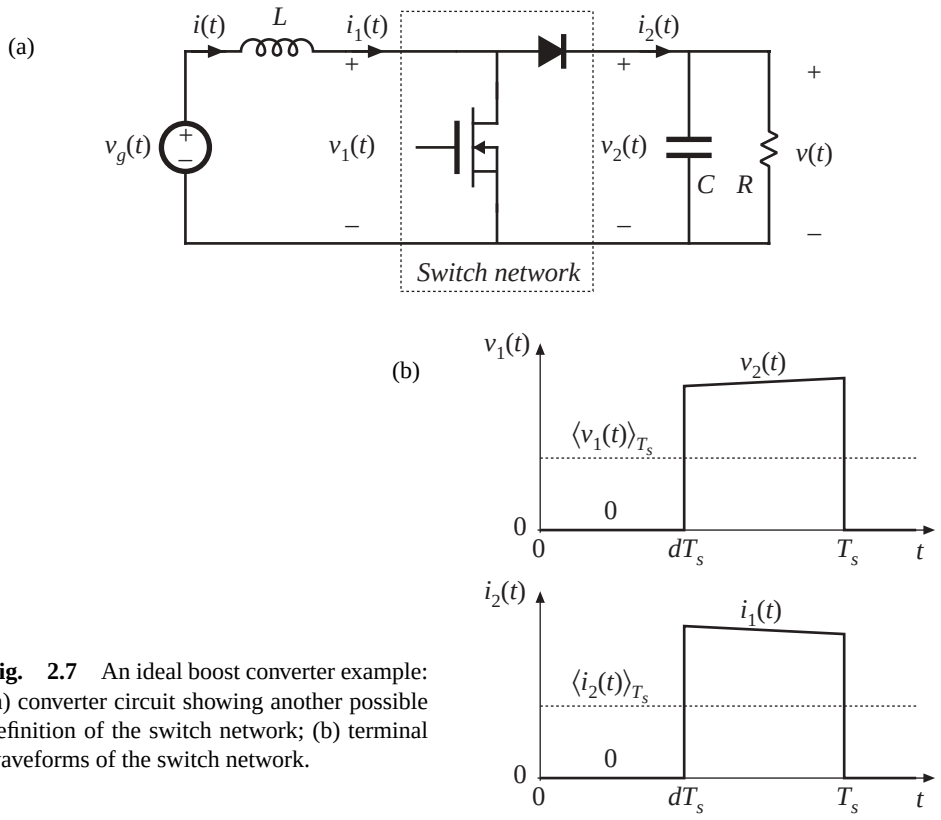


Fig. 2.7 An ideal boost converter example: (a) converter circuit showing another possible definition of the switch network; (b) terminal waveforms of the switch network.

expressed in terms of the independent inputs. The steps in the derivation of the averaged switch model are illustrated in Fig. 2.8.

First, we replace the switch network with dependent voltage and current generators as illustrated in Fig. 2.8(b). The voltage generator $v_1(t)$ models the dependent voltage waveform at the input port of the switch network, i.e., the transistor voltage. As illustrated in Fig. 2.7(b), $v_1(t)$ is zero when the transistor conducts, and is equal to $v_2(t)$ when the diode conducts:

$$v_1(t) = \begin{cases} 0, & 0 < t < dT_s \\ v_2(t), & dT_s < t < T_s \end{cases} \tag{2.7}$$

When $v_1(t)$ is defined in this manner, the inductor voltage waveform is unchanged. Likewise, $i_2(t)$ models the dependent current waveform at port 2 of the network, i.e., the diode current. As illustrated in Fig. 2.7(b), $i_2(t)$ is equal to zero when the transistor conducts, and is equal to $i_1(t)$ when the diode conducts:

$$i_2(t) = \begin{cases} 0, & 0 < t < dT_s \\ i_1(t), & dT_s < t < T_s \end{cases} \tag{2.8}$$

With $i_2(t)$ defined in this manner, the capacitor current waveform is unchanged. Therefore, the original converter circuit shown in Fig. 2.7(a), and the circuit obtained by replacing the switch network of

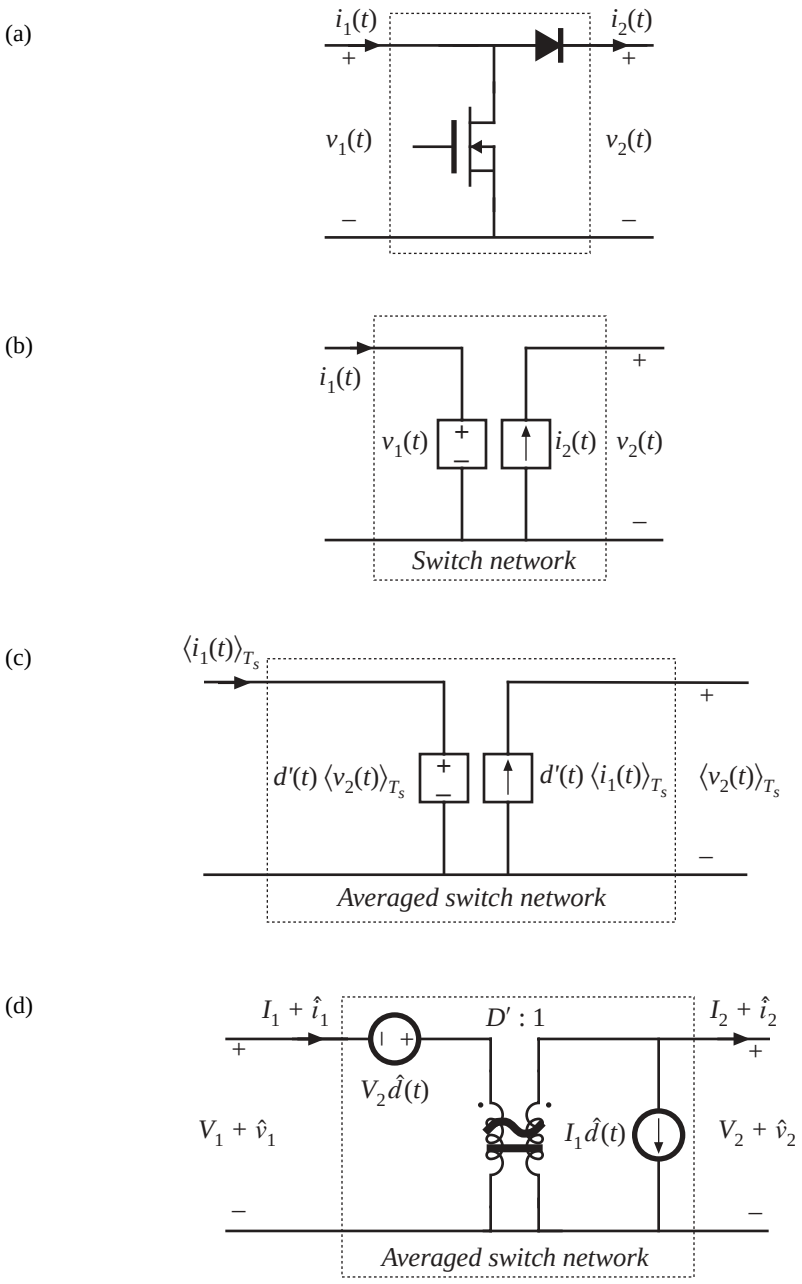


Fig. 2.8 Derivation of the averaged switch model for the CCM boost of Fig. 2.7: (a) switch network; (b) switch network where the switches are replaced by dependent sources whose waveforms match the switch terminal waveforms; (c) large-signal, nonlinear averaged switch model obtained by averaging the switch network terminal waveforms; (d) dc and ac small-signal averaged switch network model.

Fig. 2.8(a) with the switch network of Fig. 2.8(b), are electrically identical. So far, no approximations have been made. Next, we remove the switching harmonics by averaging all signals over one switching period, as in Eq. (2.3). The results are

$$\begin{aligned} \left\langle v_1(t) \right\rangle_{T_s} &= d'(t) \left\langle v_2(t) \right\rangle_{T_s} \\ \left\langle i_2(t) \right\rangle_{T_s} &= d'(t) \left\langle i_1(t) \right\rangle_{T_s} \end{aligned} \tag{2.9}$$

Here we have assumed that the switching ripples of the inductor current and capacitor voltage are small, or at least linear functions of time. The averaged switch model of Fig. 2.8(c) is now obtained. This is a large-signal, nonlinear model, which can replace the switch network in the original converter circuit, for construction of a large-signal nonlinear circuit model of the converter. The switching harmonics have been removed from all converter waveforms, leaving only the dc and low-frequency ac components.

The model can be linearized by perturbing and linearizing the converter waveforms about a quiescent operating point, in the usual manner. Let

$$\begin{aligned} \left\langle v_g(t) \right\rangle_{T_s} &= V_g + \hat{v}_g(t) \\ d(t) &= D + \hat{d}(t) \quad \Rightarrow d'(t) = D' - \hat{d}(t) \\ \left\langle i(t) \right\rangle_{T_s} &= \left\langle i_1(t) \right\rangle_{T_s} = I + \hat{i}(t) \\ \left\langle v(t) \right\rangle_{T_s} &= \left\langle v_2(t) \right\rangle_{T_s} = V + \hat{v}(t) \\ \left\langle v_1(t) \right\rangle_{T_s} &= V_1 + \hat{v}_1(t) \\ \left\langle i_2(t) \right\rangle_{T_s} &= I_2 + \hat{i}_2(t) \end{aligned} \tag{2.10}$$

The nonlinear voltage generator at port 1 of the averaged switch network has value

$$\left(D' - \hat{d}(t)\right)\left(V + \hat{v}(t)\right) = D'\left(V + \hat{v}(t)\right) - V\hat{d}(t) - \hat{v}(t)\hat{d}(t) \tag{2.11}$$

The term $\hat{v}(t)\hat{d}(t)$ is nonlinear, and is small in magnitude provided that the ac variations are much smaller than the quiescent values. When the small-signal assumption is satisfied, this term can be neglected. The term $V\hat{d}(t)$ is driven by the control input, and hence can be represented by an independent voltage source. The term $D'(V + \hat{v}(t))$ is equal to the constant value D' multiplied by the output voltage $(V + \hat{v}(t))$. This term is dependent on the output capacitor voltage; it is represented by a dependent voltage source. This dependent source will become the primary winding of an ideal transformer.

The nonlinear current generator at the port 2 of the averaged switch network is treated in a similar manner. Its current is

$$\left(D' - \hat{d}(t)\right)\left(I + \hat{i}(t)\right) = D'\left(I + \hat{i}(t)\right) - I\hat{d}(t) - \hat{i}(t)\hat{d}(t) \tag{2.12}$$

The term $\hat{i}(t)\hat{d}(t)$ is nonlinear, and can be neglected provided that the small-signal assumption is satisfied. The term $I\hat{d}(t)$ is driven by the control input $\hat{d}(t)$, and is represented by an independent current source. The term $D'(I + \hat{i}(t))$ is dependent on the inductor current $(I + \hat{i}(t))$. This term is modeled by a dependent current source; this source will become the secondary winding of an ideal transformer.

Upon elimination of the nonlinear terms, and replacement of the dependent generators with an ideal D':1 transformer, the combined dc and small-signal ac averaged switch model of Fig. 2.8(d) is obtained. Figure 2.9 shows the complete averaged circuit model of the boost converter.

The circuit model of Fig. 2.9 reveals that the switch network performs the functions of: (*i*)

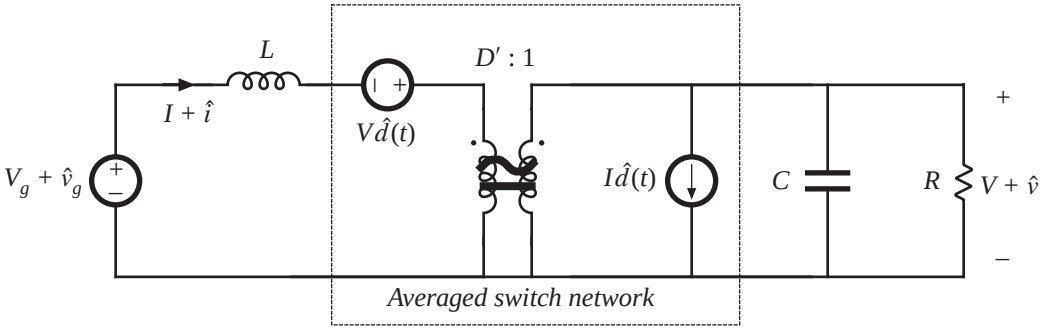


Fig. 2.9 Dc and small-signal ac averaged circuit model of the boost converter.

transformation of dc and small-signal ac voltage and current levels according to the D':1 conversion ratio, and (*ii*) introduction of ac voltage and current variations into the converter circuit, driven by the control input $d(t)$. This model can now be solved using conventional circuit analysis techniques such as phasor analysis or Laplace transform analysis, to find the small-signal ac transfer functions of the converter.

As a second example, we consider the CCM buck converter of Fig. 2.10, where the switch network ports are defined to share a common ground terminal. The derivation of the corresponding averaged switch model follows the same steps as in the boost example. Let us select $v_1(t)$ and $i_2(t)$ as the independent terminal variables of the two-port switch network, since these quantities coincide with the applied converter input voltage $v_g(t)$ and the inductor current $i(t)$, respectively. We then need to express the averaged dependent terminal waveforms $\langle i_1(t)\rangle_{T_s}$ and $\langle v_2(t)\rangle_{T_s}$ as functions of the control input $d(t)$ and of $\langle v_1(t)\rangle_{T_s}$ and $\langle i_2(t)\rangle_{T_s}$. Upon averaging the waveforms of Fig. 2.10(b), one obtains

$$\begin{aligned} \left\langle i_1(t)\right\rangle_{T_s} &= d(t)\left\langle i_2(t)\right\rangle_{T_s} \\ \left\langle v_2(t)\right\rangle_{T_s} &= d(t)\left\langle v_1(t)\right\rangle_{T_s} \end{aligned} \tag{2.13}$$

Perturbation and linearization of Eq. (2.13) then leads to

$$\begin{aligned} I_1 + \hat{i}_1(t) &= D\left(I_2 + \hat{i}_2(t)\right) + I_2\,\hat{d}(t) \\ V_2 + \hat{v}_2(t) &= D\left(V_1 + \hat{v}_1(t)\right) + V_1\,\hat{d}(t) \end{aligned} \tag{2.14}$$

An equivalent circuit corresponding to Eq. (2.14) is illustrated in Fig. 2.11(a). Replacement of the switch network in Fig. 2.10(a) with the averaged switch model of Fig. 2.11(a) leads to the converter averaged circuit model of Fig. 2.11(b). The circuit model of Fig. 2.11(b) reveals that the switch network performs the functions of: (*i*) transformation of dc and small-signal ac voltage and current levels according to the 1:D conversion ratio, and (*ii*) introduction of ac voltage and current variations into the converter circuit, driven by the control input $d(t)$. The model is easy to solve for both dc conversion ratio and small-signal frequency responses.

The three basic switch networks—the buck switch network, the boost switch network, and the general two-switch network—together with the corresponding averaged switch models are shown in Fig. 2.12. Averaged switch models can be refined to include conduction and switching losses. These models can then be used to predict the voltages, currents, and efficiencies of nonideal converters. An example of an averaged switch model that include losses is described in Section 2.2.2.

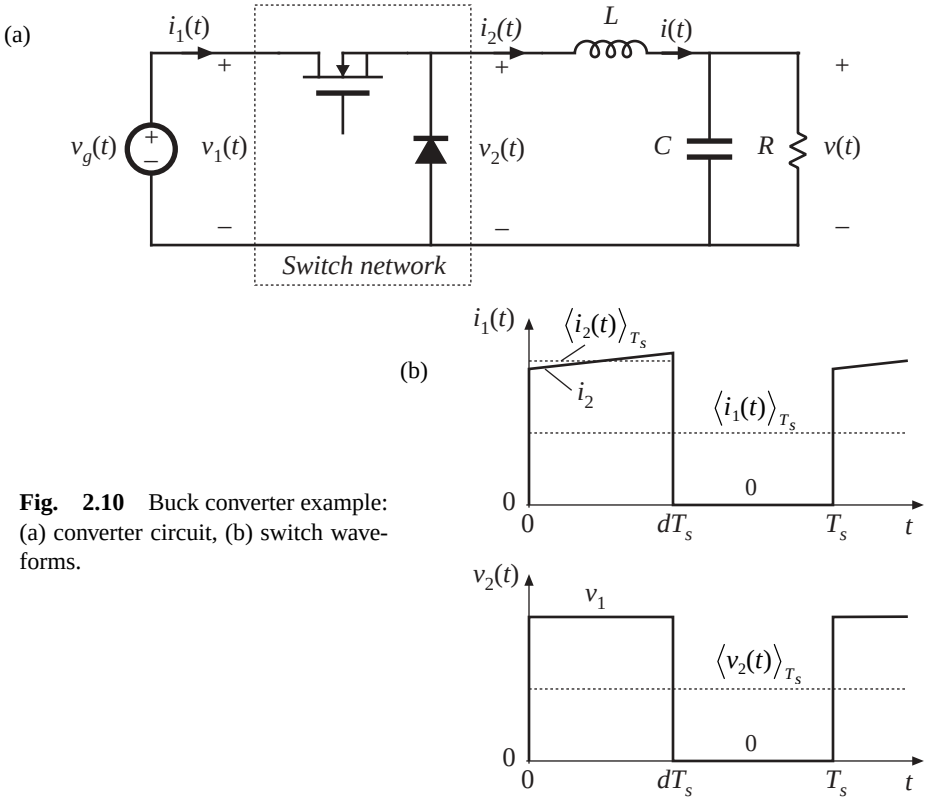


Fig. 2.10 Buck converter example: (a) converter circuit, (b) switch waveforms.

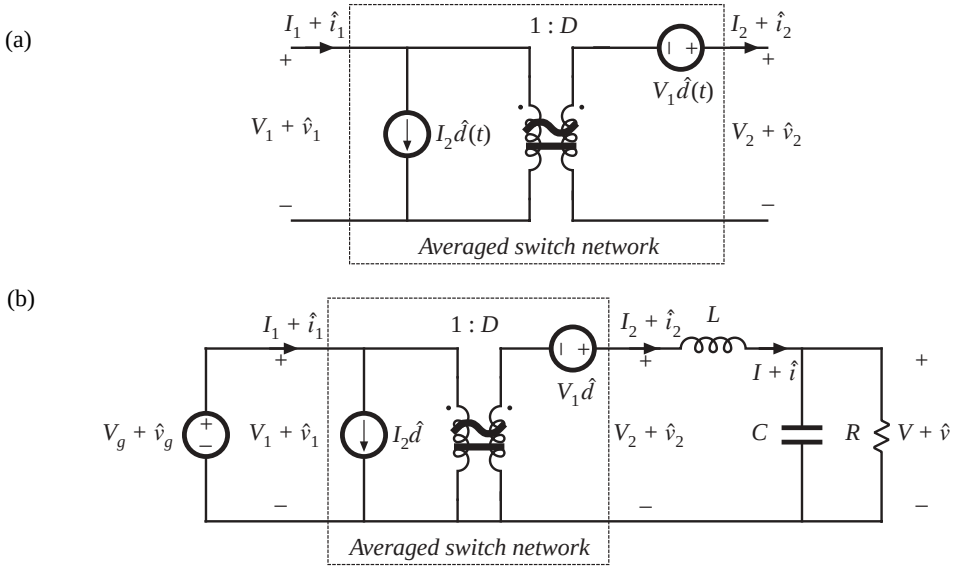


Fig. 2.11 Averaged switch modeling, buck converter example: (a) dc and small-signal ac averaged switch model; (b) Averaged circuit model of the buck converter obtained by replacement of the switch network by the averaged switch model.

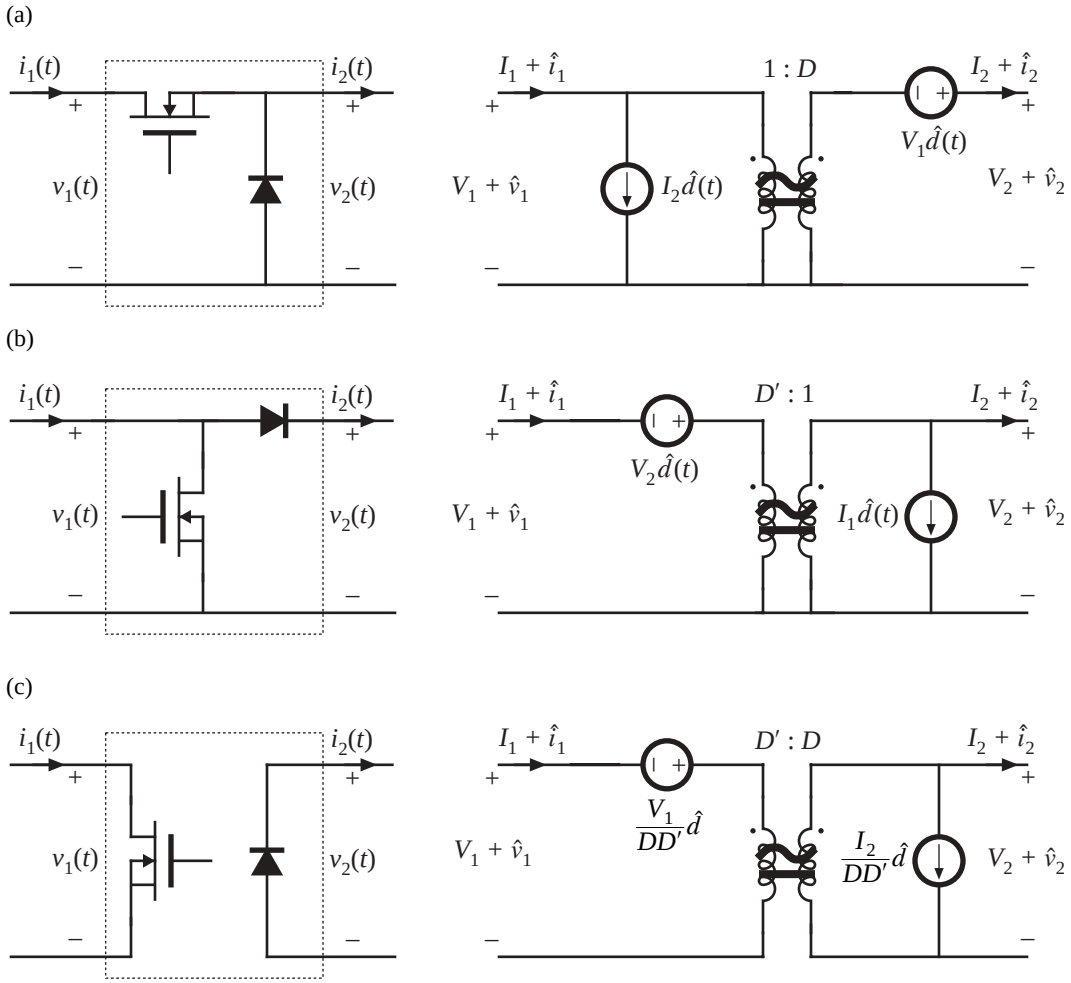


Fig. 2.12 Three basic switch networks, and their CCM dc and small-signal ac averaged switch models: (a) the buck switch network, (b) the boost switch network, and (c) the general two-switch network.

2.2.2 Example: Averaged Switch Modeling of Conduction Losses

An averaged switch model can be refined to include switch conduction losses. Consider the SEPIC of Fig. 2.13. Suppose that the transistor on-resistance is R_{on} and the diode forward voltage drop V_D are approximately constant. In this example, all other conduction or switching losses are neglected. Our objective is to derive an averaged switch model that includes conduction losses caused by the voltage drops across R_{on} and V_D. The waveforms of the switch network terminal currents are unchanged by addition of the loss elements, but the voltage waveforms are affected by the voltage drops across R_{on} and V_D

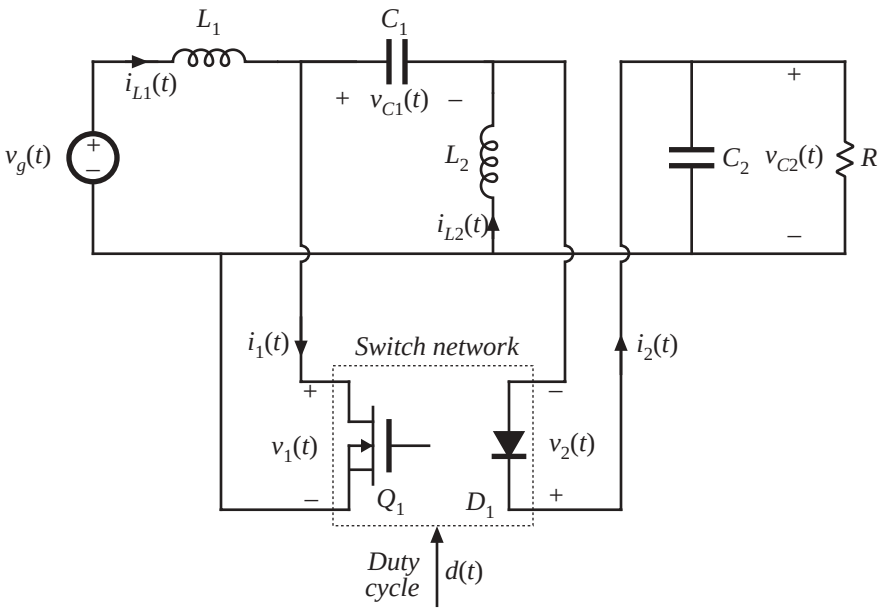


Fig. 2.13 Schematic of the SEPIC, with switch network identified.

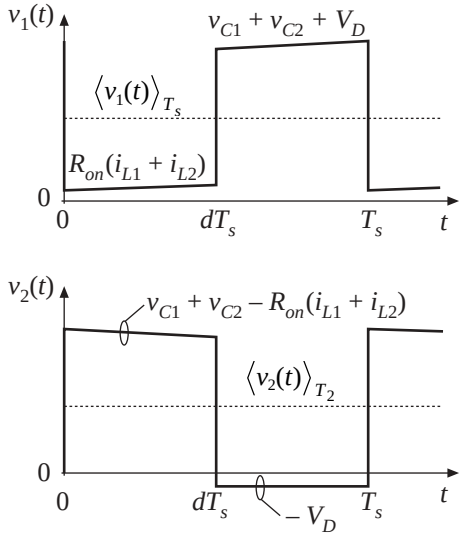


Fig. 2.14 The switch network terminal voltages $v_1(t)$ and $v_2(t)$ for the case when the transistor on-resistance is R_{on} and the diode forward voltage drop is V_D.

as shown in Fig. 2.14. We select $i_1(t)$ and $v_2(t)$ as the switch network independent inputs. The average values of $v_1(t)$ and $v_2(t)$ can be found as follows:

$$\left\langle v_1(t)\right\rangle_{T_s} = d(t)R_{on}\left(\left\langle i_{L1}(t)\right\rangle_{T_s} + \left\langle i_{L2}(t)\right\rangle_{T_s}\right) + d'(t)\left(\left\langle v_{C1}(t)\right\rangle_{T_s} + \left\langle v_{C2}(t)\right\rangle_{T_s} + V_D\right) \tag{2.15}$$

$$\left\langle v_2(t)\right\rangle_{T_s} = d(t)\left(\left\langle v_{C1}(t)\right\rangle_{T_s} + \left\langle v_{C2}(t)\right\rangle_{T_s} - R_{on}\left(\left\langle i_{L1}(t)\right\rangle_{T_s} + \left\langle i_{L2}(t)\right\rangle_{T_s}\right)\right) + d'(t)\left(-V_D\right) \tag{2.16}$$

Next, we proceed to eliminate $\langle i_{L1}(t)\rangle_{T_s}$, $\langle i_{L2}(t)\rangle_{T_s}$, $\langle v_{C1}(t)\rangle_{T_s}$, and $\langle v_{C2}(t)\rangle_{T_s}$, to write the above equations in terms of the averaged independent terminal currents and voltages of the switch network. By combining Eqs. (2.15) and (2.16), we obtain:

$$\left\langle v_{C1}(t)\right\rangle_{T_s} + \left\langle v_{C2}(t)\right\rangle_{T_s} = \left\langle v_1(t)\right\rangle_{T_s} + \left\langle v_2(t)\right\rangle_{T_s} \tag{2.17}$$

The currents can be expressed as:

$$\left\langle i_{L1}(t)\right\rangle_{T_s} + \left\langle i_{L2}(t)\right\rangle_{T_s} = \frac{\left\langle i_1(t)\right\rangle_{T_s}}{d(t)} \tag{2.18}$$

Substitution of Eqs. (2.17) and (2.18) into Eq. (2.15) results in:

$$\left\langle v_1(t)\right\rangle_{T_s} = R_{on}\left\langle i_1(t)\right\rangle_{T_s} + d'(t)\left(\left\langle v_1(t)\right\rangle_{T_s} + \left\langle v_2(t)\right\rangle_{T_s} + V_D\right) \tag{2.19}$$

Equation (2.19) can be solved for the voltage $\langle v_1(t)\rangle_{T_s}$:

$$\left\langle v_1(t)\right\rangle_{T_s} = \frac{R_{on}}{d(t)}\left\langle i_1(t)\right\rangle_{T_s} + \frac{d'(t)}{d(t)}\left(\left\langle v_2(t)\right\rangle_{T_s} + V_D\right) \tag{2.20}$$

The expression for the averaged current $\langle i_2(t)\rangle_{T_s}$ is :

$$\left\langle i_2(t)\right\rangle_{T_s} = \frac{d'(t)}{d(t)}\left\langle i_1(t)\right\rangle_{T_s} \tag{2.21}$$

Equations (2.20) and (2.21) constitute the averaged terminal relations of the switch network. An equivalent circuit corresponding to these relationships is shown in Fig. 2.15. The generators that depend on the

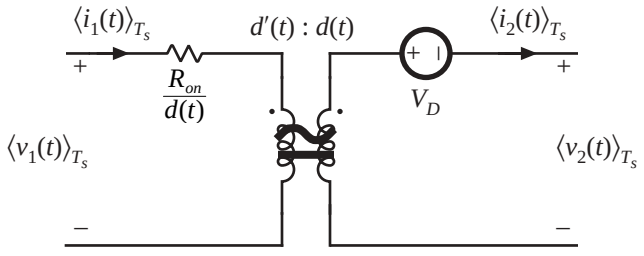


Fig. 2.15 Large-signal averaged switch model for the general two-switch network of Fig. 2.12. This model includes conduction losses due to the transistor on-resistance R_{on} and the diode forward voltage drop V_D.

transistor duty cycle $d(t)$ are combined into an ideal transformer with the turns ratio $d'(t):d(t)$. This part of the model is the same as in the averaged switch model derived earlier for the switch network with ideal switches. The elements R_{on}/d and V_D model the conduction losses in the switch network. This is a large-signal, nonlinear model. If desired, this model can be perturbed and linearized in the usual manner, to obtain a small-signal ac switch model.

The model of Fig. 2.15 is also well suited for computer simulations. As an example of this application, consider the buck-boost converter in Fig 2.16(a). In this converter, the transistor on-resistance is R_{on} = 50 mΩ, while the diode forward voltage drop is V_D = 0.8 V. Resistor R_L = 100 mΩ models the copper loss of the inductor. All other losses are neglected. Figure 2.16(b) shows the averaged circuit model of the converter obtained by replacing the switch network with the averaged switch model of Fig. 2.15.

Let's investigate how the converter output voltage reaches its steady-state value, starting from zero initial conditions. A transient simulation can be used to generate converter waveforms during the start-up transient. It is instructive to compare the responses obtained by simulation of the converter

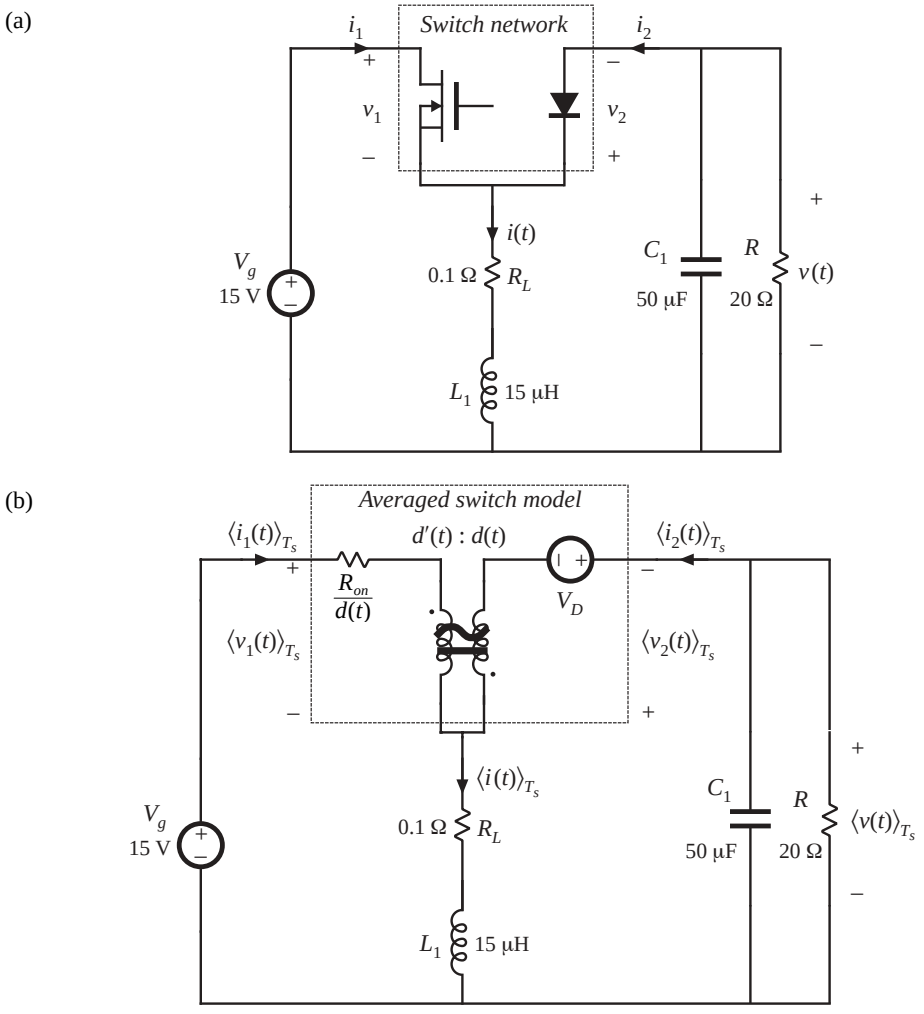


Fig. 2.16 Buck-boost converter example: (a) converter circuit; (b) averaged circuit model of the converter.

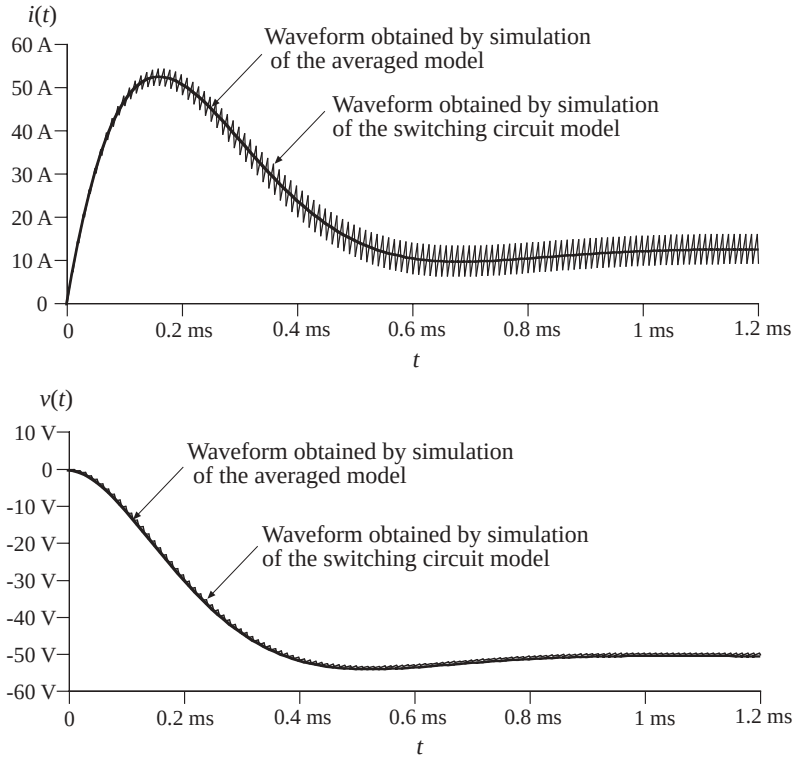


Fig. 2.17 Waveforms obtained by simulation of the switching converter circuit shown in Fig. 2.16(a) and by simulation of the averaged circuit model of Fig. 2.16(b)

switching circuit shown in Fig. 2.16(a) against the responses obtained by simulation of the averaged circuit model shown in Fig. 2.16(b). Details of how these simulations are performed can be found in Appendix B.1. Figure 2.17 shows the start-up transient waveforms of the inductor current and the output voltage. In the waveforms obtained by simulation of the averaged circuit model, the switching ripple is removed, but other features of the converter transient responses match very closely the responses obtained from the switching circuit. Simulations of averaged circuit models can be used to predict converter steady-state and dynamic responses, as well as converter losses and efficiency.

2.3 TRANSFER FUNCTIONS OF SOME BASIC CCM CONVERTERS

The salient features of the line-to-output and control-to-output transfer functions of the basic buck, boost, and buck-boost converters are summarized in Table 2.1. In each case, the control-to-output transfer function is of the form

$$G_{vd}(s) = G_{d0} \frac{\left(1 - \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)} \tag{2.22}$$

and the line-to-output transfer function is of the form

Table 2.1 Salient features of the small-signal CCM transfer functions of some basic dc–dc converters

Converter	G_{g0}	G_{d0}	ω_0	Q	ω_z
Buck	D	$\frac{V}{D}$	$\frac{1}{\sqrt{LC}}$	$R\sqrt{\frac{C}{L}}$	∞
Boost	$\frac{1}{D'}$	$\frac{V}{D'}$	$\frac{D'}{\sqrt{LC}}$	$D'R\sqrt{\frac{C}{L}}$	$\frac{D'^2R}{L}$
Buck-boost	$-\frac{D}{D'}$	$\frac{V}{DD'}$	$\frac{D'}{\sqrt{LC}}$	$D'R\sqrt{\frac{C}{L}}$	$\frac{D'^2R}{DL}$

$$G_{vg}(s) = G_{g0}\frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{2.23}$$

The boost and buck-boost converters exhibit control-to-output transfer functions containing two poles and a right half-plane zero. The buck converter $G_{vg}(s)$ exhibits two poles but no zero. The line-to-output transfer functions of all three ideal converters contain two poles and no zeroes.

2.3.1 Physical Origins of the Right Half-Plane Zero in Converters

Figure 2.18 contains a block diagram that illustrates the behavior of the right half-plane zero. At low frequencies, the gain (s/ω_z) has negligible magnitude, and hence $u_{out} \approx u_{in}$. At high frequencies, where the magnitude of the gain (s/ω_z) is much greater than 1, $u_{out} \approx -(s/\omega_z)u_{in}$. The negative sign causes a phase reversal at high frequency. The implication for the transient response is that the output initially tends in the opposite direction of the final value.

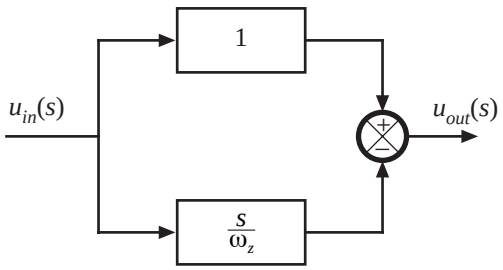


Fig. 2.18 Block diagram having a right half-plane zero transfer function, as in Eq. (2.22), with $\omega_0 = \omega_z$.

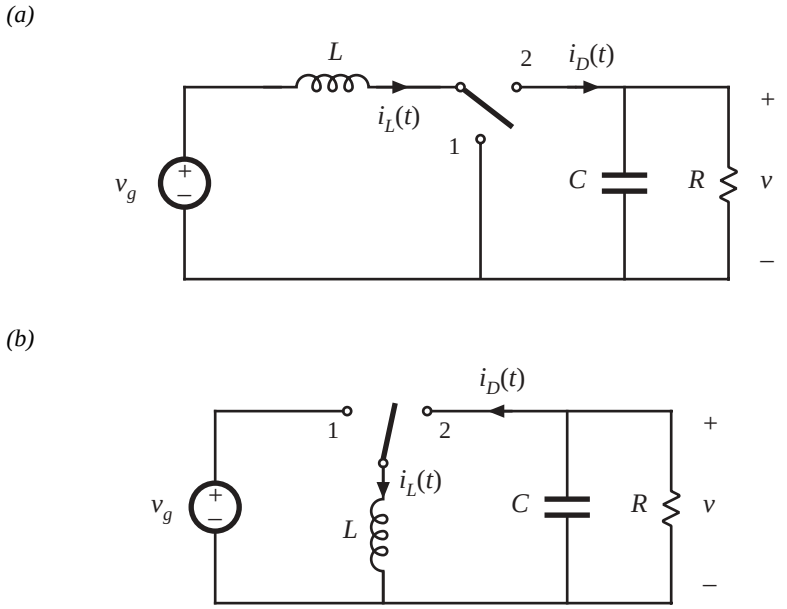


Fig. 2.19 Two basic converters whose CCM control-to-output transfer functions exhibit RHP zeroes: (a) boost, (b) buck-boost.

The control-to-output transfer functions of the boost and buck-boost converters, Fig. 2.19, exhibit RHP zeroes. Typical transient response waveforms for a step change in duty cycle are illustrated in Fig. 2.20. For this example, the converter initially operates in equilibrium, at $d = 0.4$ and $d' = 0.6$. Equilibrium inductor current $i_L(t)$, diode current $i_D(t)$, and output voltage $v(t)$ waveforms are illustrated. The average diode current is

$$\left\langle i_D \right\rangle_{T_s} = d' \left\langle i_L \right\rangle_{T_s} \tag{2.24}$$

By capacitor charge balance, this average diode current is equal to the dc load current when the converter operates in equilibrium. At time $t = t_1$, the duty cycle is increased to 0.6. In consequence, d' decreases to 0.4. The average diode current, given by Eq. (2.24), therefore decreases, and the output capacitor begins to discharge. The output voltage magnitude initially decreases as illustrated.

The increased duty cycle causes the inductor current to slowly increase, and hence the average diode current eventually exceeds its original $d = 0.4$ equilibrium value. The output voltage eventually increases in magnitude, to the new equilibrium value corresponding to $d = 0.6$.

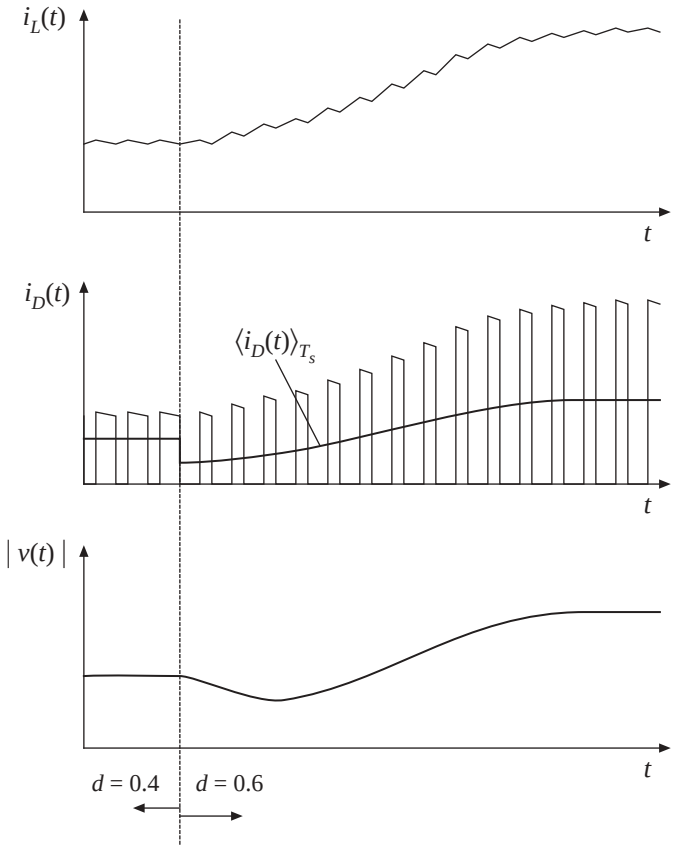
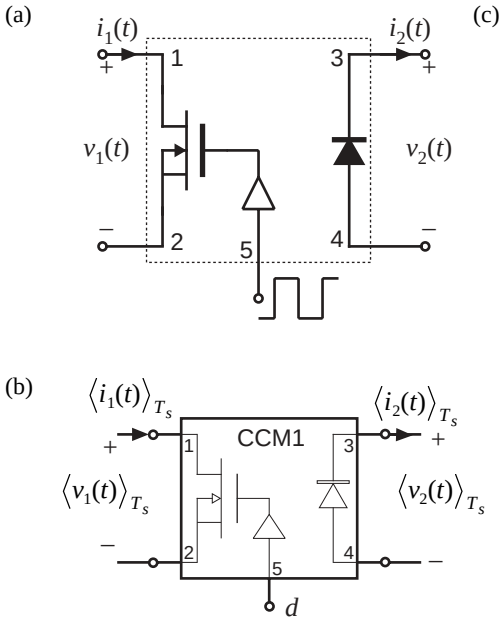


Fig. 2.20 Waveforms of the converters of Fig. 2.19, for a step response in duty cycle. The average diode current and output voltage initially decrease, as predicted by the RHP zero. Eventually, the inductor current increases, causing the average diode current and the output voltage to increase.

The presence of a right half-plane zero tends to destabilize wide-bandwidth feedback loops, because during a transient the output initially changes in the wrong direction. The phase margin test for feedback loop stability is discussed in the next chapter; when a RHP zero is present, it is difficult to obtain an adequate phase margin in conventional single-loop feedback systems having wide bandwidth. Prediction of the right half-plane zero, and the consequent explanation of why the feedback loops controlling CCM boost and buck-boost converters tend to oscillate, was one of the early successes of averaged converter modeling.

2.4 AVERAGED SWITCH MODELS FOR SIMULATION

The central idea of the *averaged switch modeling* described in the previous sections is to identify a switch network in the converter, and then to find an averaged circuit model. The resulting averaged switch model can then be inserted into the converter circuit to obtain a complete model of the converter. An important feature of the averaged switch modeling approach is that the same model can be used in many different converter configurations; it is not necessary to rederive an averaged equivalent circuit for each particular converter. This feature is also very convenient for construction of averaged circuit models for simulation. A general-purpose subcircuit represents a large-signal nonlinear averaged switch model. The converter averaged circuit for simulation is then obtained by replacing the switch network with this subcircuit. Based on the discussion in Section 7.4, subcircuits that represent CCM averaged switch mod-



(c)

```
*********************************************************************
* Subcircuit: CCM1
* Application: two-switch PWM converters
* Limitations: ideal switches, CCM only, no transformer
*********************************************************************
* Parameters: none
*********************************************************************
* Nodes:
* 1: transistor positive (drain for an n-channel MOS)
* 2: transistor negative  (source for an n-channel MOS)
* 3: diode cathode
* 4: diode anode
* 5: duty cycle control input
*********************************************************************
.subckt CCM1 1  2  3  4  5
Et 1 2 value={(1-v(5))*v(3,4)/v(5)}
Gd 4 3 value={(1-v(5))*i(Et)/v(5)}
.ends
*********************************************************************
```

Fig. 2.21 Averaged switch model CCM1: (a) the general two-switch network: (b) symbol for the averaged switch subcircuit model; (c) PSpice netlist of the subcircuit.

els are described in this section, together with application examples.

2.4.1 Basic CCM Averaged Switch Model

The large-signal averaged switch model for the general two-switch network of Fig. 2.12(c) is shown in Fig. 2.21(b). A PSpice subcircuit implementation of this model is also shown in Fig. 2.21. The subcircuit has five nodes. The transistor port of the averaged switch network is connected between the nodes 1 and 2, while the diode port is comprised of nodes 3 and 4. The duty ratio $d = v(5)$ is the control input to the subcircuit at the node 5. The quantity $v(5)$ is a voltage that is equal to the duty cycle, and that lies in the range zero to one volt. Figure 2.21(c) shows the netlist of the subcircuit. The netlist consists of only four lines of code and several comment lines (the lines starting with *). The .subckt line defines the name (CCM1) of the subcircuit and the interface nodes. The value of the controlled voltage source E_t, which models the transistor port of the averaged switch network, is written according to Eq. (7.136):

$$\langle v_1(t)\rangle_{T_s} = \frac{d'(t)}{d(t)} \langle v_2(t)\rangle_{T_s} \tag{2.25}$$

Note that $v(3,4)$ in the subcircuit of Fig. 2.21 is equal to the switch network independent input $\langle v_2(t)\rangle_{T_s}$. Also, $d(t) = v(5)$, and $d'(t) = 1 - d(t) = 1 - v(5)$. The value of the controlled current source G_d, which models the diode port, is computed according to:

$$\langle i_2(t)\rangle_{T_s} = \frac{d'(t)}{d(t)} \langle i_1(t)\rangle_{T_s} \tag{2.26}$$

The switch network independent input $\langle i_1(t)\rangle_{T_s}$ equals the current $i(E_t)$ through the controlled voltage source E_t. The .ends line completes the subcircuit netlist. The subcircuit CCM1 is included in the model

library *switch.lib*, which can be downloaded from the course web site.

An advantage of the subcircuit CCM1 of Fig. 2.21 is that it can be used to construct an averaged circuit model for simulation of any two-switch PWM converter operating in continuous conduction mode, subject to the assumptions that the switches can be considered ideal, and that the converter does not include a step-up or step-down transformer. The subcircuit can be further refined to remove these limitations. In converters with an isolation transformer, the right-hand side of Eqs. (2.25) and (2.26) should be divided by the transformer turns ratio. Inclusion of switch conduction losses is discussed in the next section.

A disadvantage of the model in Fig. 2.21 is that Eqs. (2.25) and (2.26) have a discontinuity at duty cycle equal to zero. In applications of the subcircuit, it is necessary to restrict the duty-cycle to the range $0 < D_{min} \le d \le 1$.

Following the approach of this section, subcircuits can be constructed for the large-signal averaged models of the buck switch network (see Fig. 2.12(a)), and the boost switch network (see Fig. 2.12(b)). An advantage of these models is that their defining equations do not have the discontinuity problem at $d = 0$.

2.4.2 CCM Averaged Switch Model that Includes Switch Conduction Losses

Let us modify the model of Fig. 2.21 to include switch conduction losses. Figure 2.22 shows simple device models that include transistor and diode conduction losses in the general two-switch network of Fig. 2.21(a). The transistor is modeled as an ideal switch in series with an on-resistance R_{on}. The diode is modeled as an ideal diode in series with a forward voltage drop V_D and resistance R_D.

Following the same averaged switch modeling approach, we can find the following relationships that describe the averaged switch model for the switch network of Fig. 2.22:

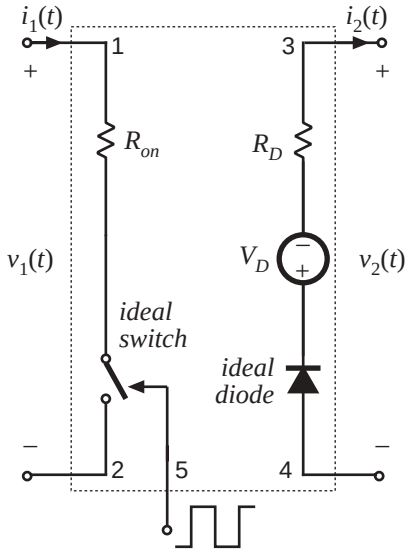
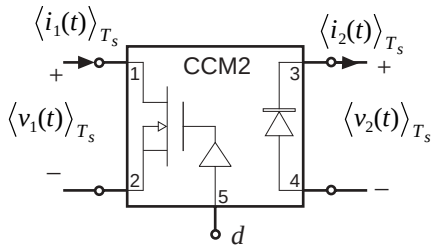


Fig. 2.22 Switch network model that includes conduction loss elements R_{on}, V_D and

(a)



(b)

```
*************************************************************
* MODEL: CCM2
* Application: two-switch PWM converters, includes
*              conduction losses due to Ron, VD, RD
* Limitations: CCM only, no transformer
*************************************************************
* Parameters:
*      Ron = transistor on-resistance
*      VD = diode forward voltage drop
*      RD = diode on-resistance
*************************************************************
* Nodes:
* 1: transistor positive (drain for an n-channel MOS)
* 2: transistor negative (source for an n-channel MOS)
* 3: diode cathode
* 4: diode anode
* 5: duty cycle control input
*************************************************************
.subckt CCM2 1  2  3  4  5
+params: Ron=0 VD=0 RD=0
Er 1 1x value={i(Et)*(Ron+(1-v(5))*RD/v(5))/v(5)}
Et 1x 2 value={(1-v(5))*(v(3,4)+VD)/v(5)}
Gd 4 3 value={(1-v(5))*i(Et)/v(5)}
.ends
*************************************************************
```

Fig. 2.23 Subcircuit implementation of the CCM averaged switch model that includes conduction losses: (a) circuit symbol; (b) PSpice netlist for the subcircuit.

$$\langle v_1(t)\rangle_{T_s} = \left(\frac{R_{on}}{d(t)} + \frac{d'(t)R_D}{d^2(t)}\right)\langle i_1(t)\rangle_{T_s} + \frac{d'(t)}{d(t)}\left(\langle v_2(t)\rangle_{T_s} + V_D\right) \tag{2.27}$$

$$\langle i_2(t)\rangle_{T_s} = \frac{d'(t)}{d(t)}\langle i_1(t)\rangle_{T_s} \tag{2.28}$$

A subcircuit implementation of the averaged switch model described by Eqs. (2.27) and (2.28) is shown in Fig. 2.23 The subcircuit terminal nodes are the same as in the CCM1 subcircuit: the transistor port is between the nodes 1 and 2; the diode port is between the nodes 3 and 4; the duty ratio $d = v(5)$ is the control input to the subcircuit at the node 5. Two controlled voltage sources in series, E_r and E_t, are used to generate the port 1 (transistor) averaged voltage according to Eq. (2.27). The controlled voltage source E_r models the voltage drop across the equivalent resistance $R_{on}/d(t) + d'(t)R_D/d^2(t)$ in Eq. (2.27). Note that this equivalent resistance is a nonlinear function of the switch duty cycle $d(t)$. The controlled voltage source E_t shows how the port 1 (transistor) averaged voltage depends on the port 2 (diode) averaged voltage. The controlled current source G_d models the averaged diode current according to Eq. (2.28). The subcircuit CCM2 has three parameters (R_{on}, V_D, and R_D) that can be specified when the subcircuit is used in a converter circuit. The default values of the subcircuit parameters, $R_{on} = 0$, $V_D = 0$, and $R_D = 0$, are defined in the .subckt line. These values correspond to the ideal case of no conduction losses. The subcircuit CCM2 is included in the model library *switch.lib.*

The model of Fig. 2.23 is based on the simple device models of Fig. 2.22. It is assumed that inductor current ripples are small and that the converter operates in continuous conduction mode. Many practical converters, however, must operate in discontinuous conduction mode at low duty cycles where the diode forward voltage drop is comparable to or larger than the output voltage. In such cases, the model of Fig. 2.22, which includes V_D as a fixed voltage generator, gives incorrect, physically impossible results for polarities of converter voltages and currents, losses and efficiency.

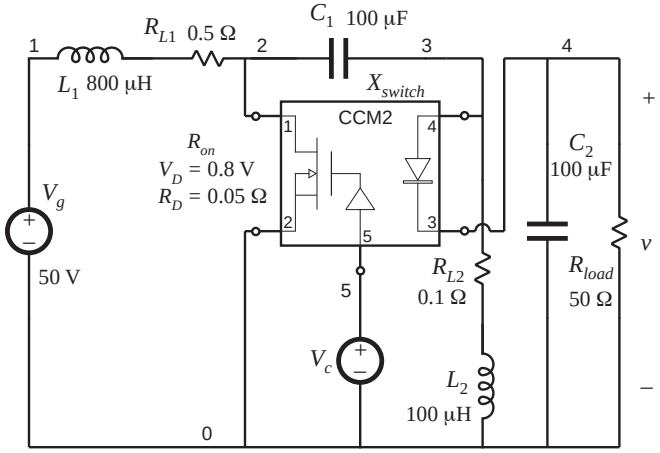


Fig. 2.24 SEPIC simulation example.

```
SEPIC DC conversion ratio and efficiency

* Define parameters:
.param  Ron=0.0 VD=0.8 RD=0.05
* Analysis setup:
.dc lin Vc 0.1 1 0.01
.step lin PARAM Ron 0 1 0.5

* Converter netlist:
Vg 1 0 50V
L1 1 2x  800u
RL1 2x 2 0.5
L2 0 3x 100uH
RL2 3x 3 0.1
C1 2 3 100uF
C2 4 0 100uF
Xswitch 2 0 4 3 5 CCM2
+params: Ron={Ron} VD={VD} RD={RD}
Rload 4 0 50

* Duty cycle input:
Vc  5 0 0.5

.lib switch.lib
.probe
.end
```

2.4.3 Example: SEPIC DC Conversion Ratio and Efficiency

Let us consider an example of how the subcircuit CCM2 can be used to generate dc conversion ratio and efficiency curves for a CCM converter. As an example, Figure 2.24 shows a SEPIC averaged circuit model. To construct the averaged circuit model for simulation, the switch network is replaced by the subcircuit CCM2. In the converter netlist shown in Fig. 2.24, the X_{switch} line shows how the subcircuit is connected to other parts of the converter. The switch duty cycle is set by the voltage source V_c. All other parts of the converter circuit are simply copied to the averaged circuit model. Inductor winding resistances R_{L1} = 0.5 Ω and R_{L2} = 0.1 Ω are included to model copper losses of the inductors L_1 and L_2, respectively. The switch conduction loss parameters are defined by the .param line in the netlist: R_{on} = 0, V_D = 0.8 V, R_D = 0.05 Ω. Notice how these values are passed to the subcircuit CCM2 in the X_{switch} line. In this example, all other losses in the converter are neglected. A dc sweep analysis (see the .dc line in the netlist) is set to vary the dc voltage source V_c from 0.1 V to 1 V, in 0.01 V increments, which corresponds to varying the switch duty cycle over the range from D = 0.1 to D = 1. The range of duty cycles from zero to 0.1 is not covered because of the model discontinuity problem at D = 0 (discussed in Section 2.4.1), and because the model predictions for conduction losses at low duty cycles are not valid, as discussed in Section 2.4.2. The dc sweep analysis is repeated for values of the switch on-resistance in the range from R_{on} = 0 Ω to R_{on} = 1 Ω in 0.5 Ω increments (see the .step line in the netlist). The .lib line refers to the *switch.lib* library, which contains definitions of the subcircuit CCM2 and all other subcircuit models described in this document.

Simulation results for the dc output voltage V and the converter efficiency η are shown in Fig. 2.25. At low duty cycles, efficiency drops because the diode forward voltage drop is comparable to the output voltage. At higher duty cycles, the converter currents increase, so that the conduction losses increase. Eventually, for duty cycles approaching 1, both the output voltage and the efficiency approach zero. Given a desired dc output voltage and efficiency, the plots in Fig. 2.25 can be used to select the

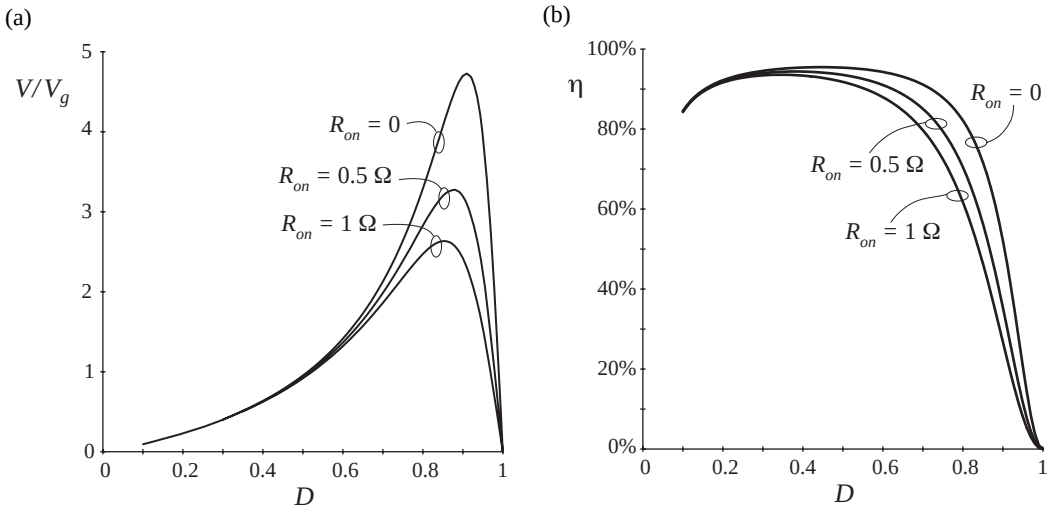


Fig. 2.25 SEPIC simulation example: (a) dc conversion ratio and (b) efficiency.

transistor with an appropriate value of the on-resistance.

2.4.4 Example: Transient Response of a Buck–Boost Converter

In addition to steady-state conversion characteristics, it is often of interest to investigate converter transient responses. For example, in voltage regulator designs, it is necessary to verify whether the output voltage remains within specified limits when the load current takes a step change. As another example, during a start-up transient when the converter is powered up, converter components can be exposed to significantly higher stresses than in steady state. It is of interest to verify that component stresses are within specifications or to make design modifications to reduce the stresses. In these examples, transient simulations can be used to test for converter responses.

Transient simulations can be performed on the converter switching circuit model or on the converter averaged circuit model. As an example, let us apply these two approaches to investigate a start-up transient response of the buck-boost converter shown in Fig. 2.26.

Figure 2.27 shows a switching circuit model of the buck-boost converter. The inductor winding resistance R_L is included to model the inductor copper losses. The MOSFET is modeled as a voltage-controlled switch S_{q1} controlled by a pulsating voltage source v_c. The switch .model line specifies the switch on-resistance R_{on} = 50 mΩ, and the switch off-resistance R_{off} = 10 MΩ. The switch is on when the controlling voltage v_c is greater than V_{on} = 6 V, and off when the controlling voltage v_c is less than V_{off} = 4 V. The pulsating source v_c has the pulse amplitude equal to 10 V. The period is $T_s = 1/f_s$ = 10 μs, the rise and fall times are $t_r = t_f$ = 100 ns, and the pulse width is t_p = 7.9 μs. The switch duty cycle is $D = (t_p + 0.5(t_r + t_f))/T_s = 0.8$. The built-in nonlinear Spice model is used for the diode. In the diode .model statement, only the parameter I_s is specified, to set the forward voltage drop across the diode. The switch and the diode models used in this example are very simple. Conduction losses are modeled in a simple manner, and details of complex device behavior during switching transitions are neglected. Therefore, the circuit model of Fig. 2.27 cannot be used to examine switching transitions or to predict

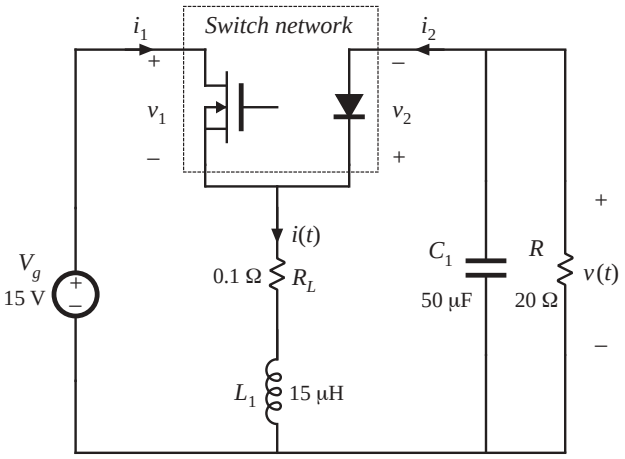
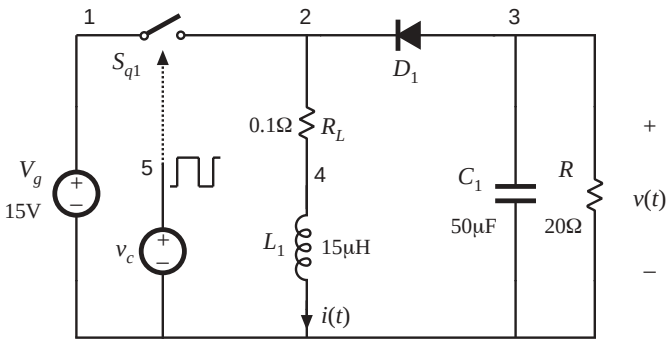


Fig. 2.26 Buck-boost converter example.

switching losses in the converter. Nevertheless, basic switching operation is modeled, and a transient simulation can be used to find out how the converter waveforms evolve in time over many switching cycles. Transient simulation parameters are defined by the .tran line: the output time step is 1 μs, the final simulation time is 1.2 ms, the output waveforms are generated from the start of simulation at time equal to zero, and the maximum allowed time step is 1 μs. The uic ("use initial conditions") option tells the simulator to start with all capacitor voltages and inductor currents equal to the specified initial values. For example, ic=0 in the L_1 line sets the initial inductor current to zero. In Spice, the default initial conditions are always zero, so that ic=0 statements can be omitted.

An averaged circuit model of the buck-boost converter is shown in Fig. 2.28. This circuit model is obtained by replacing the switch network in the converter of Fig. 2.26 by the CCM2 subcircuit. Notice that the circuits and the netlists of Figs. 2.27 and Fig. 2.28 are very similar. The only difference is that the switching devices in the converter circuit of Fig. 2.27 are replaced by the CCM2 subcircuit X_{switch} in Fig. 2.28. Also, the pulsating source $v_c(t)$ in the switching circuit is replaced by a constant voltage source v_c equal to the switch duty cycle $D = 0.8$.

The inductor current and the capacitor voltage waveforms during the start-up transient are shown in Fig. 2.29. For comparison, the waveforms obtained by transient simulation of the switching




```
Buck-boost converter: switching circuit
Vg 1 0 15V
Sq1 1 2 5 0 switch
D1 3 2 diode
RL 2 4 0.1
L1 4 0 15uH ic=0
C1 3 0 50uF ic=0
R 3 0 20
Vc 5 0 pulse
+(0 10V 0us 100ns 100ns 7.9us 10us)
.model switch vswitch
+(Ron=0.05 Roff=10meg Von=6V Voff=4V)
.model diode d (Is=1e-12)
.tran 1u 1.2m 0m 1u uic
.probe
.end
```

Fig. 2.27 Buck-boost converter simulation example, switching circuit model.

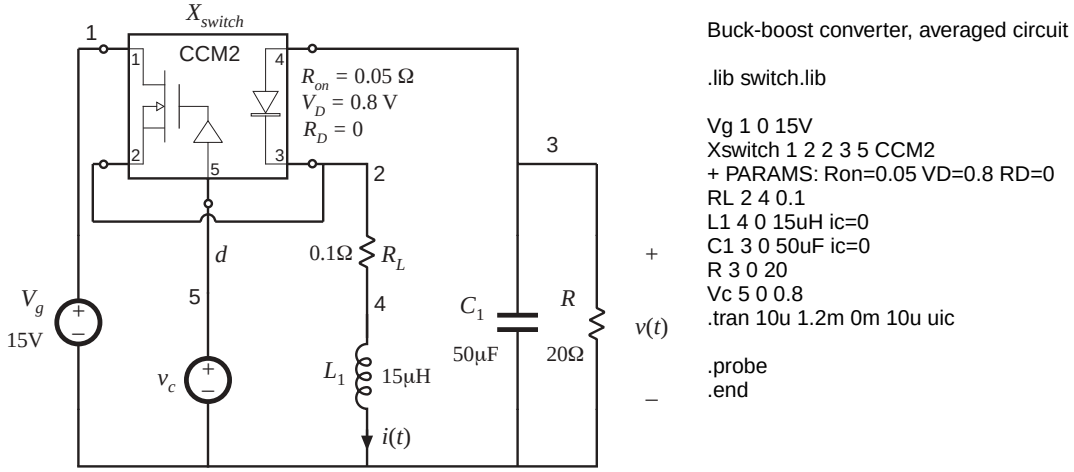


Fig. 2.28 Buck-boost converter simulation example, averaged circuit model.

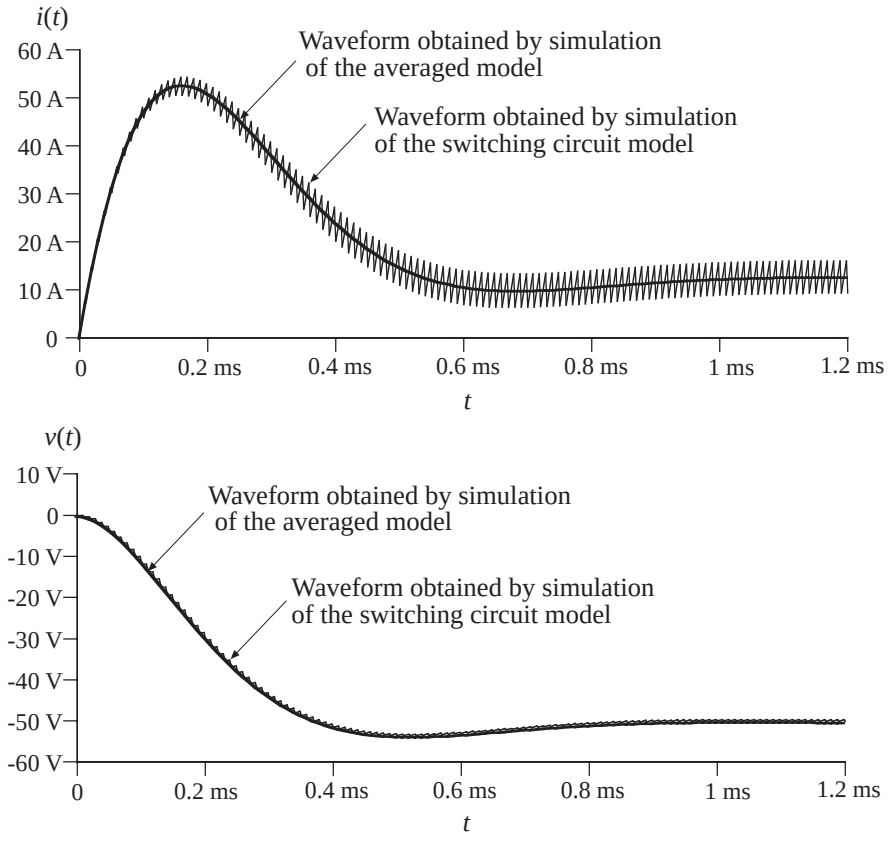


Fig. 2.29 Inductor current and output voltage waveforms obtained by transient simulation of the switching converter circuit shown in Fig. 2.27, and by simulation of the averaged circuit model of Fig. 2.28

converter circuit shown in Fig. 2.27, and by simulation of the averaged circuit model of Fig. 2.28 are shown. Switching ripples can be observed in the waveforms obtained by simulation of the switching circuit model. The converter transient response is governed by the converter natural time constants. Since these time constants are much longer than the switching period, the converter start-up transient responses in Fig. 2.29 take many switching cycles to reach the steady state. In the results obtained by simulation of the averaged circuit model, the switching ripples are removed, but the low-frequency portions of the converter transient responses, which are governed by the natural time constants of the converter network, match very closely the responses obtained by simulation of the switching circuit.

Based on the results shown in Fig. 2.29, we can see that converter components are exposed to significantly higher current stresses during the start-up transient than during steady state operation. The problem of excessive stresses in the start-up transient is quite typical for switching power converters. Practical designs usually include a "soft-start" circuit, where the switch duty cycle is slowly increased from zero to the steady-state value to reduce start-up transient stresses.

This simulation example illustrates how an averaged circuit model can be used in place of a switching circuit model to investigate converter large-signal transient responses. An advantage of the averaged circuit model is that transient simulations can be completed much more quickly because the averaged model is time invariant, and the simulator does not spend time computing the details of the fast switching transitions. This advantage can be important in simulations of larger electronic systems that include switching power converters. Another important advantage also comes from the fact that the averaged circuit model is nonlinear but time-invariant: ac simulations can be used to linearize the model and generate small-signal frequency responses of interest. This is not possible with switching circuit models. Examples of small-signal ac simulations can be found in the following sections.

2.4.5 Combined CCM/DCM Averaged Switch Model

The models and examples of above are all based on the assumption that the converters operate in continuous conduction mode (CCM). All converters containing a diode rectifier operate in discontinuous conduction mode (DCM) if the load current is sufficiently low. In some cases, converters are purposely designed to operate in DCM. It is therefore of interest to develop averaged models suitable for simulation of converters that may operate in either CCM or DCM.

Figure 2.30 illustrates the general two-switch network, and the corresponding large-signal averaged models in CCM and DCM. The CCM averaged switch model, which is derived in Section 7.4, is an ideal transformer with $d' : d$ turns ratio. In DCM, the large-signal averaged switch model is a loss-free resistor, as derived in Section 11.1. Our objective is to construct a combined CCM/DCM averaged switch model that reduces to the model of Fig. 2.30(a) or to the model of Fig. 2.30(c) depending on the operating mode of the converter. Let us define an effective switch conversion ratio $\mu(t)$, so that the averaged switch model in both modes has the same form as in CCM, as shown in Fig. 2.31. If the converter operates in CCM, then the switch conversion ratio $\mu(t)$ is equal to the switch duty cycle $d(t)$,

$$\mu = d \tag{2.29}$$

If the converter operates in DCM, then the effective switch conversion ratio can be computed so that the terminal characteristics of the averaged-switch model of Fig. 2.31 match the terminal characteristics of the loss-free resistor model of Fig. 2.30(c). Matching the port 1 characteristics gives

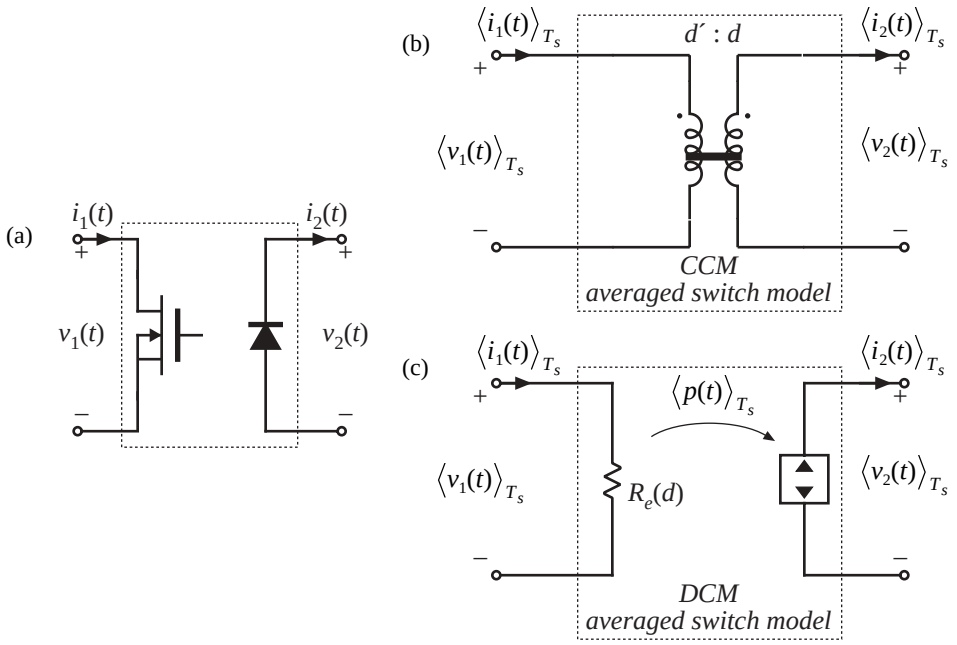


Fig. 2.30 Summary of averaged switch modeling: (a) general two-switch network, (b) averaged switch model in CCM, and (c) averaged switch model in DCM.

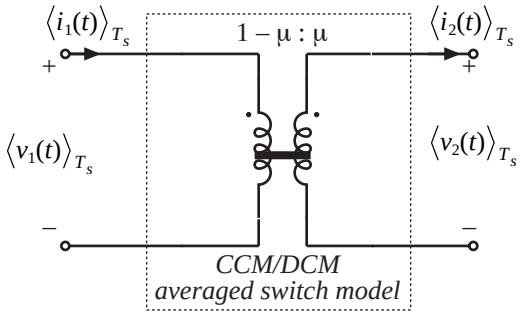


Fig. 2.31 A general averaged switch model using the equivalent switch conversion ratio μ.

$$\langle v_1(t)\rangle_{T_s} = \frac{1-\mu}{\mu}\langle v_2(t)\rangle_{T_s} = R_e\langle i_1(t)\rangle_{T_s} \tag{2.30}$$

which can be solved for the switch conversion ratio μ,

$$\mu = \frac{1}{1+\dfrac{R_e\langle i_1(t)\rangle_{T_s}}{\langle v_2(t)\rangle_{T_s}}} \tag{2.31}$$

It can be verified that matching the port 2 characteristics of the models in Figs. 2.30(c) and 2.31 gives

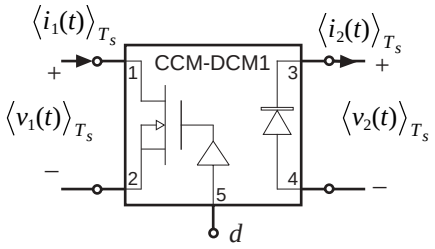


Fig. 2.32 Implementation of the combined CCM/DCM averaged switch model.

```
**********************************************************************
* MODEL: CCM-DCM1
* Application: two-switch PWM converters, CCM or DCM
* Limitations: ideal switches, no transformer
**********************************************************************
* Parameters:
*      L = equivalent inductance for DCM
*      fs = switching frequency
**********************************************************************
* Nodes:
* 1: transistor positive (drain for an n-channel MOS)
* 2: transistor negative  (source for an n-channel MOS)
* 3: diode cathode
* 4: diode anode
* 5: duty cycle control input
**********************************************************************
.subckt CCM-DCM1 1  2  3  4  5
+ params: L=100u fs=1E5
Et 1 2 value={(1-v(u))*v(3,4)/v(u)}
Gd 4 3 value={(1-v(u))*i(Et)/v(u)}
Ga 0 a value={MAX(i(Et),0)}
Va a b
Ra b 0 1k
Eu u 0 table {MAX(v(5),
+ v(5)*v(5)/(v(5)*v(5)+2*L*fs*i(Va)/v(3,4)))} (0 0) (1 1)
.ends
**********************************************************************
```

exactly the same result for the effective switch conversion ratio in DCM.

The switch conversion ratio $\mu(t)$ can be considered a generalization of the duty cycle $d(t)$ of CCM switch networks. Based on this approach, models and results developed for converters in CCM can be used not only for DCM but also for other operating modes or even for other converter configurations by simply replacing the switch duty cycle $d(t)$ with the appropriate switch conversion ratio $\mu(t)$. For example, if $M(d)$ is the conversion ratio in CCM, then $M(\mu)$, with μ given by Eq. (2.31), is the conversion ratio in DCM. The switch conversion ratio in DCM depends on the averaged terminal voltage and current, as well as the switch duty cycle d through the effective resistance $R_e = 2L/d^2T_s$. If the converter is completely unloaded, then the average transistor current $\langle i_1(t)\rangle_{T_s}$ is zero, and the DCM switch conversion ratio becomes $\mu = 1$. As a result, the dc output voltage attains the maximum possible value $V = V_g M(1)$.

To construct a combined CCM/DCM averaged switch model based on the general averaged switch model of Fig. 2.31, it is necessary to specify which of the two expressions for the switch conversion ratio to use: Eq. (2.29), which is valid in CCM, or Eq. (2.31), which is valid in DCM. At the CCM/DCM boundary, these two expressions must give the same result, $\mu = d$. If the load current decreases further, the converter operates in DCM, the average switch current $\langle i_1(t)\rangle_{T_s}$ decreases, and the DCM switch conversion ratio in Eq. (2.31) becomes greater than the switch duty cycle d. We conclude that the correct value of the switch conversion ratio, which takes into account operation in CCM or DCM, is the larger of the two values computed using Eq. (2.29) and Eq. (2.31).

Figure 2.32 shows an implementation of the combined CCM/DCM model as a PSpice subcircuit CCM-DCM1. This subcircuit has the same five interface nodes as the subcircuits CCM1 and CCM2 of Section B.1. The controlled sources E_t and G_d model the port 1 (transistor) and port 2 (diode) averaged characteristics, as shown in Fig. 2.31. The switch conversion ratio μ is equal to the voltage v(u) at the subcircuit node u. The controlled voltage source E_u computes the switch conversion ratio as the greater of the two values obtained from Eqs. (2.29) and (2.31). The controlled current source G_a, the zero-value

voltage source V_a, and the resistor R_a form an auxiliary circuit to ensure that the solution found by the simulator has the transistor and the diode currents with correct polarities, $\langle i_1(t)\rangle_{T_s} > 0$, $\langle i_2(t)\rangle_{T_s} > 0$. The subcircuit parameters are the inductance L relevant for CCM/DCM operation, and the switching frequency f_s. The default values in the subcircuit are arbitrarily set to $L = 100$ μH and $f_s = 100$ kHz.

The PSpice subcircuit CCM-DCM1 of Fig. 2.32 can be used for dc, ac, and transient simulations of PWM converters containing a transistor switch and a diode switch. This subcircuit is included in the model library *switch.lib*. It can be modified further for use in converters with isolation transformer.

2.4.6 Example: SEPIC Frequency Responses

As an example, Fig. 2.33 shows a SEPIC circuit and the averaged circuit model obtained by replacing the switch network with the CCM-DCM1 subcircuit of Fig. 2.32. A part of the circuit netlist is included in Fig. 2.33. The connections and the parameters of the CCM-DCM1 subcircuit are defined by the X_{switch}

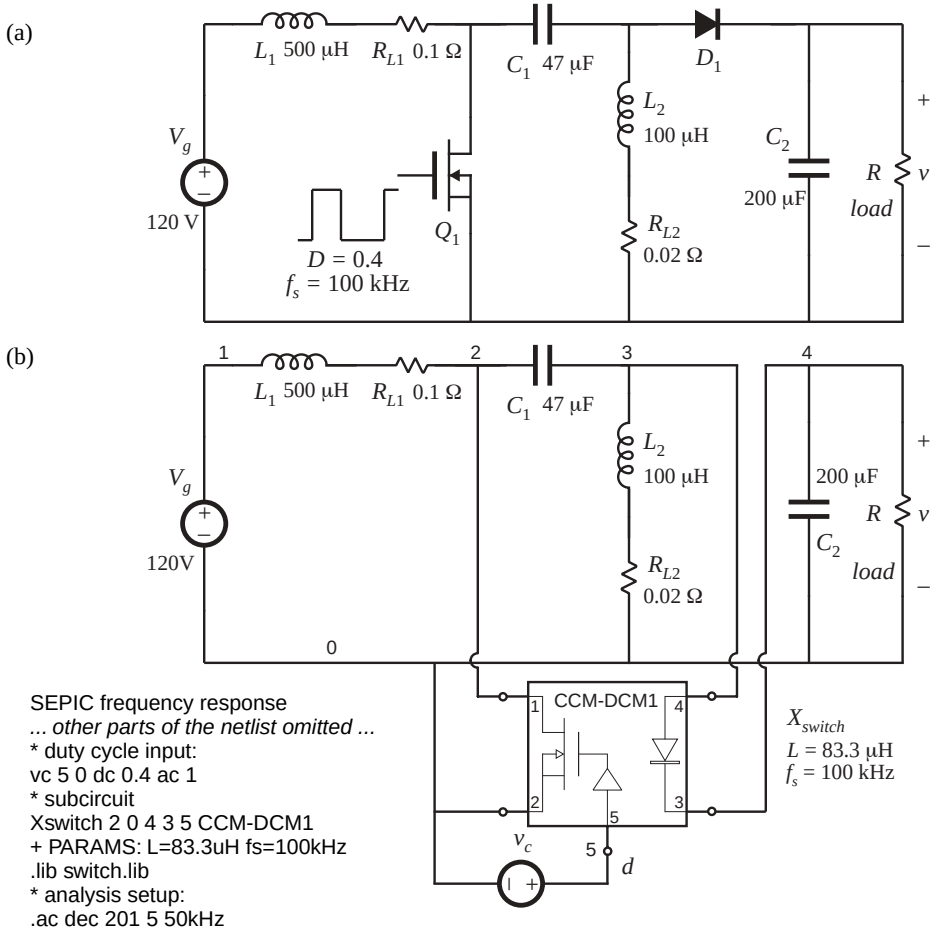


Fig. 2.33 SEPIC simulation example: (a) converter circuit, (b) averaged circuit model for simulation.

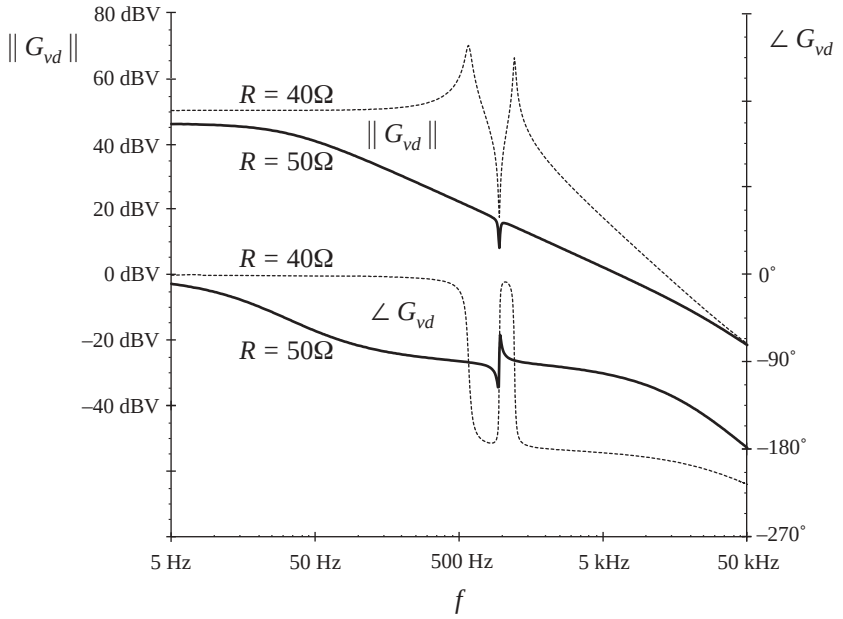


Fig. 2.34 Magnitude and phase responses of the control-to-output transfer function obtained by simulation of the SEPIC example, for two values of the load resistance. For R = 50 Ω, the converter operates in DCM (solid lines), and for R = 40 Ω, the converter operates in CCM (dotted lines).

line. In the SEPIC, the inductance parameter L = 83.3 μH is equal to the parallel combination of L_1 and L_2. The voltage source v_c sets the quiescent value of the duty cycle to D = 0.4, and the small-signal ac value to $\hat{d}$ = 1. Ac simulation is performed on a linearized circuit model, so that amplitudes of all small-signal ac waveforms are directly proportional to the amplitude of the ac input, regardless of the input ac amplitude value. For example, the control-to-output transfer function is $G_{vd} = \hat{v}/\hat{d}$, where $\hat{v} = v(4)$ in the circuit of Fig. 2.33(b). We can set the input ac amplitude to 1, so that the control-to-output transfer function G_{vd} can be measured directly as $v(5)$. This setup is just for convenience in finding small-signal frequency responses by simulation. For measurements of converter transfer functions in an experimental circuit (see Section 8.5), the actual amplitude of the small-signal ac variation $\hat{d}$ would be set to a fraction of the quiescent duty cycle D. Parameters of the ac simulation are set by the .ac line in the netlist: the signal frequency is swept from the minimum frequency of 5 Hz to the maximum frequency of 50 kHz in 201 points per decade.

Figure 2.34 shows magnitude and phase responses of the control-to-output transfer function obtained by ac simulations for two different values of the load resistance: R = 40 Ω, for which the converter operates in CCM, and R = 50 Ω, for which the converter operates in DCM. For these two operating points, the quiescent (dc) voltages and currents in the circuit are nearly the same. Nevertheless, the frequency responses are qualitatively very different in the two operating modes. In CCM, the converter exhibits a fourth-order response with two pairs of high-Q complex-conjugate poles and a pair of complex-conjugate zeros. Another RHP (right-half plane) zero can be observed at frequencies approaching 50 kHz. In DCM, there is a dominant low-frequency pole followed by a pair of complex-conjugate poles and a pair of complex-conjugate zeros. The frequencies of the complex poles and zeros are very close in value. A high-frequency pole and a RHP zero contribute additional phase lag at higher frequencies.

In the design of a feedback controller around a converter that may operate in CCM or in DCM,

one should take into account that the crossover frequency, the phase margin, and the closed-loop responses can be substantially different depending on the operating mode. This point is illustrated by the example of the next section.

2.4.7 Example: Loop Gain and Closed-Loop Responses of a Buck Voltage Regulator

A controller design for a buck converter example is discussed in Section 9.5.4. The converter and the block diagram of the controller are shown in Fig. 9.22. This converter system is designed to regulate the dc output voltage at $V = 15$ V for the load current up to 5 A. Let us test this design by simulation. An averaged circuit model of a practical realization of the buck voltage regulator described in Section 9.5.4 is shown in Fig. 2.35. The MOSFET and the diode switch are replaced by the averaged switch model implemented as the CCM-DCM1 subcircuit. The pulse-width modulator with $V_M = 4$ V is modeled according to the discussion in Section 7.6 as a dependent voltage source E_{pwm} controlled by the PWM input voltage v_x. The value of E_{pwm} is equal to $1/V_M = 0.25$ times the PWM input voltage v_x, with a limit for the minimum value set to 0.1 V, and a limit for the maximum value set to 0.9 V. The output of the pulse-width modulator is the control duty-cycle input to the CCM-DCM1 averaged switch subcircuit. Given the specified limits for E_{pwm}, the switch duty cycle $d(t)$ can take values in the range:

$$D_{\min} \le d(t) \le D_{\max} \tag{2.32}$$

where $D_{min} = 0.1$, and $D_{max} = 0.9$. Practical PWM integrated circuits often have a limit $D_{max} < 1$ for the maximum possible duty cycle. The voltage sensor and the compensator are implemented around an op-amp LM324. With very large loop gain in the system, the steady-state error voltage is approximately

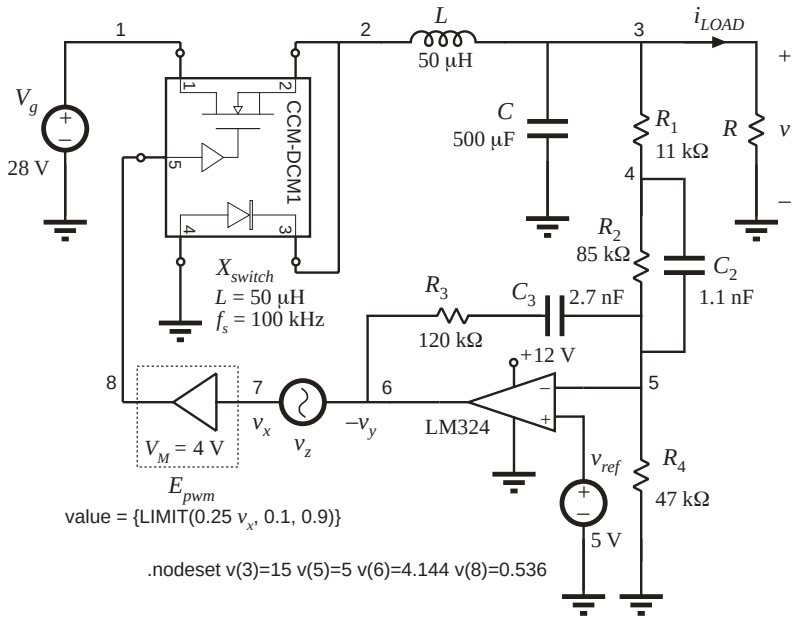


Fig. 2.35 Buck voltage regulator example.

zero, i.e., the dc voltages at the plus and the minus inputs of the op-amp are almost the same,

$$v(5) = v_{ref} \tag{2.33}$$

As a result, the quiescent (dc) output voltage V is set by the reference voltage v_{ref} and the voltage divider comprised of R_1, R_2, R_4:

$$V \frac{R_4}{R_1 + R_2 + R_4} = v_{ref} = 5 \text{ V} \tag{2.34}$$

By setting the ac reference voltage $\hat{v}_{ref}$ to zero, the combined transfer function of the voltage sensor and the compensator can be found as:

$$H(s)G_c(s) = \frac{\hat{v}_y}{\hat{v}} = \frac{R_3 + \dfrac{1}{sC_3}}{R_1 + R_2 \parallel \dfrac{1}{sC_2}} \tag{2.35}$$

This transfer function can be written in factored pole-zero form as

$$G_{cm}H \frac{\left(1 + \dfrac{s}{\omega_z}\right)\left(1 + \dfrac{\omega_L}{s}\right)}{\left(1 + \dfrac{s}{\omega_p}\right)} \tag{2.36}$$

where

$$G_{cm}H = \frac{R_3}{R_1 + R_2} \tag{2.37}$$

$$f_z = \frac{\omega_z}{2\pi} = \frac{1}{2\pi R_2 C_2} \tag{2.38}$$

$$f_L = \frac{\omega_L}{2\pi} = \frac{1}{2\pi R_3 C_3} \tag{2.39}$$

and

$$f_p = \frac{\omega_p}{2\pi} = \frac{1}{2\pi\left(R_1 \parallel R_2\right)C_2} \tag{2.40}$$

The design described in Section 9.5.4 resulted in the following values for the gain and the corner frequencies:

$$G_{cm}H = 3.7\ (1 / 3)\ = 1.23,\ \ f_z = 1.7 \text{ kHz},\ \ f_L = 500 \text{ Hz},\ \ f_p = 14.5 \text{ kHz} \tag{2.41}$$

Eqs. (2.34) and (2.37) to (2.41) can be used to select the circuit parameter values. Let us (somewhat arbitrarily) choose C_2 = 1.1 nF. Then, from Eq. (2.38), we have R_2 = 85 kΩ, and Eq. (2.40) yields R_1 = 11 kΩ. From Eq. (2.37) we obtain R_3 = 120 kΩ, and Eq. (2.39) gives C_3 = 2.7 kΩ. Finally, R_4 = 47 kΩ is found from Eq. (2.34). The voltage regulator design can now be tested by simulations of

the circuit in Fig. 2.35.

Loop gains can be obtained by simulation through injection techniques. An ac voltage source v_z is injected between the compensator output and the PWM input. This is a good injection point since the output impedance of the compensator built around the op-amp is small, and the PWM input impedance is very large (infinity in the circuit model of Fig. 2.35). With the ac source amplitude set (arbitrarily) to 1, and no other ac sources in the circuit, ac simulations are performed to find the loop gain as

$$T(s) = \frac{\hat{v}_y}{\hat{v}_x} = -\frac{v(6)}{v(7)} \tag{2.42}$$

To perform ac analysis, the simulator first solves for the quiescent (dc) operating point. The circuit is then linearized at this operating point, and small-signal frequency responses are computed for the specified range of signal frequencies. Solving for the quiescent operating point involves numerical solution of a system of nonlinear equations. In some cases, the numerical solution does not converge and the simulation is aborted with an error message. In particular, convergence problems often occur in circuits with feedback, especially when the loop gain at dc is very large. This is the case in the circuit of Fig. 2.35. To help convergence when the simulator is solving for the quiescent operating point, one can specify approximate or expected values of node voltages using the .nodeset line as shown in Fig. 2.35. In this case, we know by design that the quiescent output voltage is close to 15 V ($v(3) = 15$), that the negative input of the op-amp is very close to the reference ($v(5) = 5$), and that the quiescent duty cycle is approximately $D = V/V_g = 0.536$, so that $v(8) = 0.536$ V. Given these approximate node voltages, the numerical solution converges, and the following quiescent operating points are found by the simulator for two values of the load resistance R:

$$R = 3\ \Omega,\ v(3) = 15.2\ \text{V},\ v(5) = 5.0\ \text{V},\ v(7) = 2.173\ \text{V},\ v(8) = 0.543\ \text{V},\ D = 0.543 \tag{2.43}$$

$$R = 25\ \Omega,\ v(3) = 15.2\ \text{V},\ v(5) = 5.0\ \text{V},\ v(7) = 2.033\ \text{V},\ v(8) = 0.508\ \text{V},\ D = 0.508 \tag{2.44}$$

For the nominal load resistance $R = 3\ \Omega$, the converter operates in CCM, so that $D = V/V_g$. For $R = 25\ \Omega$, the same dc output voltage is obtained for a lower value of the quiescent duty cycle, which means that the converter operates in DCM.

The magnitude and phase responses of the loop gain found for the operating points given by Eqs. (2.43) and (2.44) are shown in Fig. 2.36. For $R = 3\ \Omega$, the crossover frequency is $f_c = 5.3$ kHz, and the phase margin is $\phi_M = 47^\circ$, very close to the values ($f_c = 5$ kHz, $\phi_M = 52^\circ$) that we designed for in Section 9.5.4. At light load, for $R = 25\ \Omega$, the loop gain responses are considerably different because the converter operates in DCM. The crossover frequency drops to $f_c = 390$ Hz, while the phase margin is $\phi_M = 55^\circ$.

The magnitude responses of the line-to-output transfer function are shown in Fig. 2.37, again for two values of the load resistance, $R = 3\ \Omega$ and $R = 25\ \Omega$. The open-loop responses are obtained by braking the feedback loop at node 8, and setting the dc voltage at this node to the quiescent value D of the duty cycle. For $R = 3\ \Omega$, the open-loop and closed-loop responses can be compared to the theoretical plots shown in Fig. 9.32. At 100 Hz, the closed-loop magnitude response is $0.012 \Rightarrow -38$ dB. A 1 V, 100 Hz variation in $v_g(t)$ would induce a 12 mV variation in the output voltage $v(t)$. For $R = 25\ \Omega$, the closed loop magnitude response is $0.02 \Rightarrow -34$ dB, which means that the 1 V, 100 Hz variation in $v_g(t)$ would induce a 20 mV variation in the output voltage. Notice how the regulator performance in terms of rejecting the input voltage disturbance is significantly worse at light load than at the nominal load.

A test of the transient response to a step change in load is shown in Fig. 2.38. The load current is initially equal to 1.5 A, and increases to $i_{LOAD} = 5$ A at $t = 0.1$ ms. When the converter is operated in

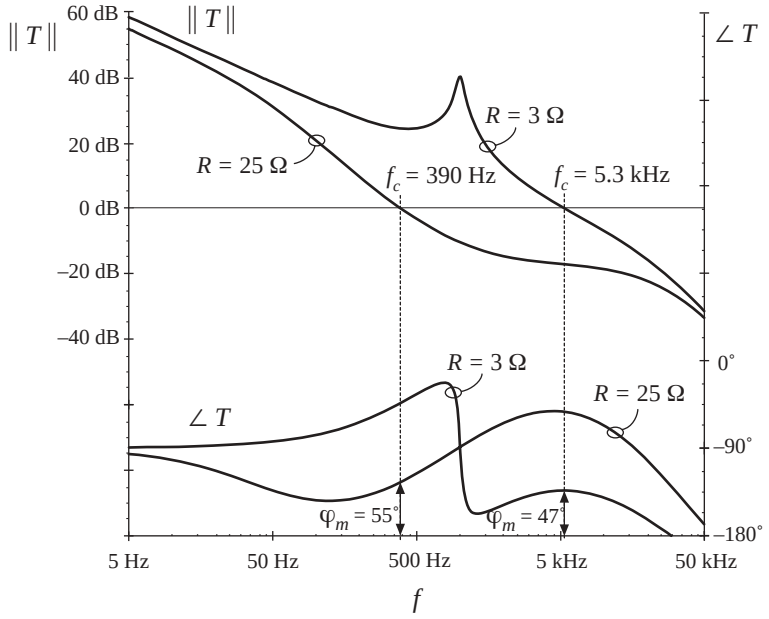


Fig. 2.36 Loop gain in the buck voltage regulator example.

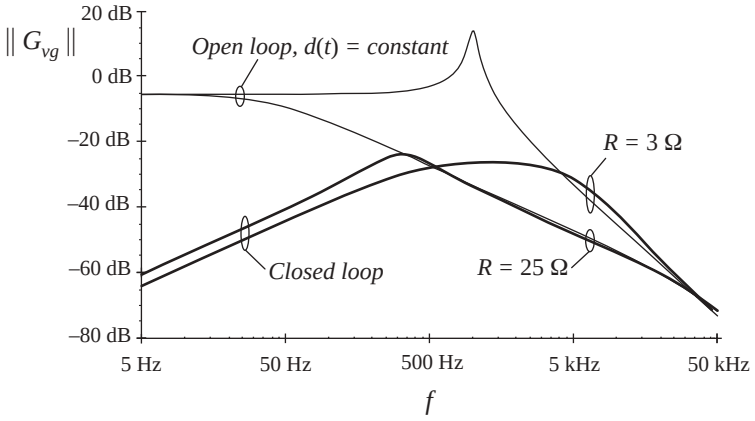


Fig. 2.37 Line to output response of the buck voltage regulator.

open loop at constant duty cycle, the response is governed by the natural time constants of the converter network. A large undershoot and long lightly-damped oscillations can be observed in the output voltage. With the feedback loop closed, the controller dynamically adjusts the duty cycle $d(t)$ trying to maintain the output voltage constant. The output voltage drops by about 0.2 V, and it returns to the regulated value after a short, well-damped transient.

The voltage regulator example of Fig. 2.35 illustrates how the performance can vary significantly if the regulator is expected to supply a wide range of loads. In practice, further tests would also be performed to account for expected ranges of input voltages, and variations in component parameter values. Design iterations may be necessary to ensure that performance specifications are met under worst case conditions.

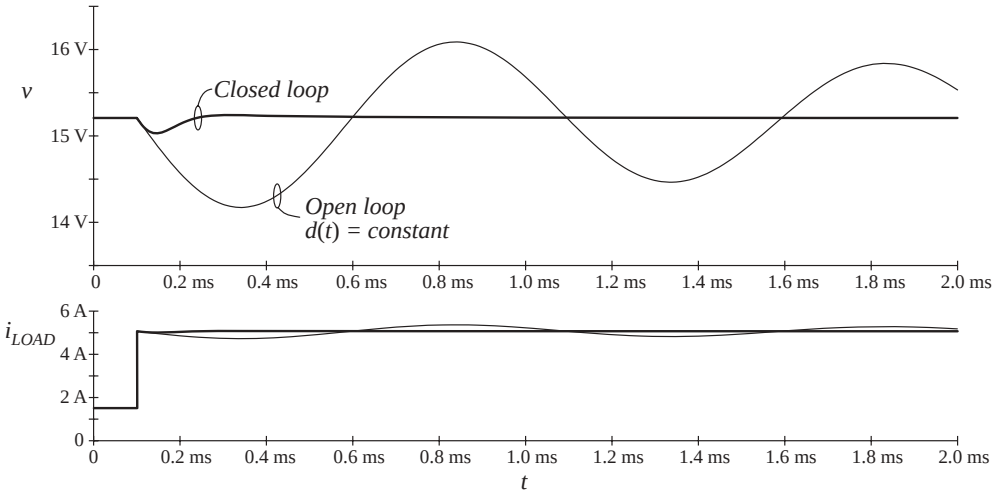


Fig. 2.38 Load transient response of the buck voltage regulator example.

2.5 MEASUREMENT OF AC TRANSFER FUNCTIONS AND IMPEDANCES

It is good engineering practice to measure the transfer functions of prototype converters and converter systems. Such an exercise can verify that the system has been correctly modeled and designed. Also, it is often useful to characterize individual circuit elements through measurement of their terminal impedances.

Small-signal ac magnitude and phase measurements can be made using an instrument known as a network analyzer, or frequency response analyzer. The key inputs and outputs of a basic network analyzer are illustrated in Fig. 2.39. The network analyzer provides a sinusoidal output voltage $\hat{v}_z$ of controllable amplitude and frequency. This signal can be injected into the system to be measured, at any desired location. The network analyzer also has two (or more) inputs, $\hat{v}_x$ and $\hat{v}_y$. The return electrodes of $\hat{v}_z$, $\hat{v}_y$, and $\hat{v}_x$ are internally connected to earth ground. The network analyzer performs the function of a narrowband tracking voltmeter: it measures the components of $\hat{v}_x$ and $\hat{v}_y$ at the injection frequency, and displays the magnitude and phase of the quantity $\hat{v}_y/\hat{v}_x$. The narrowband tracking voltmeter feature is essential for switching converter measurements; otherwise, switching ripple and noise corrupt the desired sinusoidal signals and make accurate measurements impossible. Modern network analyzers can automatically sweep the frequency of the injection source $\hat{v}_z$ to generate magnitude and phase Bode plots of the transfer function $\hat{v}_y/\hat{v}_x$.

A typical test setup for measuring the transfer function of an amplifier is illustrated in Fig. 2.40. A potentiometer, connected between a dc supply voltage V_{CC} and ground, is used to bias the amplifier input to attain the correct quiescent operating point. The injection source voltage $\hat{v}_z$ is coupled to the amplifier input terminals via a dc blocking capacitor. This blocking capacitor prevents the injection voltage source from upsetting the dc bias. The network analyzer inputs $\hat{v}_x$ and $\hat{v}_y$ are connected to the input and output terminals of the amplifier. Hence, the measured transfer function is

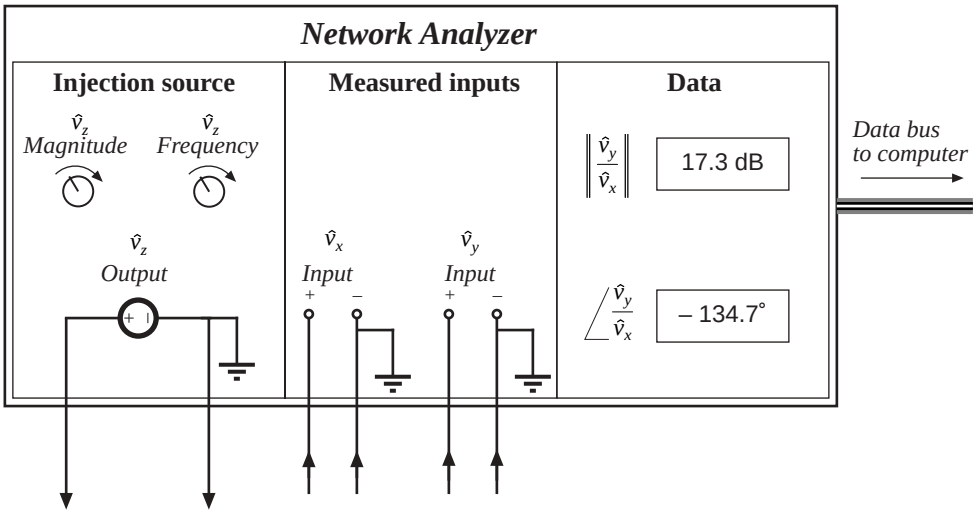


Fig. 2.39 Key features and functions of a network analyzer: sinusoidal source of controllable amplitude and frequency, two inputs, and determination of relative magnitude and phase of the input components at the injection frequency.

$$\frac{\hat{v}_y(s)}{\hat{v}_x(s)} = G(s) \tag{2.45}$$

Note that the blocking capacitance, bias potentiometer, and $\hat{v}_z$ amplitude have no effect on the measured transfer function

An impedance

$$Z(s) = \frac{\hat{v}(s)}{\hat{i}(s)} \tag{2.46}$$

can be measured by treating the impedance as a transfer function from current to voltage. For example, measurement of the output impedance of an amplifier is illustrated in Fig. 2.41. The quiescent operating condition is again established by a potentiometer which biases the amplifier input. The injection source $\hat{v}_z$ is coupled to the amplifier output through a dc blocking capacitor. The injection source voltage $\hat{v}_z$ excites a current $\hat{i}_{out}$ in impedance Z_s. This current flows into the output of the amplifier, and excites a voltage across the amplifier output impedance:

$$Z_{out}(s) = \left.\frac{\hat{v}_y(s)}{\hat{i}_{out}(s)}\right|_{\substack{amplifier \\ ac\ input}=0} \tag{2.47}$$

A current probe is used to measure $\hat{i}_{out}$. The current probe produces a voltage proportional to $\hat{i}_{out}$; this voltage is connected to the network analyzer input $\hat{v}_x$. A voltage probe is used to measure the amplifier output voltage $\hat{v}_y$. The network analyzer displays the transfer function $\hat{v}_y/\hat{v}_x$, which is proportional to Z_{out}. Note that the value of Z_s and the amplitude of $\hat{v}_z$ do not affect the measurement of Z_{out}.

In power applications, it is sometimes necessary to measure impedances that are very small in magnitude. Grounding problems cause the test setup of Fig. 2.41 to fail in such cases. The reason is

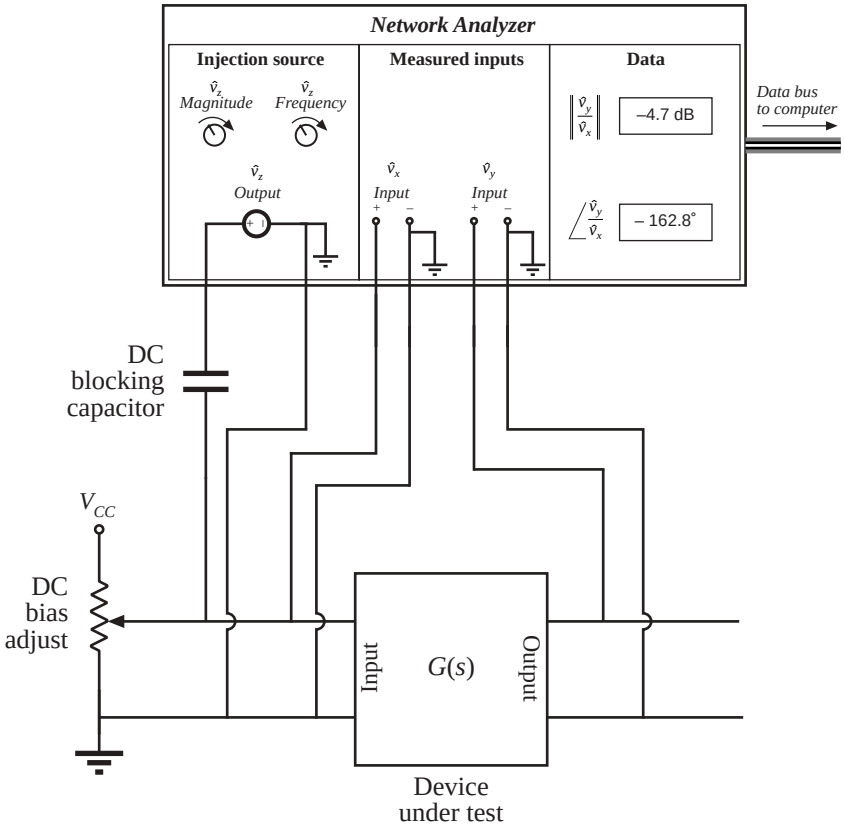


Fig. 2.40 Measurement of a transfer function.

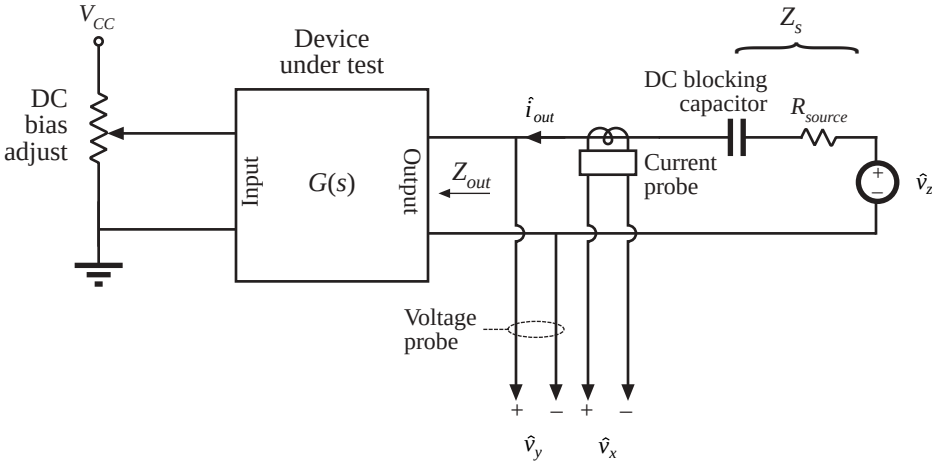


Fig. 2.41 Measurement of the output impedance of a circuit.

illustrated in Fig. 2.42(a). Since the return connections of the injection source $\hat{v}_z$ and the analyzer input $\hat{v}_y$ are both connected to earth ground, the injected current $\hat{i}_{out}$ can return to the source through the return connections of either the injection source or the voltage probe. In practice, $\hat{i}_{out}$ divides between the two paths according to their relative impedances. Hence, a significant current $(1 - k)\,\hat{i}_{out}$ flows through the return connection of the voltage probe. If the voltage probe return connection has some total contact and wiring impedance Z_{probe}, then the current induces a voltage drop $(1 - k)\hat{i}_{out}Z_{probe}$ in the voltage probe wiring, as illustrated in Fig. 2.42(a). Hence, the network analyzer does not correctly measure the voltage drop across the impedance Z. If the internal ground connections of the network analyzer have negligible impedance, then the network analyzer will display the following impedance:

$$Z + (1 - k)Z_{probe} = Z + Z_{probe} \| Z_{rz} \tag{2.48}$$

Here, Z_{rz} is the impedance of the injection source return connection. So to obtain an accurate measurement, the following condition must be satisfied:

$$\| Z \| \gg \left\| \left(Z_{probe} \| Z_{rz} \right) \right\| \tag{2.49}$$

A typical lower limit on $\| Z \|$ is a few tens or hundreds of milliohms.

An improved test setup for measurement of small impedances is illustrated in Fig. 2.42(b). An isolation transformer is inserted between the injection source and the dc blocking capacitor. The return connections of the voltage probe and injection source are no longer in parallel, and the injected current $\hat{i}_{out}$ must now return entirely through the injection source return connection. An added benefit is that the transformer turns ratio n can be increased, to better match the injection source impedance to the impedance under test. Note that the impedances of the transformer, of the blocking capacitor, and of the probe and injection source return connections, do not affect the measurement. Much smaller impedances can therefore be measured using this improved approach.

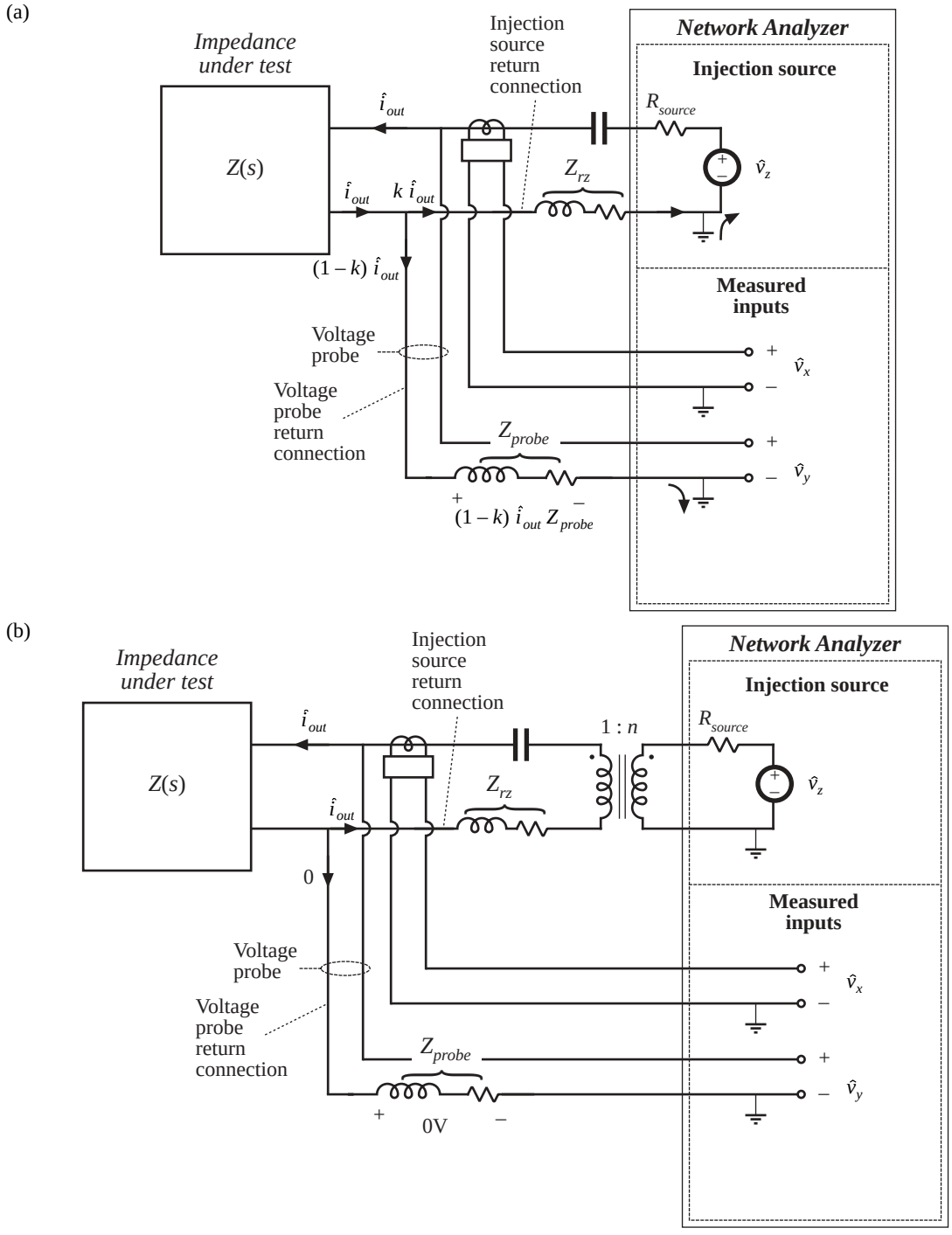


Fig. 2.42 Measurement of a small impedance $Z(s)$: (a) current flowing in the return connection of the voltage probe induces a voltage drop that corrupts the measurement; (b) an improved experiment, incorporating isolation of the injection source.