Simulation Modeling

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Circuit Simulation

- LTSpice
  - Other tools accepted, but not supported
- Choose model type (switching, averaged, dynamic)
- Supplement analytical work rather than repeating it
- Show results which clearly demonstrate what matches and what does not with respect to experiments (i.e. ringing, slopes, etc.)

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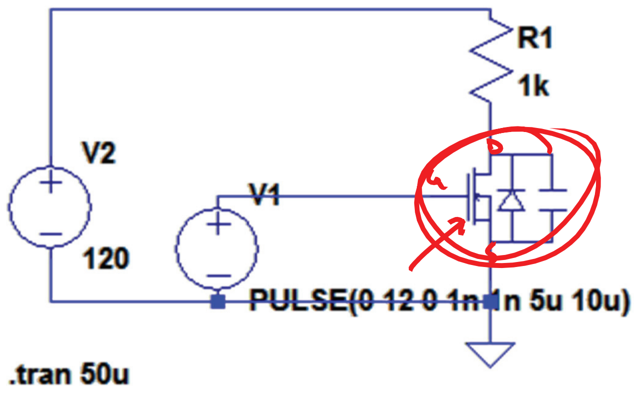
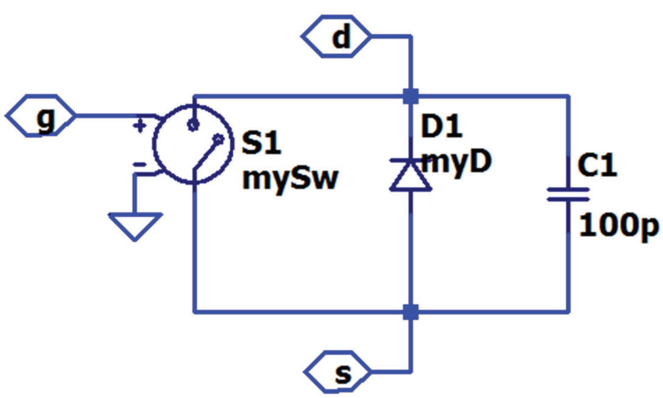
LTSpice Modeling Examples



- Example files added to course materials page
  - Custom model
  - VDMOS model
  - Manufacturer Model

Custom Transistor Model

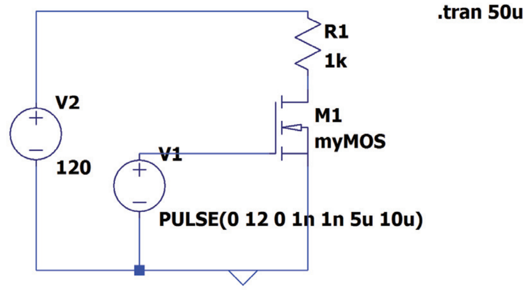
.model myD D(n=.001)
.model mySw SW(Ron=10m Roff=1G Von=1 Voff = .5)



VDMOS Model

Name	Description	Units	Default	Example
Vto	Threshold voltage	V	0	1.0
Kp	Transconductance parameter	A/V^2	1.	.5
Phi	Surface inversion potential	V	0.6	0.65
Lambda	Channel-length modulation	1/V	0.	0.02
mtriode	Conductance multiplier in triode region(allows independent fit of triode and saturation regions	-	1.	2.
subthres	Current(per volt Vds) to switch from square law to exponential subthreshold conduction	A/V	0.	1n
BV	Vds breakdown voltage	V	Infin.	40
IBV	Current at Vds=BV	A	100pA	1u
NBV	Vds breakdown emission coefficient	-	1.	10
Rd	Drain ohmic resistance	Ω	0.	1.
Rs	Source ohmic resistance	Ω	0.	1.
Rg	Gate ohmic resistance	Ω	0.	2.
Rds	Drain-source shunt resistance	Ω	Infin.	10Meg
Rb	Body diode ohmic resistance	Ω	0.	.5
Cjo	Zero-bias body diode	F	0.	1n

.model myMOS VDMOS(nchan Rg=3 Rd=14m Rs=10m Vto=-.8 Kp=32
+ Cgdmax=.5n Cgdmin=.07n Cgs=.9n Cjo=.26n Is=26p Rb=17m)

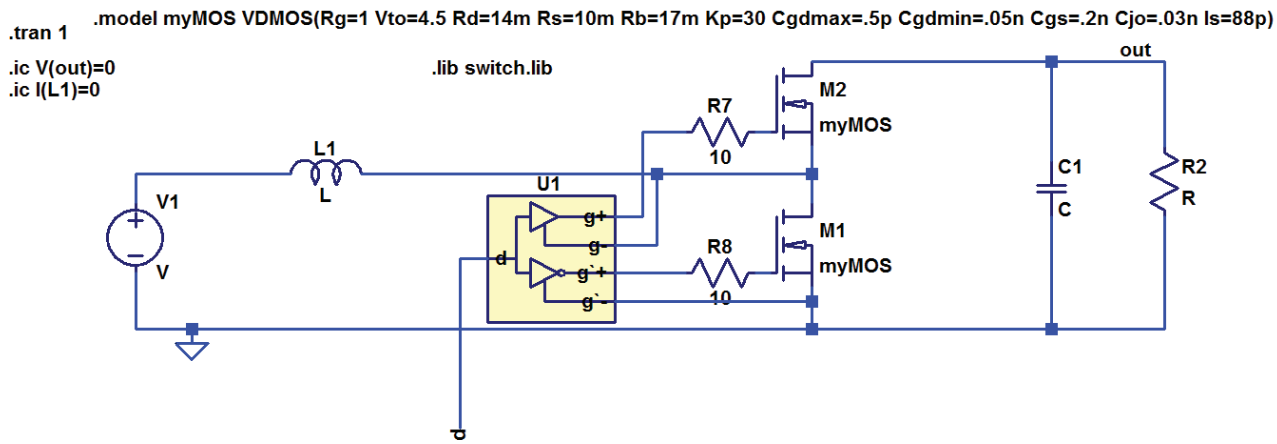


- Note: any other parameters **ignored**
  - E.g. ron = 3m Qg = 1n mfg = Infineon

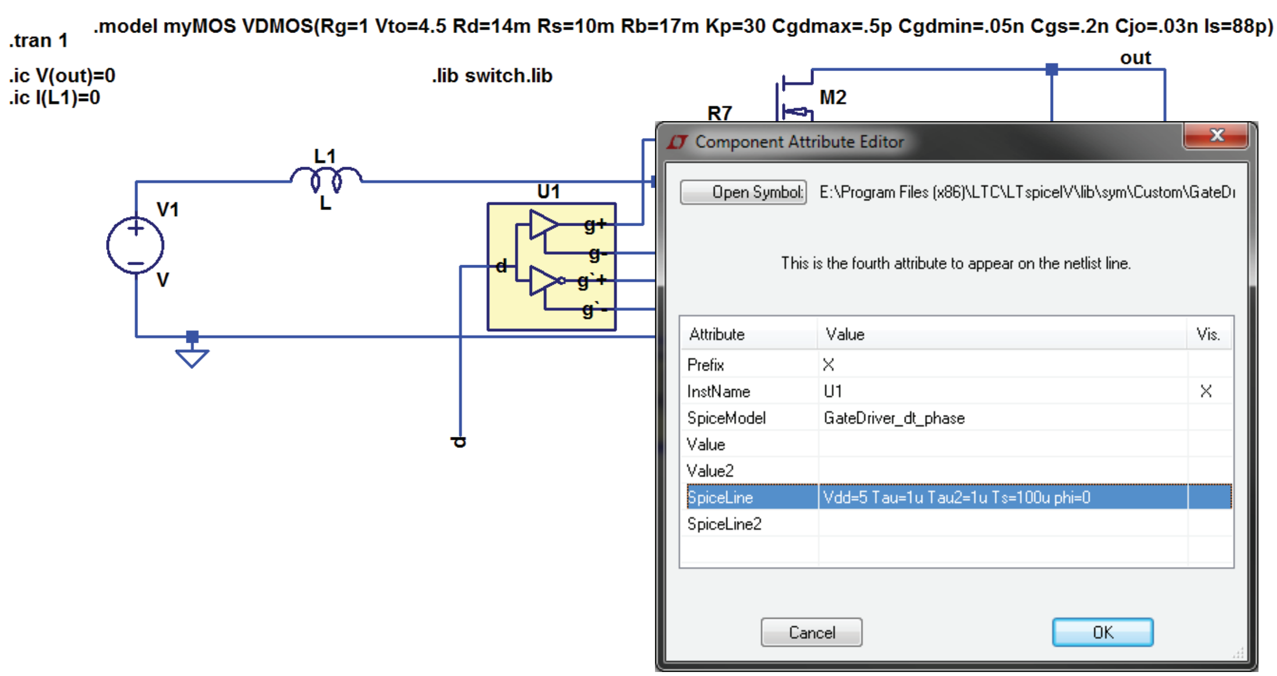
Manufacturer Device Model

- Text-only netlist model of device including additional parasitics and temperature effects
- May slow or stop simulation if timestep and accuracy are not adjusted appropriately

Full Switching Simulation



Full Switching Simulation



Experiment 2

Experiment 3

Experiment Procedure
- Prelab Assignment
- Experiment 3 Procedure

Experiment 3 Components
- Contents of the Experiment 3 Parts Kit
- Contents of the Magnetics Library
- Breakout Board Schematics and Layout (pdf)
- Breakout Board Schematics and PCB Layout (Altium)

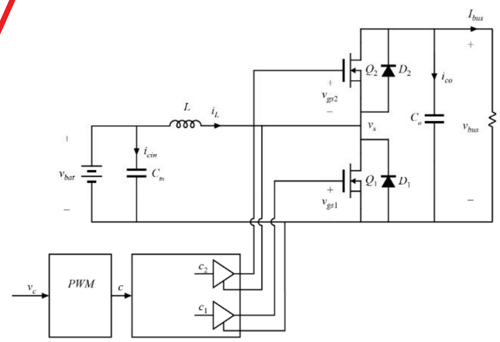
Reference Materials
- Designing Bootstrap Networks
- Power Converter Layout
- Reduction of Ringing in Power Converters (TI App. Note)
- RMS Values of Commonly Observed Waveforms

LTSpice Example Files
- Examples of power semiconductor modeling using custom or manufacturer models
- Example Switching and Averaged Boost LTSpice Models

Magnetics Design
- Filter Inductor Design Notes
- Kg Method Step-by-Step
- Kgfe Method Step-by-Step
- Overview of Empirical Core Loss Calculation Techniques
- Overview of Empirical State of Core Loss Prediction
- Magnetics Design Tables
- AWG Chart

Experiment 4

Available on Exp 3 Webpage



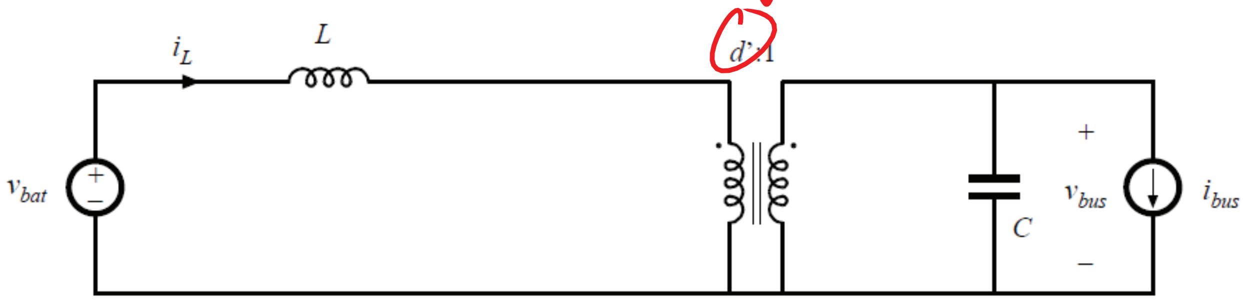
Full Switching Model

- Gives valuable insight into circuit operation
  - Understand expected waveforms
  - Identify discrepancies between predicted and experimental operation
- Slow to simulate; significant high frequency content
- Cannot perform AC analysis

Averaged Switch Modeling: Motivation

- A *large-signal, nonlinear* model of converter is difficult for hand analysis, but well suited to simulation across a wide range of operating points
- Want an *averaged* model to speed up simulation speed
- Also allows linearization (AC analysis) for control design

Nonlinear, Averaged Circuit



$d(t) \cdot v_{bus}(t)$

$$L\frac{d\langle i_L\rangle}{dt} = \langle v_{bat}\rangle - (1-d)\langle v_{bus}\rangle$$

$$C\frac{d\langle v_{bus}\rangle}{dt} = (1-d)\langle i_L\rangle - \langle i_{bus}\rangle$$

DC analysis

$\frac{dx}{dt} = \phi$

DC steady-state averaged behavior

AC analysis

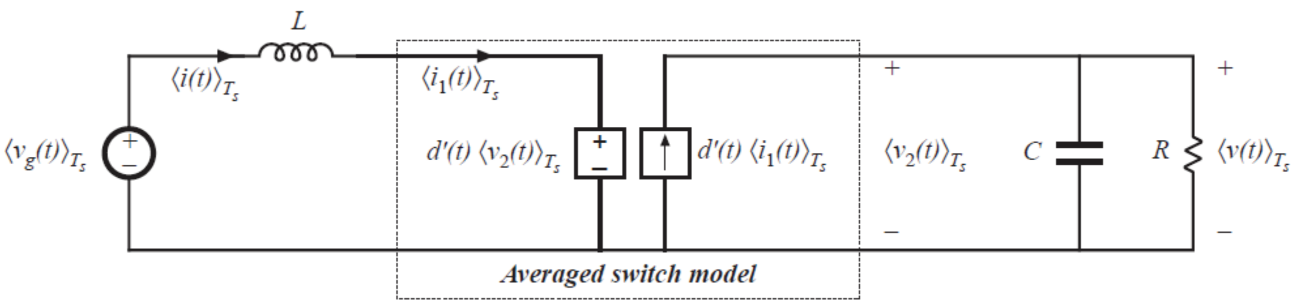
small-signal analysis

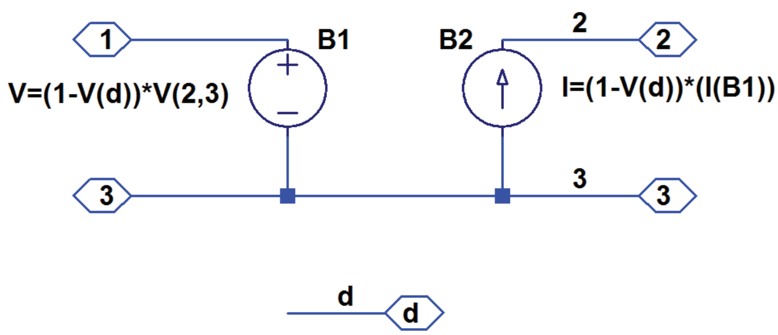
$x(t) = X + \hat{x}$

Averaged, linear small-signal equations

for simulating: no need to linearize.

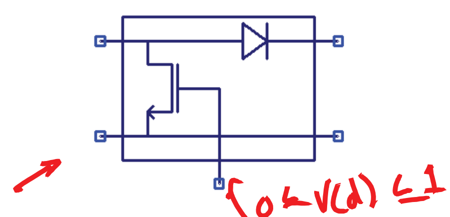
Implementation in LTSpice



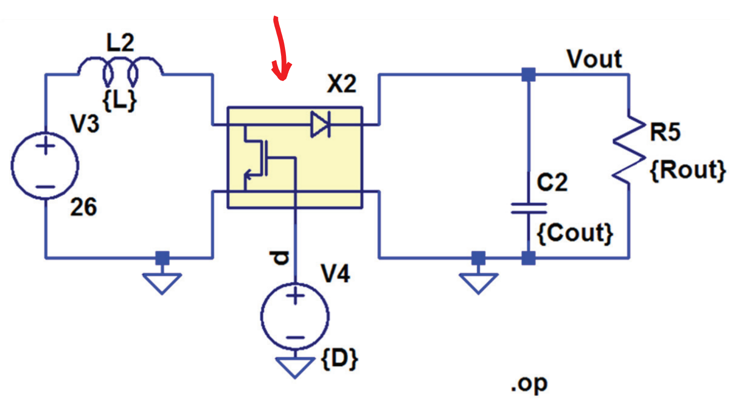


$$\langle v_1(t)\rangle_{T_s} = d'(t)\,\langle v_2(t)\rangle_{T_s}$$
$$\langle i_2(t)\rangle_{T_s} = d'(t)\,\langle i_1(t)\rangle_{T_s}$$

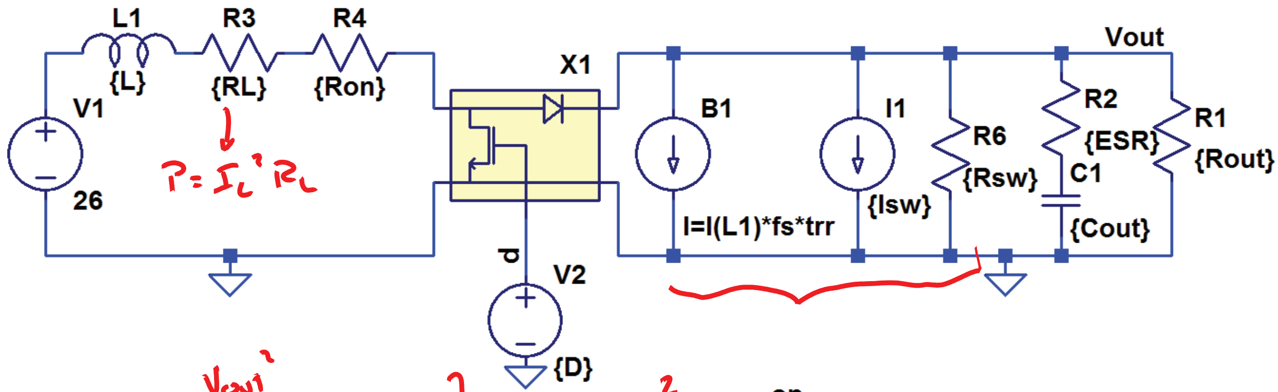
X1



Averaged Switch Model



Averaged Model With Losses



$$P_{R_{sw}} = \frac{V_{out}^2}{R_{sw}}$$

$$P_{C_{oss}} = \frac{1}{2} C_{oss} V_{out}^2 f_s$$

$$R_{sw} = \frac{2}{C_{oss} f_s}$$

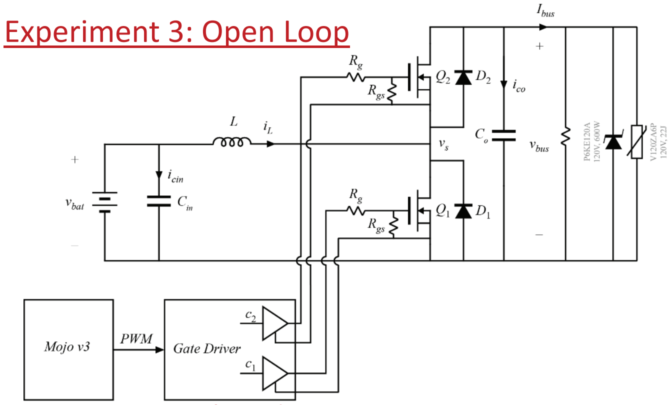
```
.op
.param Rout = 10
.step param Rout 10 100 10
```

What known error(s) will be present in loss predictions with this model?

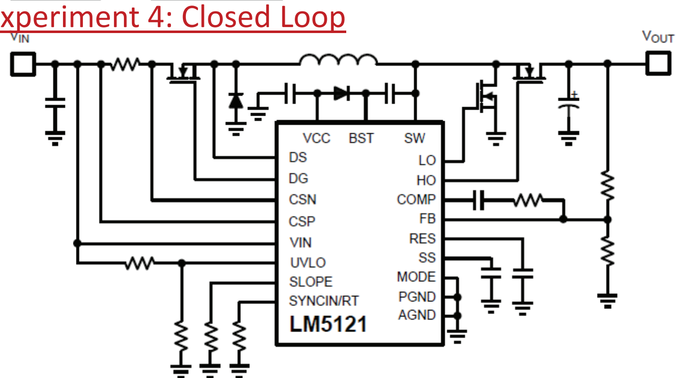
Experiment 4

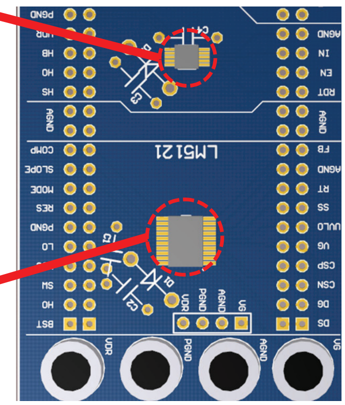
Experiment 4: Closed-Loop Boost

Experiment 3: Open Loop

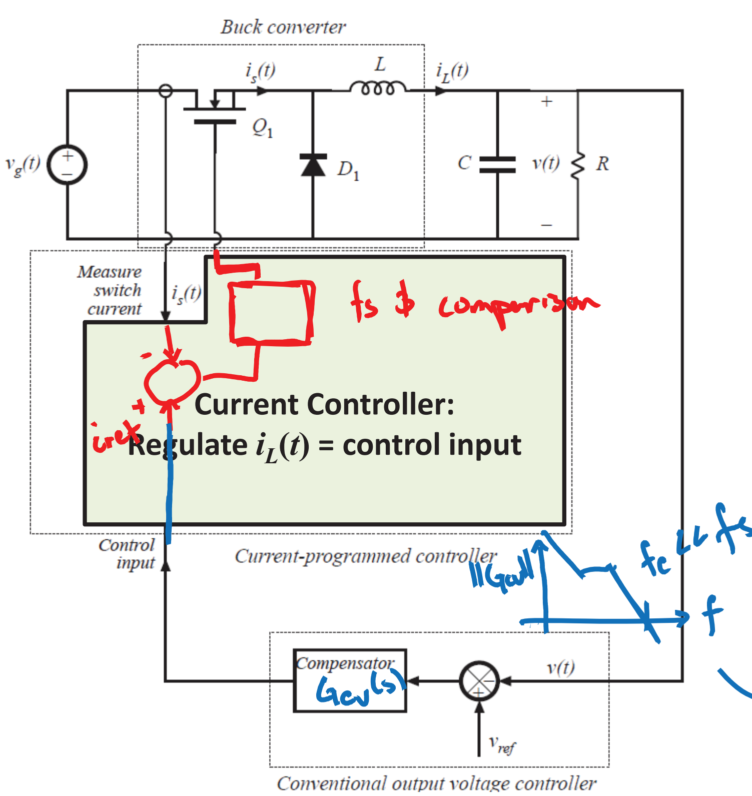


Experiment 4: Closed Loop





Current Control



Two control loops:

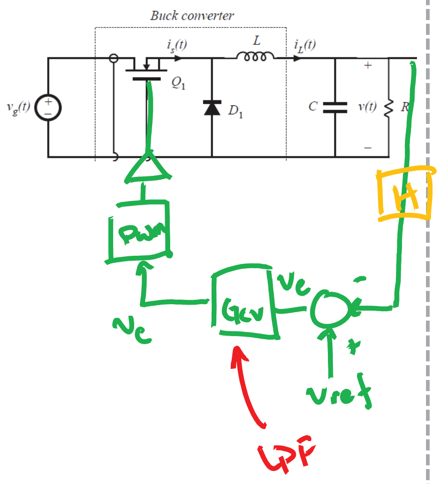
(1) Fast (inner) current loop control
- Not Averaged

(2) Slow (outer) voltage loop control
- Averaged

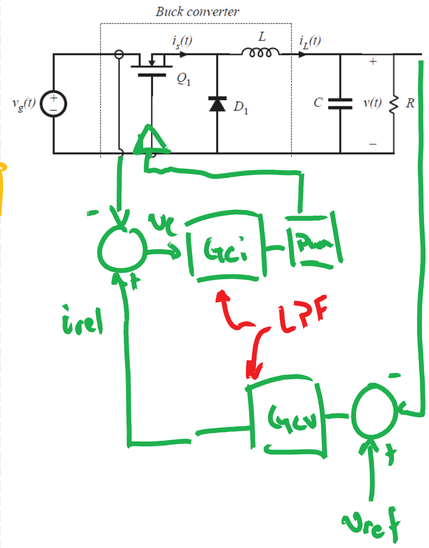
→ Effective low-pass filter averaged models can be used when fc << fs

Averaged vs CPM

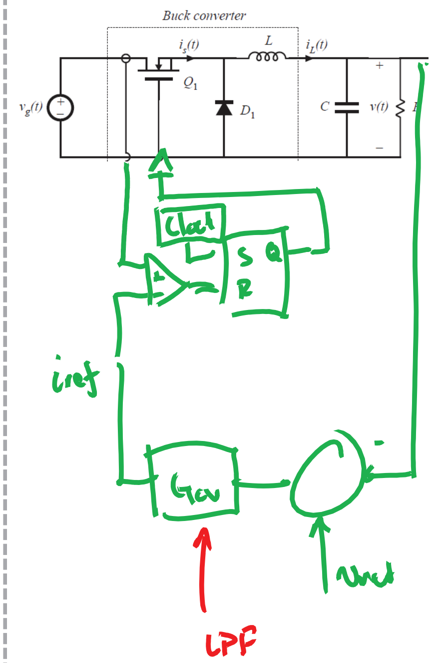
Voltage-Mode



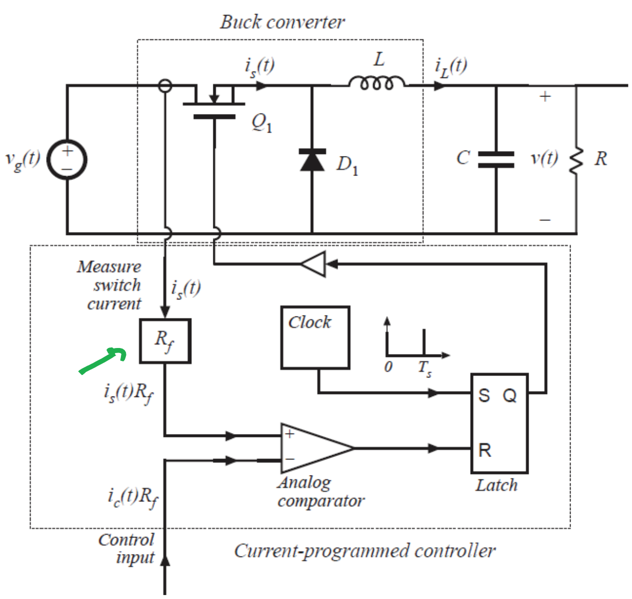
Averaged Current-Mode



Current Programmed Mode

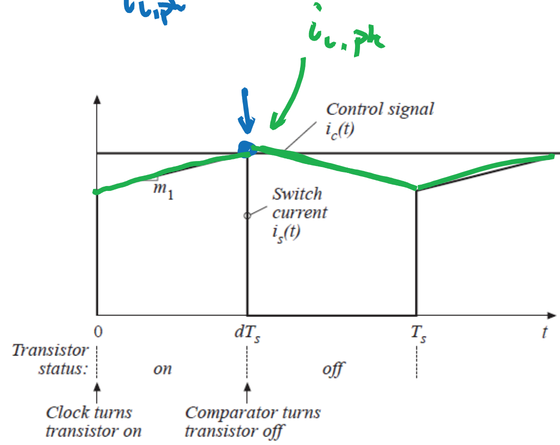


Current Programmed Control (CPM)

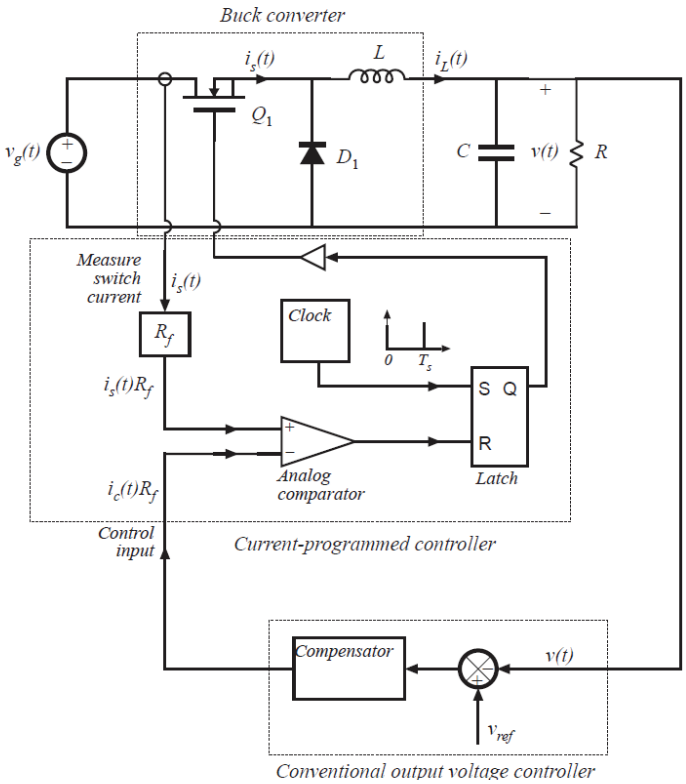


R_f → current-to-voltage gain of the sensing circuit

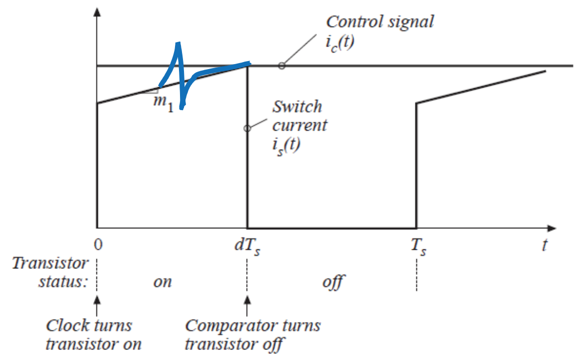
$i_{L,pk} = i_L(DT_s) = i_{ref}$ every period



CPM Voltage Loop



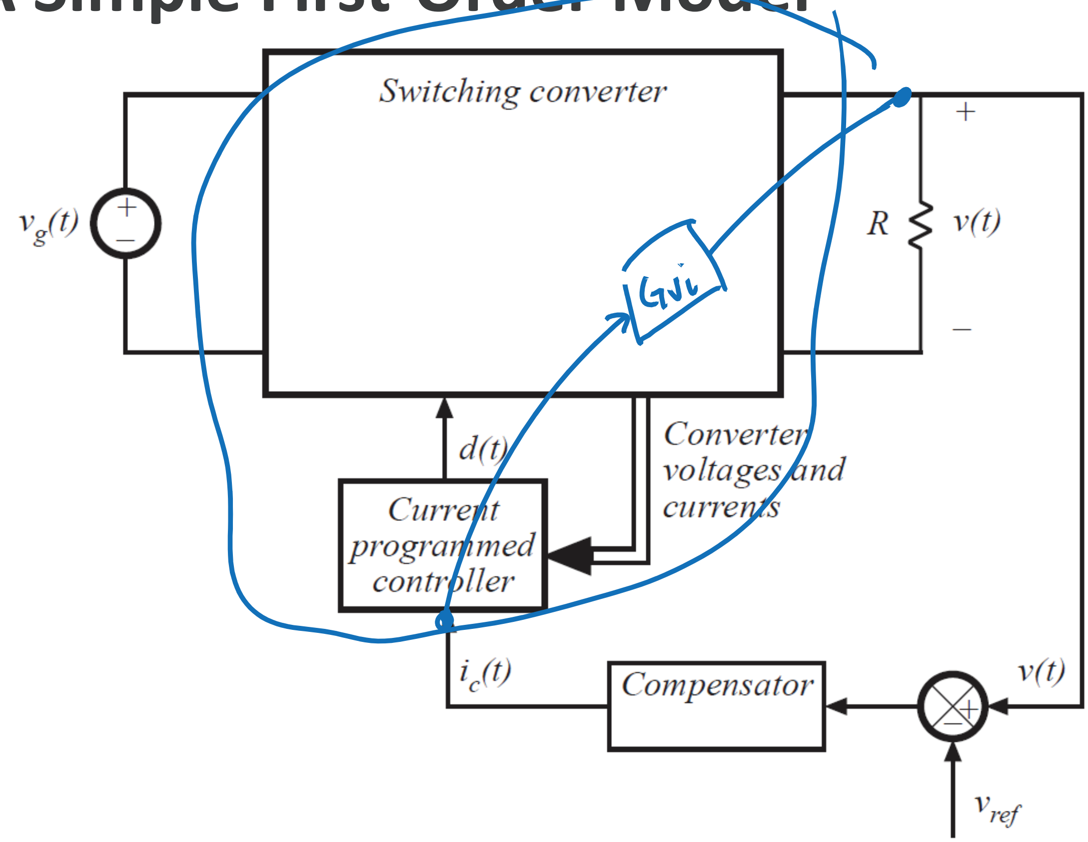
The peak transistor current replaces the duty cycle as the converter control input.



Current Programmed Control

- Covered in Ch. 12 of *Fundamentals of Power Electronics*
- Advantages of current programmed control:
  - Simpler dynamics —inductor pole is moved to high frequency
  - Simple robust output voltage control, with large phase margin, can be obtained without use of compensator lead networks
  - Transistor failures due to excessive current can be prevented simply by limiting $i_c(t)$
  - It is always necessary to sense the transistor current, to protect against overcurrent failures
  - Transformer saturation problems in bridge or push-pull converters can be mitigated
- A disadvantage: susceptibility to noise

A Simple First-Order Model



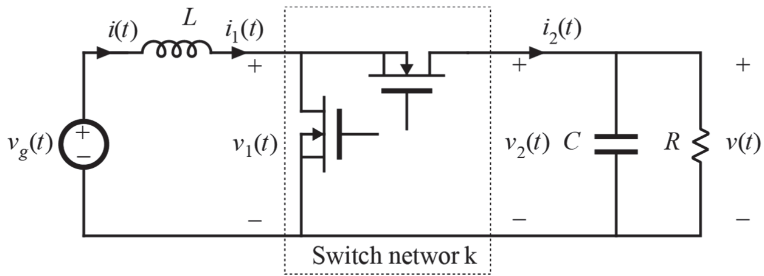
The First-Order Approximation

$$\left\langle i_L(t) \right\rangle_{T_s} = i_c(t)$$

- Neglects switching ripple
- Yields physical insight and simple first-order model
- Accurate when converter operates well into CCM (so that switching ripple is small
- Accurate when artificial ramp (discussed later) is small
- Resulting small-signal relation:

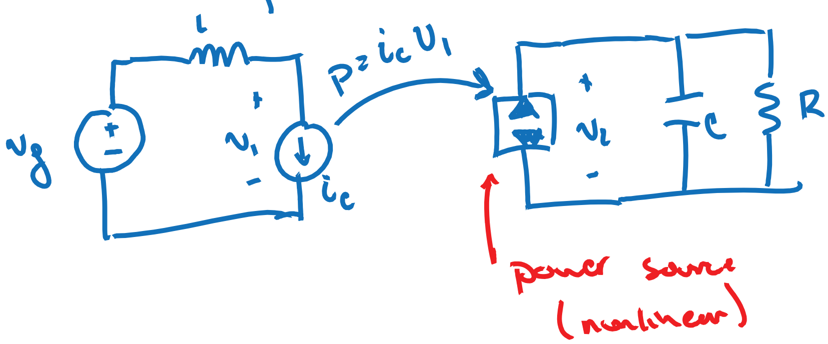
$$i_L(s) \approx i_c(s)$$

Averaged Modeling

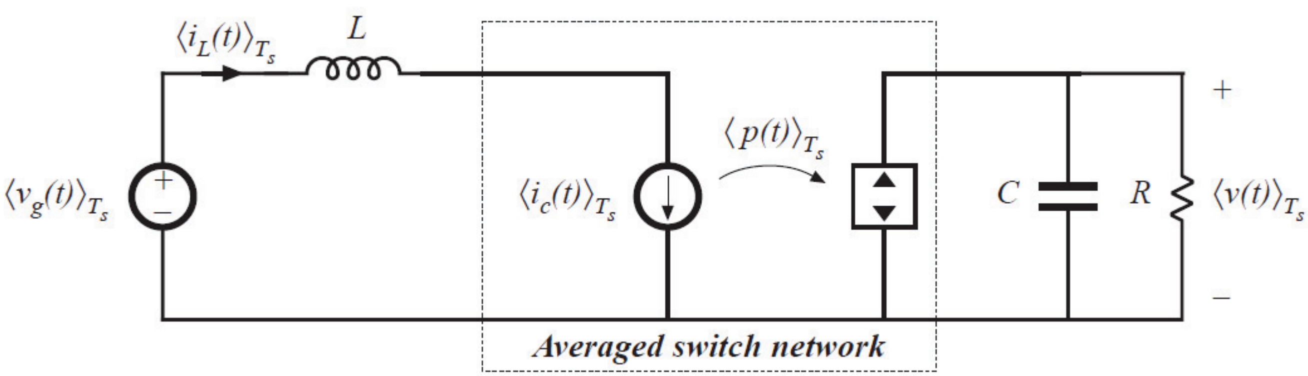


$\uparrow i_c = i_{ref}$

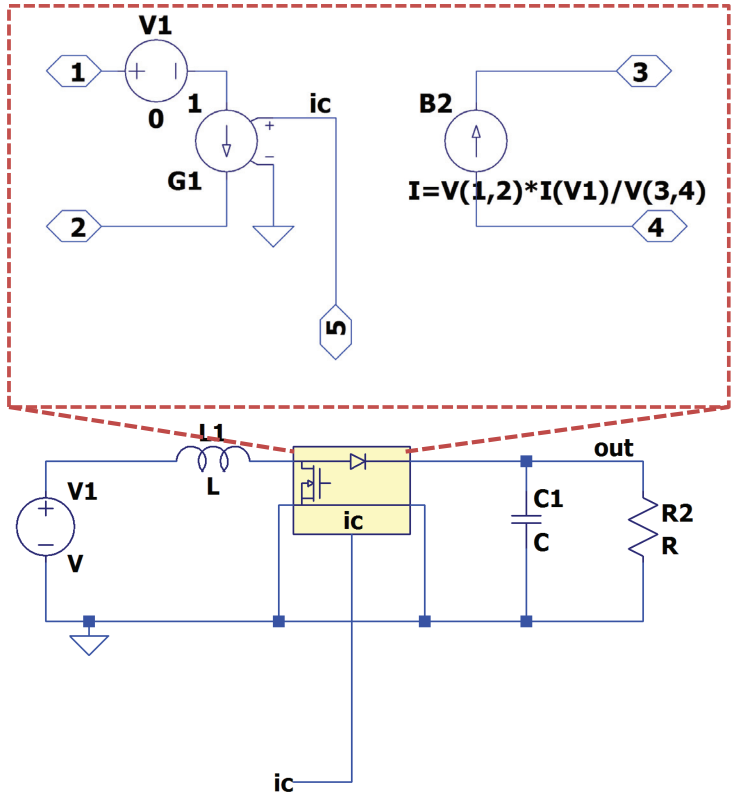
if CPM is ideal $i_L = i_c$



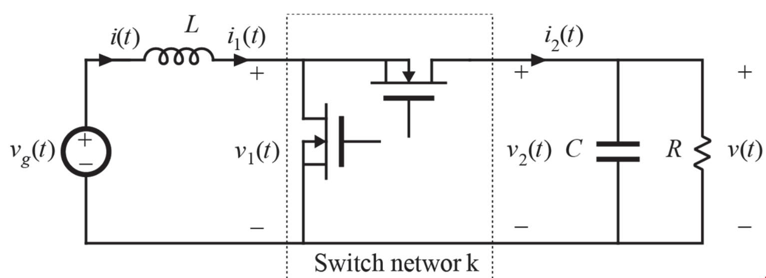
Large-Signal Nonlinear Model



Implementation in LTSpice



Averaged, Small-Signal Model



$$L\frac{d\langle i_L\rangle}{dt} = \langle v_g\rangle - d'(t)\langle v\rangle$$

$$C\frac{d\langle v\rangle}{dt} = d'(t)\langle i_L\rangle - \frac{\langle v\rangle}{R}$$

- Replace $i_L = i_c$ (assuming ideal CPM)
- Linearize in laplace domain

$$sL\hat{i}_c = \hat{v}_g + V\hat{d} - D'\hat{v}$$

$$sC\hat{v} = D'\hat{i}_c - I_L\hat{d} - \frac{\hat{v}}{R}$$

- $\hat{d}$ is no longer controlled → eliminate

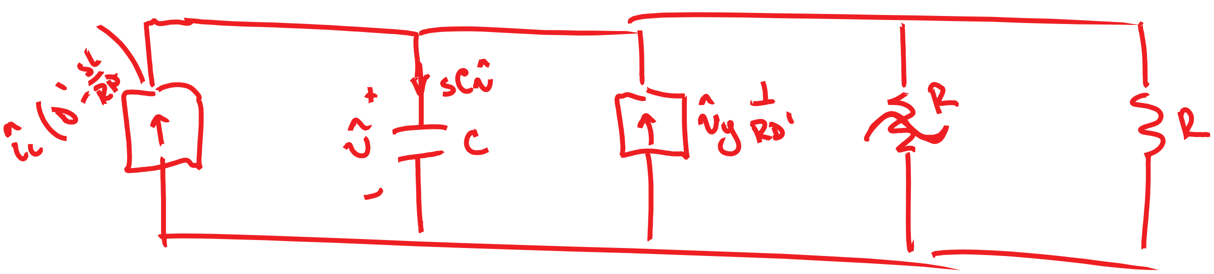
$$\hat{d} = \frac{1}{V}\left(sL\hat{i}_c - \hat{v}_g + D'\hat{v}\right)$$

$$sC\hat{v} = D'\hat{i}_c - \frac{\hat{v}}{R} - \frac{I_L}{V}\left(sL\hat{i}_c - \hat{v}_g - D'\hat{v}\right)$$

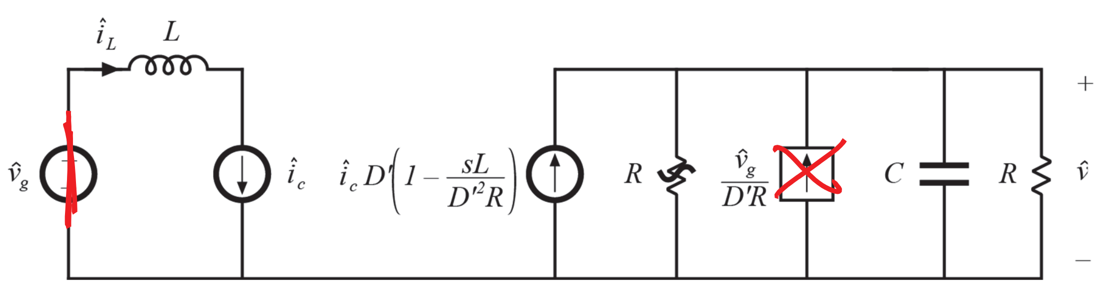
$$sC\hat{v} = \hat{i}_c\left(D' - \frac{I_L}{V}sL\right) + \hat{v}_g\frac{I_L}{V} - \frac{\hat{v}}{R} - \frac{I_L}{V}D'\hat{v}$$

$$I_{out} = D'I_L \rightarrow \frac{I_L}{V} = \frac{I_{out}}{D'V} = \frac{1}{RD'}$$

$$sC\hat{v} = \hat{i}_c\left(D' - \frac{sL}{RD'}\right) + \hat{v}_g\frac{1}{RD'} - \frac{\hat{v}}{R} - \frac{\hat{v}}{R}$$



Boost CCM CPM Small-Signal Model



$$G_{vi} = \frac{\hat{v}}{\hat{i}_c}\Big|_{\substack{\text{DC op point} \\ \hat{v}_g = 0}} = D'\left(1 - \frac{sL}{D'^2R}\right)\cdot\left(R \| R \| \frac{1}{sC}\right)$$

$$R \| R \| \frac{1}{sC} = \frac{1}{\frac{2}{R} + sC}$$

$$G_{vi} = \frac{D'R}{2}\,\frac{\left(1 - \frac{sL}{D'^2R}\right)}{1 + s\frac{RC}{2}}$$

Same RHP zero as in G_{vd}

single pole!!

for PWM control

$$G_{vd} = \frac{V}{D'}\,\frac{\left(1 - \frac{sL}{D'^2R}\right)}{1 + s\frac{L}{RD'} + s^2\frac{LC}{D'^2}}$$

CPM Transfer Functions

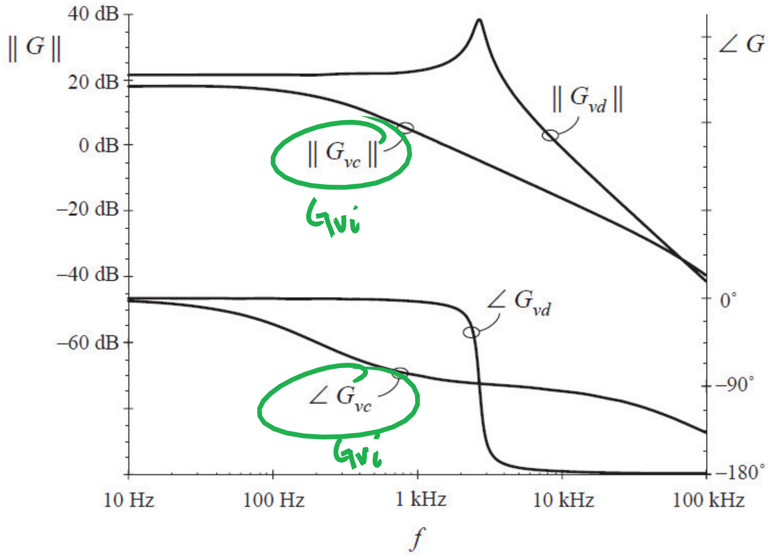
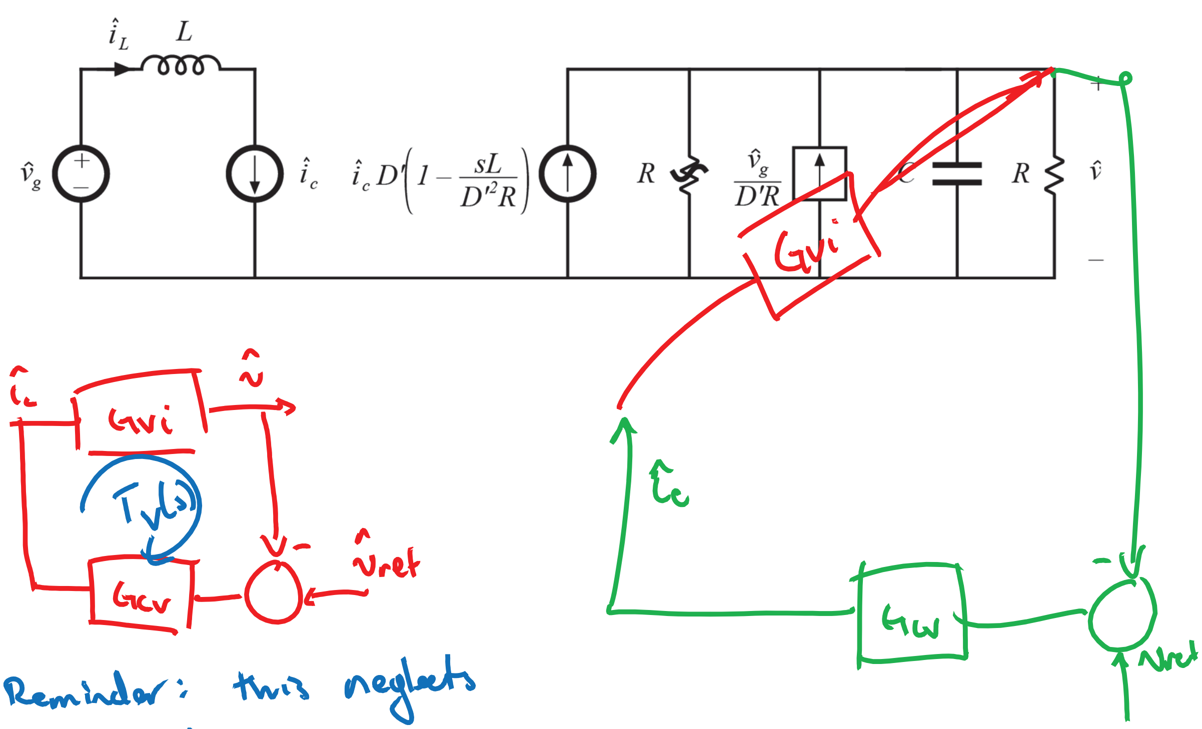


Fig. 12.28 Comparison of CPM control with duty-cycle control, for the control-to-output frequency response of the buck converter example.

Voltage Control



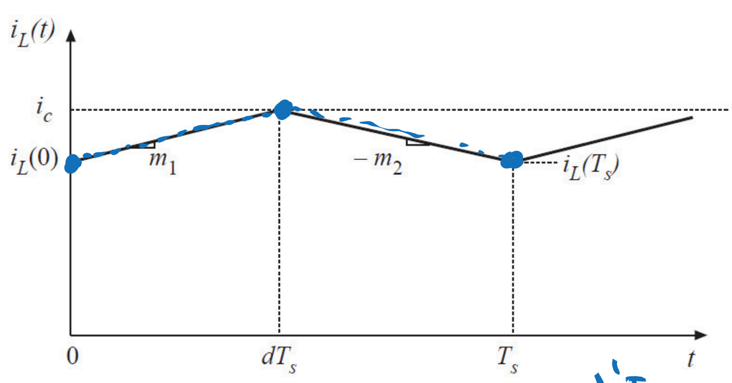
* Reminder: this neglects R_f, H

CPM Oscillations for D>0.5

- The current programmed controller is inherently unstable for $D > 0.5$, regardless of the converter topology
- Controller can be stabilized by addition of an artificial ramp

Inductor Current Waveform in CCM

In steady-state $i_L(0) = i_L(T_s)$



$i_L(T)_s = i_L(0) + m_1 dT_s - m_2 d' T_s$

in steady-state

$0 = m_1 D T_s - m_2 D' T_s$

$\frac{m_2}{m_1} = \frac{D}{D'}$

Inductor current slopes m_1 *and* $-m_2$

buck converter

$$m_1 = \frac{v_g - v}{L} \qquad -m_2 = -\frac{v}{L}$$

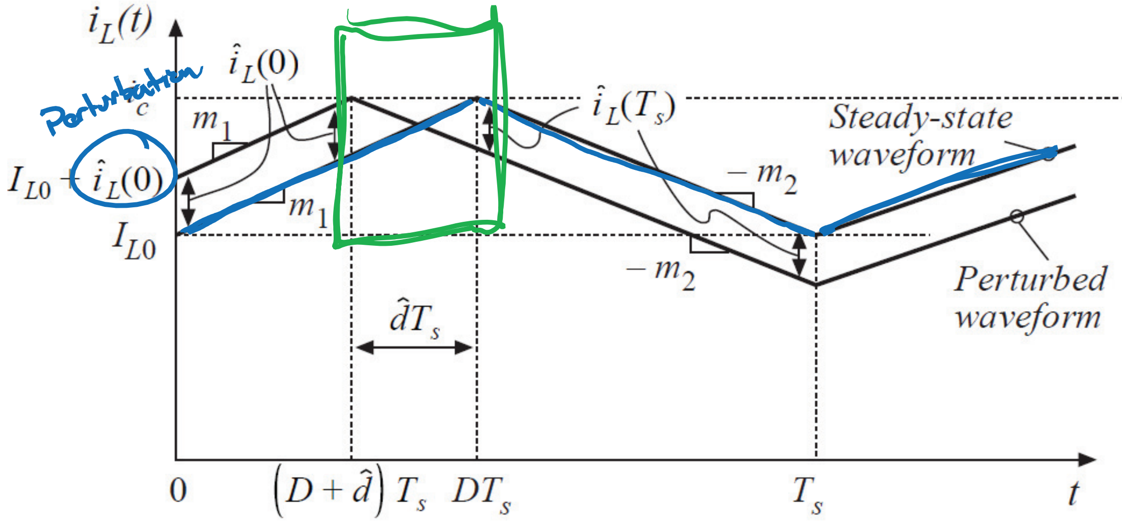
boost converter

$$m_1 = \frac{v_g}{L} \qquad -m_2 = \frac{v_g - v}{L}$$

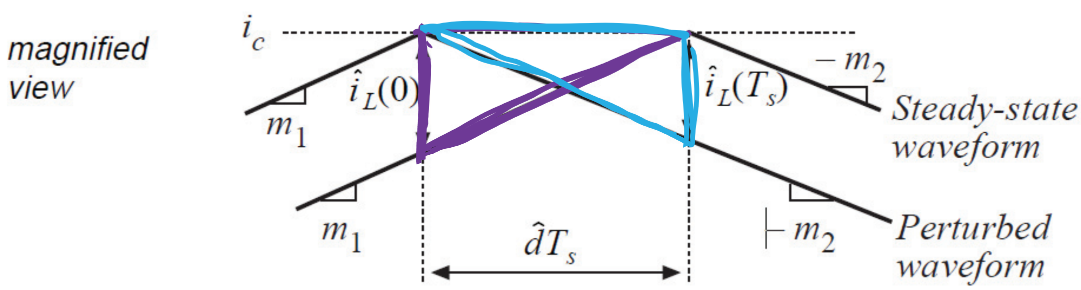
buck–boost converter

$$m_1 = \frac{v_g}{L} \qquad -m_2 = \frac{v}{L}$$

Introducing a Perturbation



Change in Inductor Current Over T_s



$\hat{i}_L(0) = m_1 \hat{d} T_s$

$\hat{i}_L(T_s) = -m_2 \hat{d} T_s$

$\hat{i}_L(T_s) = \hat{i}_L(0)\frac{-m_2}{m_1}$

$\hat{i}_L(2T_s) = \hat{i}_L(T_s)\left(\frac{-m_2}{m_1}\right) = \hat{i}_L(0)\left(\frac{-m_2}{m_1}\right)^2$

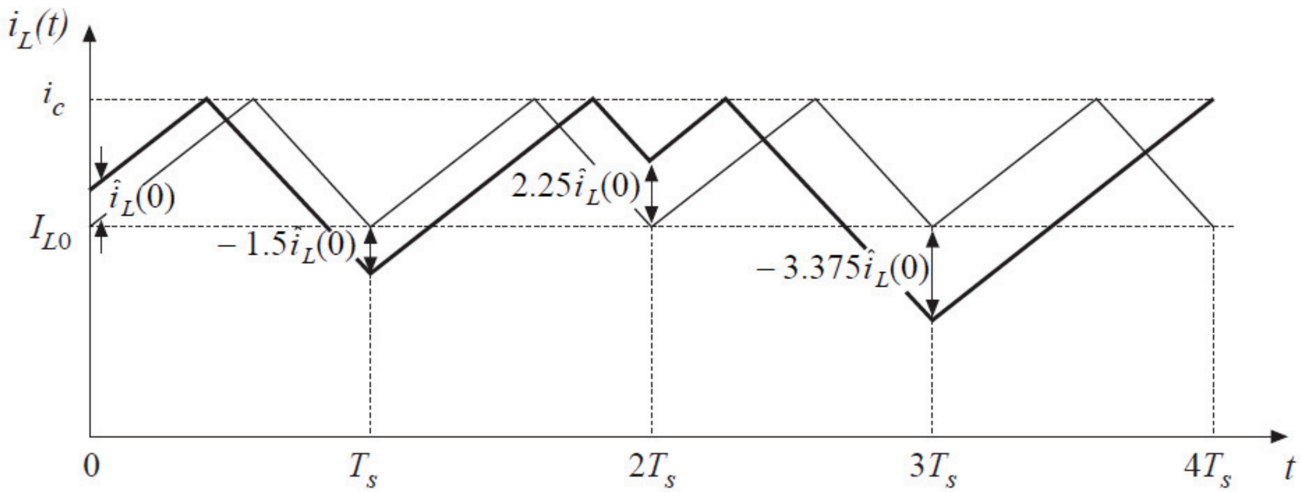
$\hat{i}_L(nT_s) = \hat{i}_L(0)\left(\frac{-m_2}{m_1}\right)^n$

$\alpha = \frac{-m_2}{m_1} = \frac{D}{D'}$

need $|\alpha| < 1$ for stability

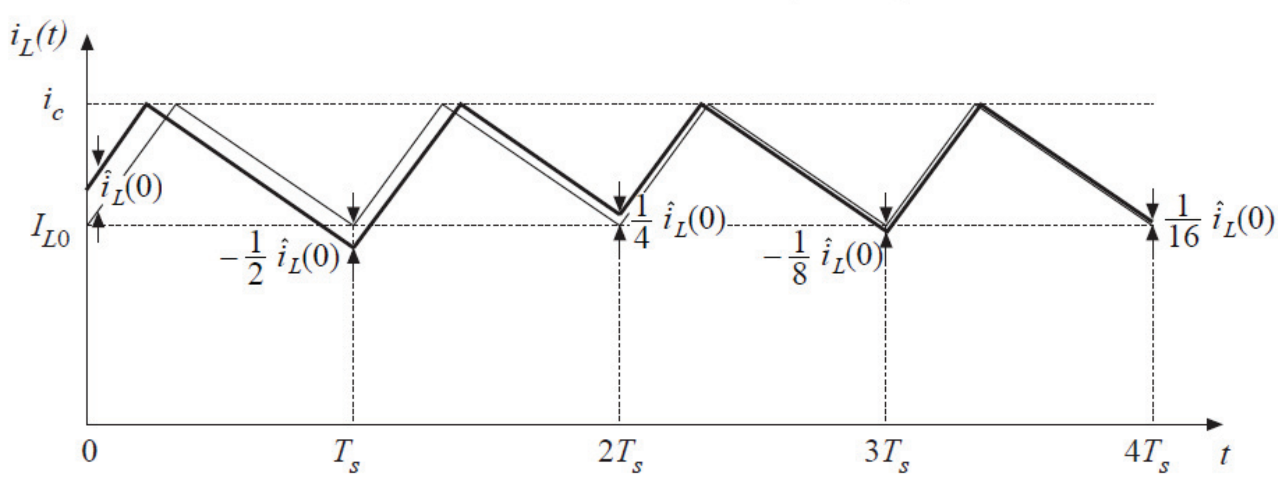
Example: Unstable operation for D=0.6

$$\alpha = -\frac{D}{D'} = \left(-\frac{0.6}{0.4}\right) = -1.5$$

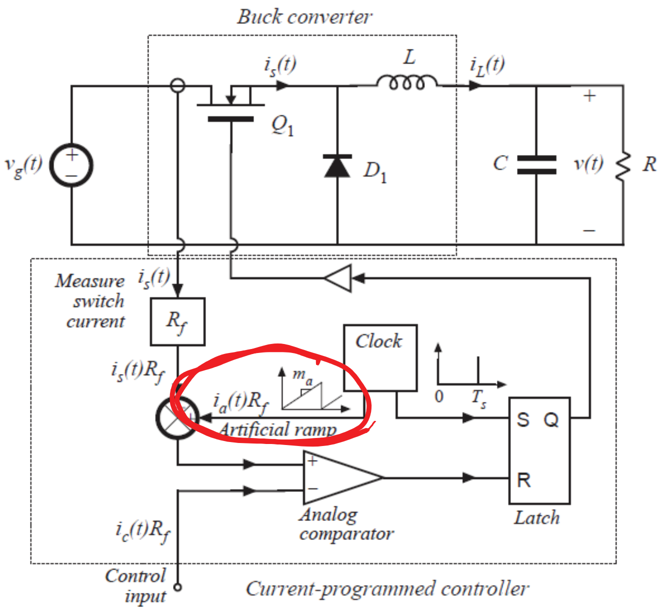


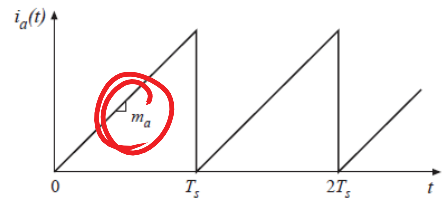
Example: Stable operation for D=1/3

$$\alpha = -\frac{D}{D'} = \left(-\frac{1/3}{2/3}\right) = -0.5$$



Stabilization Through Artificial Ramp





Now, transistor switches off when

$$i_a(dT_s) + i_L(dT_s) = i_c$$

or,

$$i_L(dT_s) = i_c - i_a(dT_s)$$

if $i_a >> i_L$ → PWM control

if $i_a << i_L$ → CPM

Final Value of Inductor Current

First subinterval:

$$\hat{i}_L(0) = -\hat{d}T_s\left(m_1 + m_a\right)$$

Second subinterval:

$$\hat{i}_L(T_s) = -\hat{d}T_s\left(m_a - m_2\right)$$

Net change over one switching period:

$$\hat{i}_L(T_s) = \hat{i}_L(0)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right)$$

After n switching periods:

$$\hat{i}_L(nT_s) = \hat{i}_L((n-1)T_s)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right) = \hat{i}_L(0)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right)^n = \hat{i}_L(0)\,\alpha^n$$

Characteristic value:

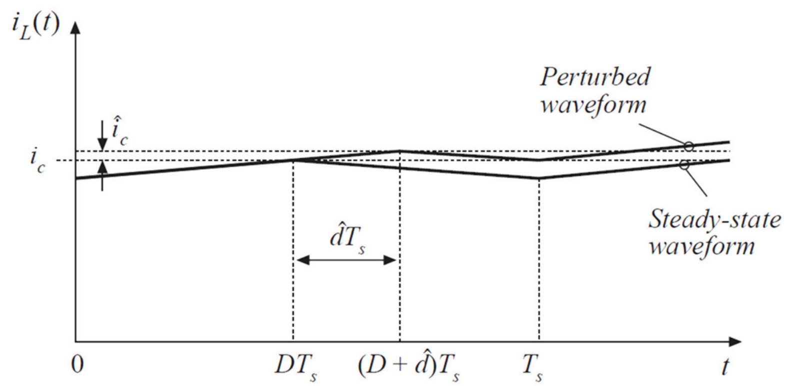
$$\alpha = -\frac{m_2 - m_a}{m_1 + m_a}$$

$$\left|\hat{i}_L(nT_s)\right| \to \begin{cases} 0 & \text{when } |\alpha| < 1 \\ \infty & \text{when } |\alpha| > 1 \end{cases}$$

Artificial Ramp: Additional Notes

$$\alpha = -\frac{1 - \frac{m_a}{m_2}}{\frac{D'}{D} + \frac{m_a}{m_2}}$$

- For stability, require $|\alpha|<1$
- Common choices:
  - $m_a = 0.5\, m_2$ (stable for all duty cycles)
  - $m_a = m_2$ (deadbeat)
- Artificial ramp decreases sensitivity to noise



More Accurate Models

- The simple models of the previous section yield insight into the low- frequency behavior of CPM converters
- Unfortunately, they do not always predict everything that we need to know:
  - Line-to-output transfer function of the buck converter
  - Dynamics at frequencies approaching f_s
- More accurate model accounts for nonideal operation of current mode controller built-in feedback loop
- Converter duty-cycle-controlled model, plus block diagram that accurately models equations of current mode controller
- See Section 12.3 for additional info

More Accurate Model

- Simple model assumes $i_L = i_c$ always
- Accounting for ripple, and artificial ramp weakens this approximation
- Using sampled data modeling

$$\frac{\hat{i}_L}{\hat{i}_C} = \frac{1}{1 + \frac{1}{Q_s}\left(\frac{s}{2\pi \, {}^{f_s}\!/_2}\right) + \left(\frac{s}{2\pi \, {}^{f_s}\!/_2}\right)^2}$$

Where

$$Q_s = \frac{2}{\pi\left(\frac{2}{1-\alpha} - 1\right)}$$

if my bandwidth of voltage loop is well below $f_s/2$ then $i_L \approx i_c$ applies

F. Dong Tan and R. D. Middlebrook, "A Unified Model for Current Programmed Converters," IEEE Transactions on Power Electronics, vol. 10, no. 4, July 1995.

Note: Comparison to Datasheet

Application Information (continued)

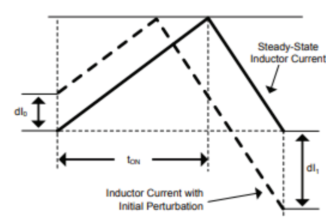


Figure 30. Effect of Initial Perturbation when $dI_1/dI_0 < -1$

dI_1/dI_0 can be calculated as:

$$\frac{dI_1}{dI_0} = 1 - \frac{1}{K} \quad (19)$$

$\alpha = 1 - \frac{1}{K}$

The relationship between dI_1/dI_0 and K factor is illustrated in the graphic below.

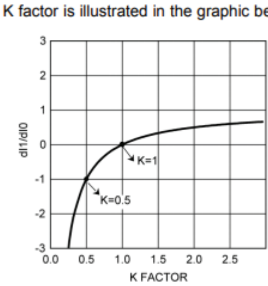
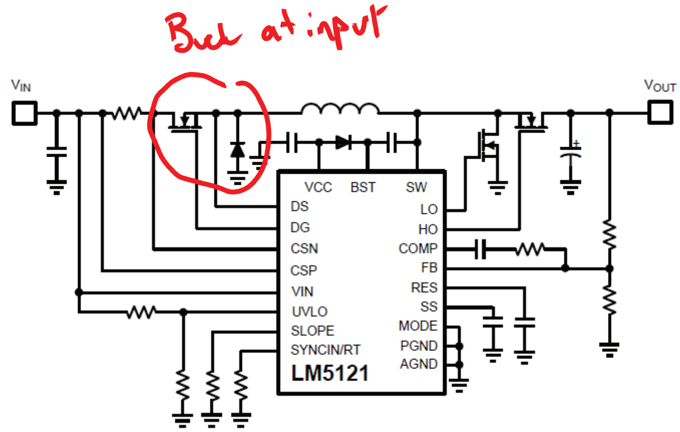


Figure 31. dI_1/dI_0 vs K Factor

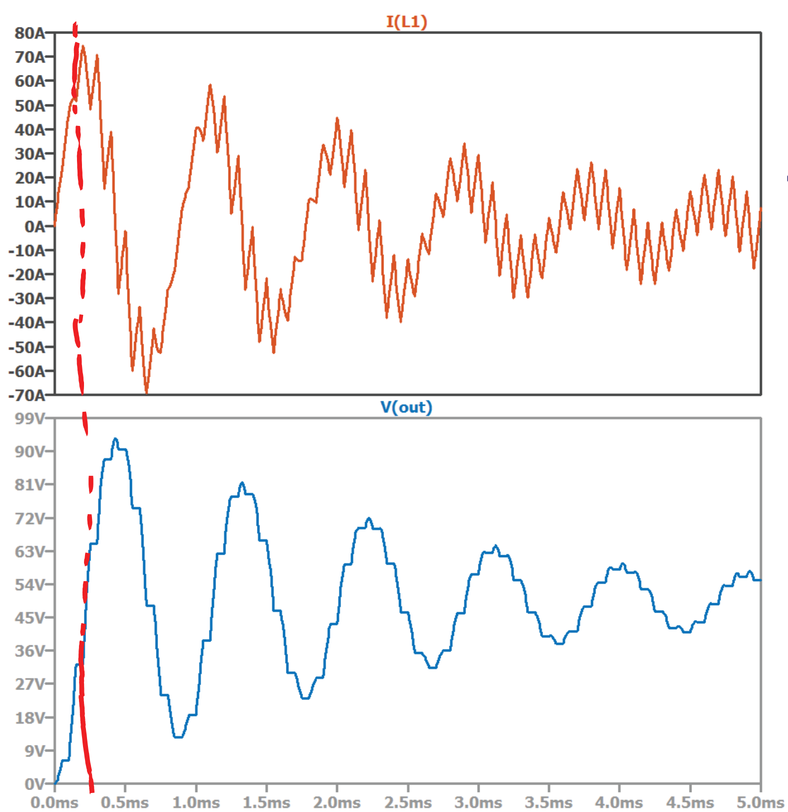
The absolute minimum value of K is 0.5. When K<0.5, the amplitude of dI_1 is greater than the amplitude of dI_0 and any initial perturbation results in sub-harmonic oscillation. If K=1, any initial perturbation will be removed in one switching cycle. This is known as one-cycle damping. When $-1<dI_1/dI_0<0$, any initial perturbation will be under-damped. Any perturbation will be over-damped when $0<dI_1/dI_0<1$.

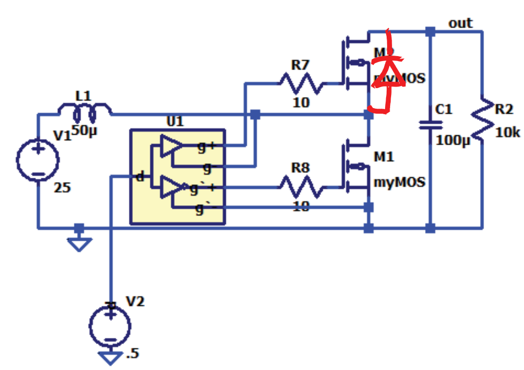
Application to Experiment 4



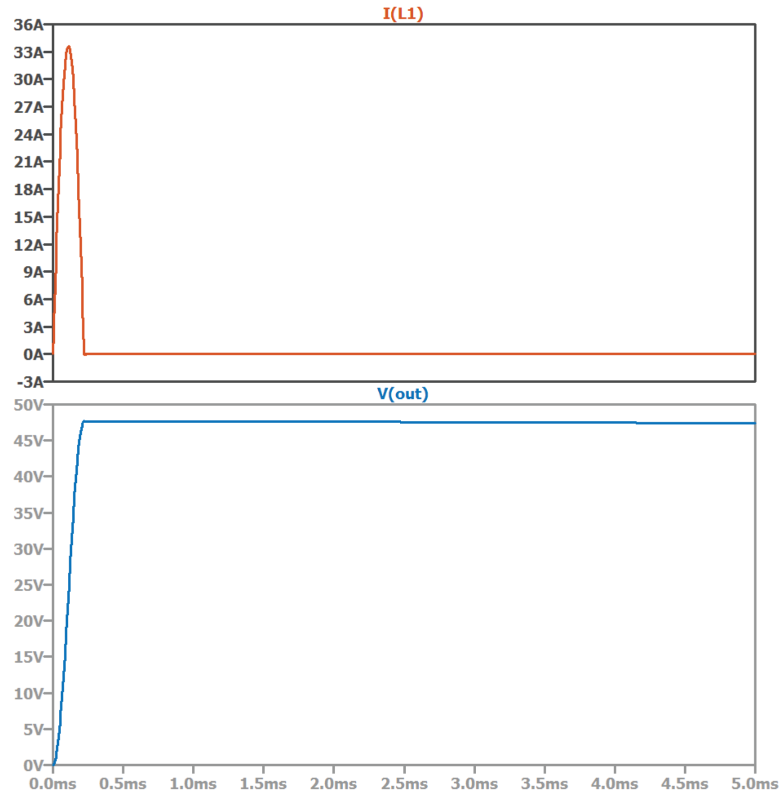
- Complex switching controller
- **Read** the datasheet first

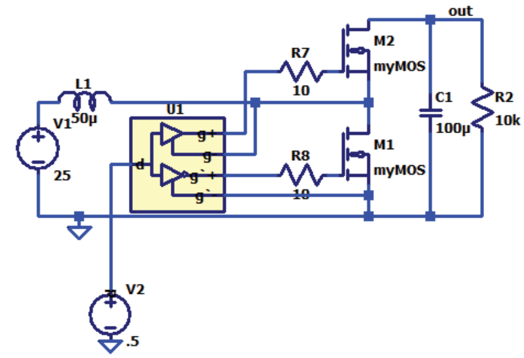
Startup: Switching





Startup: No Switching





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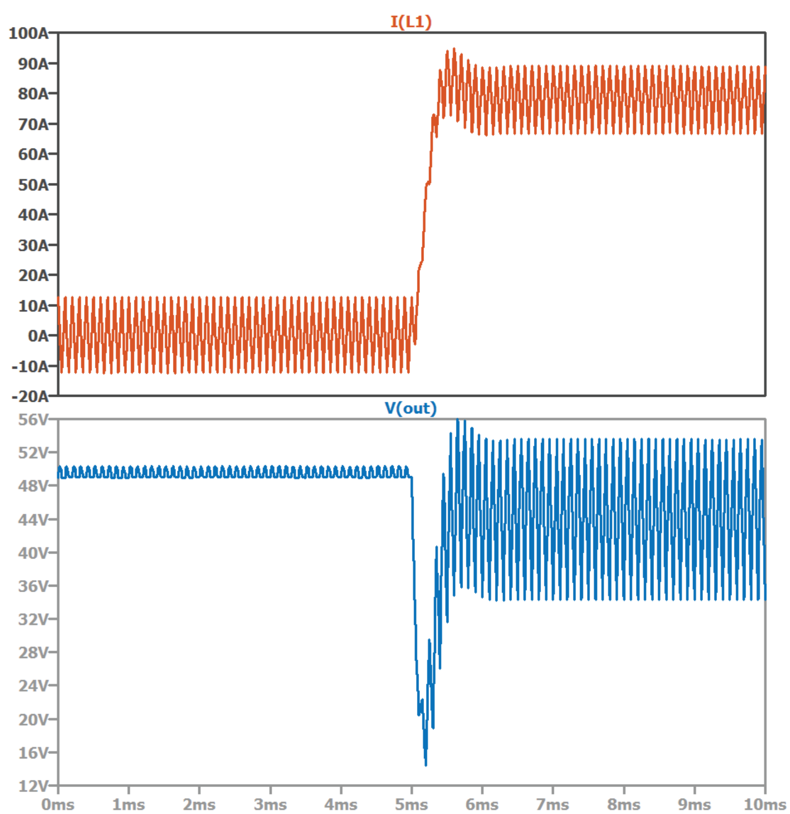
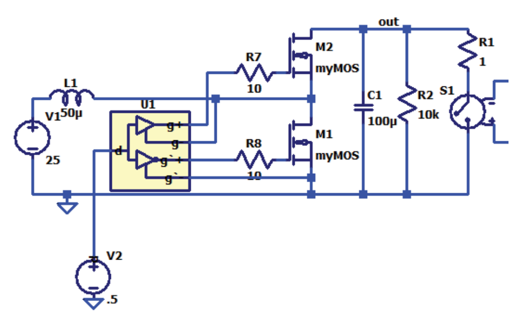
Short-Circuit: Switching





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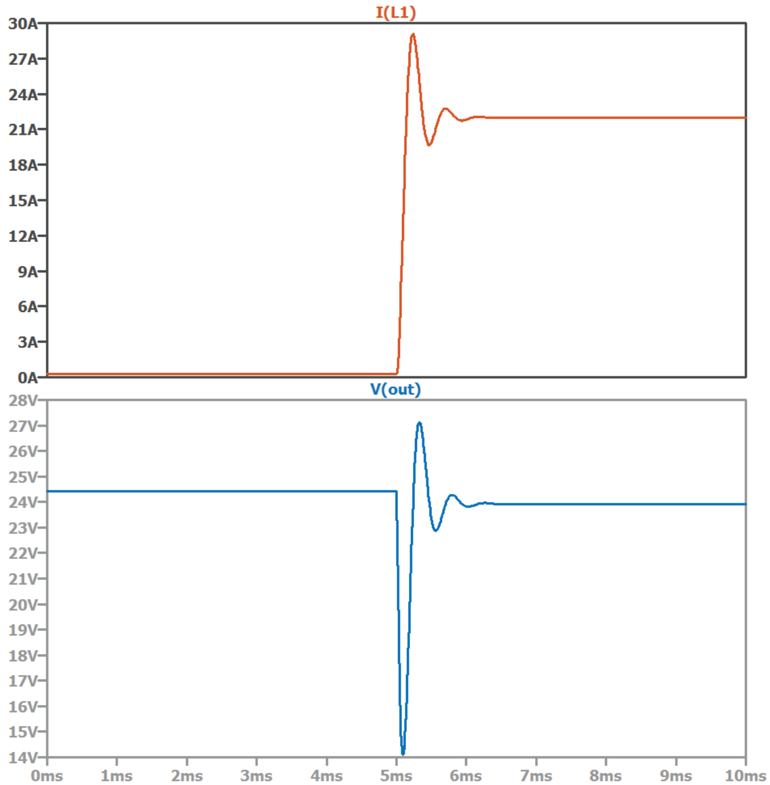
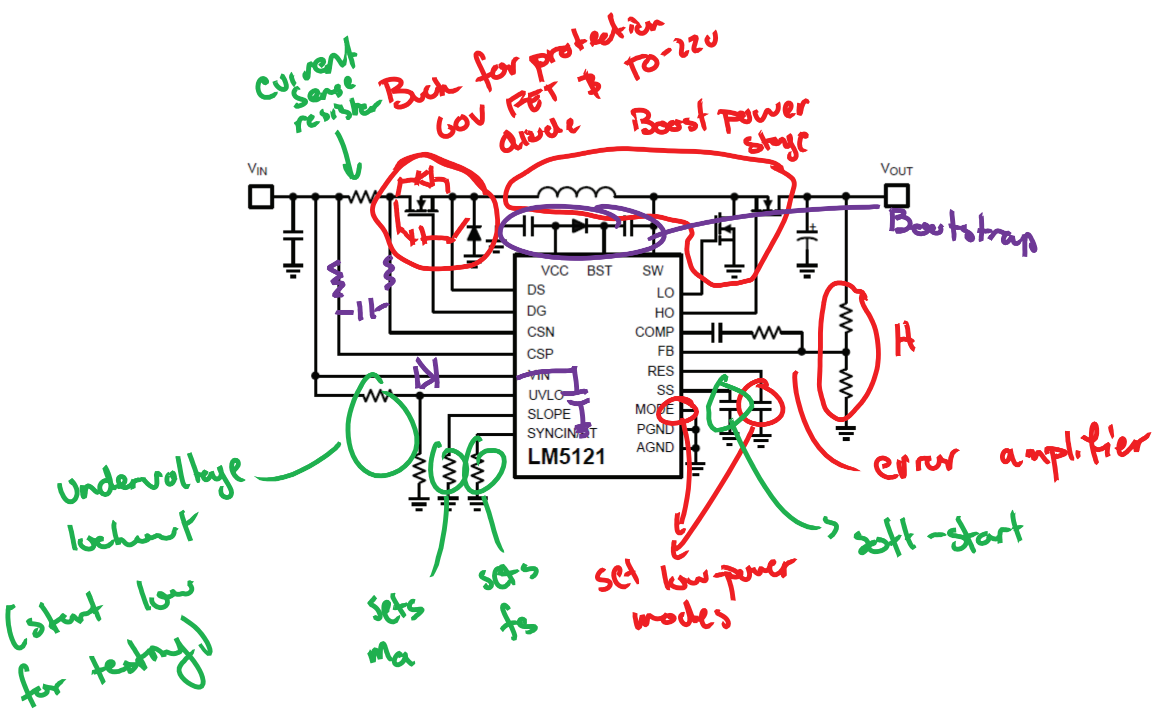
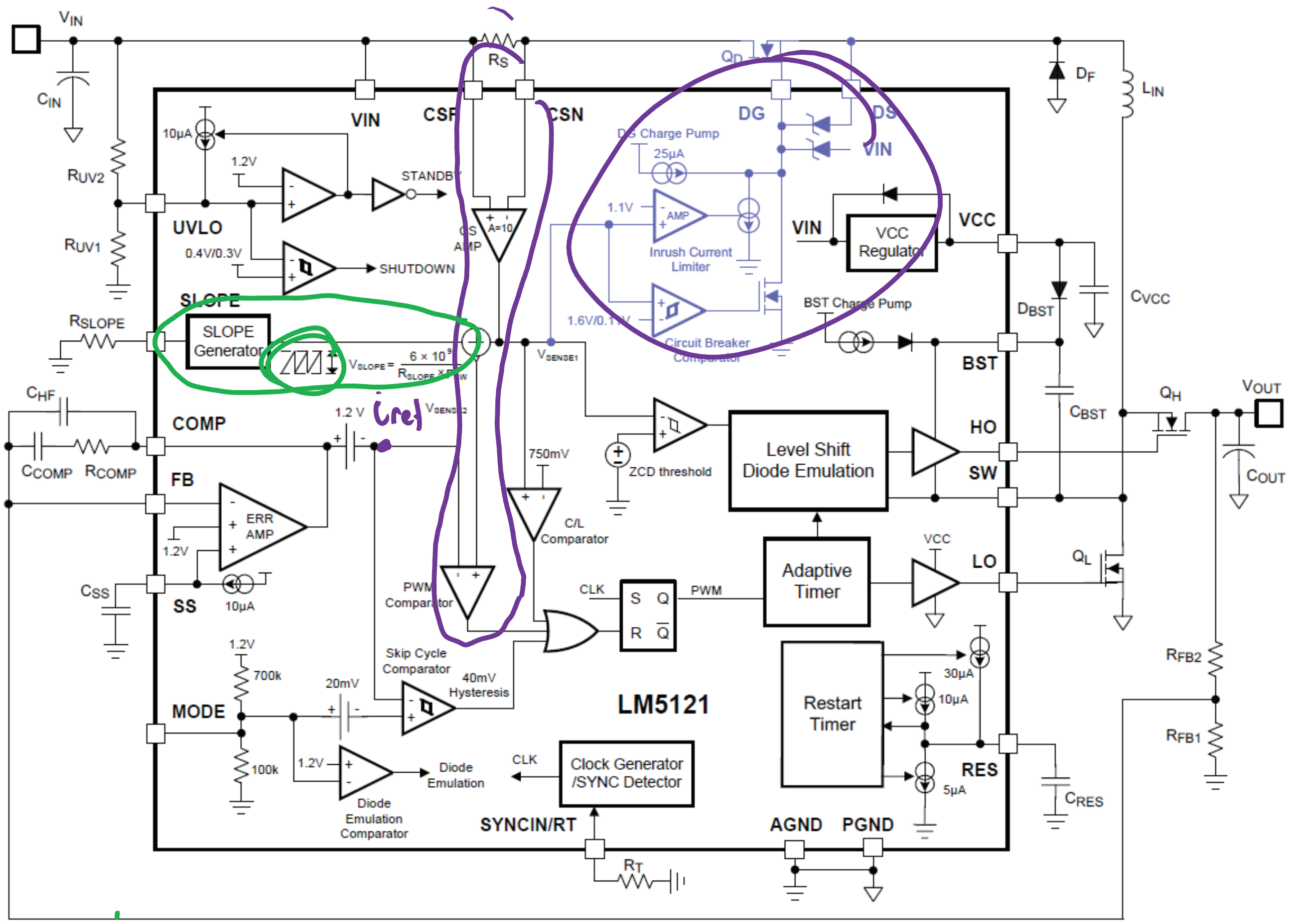
Short-Circuit: No Switching



LM5121: Functionality





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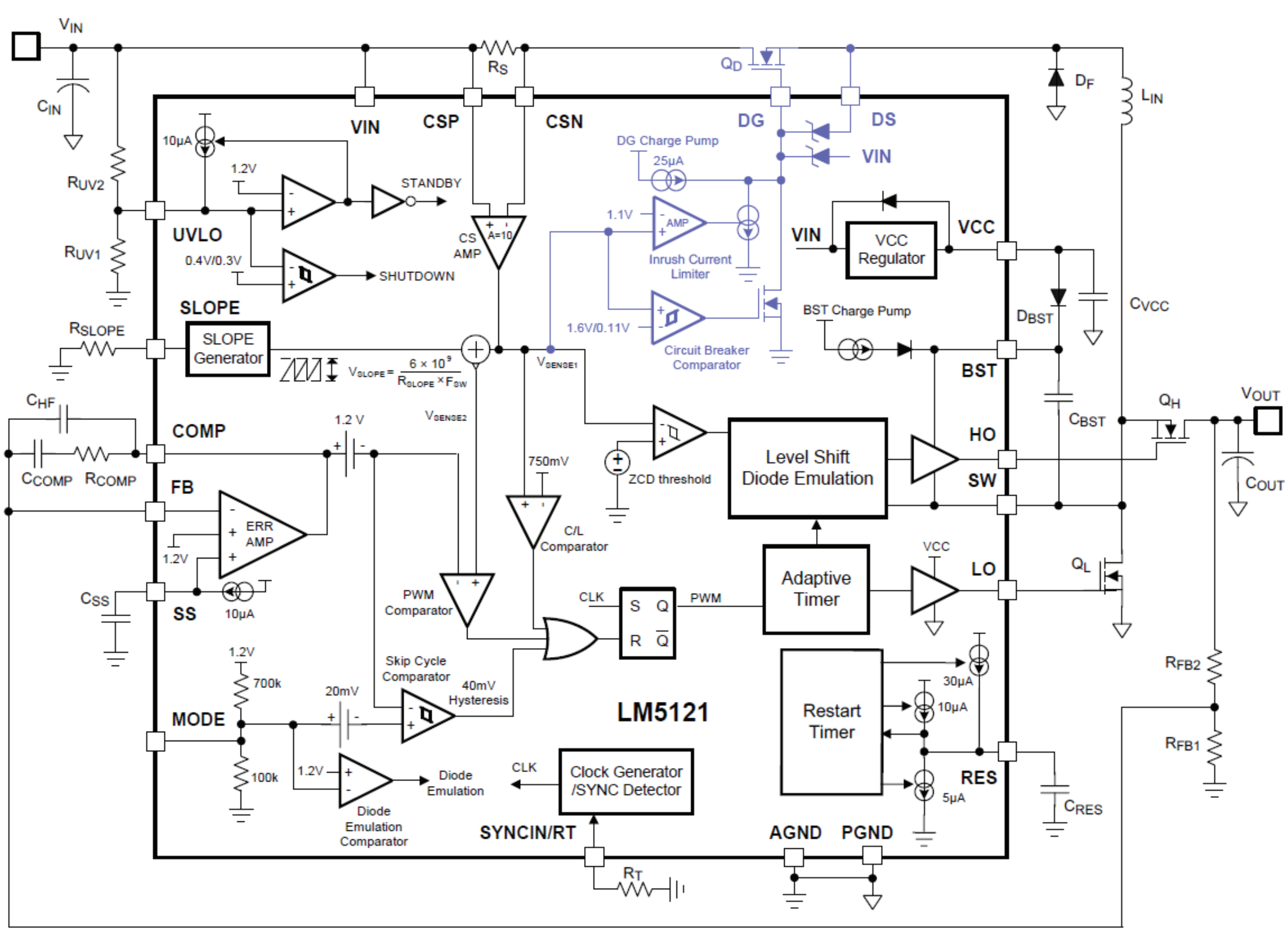

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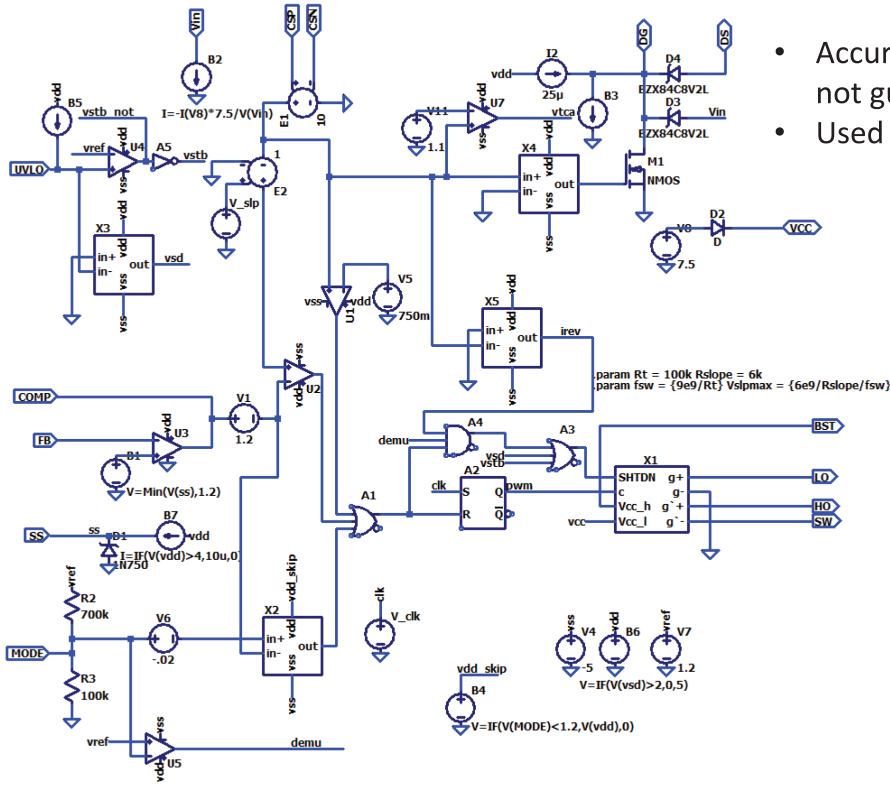
Internal Functional Model in LTSpice

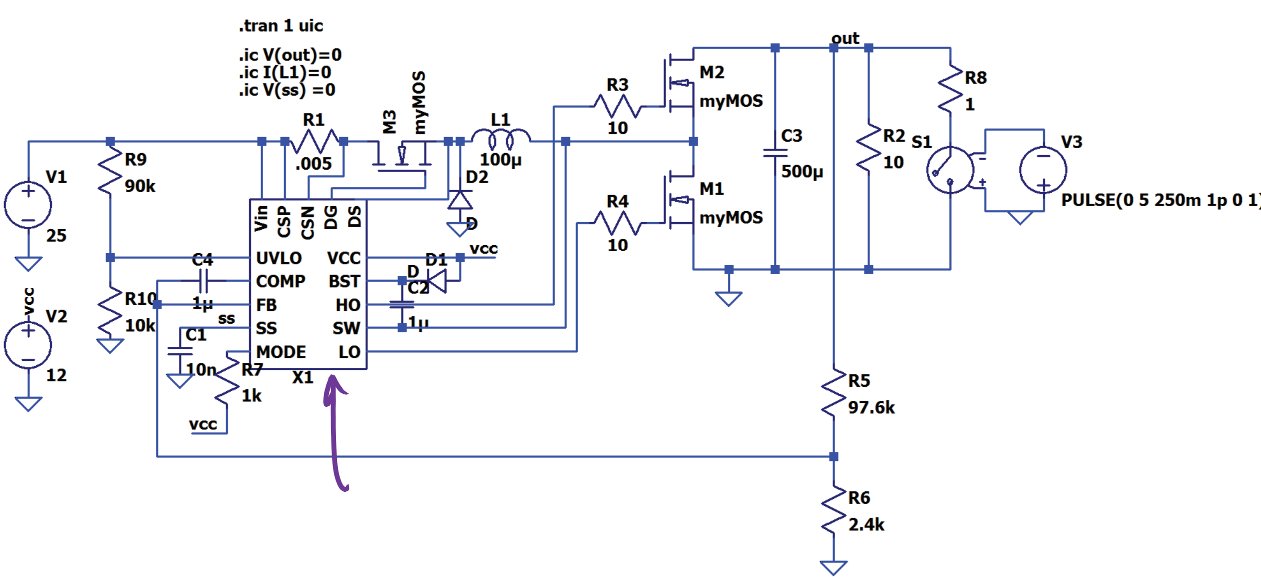


- Accuracy/functionality not guaranteed
- Used for insight only

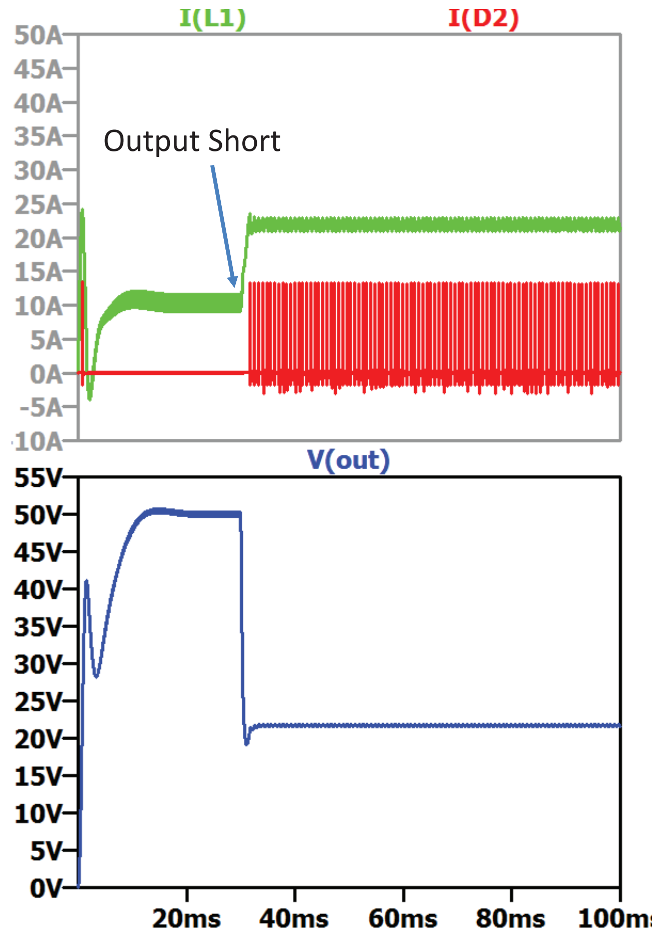
In-Circuit Simulation

.model mysw sw(Von=3 Voff=2 Ron=.1 Roff = 1Meg)

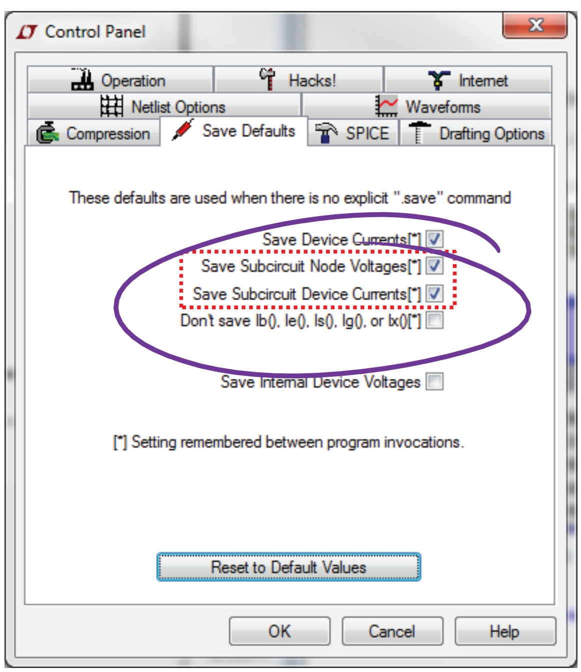
.model myMOS VDMOS(Rg=1 Vto=4.5 Rd=14m Rs=10m Rb=17m Kp=30 Cgdmax=.5p Cgdmin=.05n Cgs=.2n Cjo=.03p Is=88p)



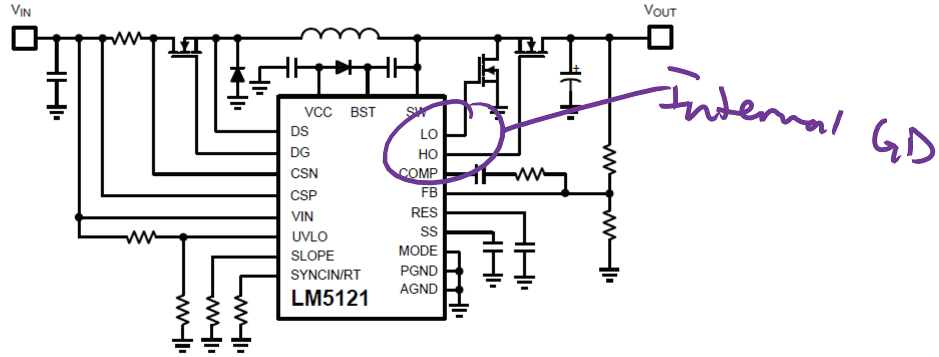
Sim Results

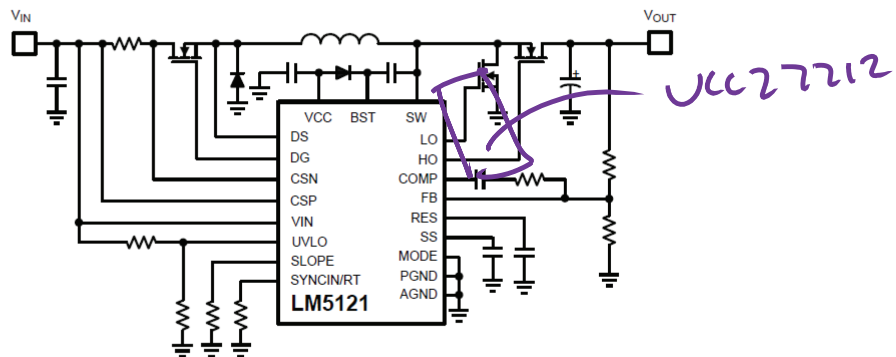


A Tip: Debug Internal of Subcircuit



Experiment 4: Gate Driver Selection





Experiment 4: Closing the Loop

- Closed-loop operation in steps
  1. Open-loop operation with LM5121 modulator
     - Requires “tricking” LM5121
  2. Closed-loop current regulation
  3. Closed-loop voltage and current regulation

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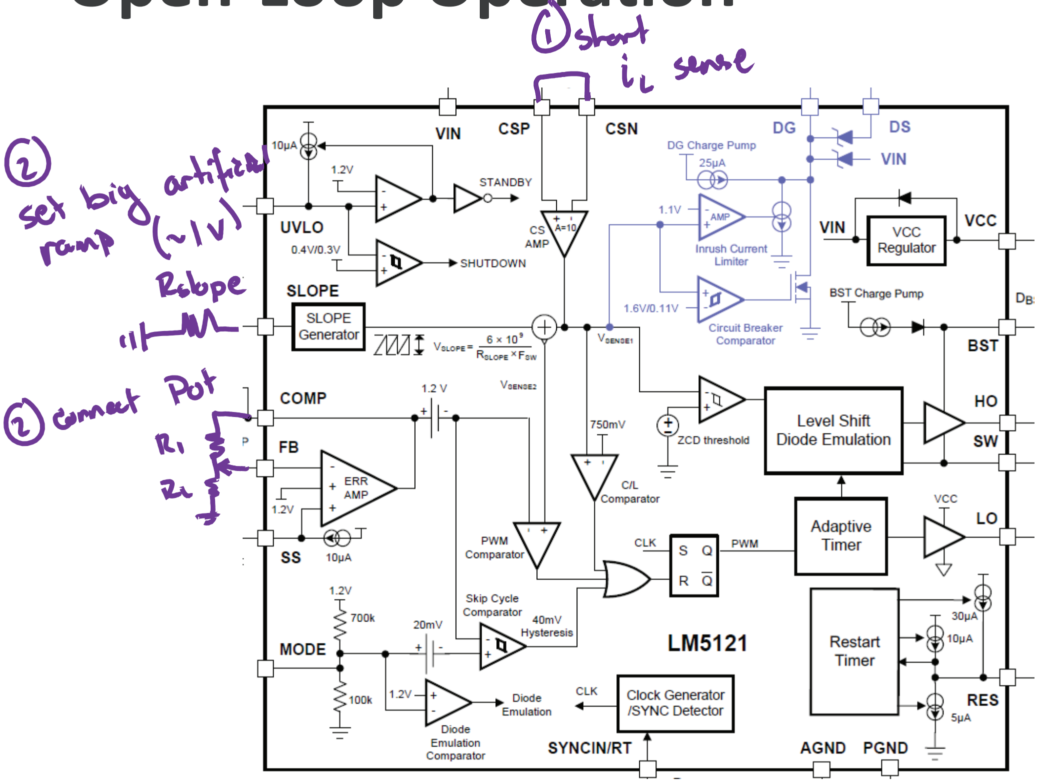
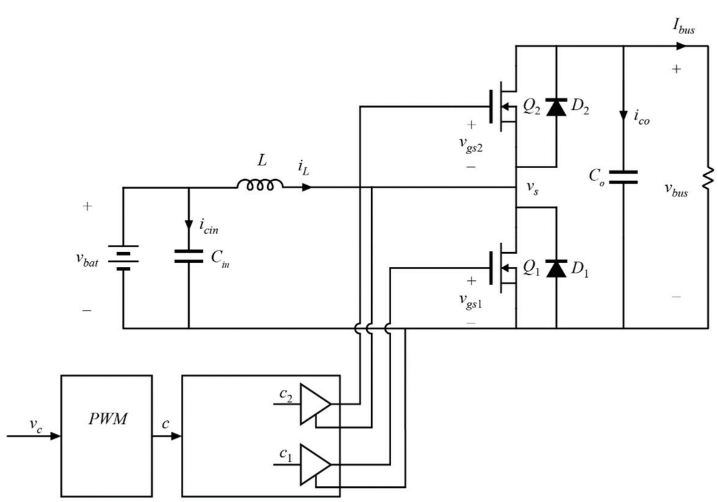
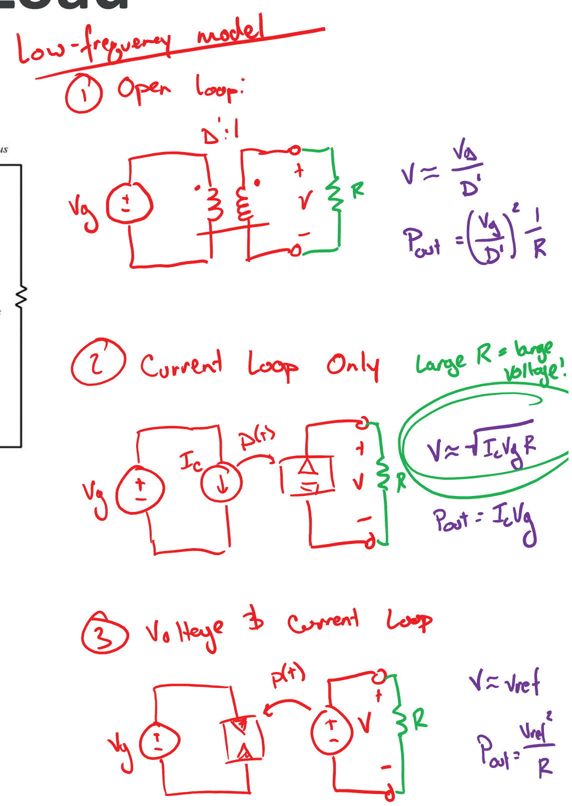
Open-Loop Operation



Setting the Electronic Load





Be careful with how you set electronic load

Safest: ① & ③ current or resistance

② voltage