# Simulation Modeling

Circuit Simulation

- LTSpice
  - Other tools accepted, but not supported
- Choose model type (switching, averaged, dynamic)
- Supplement analytical work rather than repeating it
- Show results which clearly demonstrate what matches and what does not with respect to experiments (i.e. ringing, slopes, etc.)

LTSpice Modeling Examples
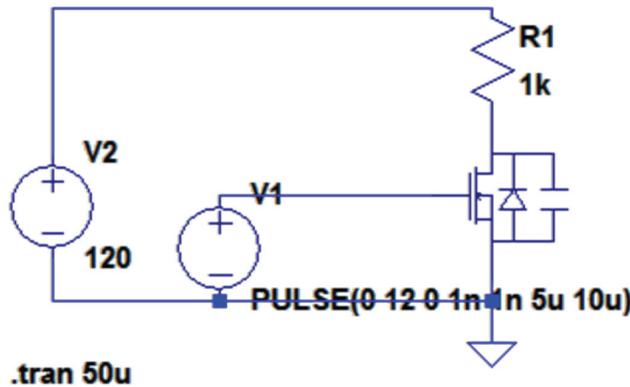
- Example files added to course materials page
  - Custom model
  - VDMOS model
  - Manufacturer Model

Custom Transistor Model

```
.model myD D(n=.001)
.model mySw SW(Ron=10m Roff=1G Von=1 Voff = .5 )
```
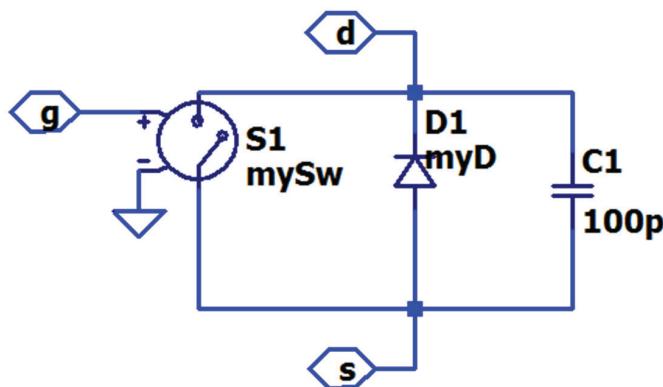
VDMOS Model

Name	Description	Units	Default	Example
Vto	Threshold voltage	V	0	1.0
Kp	Transconductance parameter	A/V^2	1.	.5
Phi	Surface inversion potential	V	0.6	0.65
Lambda	Channel-length modulation	1/V	0.	0.02
mtriode	Conductance multiplier in triode region(allows independent fit of triode and saturation regions	–	1.	2.
subthres	Current(per volt Vds) to switch from square law to exponential subthreshold conduction	A/V	0.	1n
BV	Vds breakdown voltage	V	Infin.	40
IBV	Current at Vds=BV	A	100pA	1u
NBV	Vds breakdown emission coefficient	–	1.	10
Rd	Drain ohmic resistance	Ω	0.	1.
Rs	Source ohmic resistance	Ω	0.	1.
Rg	Gate ohmic resistance	Ω	0.	2.
Rds	Drain-source shunt resistance	Ω	Infin.	10Meg
Rb	Body diode ohmic resistance	Ω	0.	.5
Cjo	Zero-bias body diode	F	0.	1n

.model myMOS VDMOS(nchan Rg=3 Rd=14m Rs=10m Vto=-.8 Kp=32
+ Cgdmax=.5n Cgdmin=.07n Cgs=.9n Cjo=.26n Is=26p Rb=17m)

.tran 50u

R1
1k

V2

M1
myMOS

120
V1

PULSE(0 12 0 1n 1n 5u 10u)
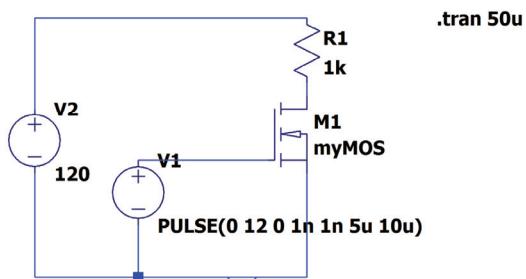
- Note: any other parameters **ignored**
  - E.g. ron = 3m Qg = 1n mfg = Infineon

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Manufacturer Device Model

- Text-only netlist model of device including additional parasitics and temperature effects
- May slow or stop simulation if timestep and accuracy are not adjusted appropriately

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Full Switching Simulation

.tran 1

.model myMOS VDMOS(Rg=1 Vto=4.5 Rd=14m Rs=10m Rb=17m Kp=30 Cgdmax=.5p Cgdmin=.05n Cgs=.2n Cjo=.03n Is=88p)

.ic V(out)=0
.ic I(L1)=0

.lib switch.lib

out

L1
L

V1
V

U1

R7
10

M2
myMOS

R8
10

M1
myMOS

C1
C

R2
R

g+
g
g`+
g`

d

Component Attribute Editor

Open Symbol: E:\Program Files (x86)\LTC\LTspiceIV\lib\sym\Custom\GateDr

This is the fourth attribute to appear on the netlist line.

Attribute	Value	Vis.
Prefix	X	
InstName	U1	X
SpiceModel	GateDriver_dt_phase	
Value		
Value2		
SpiceLine	Vdd=5 Tau=1u Tau2=1u Ts=100u phi=0	
SpiceLine2		

Cancel   OK

Experiment 1

Experiment 2

Experiment 3

Experiment Procedure
  Prelab Assignment
  Experiment 3 Procedure

Experiment 3 Components
  Contents of the Experiment 3 Parts Kit
  Contents of the Magnetics Library
  Breakout Board Schematics and Layout (pdf)
  Breakout Board Schematics and PCB Layout (Altium)
Reference Materials
  Designing Bootstrap Networks
  Power Converter Layout
  Reduction of Ringing in Power Converters (TI App. Note)
 RMS Values of Commonly Observed Waveforms
LTSpice Example Files
  Examples of power semiconductor modeling using custom or manufacturer models
  Example Switching and Averaged Boost LTSpice Models
Magnetics Design
  Filter Inductor Design Notes
  Kg Method Step-by-Step
  Kgfe Method Step-by-Step
  Overview of Empirical Core Loss Calculation Techniques
  Overview of Empirical State of Core Loss Prediction
  Magnetics Design Tables
  AWG Chart

Experiment 4

Available on Exp 3 Webpage
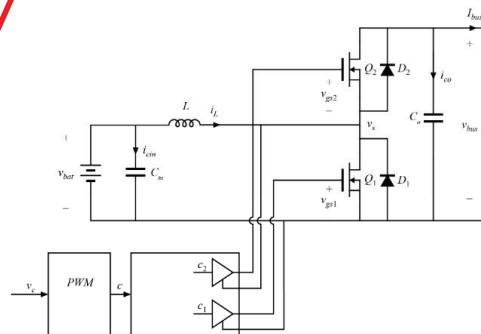
Full Switching Model

- Gives valuable insight into circuit operation
  - Understand expected waveforms
  - Identify discrepancies between predicted and experimental operation
- Slow to simulate; significant high frequency content
- Cannot perform AC analysis

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Averaged Switch Modeling: Motivation

- A *large-signal, nonlinear* model of converter is difficult for hand analysis, but well suited to simulation across a wide range of operating points
- Want an *averaged* model to speed up simulation speed
- Also allows linearization (AC analysis) for control design

Nonlinear, Averaged Circuit
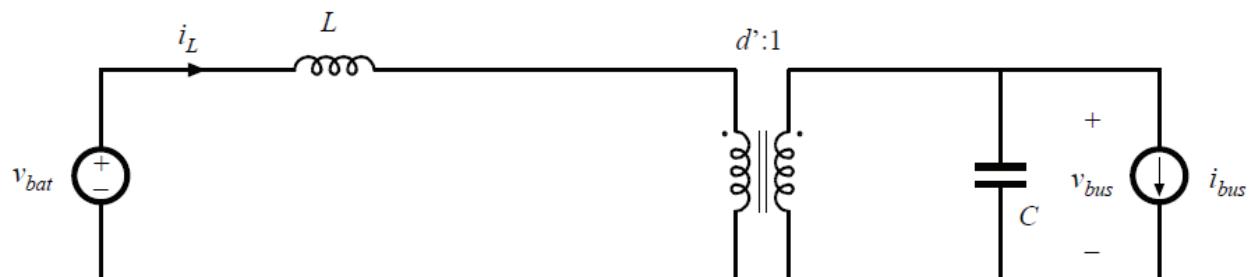
$$L\frac{d\langle i_L \rangle}{dt} = \langle v_{bat} \rangle - (1-d)\langle v_{bus} \rangle$$

$$C\frac{d\langle v_{bus} \rangle}{dt} = (1-d)\langle i_L \rangle - \langle i_{bus} \rangle$$

Implementation in LTSpice
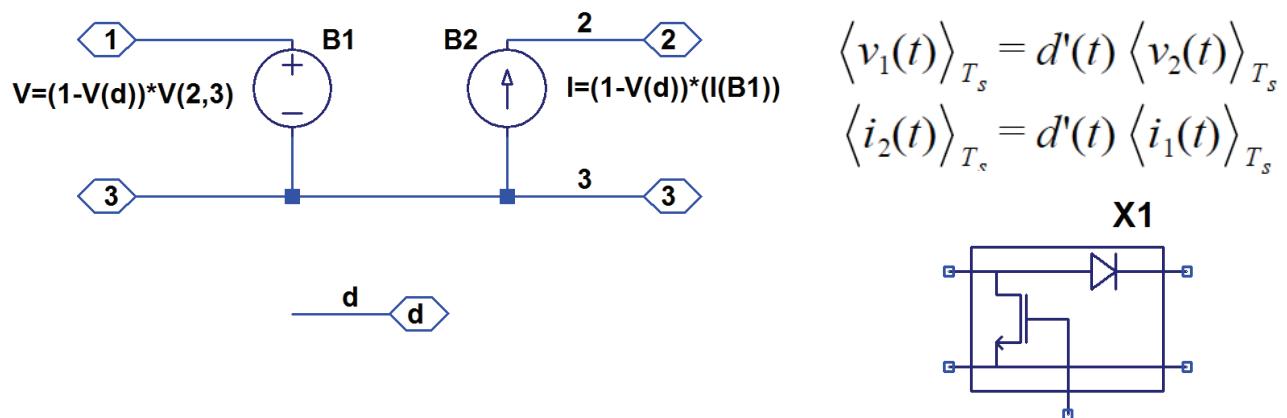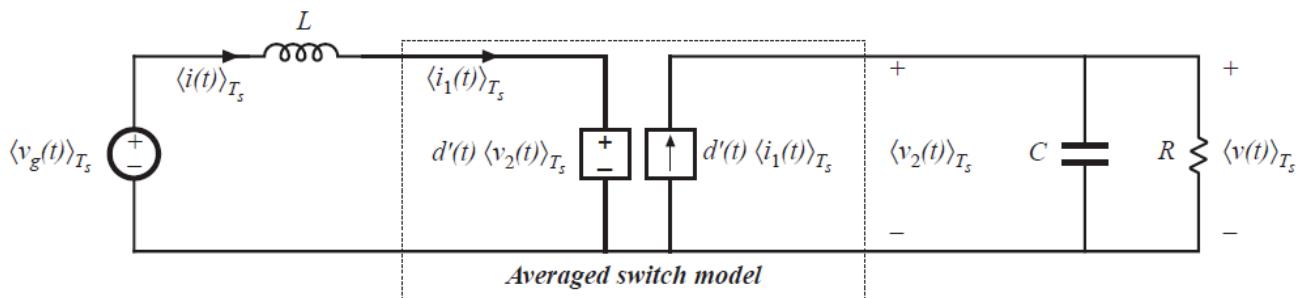
Averaged switch model

$$\langle v_1(t) \rangle_{T_s} = d'(t) \langle v_2(t) \rangle_{T_s}$$

$$\langle i_2(t) \rangle_{T_s} = d'(t) \langle i_1(t) \rangle_{T_s}$$

B1 V=(1-V(d))*V(2,3)

B2 I=(1-V(d))*(I(B1))

X1

Averaged Switch Model

.op
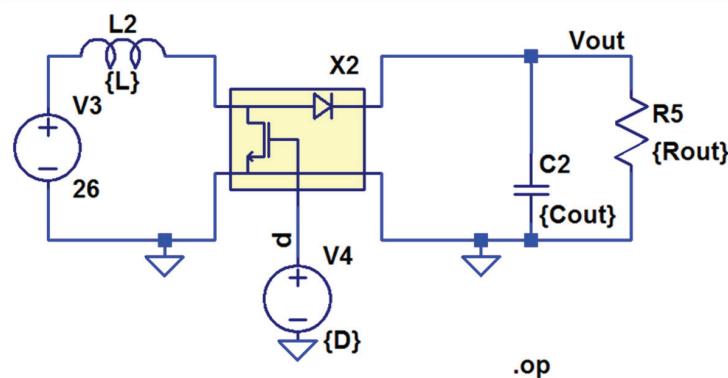
Averaged Model With Losses



```
.op
.param Rout = 10
.step param Rout 10 100 10
```
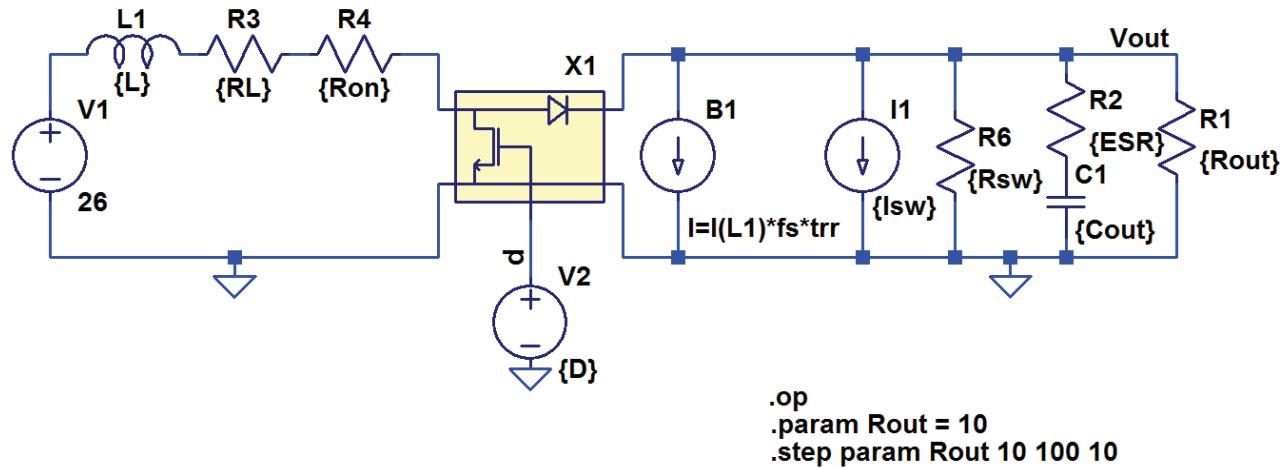
What known error(s) will be present in loss predictions with this model?

Experiment 4

Experiment 4: Closed-Loop Boost
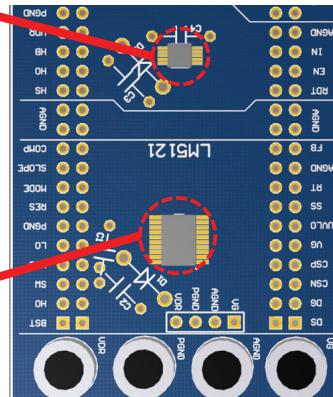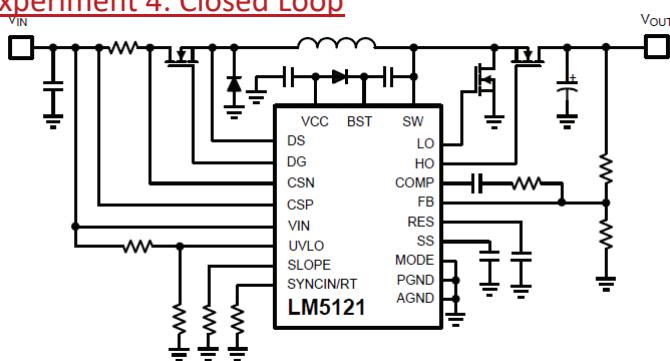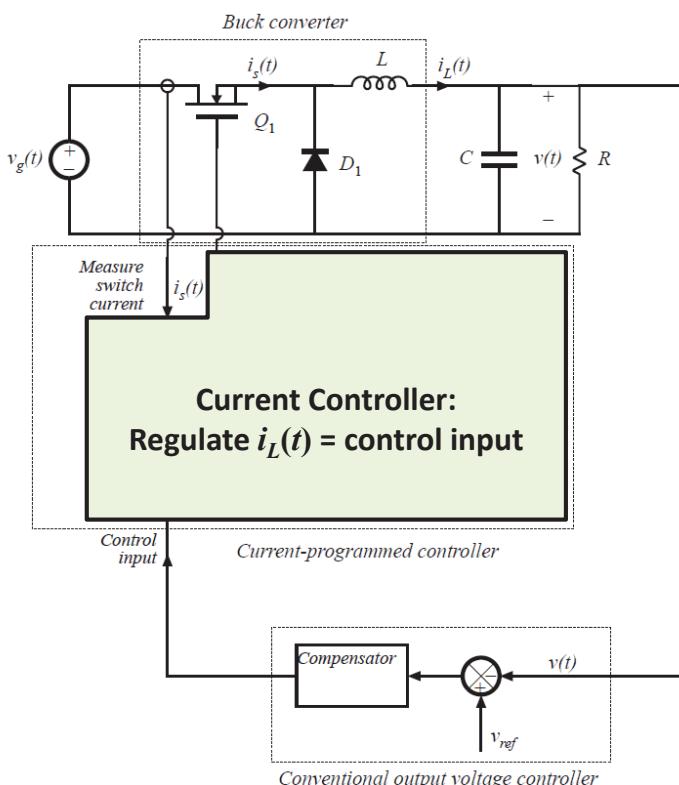
Current Control

**Current Controller:**
Regulate $i_L(t)$ = control input

Measure switch current $i_s(t)$

Control input

Current-programmed controller

Compensator

$v(t)$

v_{ref}

Conventional output voltage controller

Averaged vs CPM

Voltage-Mode

Buck converter

Averaged Current-Mode
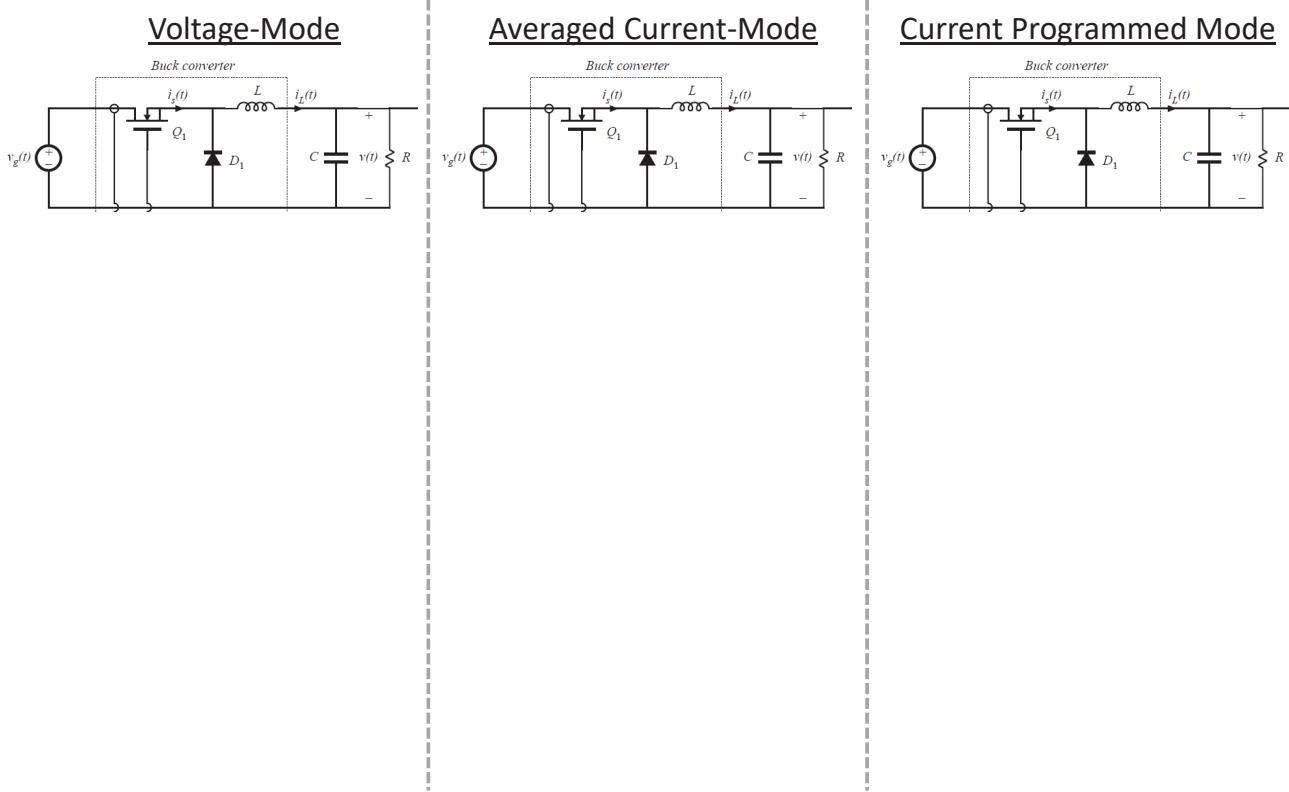
Buck converter

Current Programmed Mode

Buck converter

Current Programmed Control (CPM)
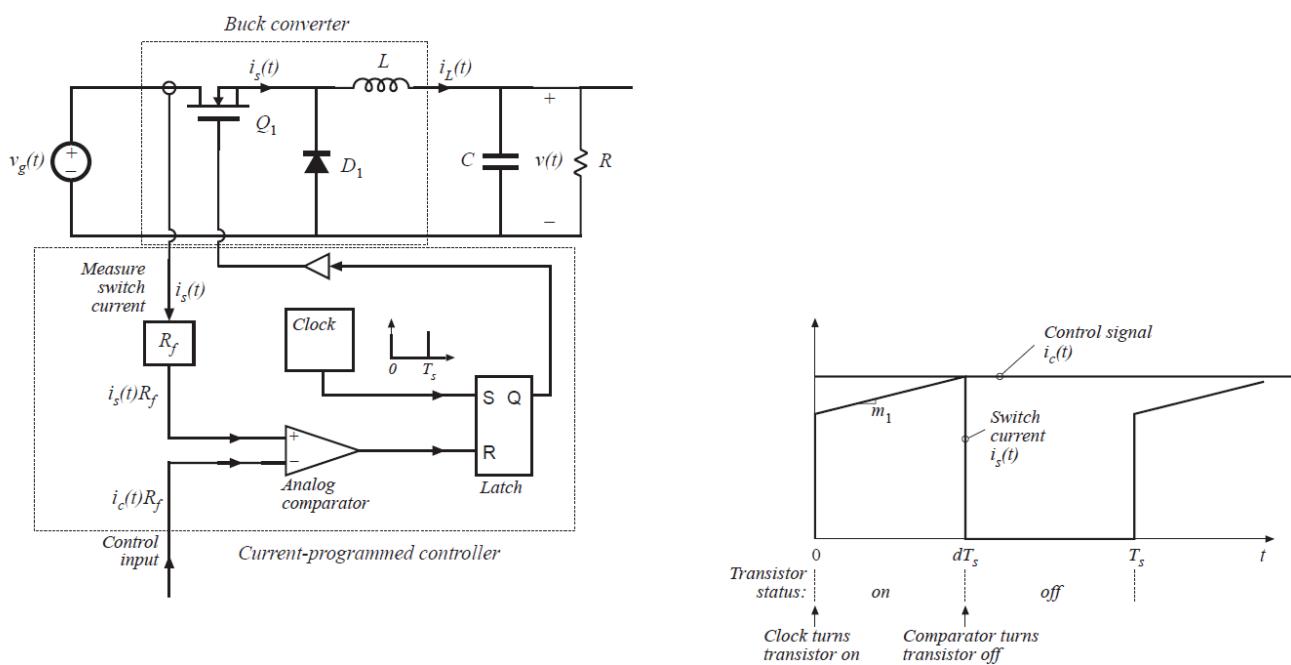
Buck converter

CPM Voltage Loop
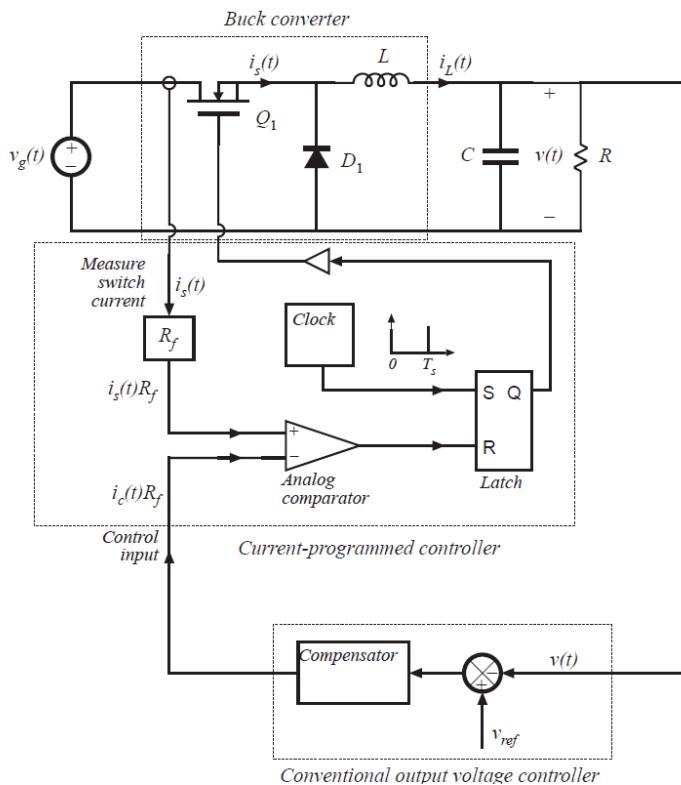
Buck converter

The peak transistor current replaces the duty cycle as the converter control input.

Current-programmed controller

Conventional output voltage controller
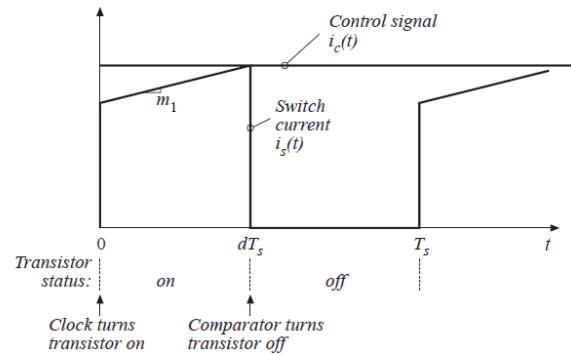
Current Programmed Control

- Covered in Ch. 12 of *Fundamentals of Power Electronics*
- Advantages of current programmed control:
  - Simpler dynamics —inductor pole is moved to high frequency
  - Simple robust output voltage control, with large phase margin, can be obtained without use of compensator lead networks
  - Transistor failures due to excessive current can be prevented simply by limiting $i_c(t)$
  - It is always necessary to sense the transistor current, to protect against overcurrent failures
  - Transformer saturation problems in bridge or push-pull converters can be mitigated
- A disadvantage: susceptibility to noise

A Simple First-Order Model
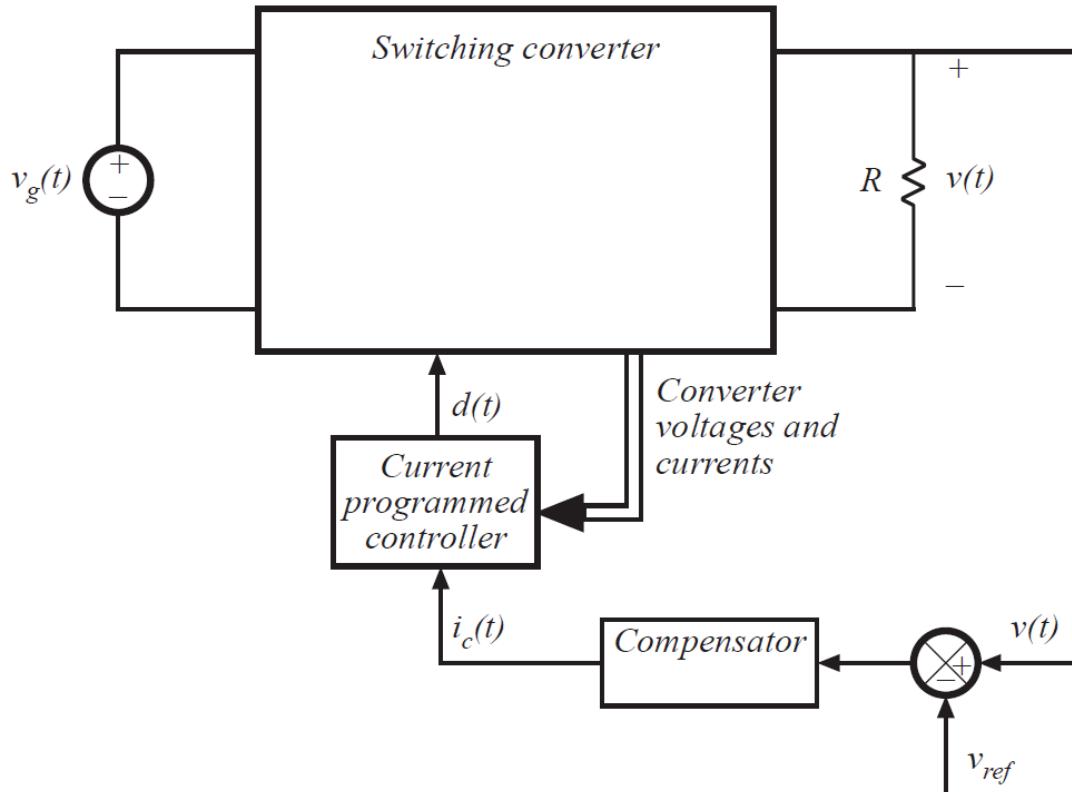
The First-Order Approximation

$$\left\langle i_L(t) \right\rangle_{T_s} = i_c(t)$$

- Neglects switching ripple
- Yields physical insight and simple first-order model
- Accurate when converter operates well into CCM (so that switching ripple is small
- Accurate when artificial ramp (discussed later) is small
- Resulting small-signal relation:

$$i_L(s) \approx i_c(s)$$

Averaged Modeling
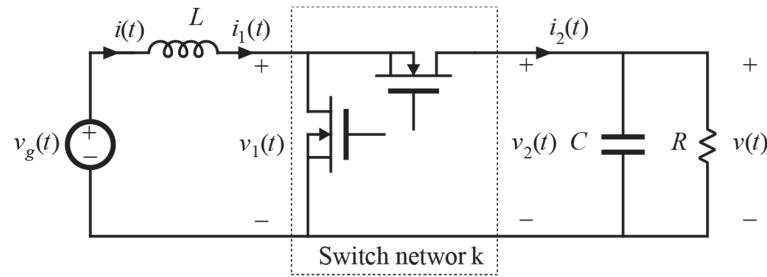
Large-Signal Nonlinear Model

Implementation in LTSpice

V1

1 — V1 (+ |) — 3 B2

1 0 1 ic

G1 ⊕ (+ / −)

2

I=V(1,2)*I(V1)/V(3,4)

4

5

L1
L

V1 (+ / −)
V

ic **out**

C1
C

R2
R

ic
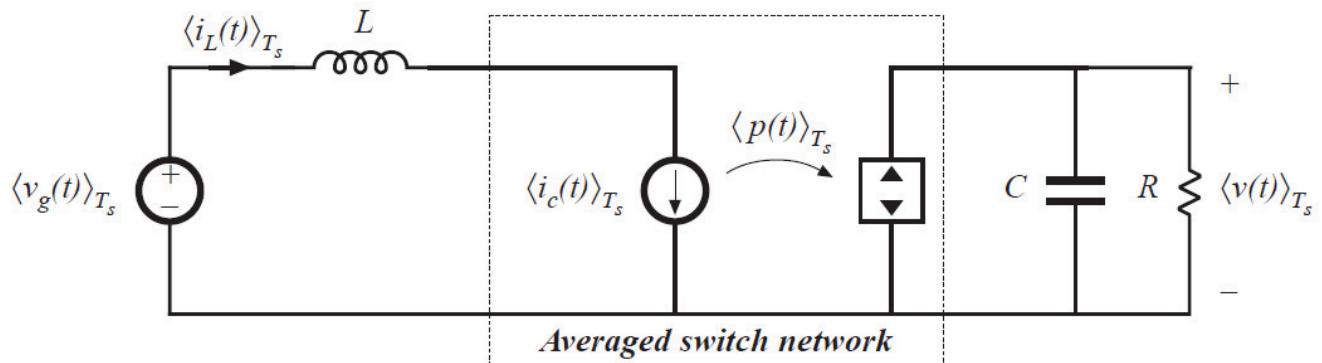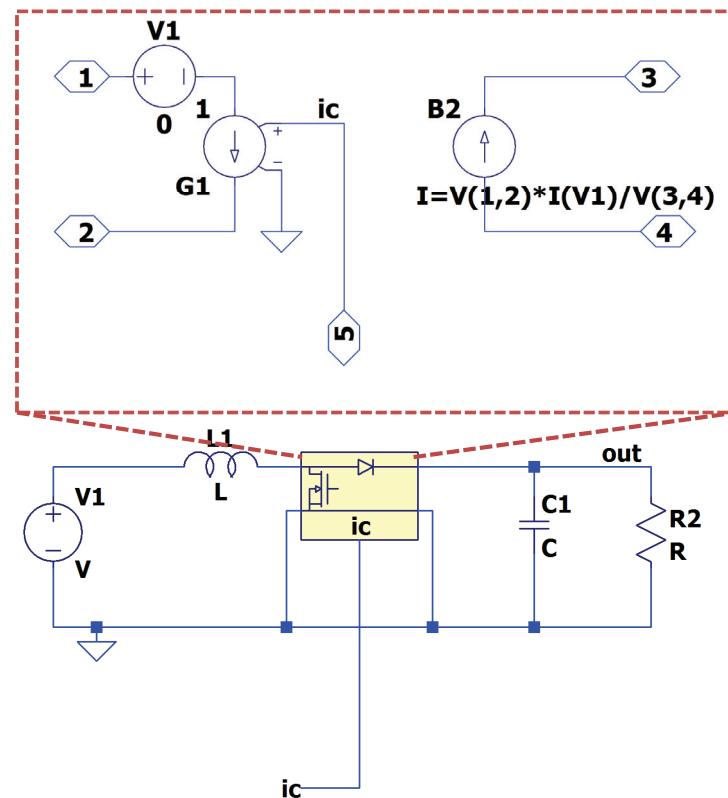
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Averaged, Small-Signal Model

$i(t)$ L $i_1(t)$ $i_2(t)$

$v_g(t)$ $v_1(t)$ $v_2(t)$ C R $v(t)$

Switch networ k
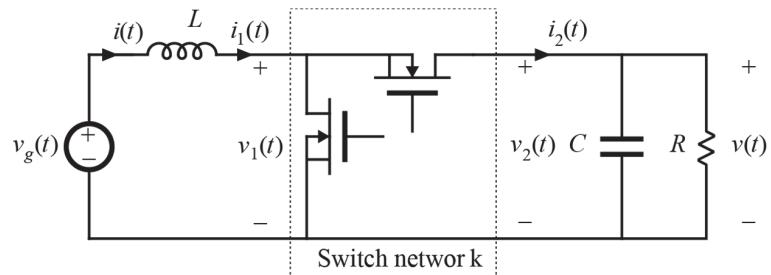
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Boost CCM CPM Small-Signal Model
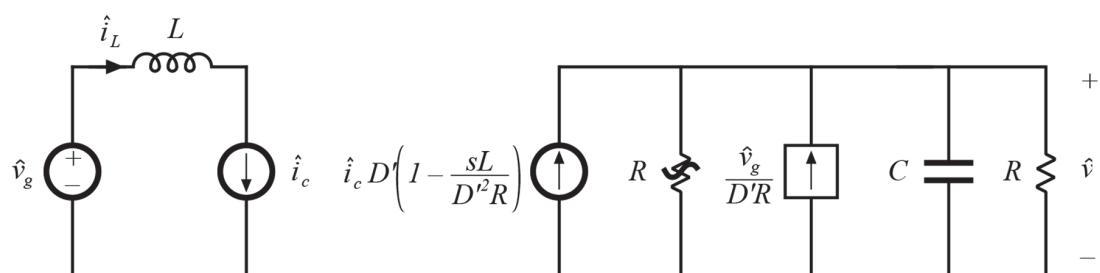
CPM Transfer Functions
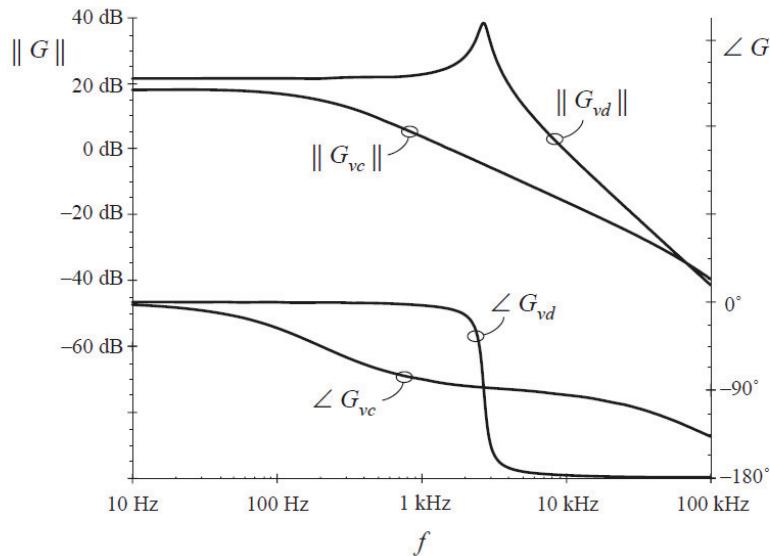

Fig. 12.28 Comparison of CPM control with duty-cycle control, for the control-to-output frequency response of the buck converter example.

Voltage Control
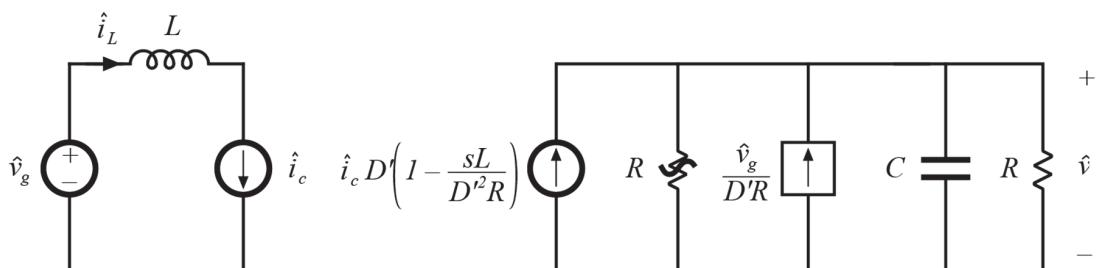
CPM Oscillations for D>0.5

- The current programmed controller is inherently unstable for $D > 0.5$, regardless of the converter topology

- Controller can be stabilized by addition of an artificial ramp

Inductor Current Waveform in CCM
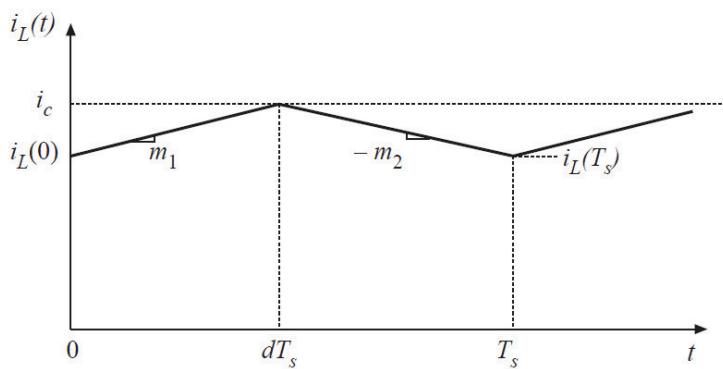
Inductor current slopes m_1 and $-m_2$

buck converter

$$m_1 = \frac{v_g - v}{L} \qquad -m_2 = -\frac{v}{L}$$

boost converter

$$m_1 = \frac{v_g}{L} \qquad -m_2 = \frac{v_g - v}{L}$$

buck–boost converter

$$m_1 = \frac{v_g}{L} \qquad -m_2 = \frac{v}{L}$$

Introducing a Perturbation
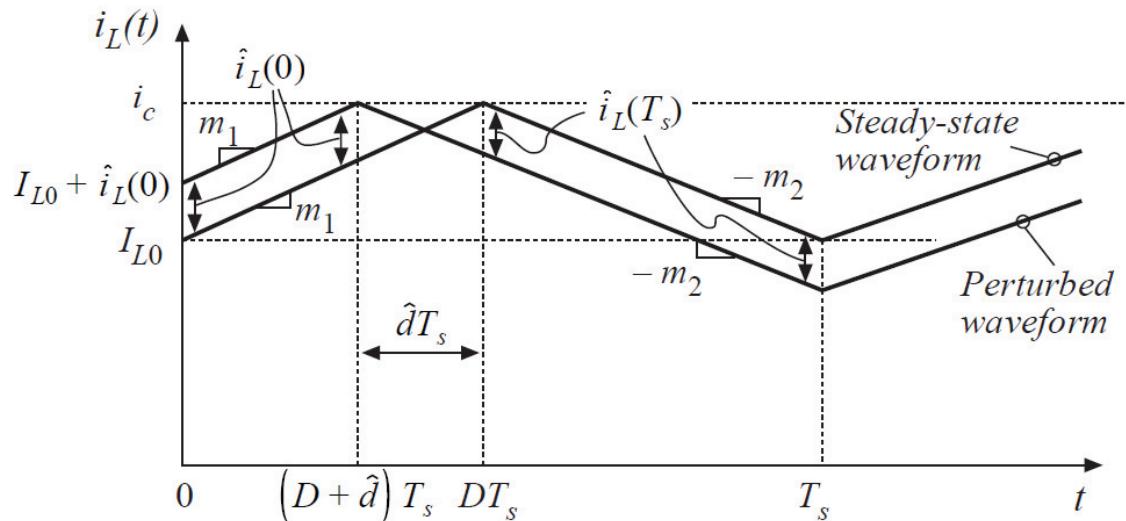
Change in Inductor Current Over T_s
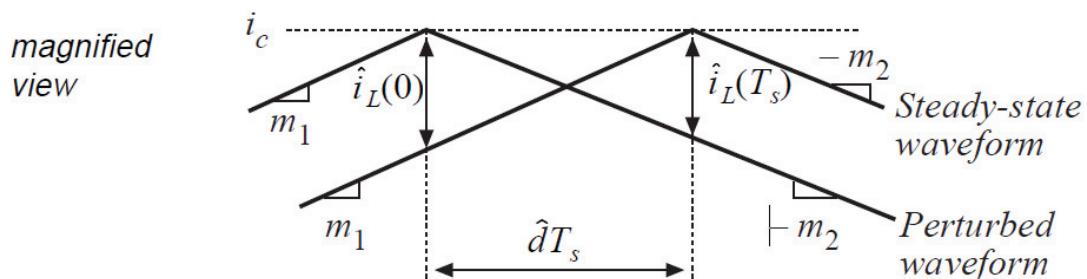
Example: Unstable operation for $D=0.6$

$$\alpha = -\frac{D}{D'} = \left(-\frac{0.6}{0.4}\right) = -1.5$$

$i_L(t)$, i_c, $\hat{i}_L(0)$, I_{L0}, $-1.5\hat{i}_L(0)$, $2.25\hat{i}_L(0)$, $-3.375\hat{i}_L(0)$, 0, T_s, $2T_s$, $3T_s$, $4T_s$, t
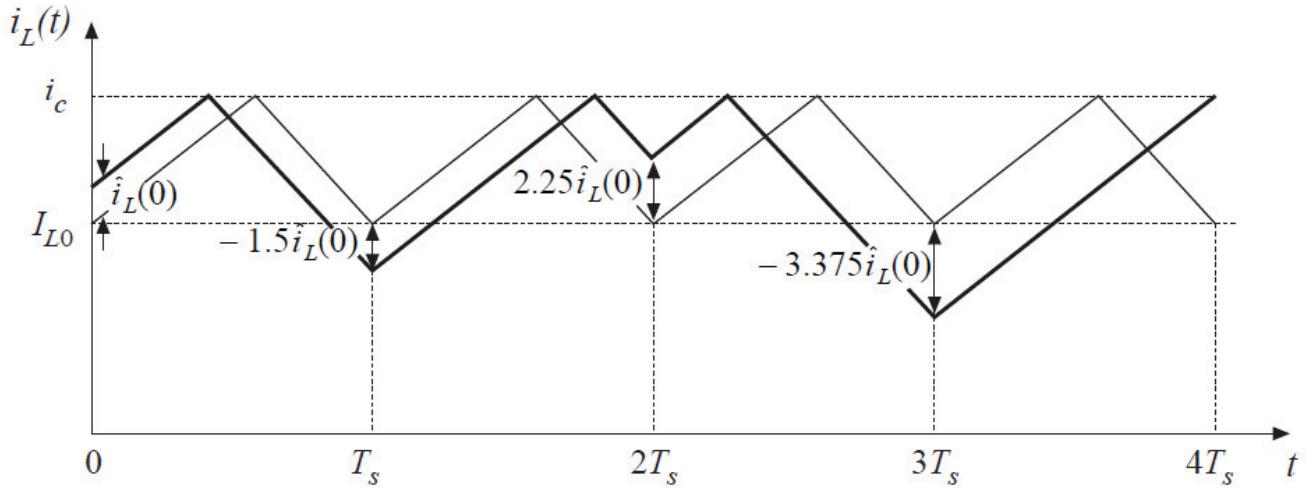
Example: Stable operation for $D=1/3$

$$\alpha = -\frac{D}{D'} = \left(-\frac{1/3}{2/3}\right) = -0.5$$

$i_L(t)$, i_c, $\hat{i}_L(0)$, I_{L0}, $-\frac{1}{2}\hat{i}_L(0)$, $\frac{1}{4}\hat{i}_L(0)$, $-\frac{1}{8}\hat{i}_L(0)$, $\frac{1}{16}\hat{i}_L(0)$, 0, T_s, $2T_s$, $3T_s$, $4T_s$, t
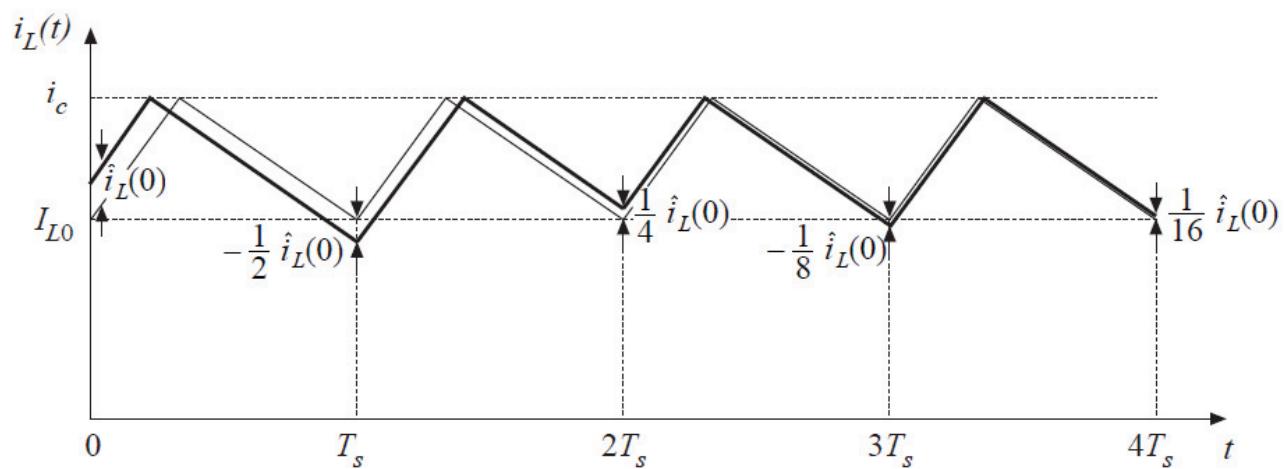
Stabilization Through Artificial Ramp

Buck converter

Current-programmed controller
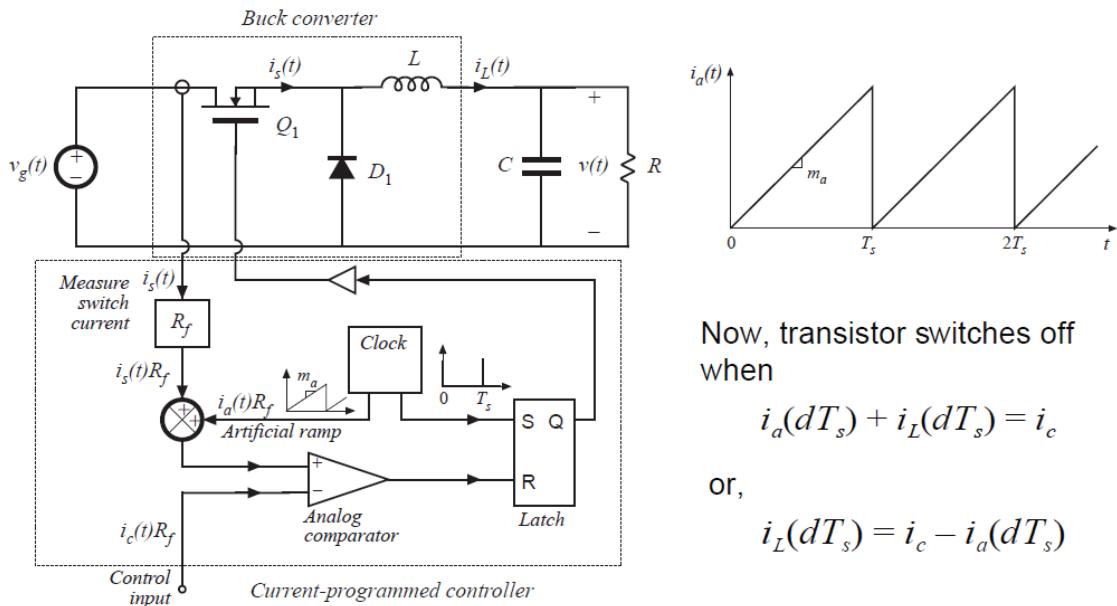
Now, transistor switches off when

$$i_a(dT_s) + i_L(dT_s) = i_c$$

or,

$$i_L(dT_s) = i_c - i_a(dT_s)$$

Final Value of Inductor Current

First subinterval:

$$\hat{i}_L(0) = -\hat{d}T_s\left(m_1 + m_a\right)$$

Second subinterval:

$$\hat{i}_L(T_s) = -\hat{d}T_s\left(m_a - m_2\right)$$

Net change over one switching period:

$$\hat{i}_L(T_s) = \hat{i}_L(0)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right)$$

After n switching periods:

$$\hat{i}_L(nT_s) = \hat{i}_L((n-1)T_s)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right) = \hat{i}_L(0)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right)^n = \hat{i}_L(0)\,\alpha^n$$

Characteristic value:

$$\alpha = -\frac{m_2 - m_a}{m_1 + m_a} \qquad |\hat{i}_L(nT_s)| \to \begin{cases} 0 & \text{when } |\alpha| < 1 \\ \infty & \text{when } |\alpha| > 1 \end{cases}$$

Artificial Ramp: Additional Notes

- For stability, require $|\alpha|<1$

$$\alpha = -\frac{1-\dfrac{m_a}{m_2}}{\dfrac{D'}{D}+\dfrac{m_a}{m_2}}$$

- Common choices:
  - $m_a = 0.5\, m_2$ (stable for all duty cycles)
  - $m_a = m_2$ (deadbeat)
- Artificial ramp decreases sensitivity to noise
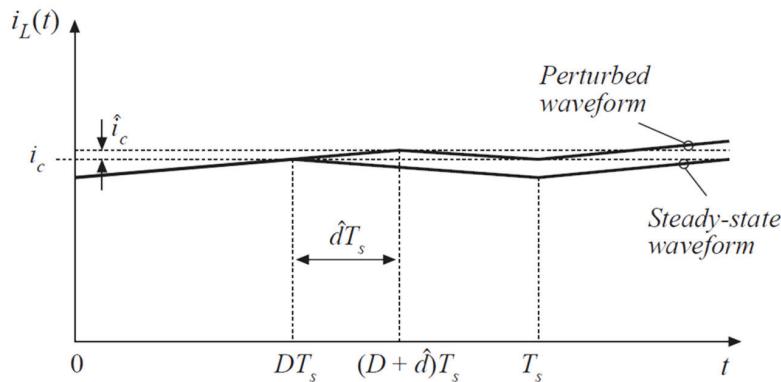
More Accurate Models

- The simple models of the previous section yield insight into the low- frequency behavior of CPM converters
- Unfortunately, they do not always predict everything that we need to know:
  - Line-to-output transfer function of the buck converter
  - Dynamics at frequencies approaching f_s
- More accurate model accounts for nonideal operation of current mode controller built-in feedback loop
- Converter duty-cycle-controlled model, plus block diagram that accurately models equations of current mode controller
- See Section 12.3 for additional info

More Accurate Model

- Simple model assumes $i_L = i_C$ always
- Accounting for ripple, and artificial ramp weakens this approximation
- Using sampled data modeling

$$\frac{\hat{i}_L}{\hat{i}_C} = \frac{1}{1 + \frac{1}{Q_s}\left(\dfrac{s}{2\pi\,{f_s}/{2}}\right) + \left(\dfrac{s}{2\pi\,{f_s}/{2}}\right)^2}$$

Where

$$Q_s = \frac{2}{\pi\left(\dfrac{2}{1-\alpha} - 1\right)}$$

F. Dong Tan and R. D. Middlebrook, "A Unified Model for Current Programmed Converters," IEEE Transactions on Power Electronics, vol. 10, no. 4, July 1995.

Note: Comparison to Datasheet

Application Information (continued)
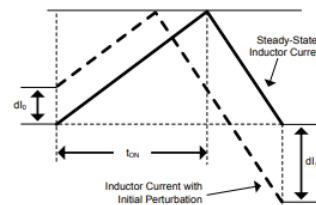
Figure 30. Effect of Initial Perturbation when $dI_1/dI_0 < -1$

dI_1/dI_0 can be calculated as:

$$\frac{dI_1}{dI_0} = 1 - \frac{1}{K} \tag{19}$$

The relationship between dI_1/dI_0 and K factor is illustrated in the graphic below.
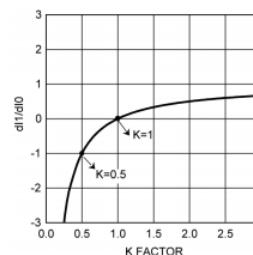
Figure 31. dI_1/dI_0 vs K Factor

The absolute minimum value of K is 0.5. When K<0.5, the amplitude of dI_1 is greater than the amplitude of dI_0 and any initial perturbation results in sub-harmonic oscillation. If K=1, any initial perturbation will be removed in one switching cycle. This is known as one-cycle damping. When -1<dI_1/dI_0<0, any initial perturbation will be under-damped. Any perturbation will be over-damped when 0<dI_1/dI_0<1.

Application to Experiment 4
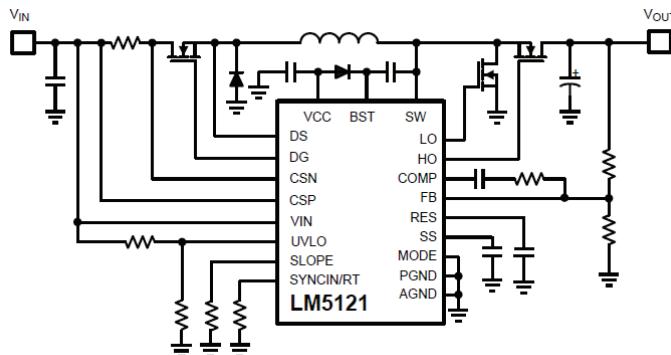
- Complex switching controller
- **Read** the datasheet first

Startup: Switching
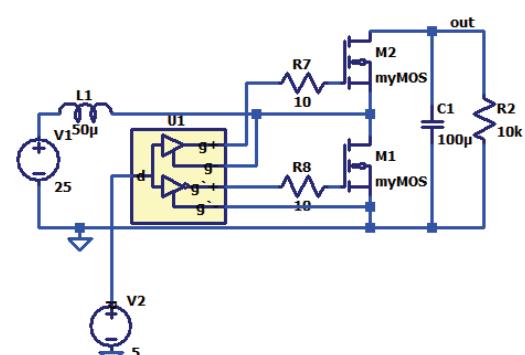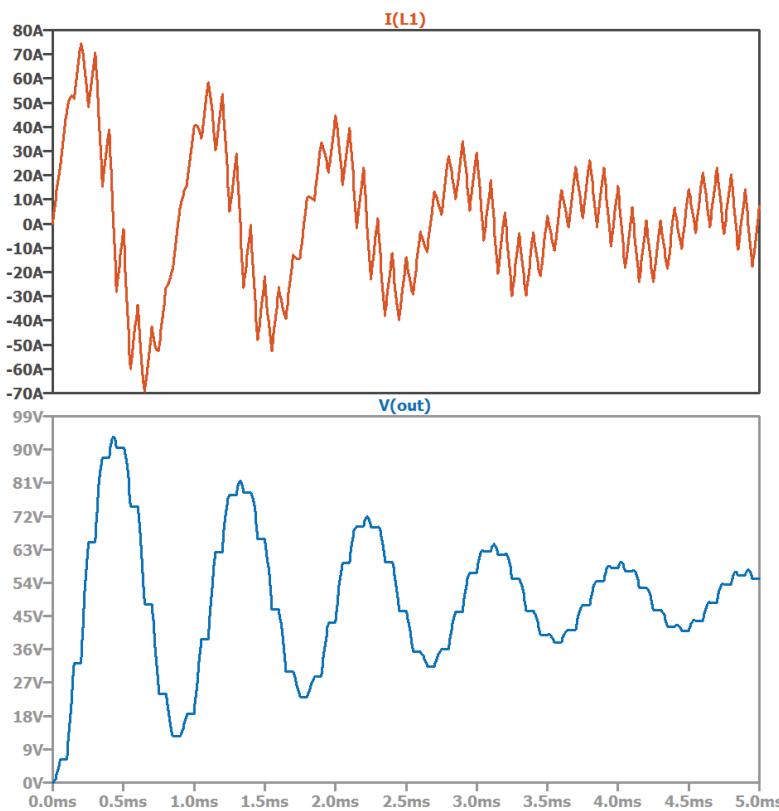
Startup: No Switching
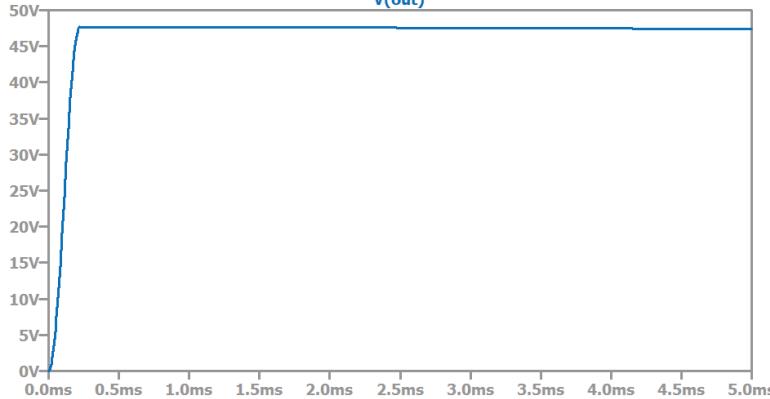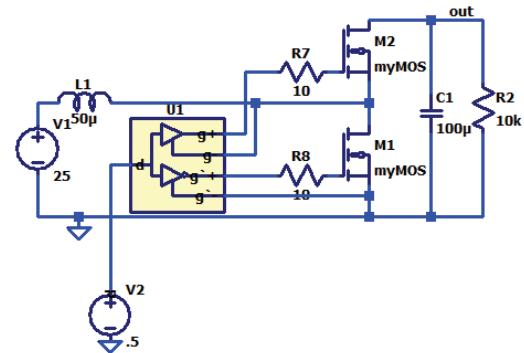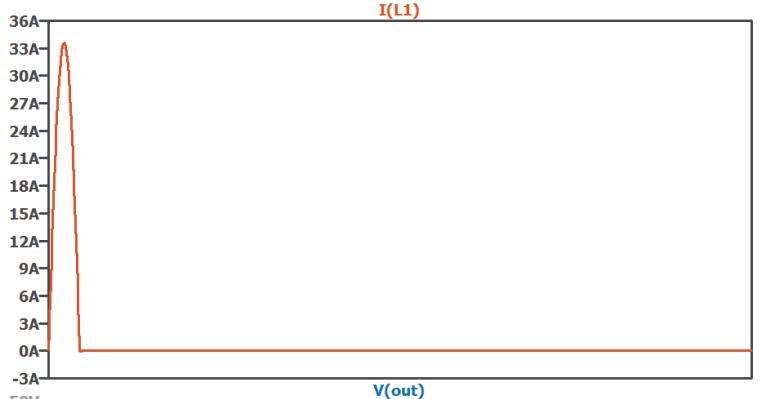
Short-Circuit: Switching
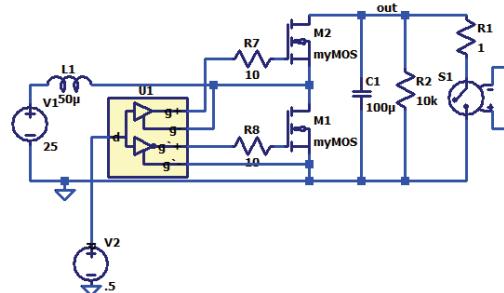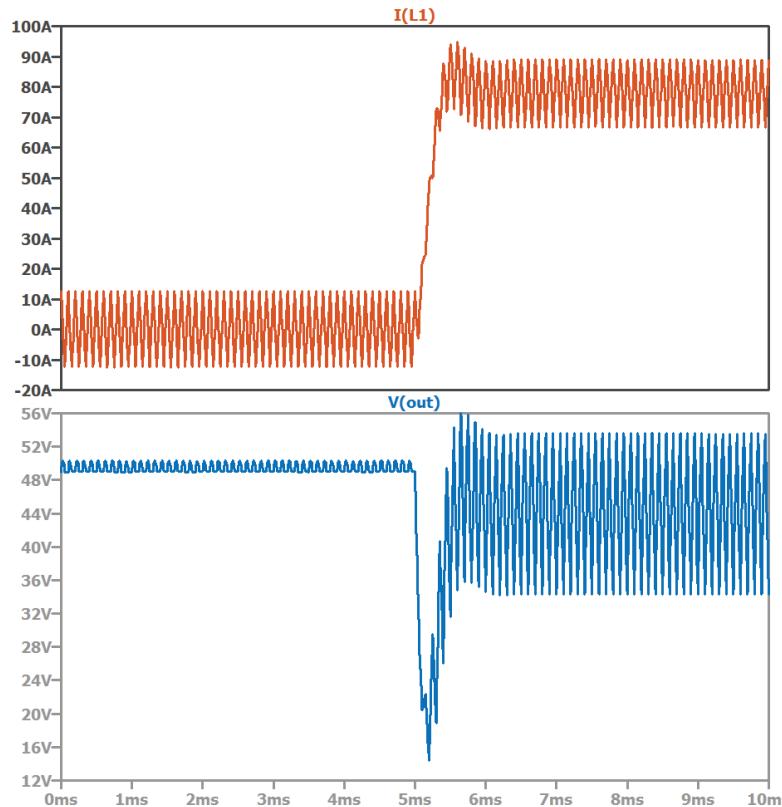
Short-Circuit: No Switching

LM5121: Functionality

VIN
CIN
RUV2
RUV1
RSLOPE
CHF
CCOMP RCOMP
CSS

10µA
1.2V
UVLO
0.4V/0.3V
SLOPE
SLOPE Generator
$V_{SLOPE} = \dfrac{6 \times 10^9}{R_{SLOPE} \times F_{SW}}$

VIN   CSP
RS
CSN
CS AMP
A=10

STANDBY
SHUTDOWN

DG Charge Pump
25µA
1.1V – AMP +
Inrush Current Limiter
1.6V/0.11V +
Circuit Breaker Comparator

QD
DG   DS
VIN

VCC Regulator
VIN   VCC
BST Charge Pump
BST

DF   LIN

DBST   CVCC

CBST   QH   VOUT
COUT

VSENSE1
VSENSE2

COMP
1.2 V – +
FB
– + ERR AMP
1.2V
SS
10µA

750mV
– +
C/L Comparator

PWM Comparator

ZCD threshold
– +

Level Shift Diode Emulation

HO
SW

1.2V
700k
MODE
100k
20mV + –
Skip Cycle Comparator
40mV Hysteresis
1.2V – +
Diode Emulation Comparator

CLK
S Q
R Q̄
PWM

Adaptive Timer

VCC
LO

QL

Restart Timer
30µA
10µA
RES
5µA

RFB2
RFB1
CRES

CLK
Clock Generator /SYNC Detector
SYNCIN/RT
RT
AGND   PGND

LM5121
Diode Emulation

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Internal Functional Model in LTSpice
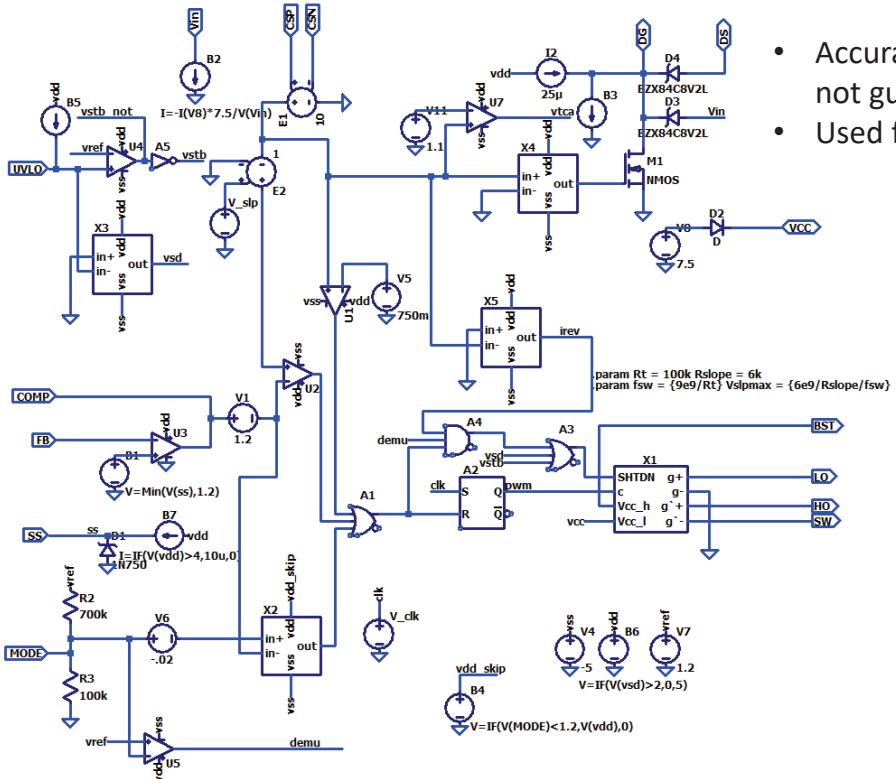
- Accuracy/functionality not guaranteed
- Used for insight only

Vin CSP CSN DG DS

B2 I=-I(V8)*7.5/V(Vin)

vdd vstb_not B5
UVLO vref U4 A5 vstb
X3 in+ out vsd in-
V_slp E1 10 E2 1

I2 25μ D4 EZX84C8V2L D3 EZX84C8V2L Vin
vdd V11 1.1 U7 vtca B3 M1 NMOS
X4 in+ out in-
V8 7.5 D2 D VCC

V5 750m U1
vss vdd
X5 in+ out irev in-
.param Rt = 100k Rslope = 6k
.param fsw = {9e9/Rt} Vslpmax = {6e9/Rslope/fsw}

COMP U3 V1 1.2 U2
FB B1 V=Min(V(ss),1.2)

demu A4 vsd A3 vstb BST
clk A2 S Q pwm X1 SHTDN g+
A1 R Q c g- LO
Vcc_h g`+ HO
vcc Vcc_l g`- SW

SS ss D1 vdd B7
I=IF(V(vdd)>4,10u,0) 1N750

R2 700k vref
V6 -.02 X2 vdd_skip
MODE in+ out in- V_clk clk
R3 100k
vss vref V4 -5 B6 vdd V7 1.2
V=IF(V(vsd)>2,0,5)
vdd_skip B4
V=IF(V(MODE)<1.2,V(vdd),0)
vref U5 demu

In-Circuit Simulation

.model mysw sw(Von=3 Voff=2 Ron=.1 Roff = 1Meg)

.model myMOS VDMOS(Rg=1 Vto=4.5 Rd=14m Rs=10m Rb=17m Kp=30 Cgdmax=.5p Cgdmin=.05n Cgs=.2n Cjo=.03p Is=88p)

.tran 1 uic
.ic V(out)=0
.ic I(L1)=0
.ic V(ss) =0

out M2 myMOS R8 1
R3 10 C3 500μ R2 10 S1 V3 PULSE(0 5 250m 1p 0 1)
M1 myMOS
R4 10

V1 25 R9 90k R1 .005 M3 myMOS L1 100μ D2 D
vcc
V2 12 C4 1μ ss R10 10k C1 10n R7 1k
Vin CSP CSN DG DS
UVLO VCC
COMP BST D1 D C2 1μ
FB HO
SS SW
MODE LO X1
vcc

R5 97.6k
R6 2.4k

Sim Results

I(L1)   I(D2)

Output Short

V(out)
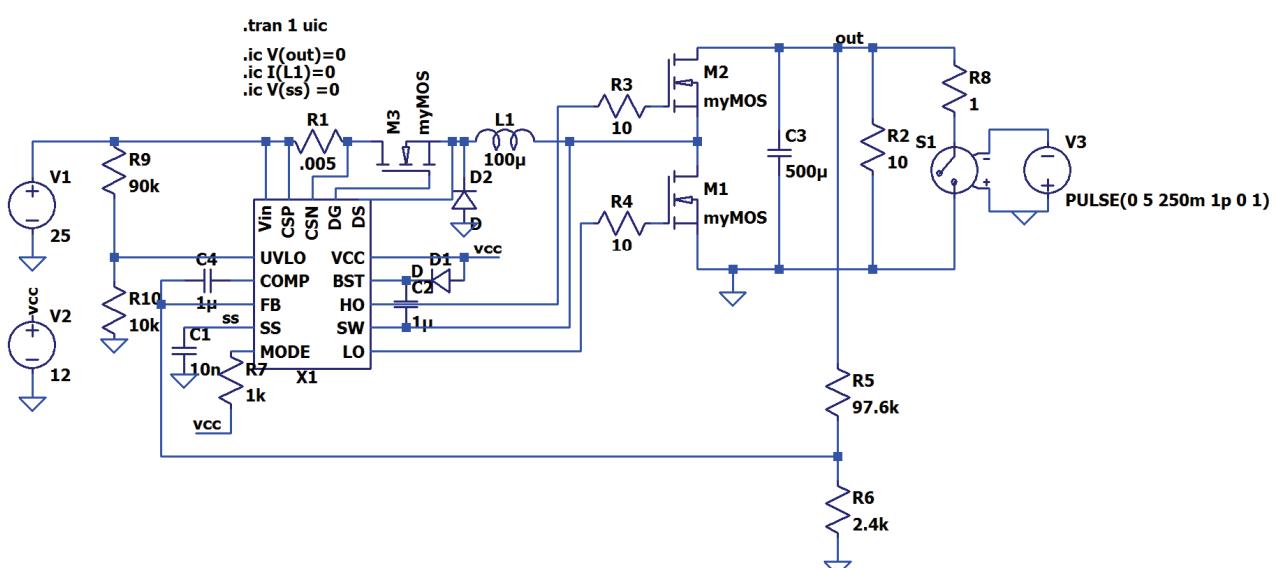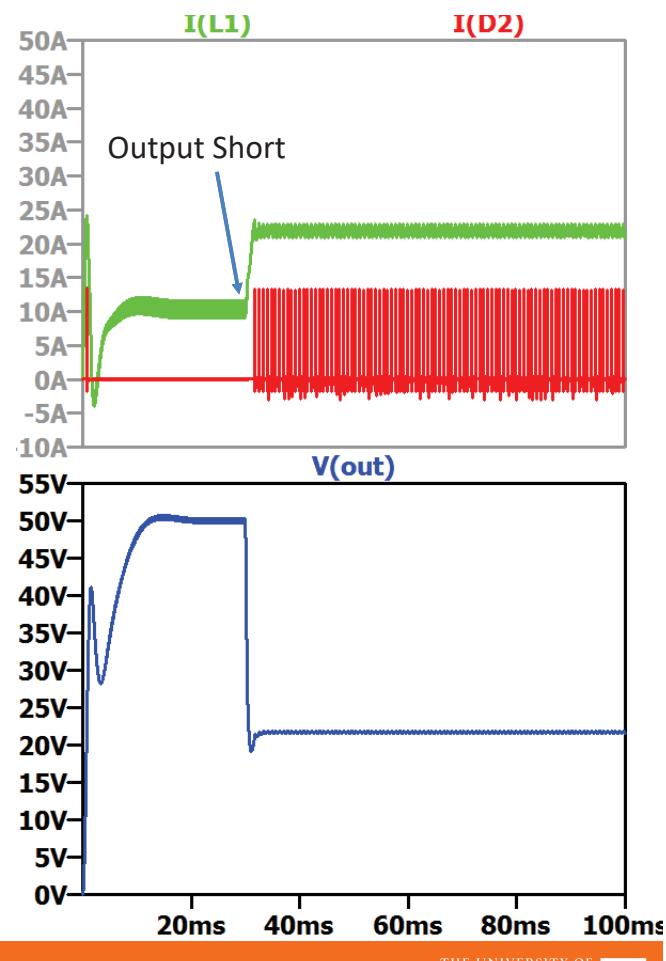
A Tip: Debug Internal of Subcircuit
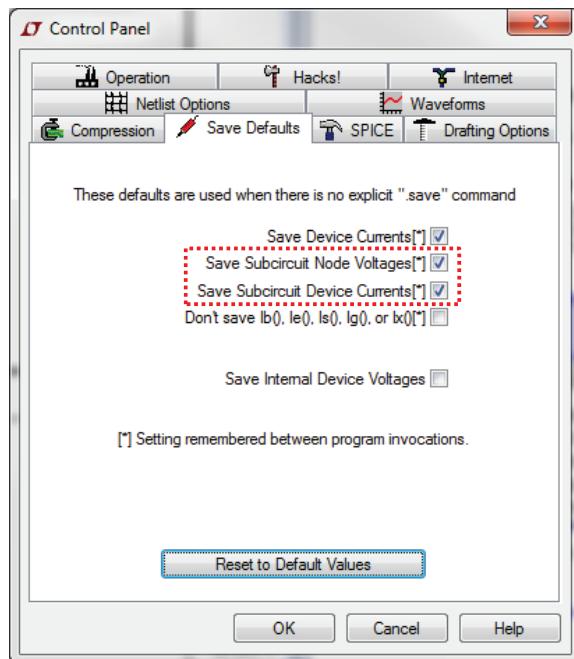
Experiment 4: Gate Driver Selection
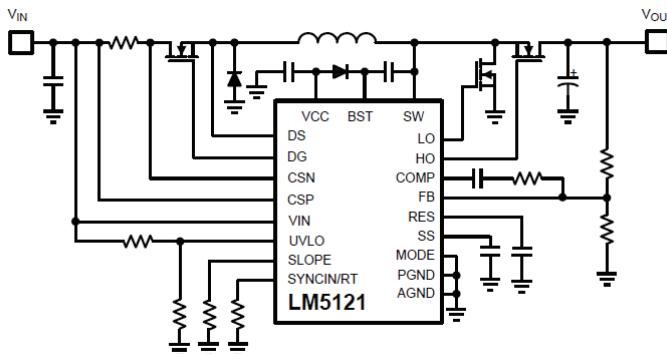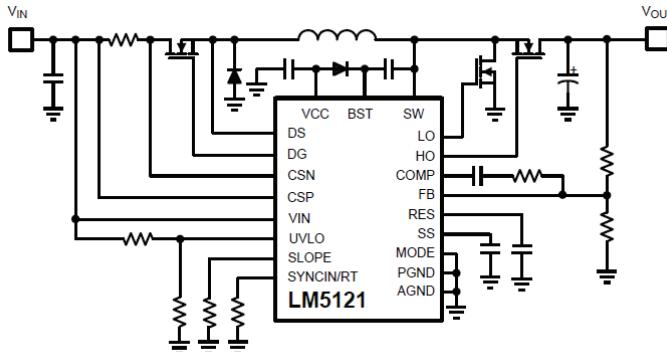
Experiment 4: Closing the Loop

- Closed-loop operation in steps
    1. Open-loop operation with LM5121 modulator
        - Requires "tricking" LM5121
    2. Closed-loop current regulation
    3. Closed-loop voltage and current regulation

Open-Loop Operation
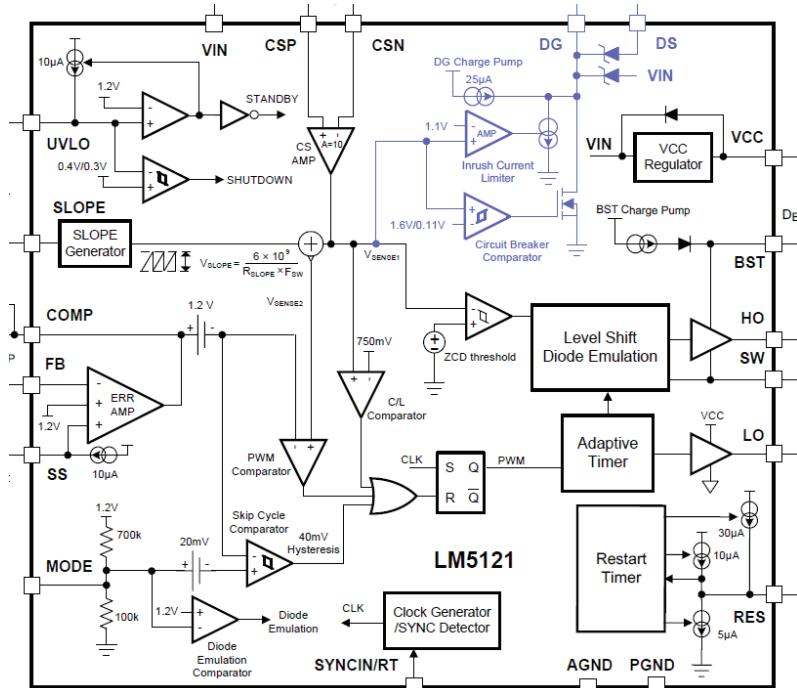
Setting the Electronic Load