PCB Layout

ECE 482 Lecture 5
March 14, 2018

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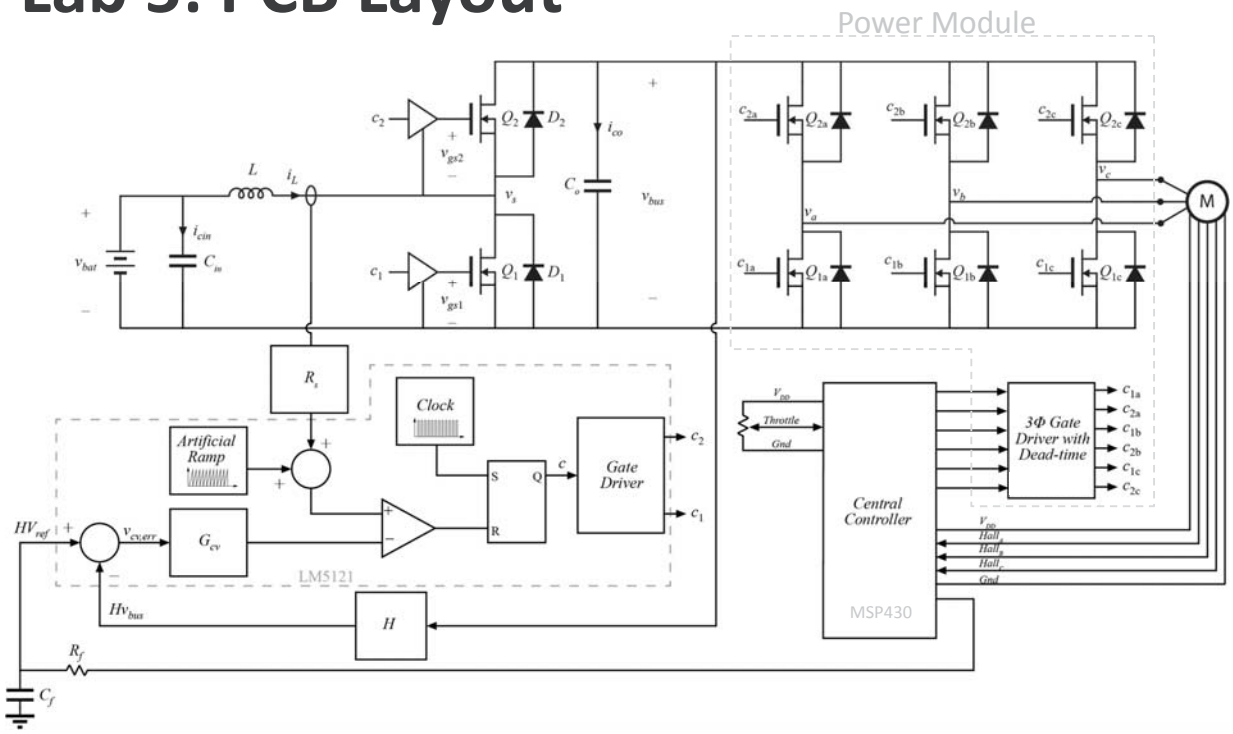
Announcements

- Prelab 5
  - Decide on System Improvements
  - Redesign using GaN Devices
- Midterm after Experiment 5
  - Open note, book, instructor
- Today: Experiment 5
  - No report; deliverables are layout files and BOM

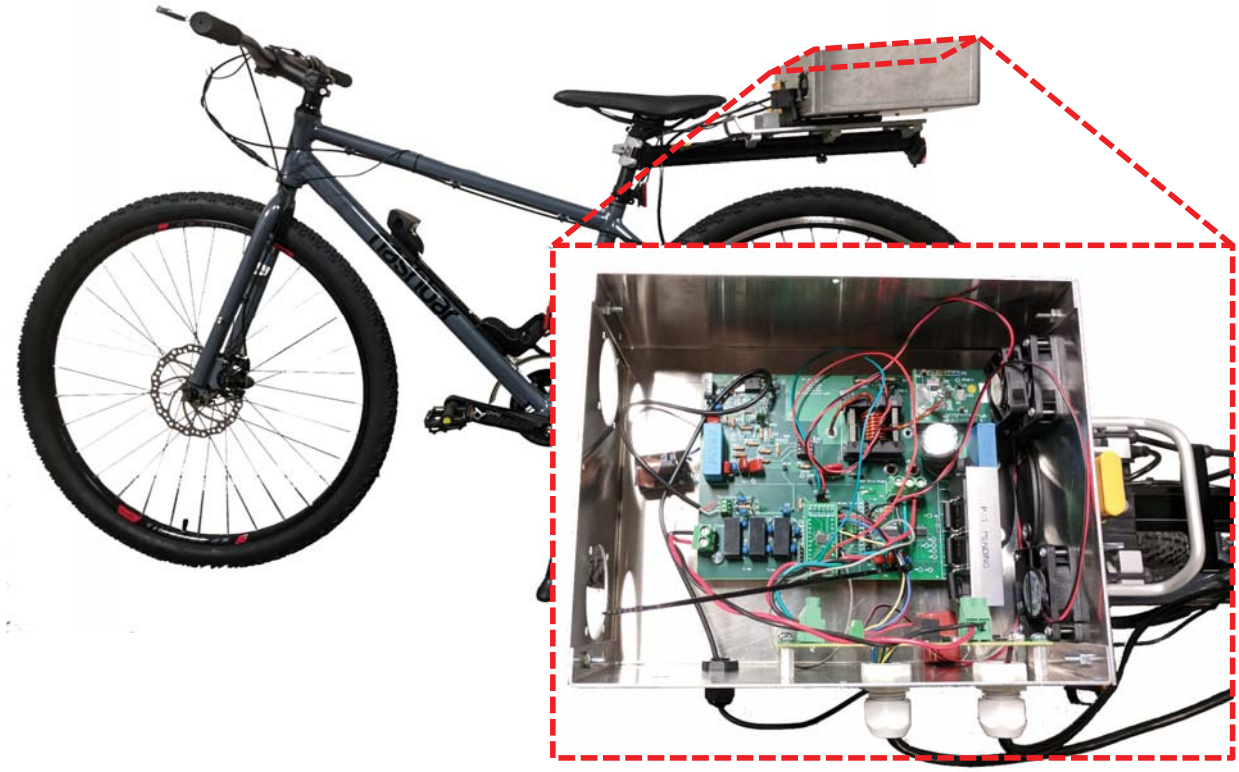
Lab 5: PCB Layout



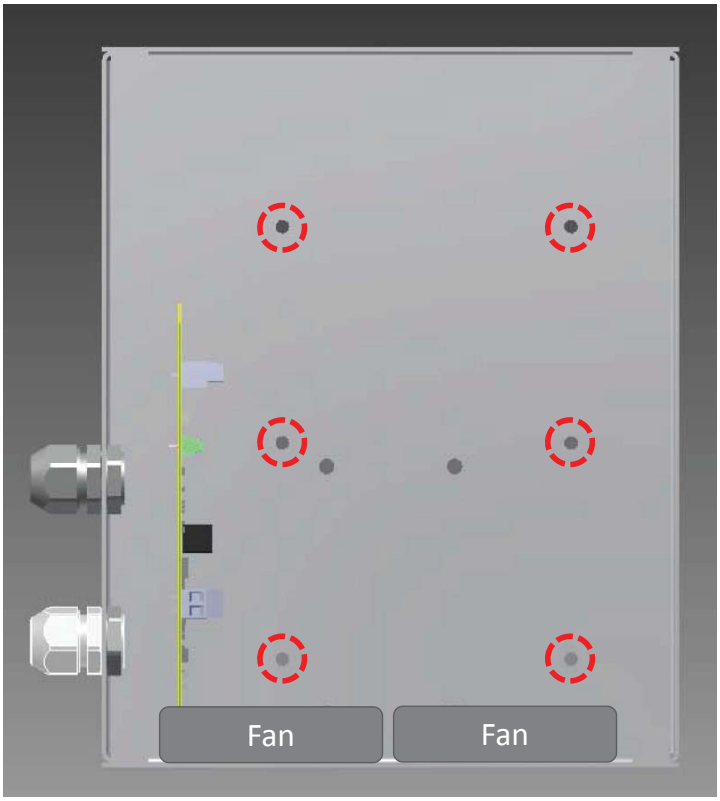
Design Modification

- You may order additional parts, at reasonable cost/benefit
  - Will need to provide a listing of parts from digikey with final Exp 5 files
  - May not exceed $350 for parts and PCB
- Reuse components from lab kit where possible
- Use SMD ceramic, low ESR caps for power stage and gate drive decoupling

Circuit Enclosure

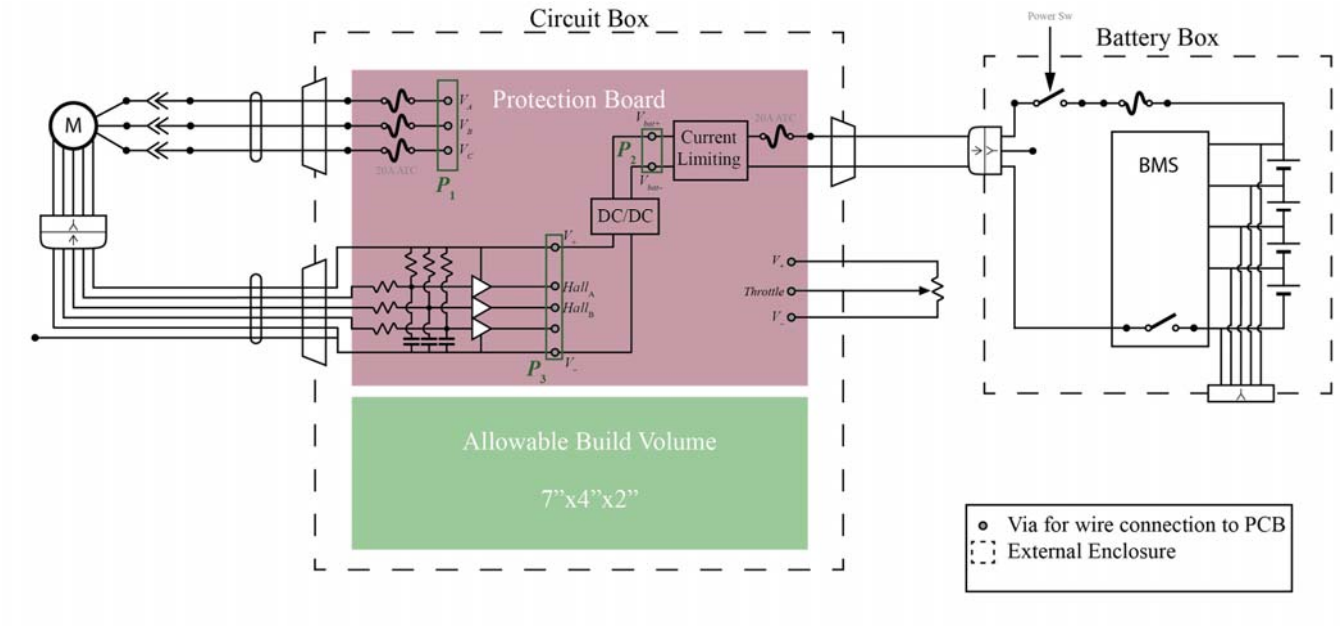


Circuit Enclosure - Mounting



Fans – 1 W each, need to be powered from your board

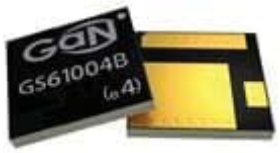
Circuit Connections



Prelab for Experiment 5: Redesign with GaN

GaN Systems GS61004T

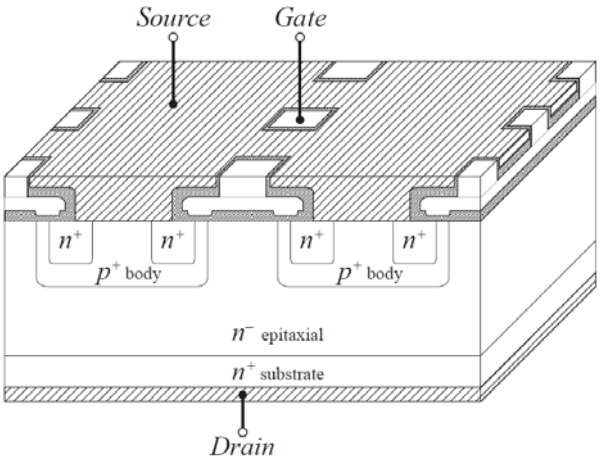
- 15 mOhm
- 100V/40A
- Q_g = 6.2 nC
- C_{oss} = 140 pF (50V)



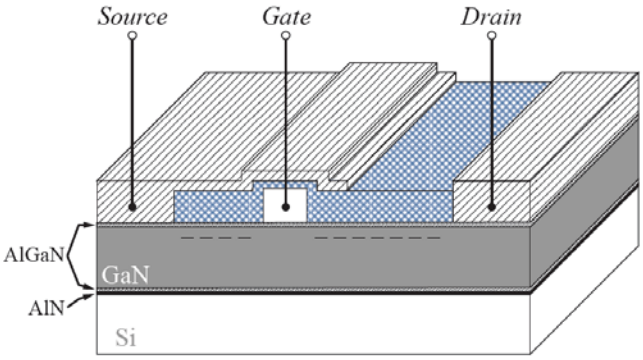
EPC EPC2001C

- 7 mOhm
- 100V/36A
- Q_g = 9 nC
- C_{oss} = 375 pF (80V)

GaN Devices



Vertical Silicon Power MOSFET



Lateral GaN HEMT

- No body diode (reverse conduction due to $V_{gd} > V_{gd,th} \approx 2V$)
  - Use antiparallel (schottky) diode or precise dead time
- Significantly faster switching

Designing with GaN

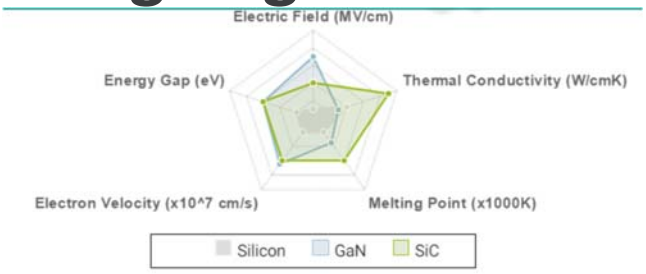
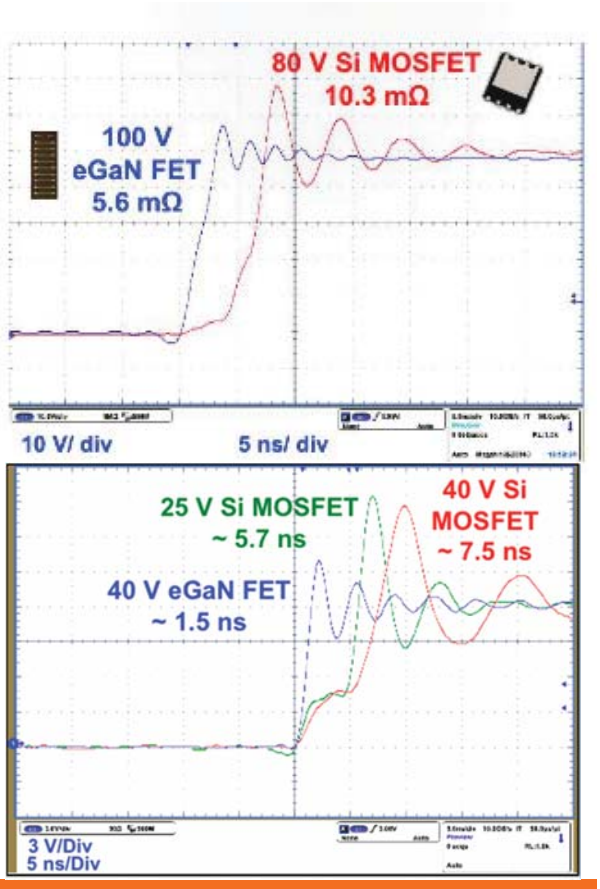


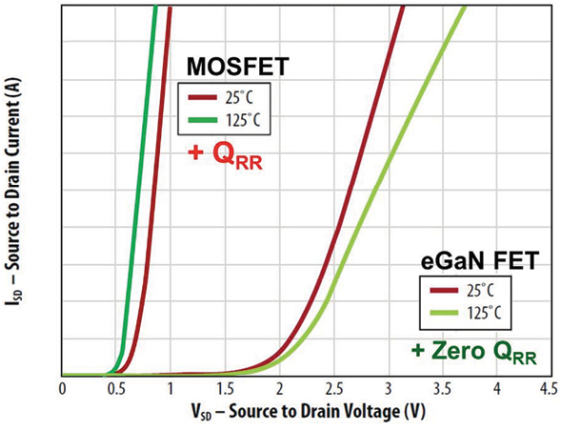
Fig. 1: Material properties of silicon, silicon carbide, and gallium nitride.

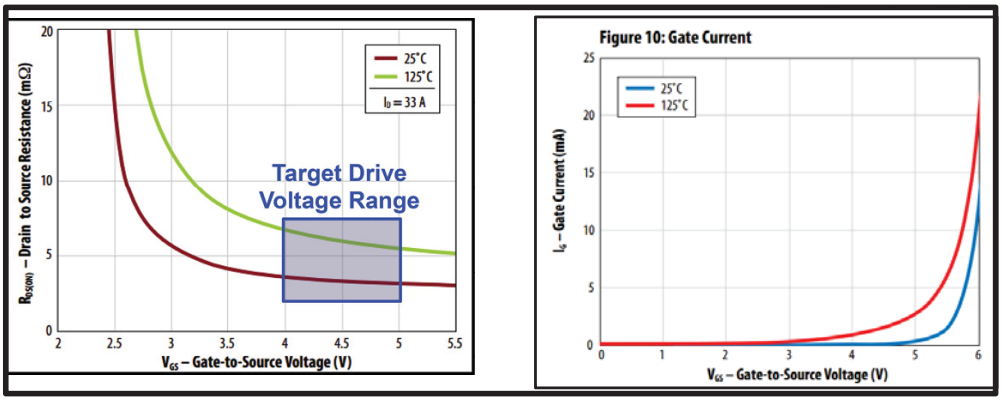
- Because of high electric breakdown field and high electron velocity, GaN devices with comparable R_{on} can be significantly smaller and switch must faster.
- Need **very** good layout to prevent ringing from causing overvoltage and device failure.
- More information:
  - http://potenntial.eecs.utk.edu/About.php?topic=PowerSemiconductors



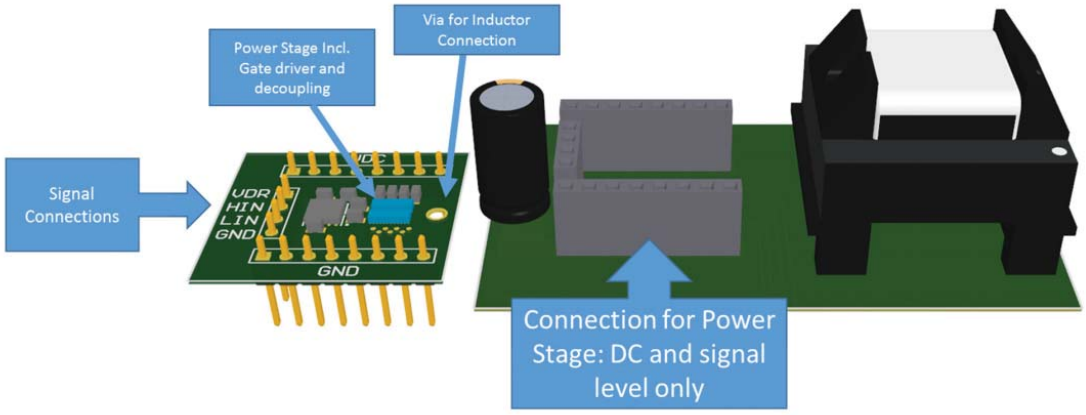
GaN Design Issues

1. Reverse conduction mechanism
2. Sensitivity to parasitics
3. Gate robustness
4. Small size -> Thermal, soldering difficult





Daughter Boards



Motor Control

- Motor control is open-loop
- User throttle monotonically increases power
  - Controlled as BLDC motor
- Two options to change throttle
  - Alter boost output voltage
  - Alter duty cycle of motor drive

Motor Driver: Trapezoidal Control

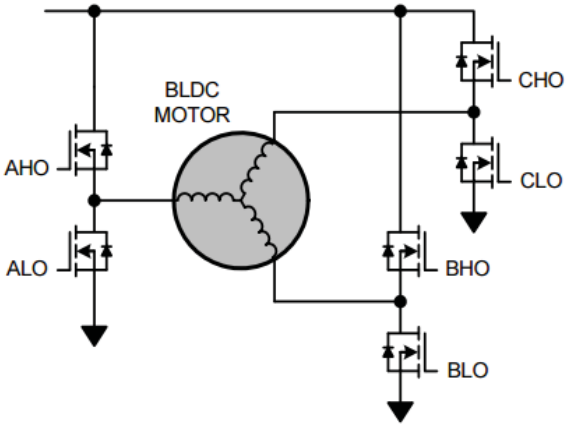


FIGURE 3. BASIC BLDC MOTOR POWER TOPOLOGY

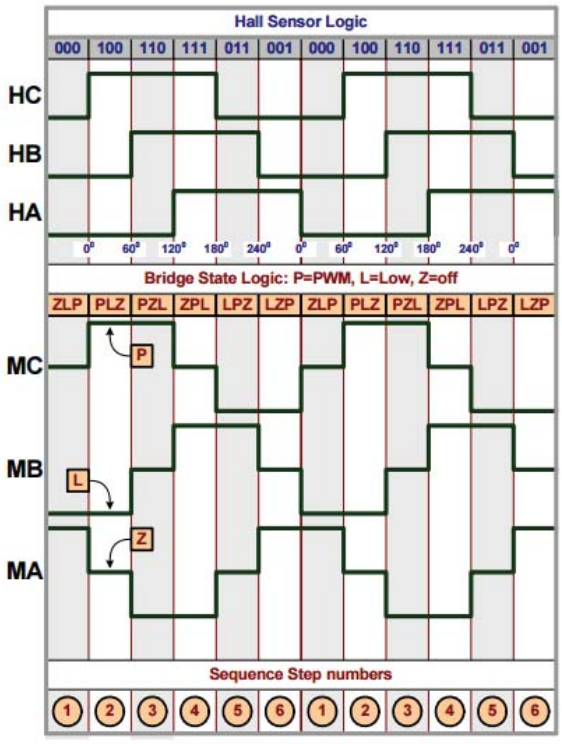


FIGURE 4. HALL SENSOR LOGIC vs BRIDGE STATE LOGIC

Trapezoidal Control: HF PWM

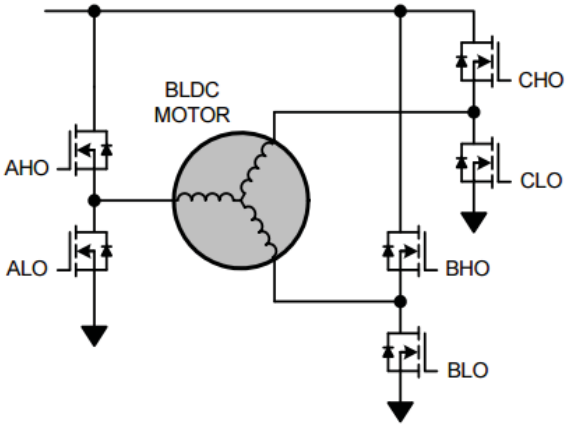


FIGURE 3. BASIC BLDC MOTOR POWER TOPOLOGY

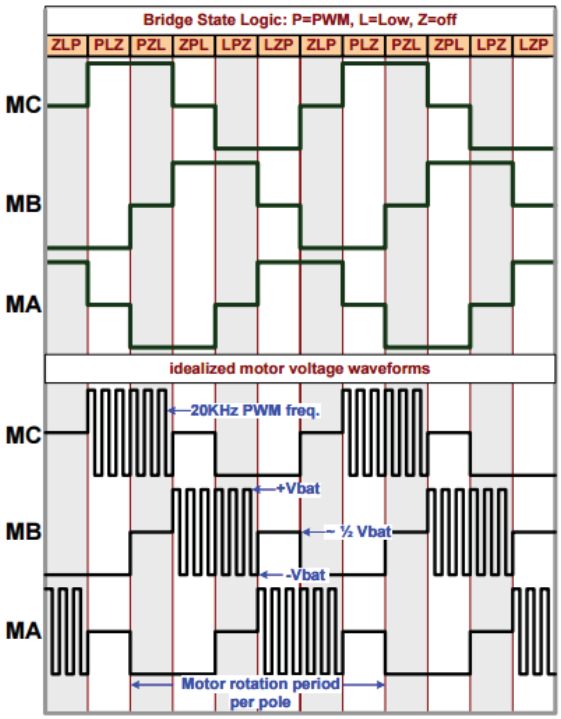
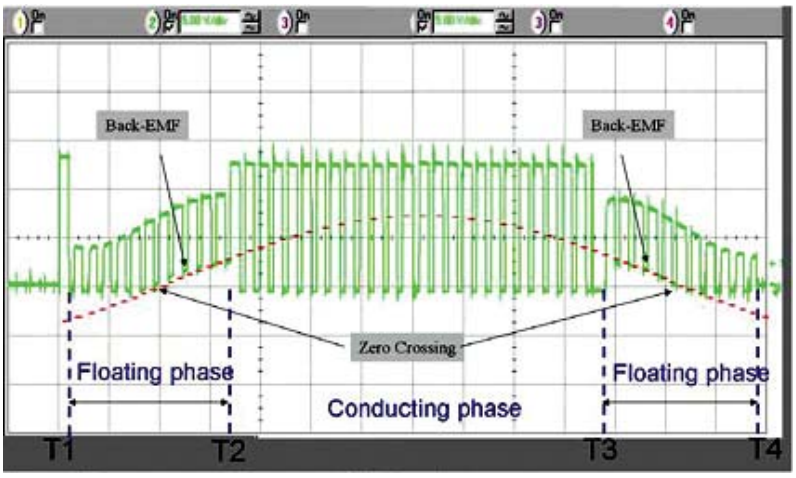


FIGURE 5. BRIDGE STATE LOGIC vs MOTOR VOLTAGE

A Note: Reflected Voltages



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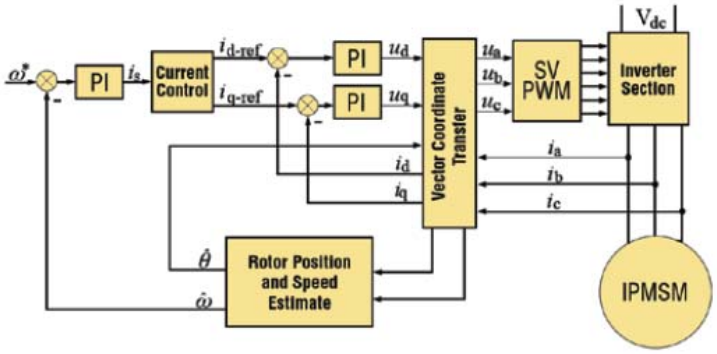
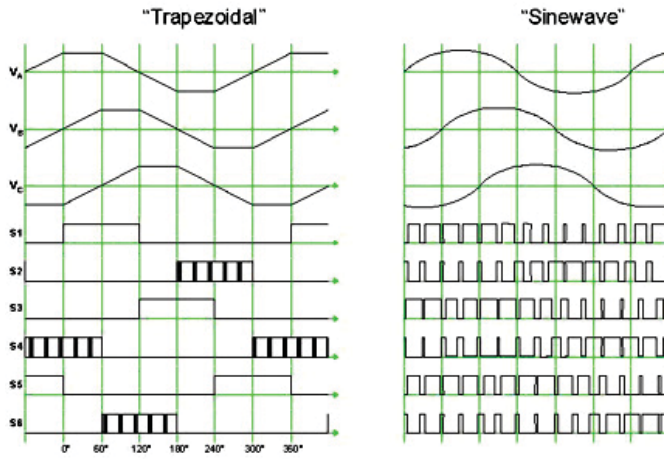
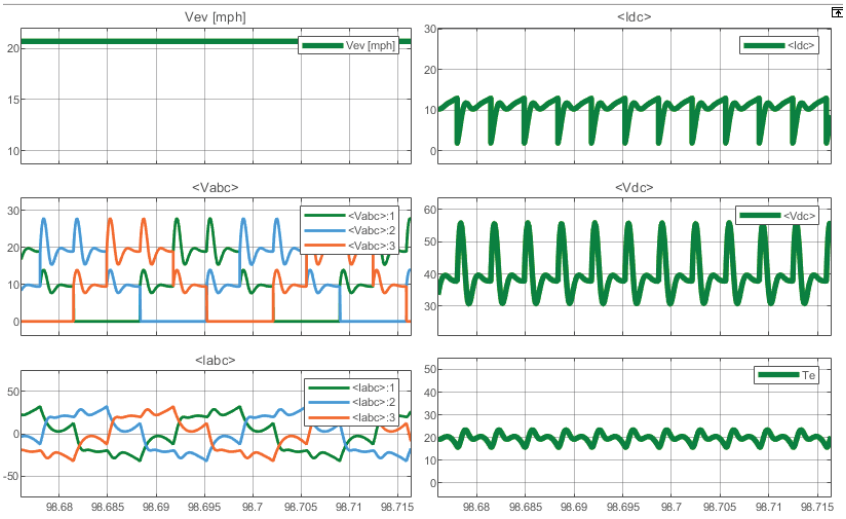
Sinusoidal (Vector) Control





DC Bus Ripple – Trapezoidal Control

- C_{DC} = 100µF



DC Bus Ripple – Sinusoidal Control

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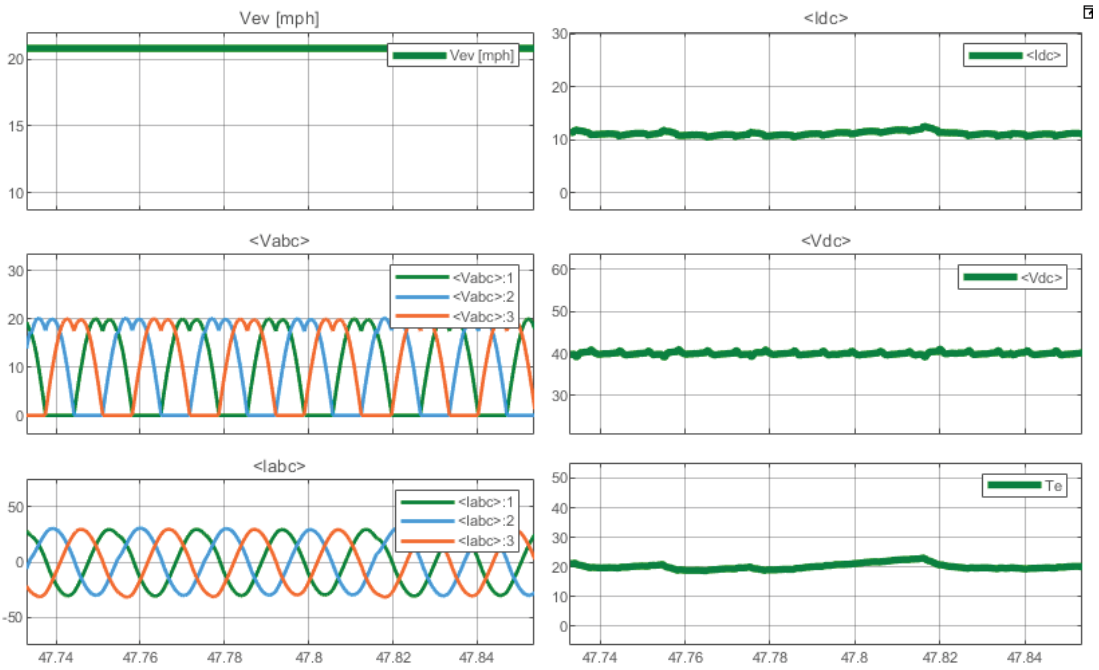
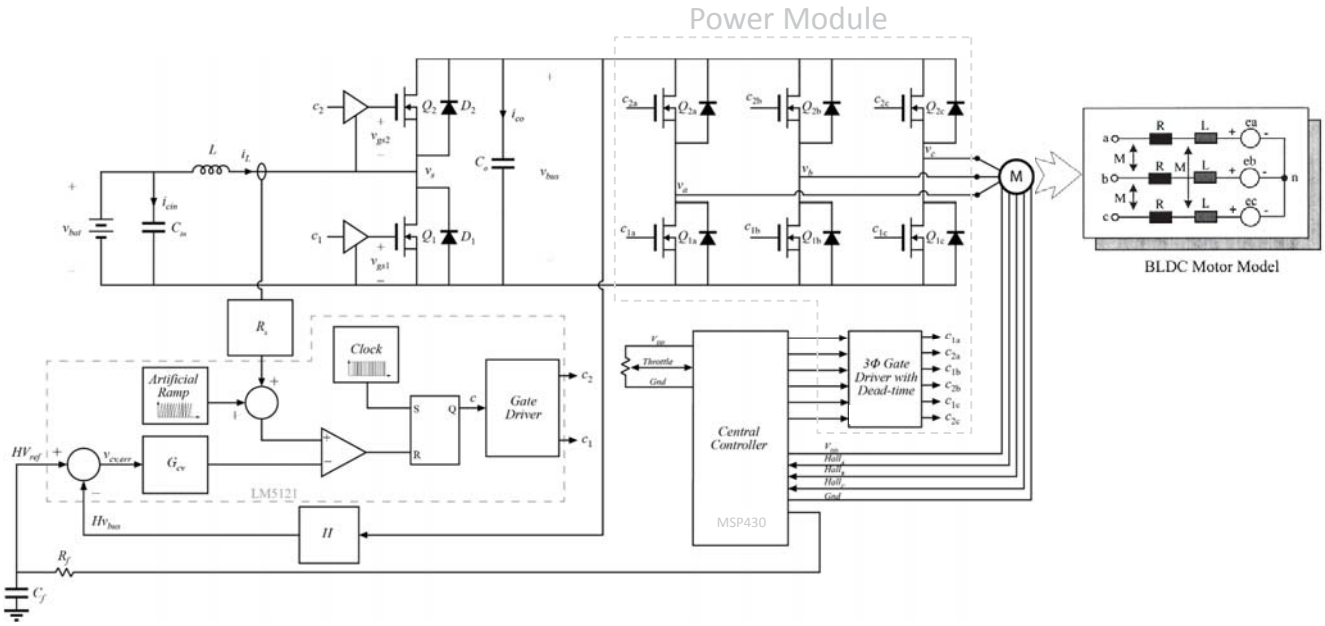


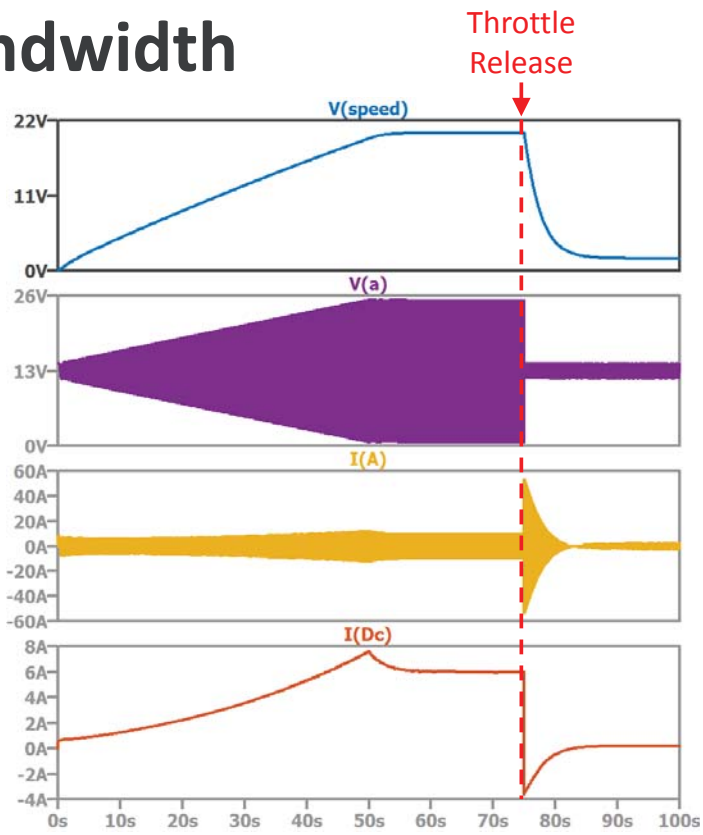
Reference Filtering



Motor Control Bandwidth

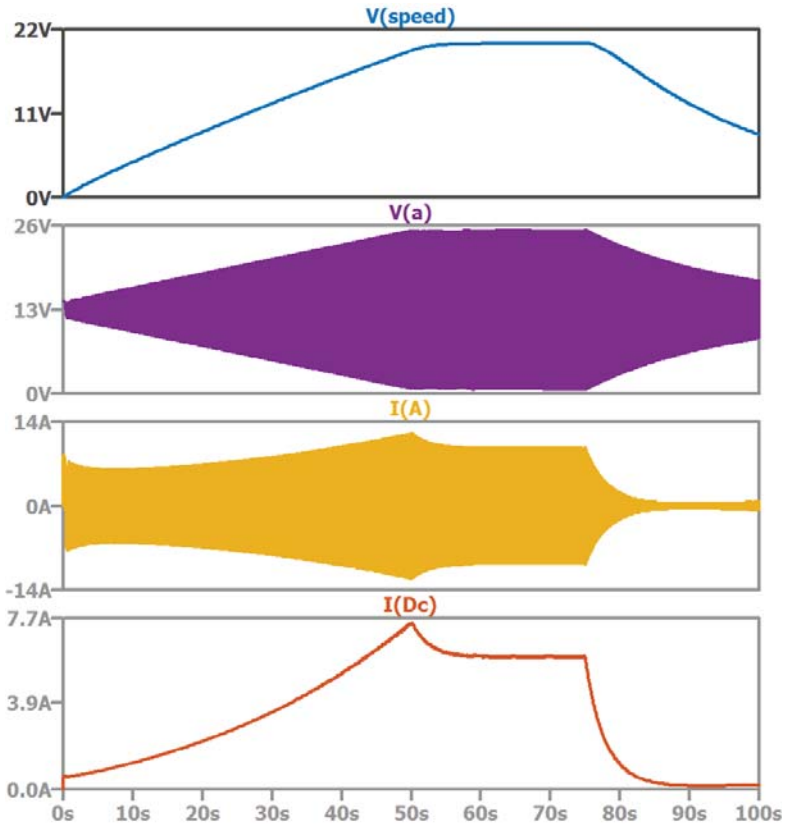
No Filter

May require braking circuit



Motor Control Bandwidth

f_c = 8 mHz + antiparallel diode



Motor Drive

- Power Stage
  - Power module
    - Integrated devices, and/or drivers
    - 3Φ bridge (e.g. MTI85W100GC, IRAM136-3023B)
    - Half bridge (e.g. SQJ974EP, IPG20N10S4L)
  - Individual FETs
- Controller
  - Allegro A4915
  - Toshiba TB6551FAG
  - TI DRV8308
  - Other options
- Example Schematics in Starter Files for Experiment 5

PCB Layout for Experiment 5

- Include test points for voltages/currents to aid debugging
- Where possible, give yourself “backup options”
- Include option for heatsink
- Fans available, but consider power consumption
- Make sure parts you select are available and have sufficient stock
  - even if some get ordered in the interim

Basic PCB Layout Concepts

- Kelvin Connection
- Parasitic Capacitances and Decoupling
- Loop Inductances / Complete Routing
- Decoupling
- Ground Plane / Return Currents
- Partitioning

Trace Parasitics

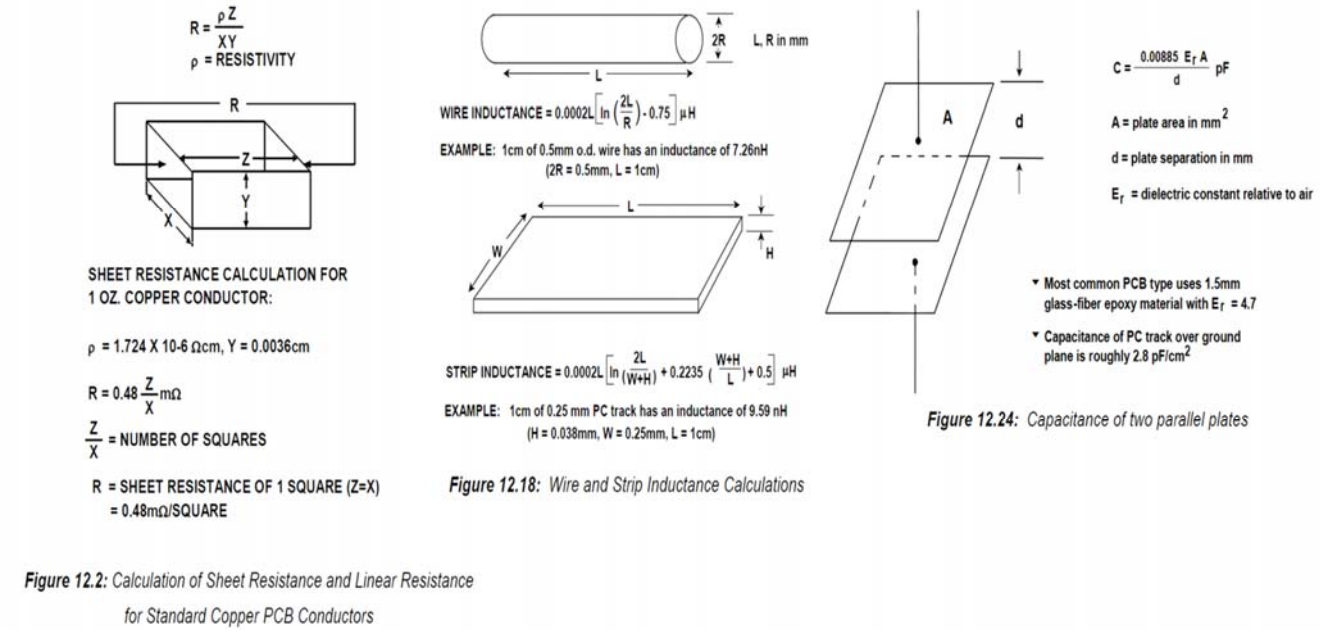


Figure 12.2: Calculation of Sheet Resistance and Linear Resistance for Standard Copper PCB Conductors

Figure 12.18: Wire and Strip Inductance Calculations

Figure 12.24: Capacitance of two parallel plates

Kester, W. "Tips about printed circuit board design: Part 1 - Dealing with harmful PCB effects"

Kelvin Connection

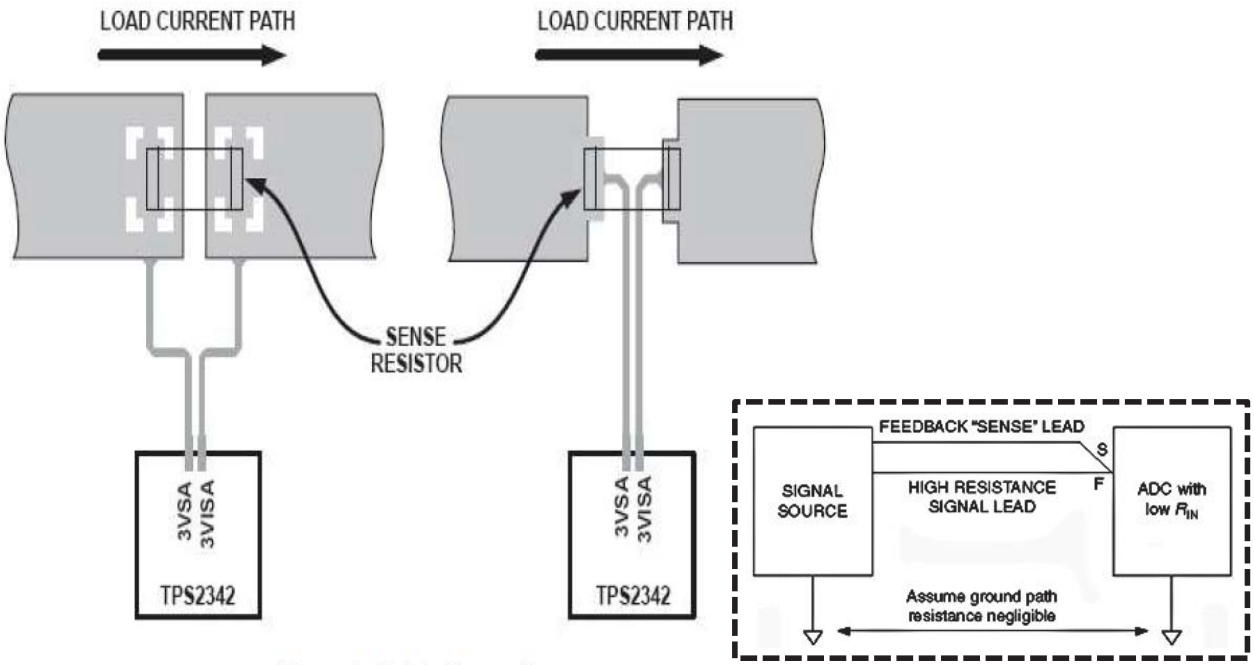


Figure 1. Kelvin Connection

Texas Instruments, "LMP8640/-Q1/HV Precision High Voltage Current Sense Amplifiers"

Decoupling

- Always add bypass capacitor at power supply for any IC/reference
- Use small-valued (~100nf), low ESR and ESL capacitors (ceramic)
- Limit loop for any di/dt

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Decoupling Capacitance

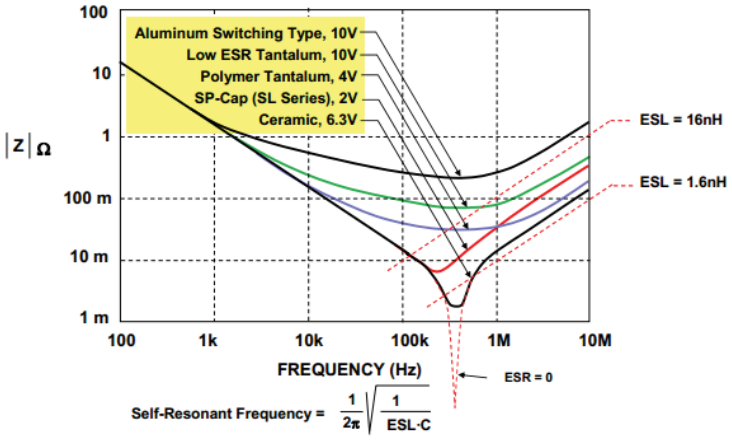
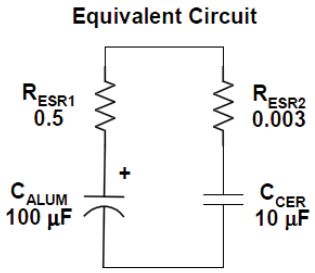


Figure 4: Impedance of Various 100µF Capacitors



High Impedance Nodes and Capacitive Coupling

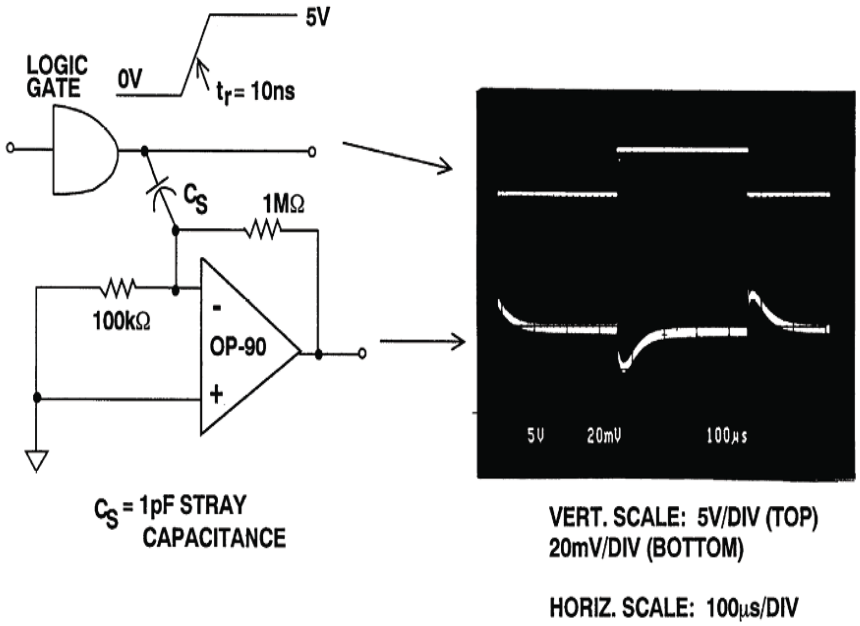


Figure 12.29 *High Circuit Impedances Increase Susceptibility to Noise Pickup*

Capacitive Shielding

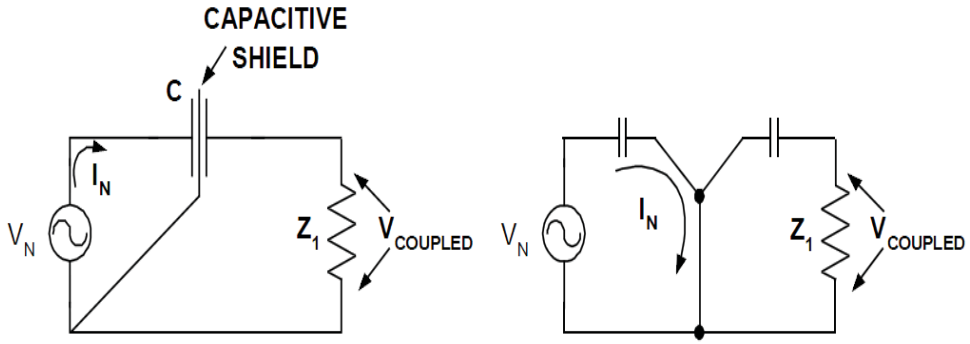
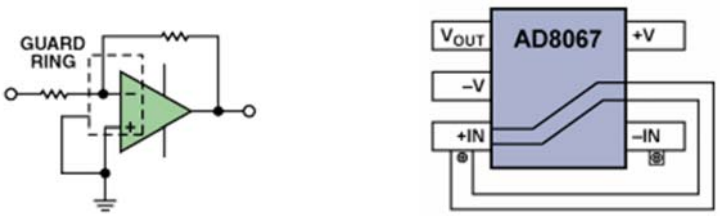
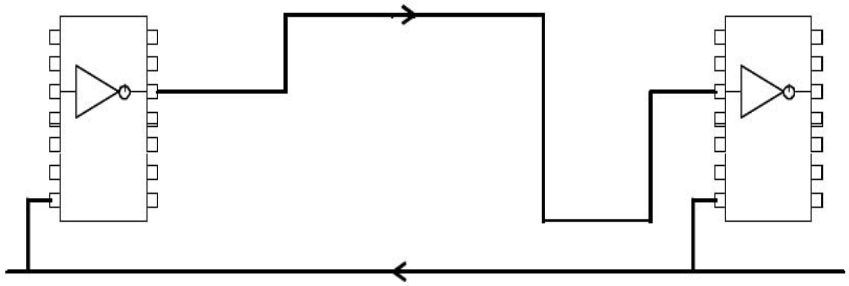


Figure 12.26: *An Operational Model of a Faraday Shield*

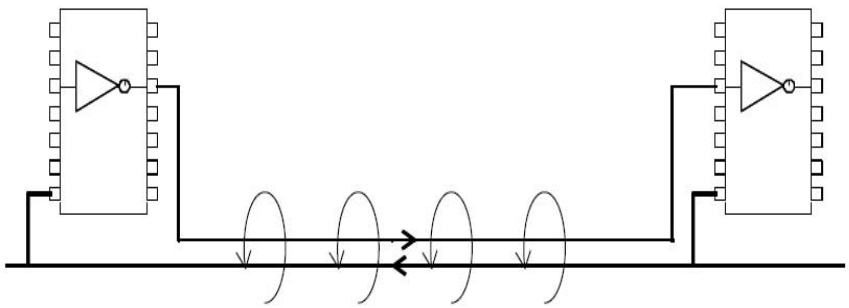


Analog Devices, "Decoupling Techniques," MT-101
Analog Devices, "A Practical Guide to High-Speed Printed-Circuit-Board Layout"

Loop Inductances

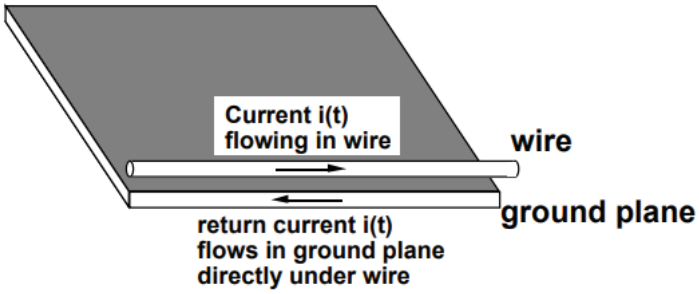


Bad practice: wide separation of signal and return



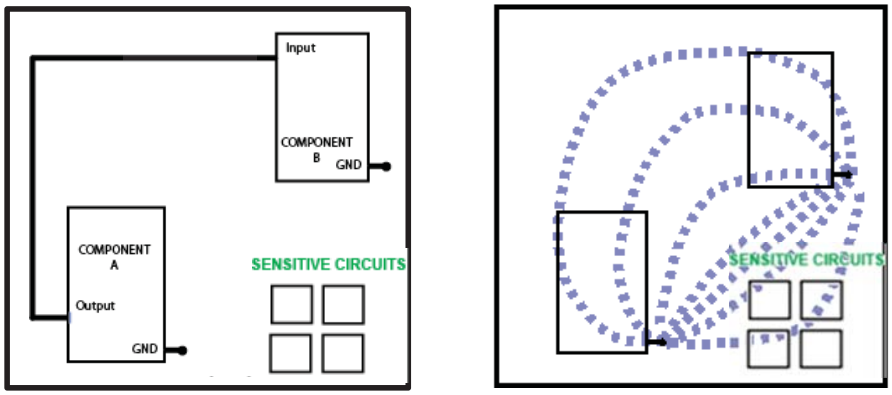
Good practice: close coupling of signal and return

Ground Plane



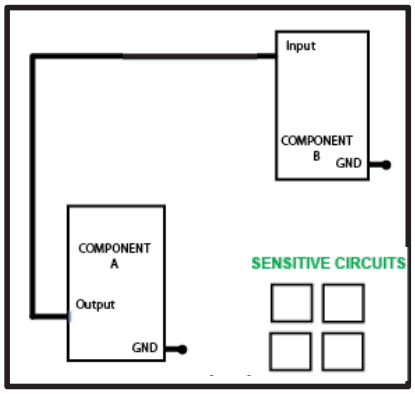
- Benefits:
  - Common reference
  - Shielding
  - Heat dissipation
  - Reduced inductance (increased capacitance)
- Resist urge to cut ground plane as much as possible; consider paths of return currents when cuts are unavoidable

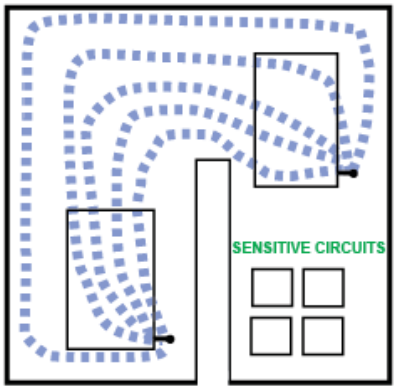
Ground Plane Cuts



Ground return current path

Ground Plane Cuts





Ground return current path

Cuts in Ground Plane

- Goals:
  - minimize inductance/loops
  - Minimize ground interference
- Routing cuts should be kept short and out of the path of any significant (high frequency) return paths
- Cuts can be used effectively for ground isolation, and to reduce noise coupled between digital/analog/power circuitry
- Reducing parasitic capacitance in sensitive signal locations (i.e. op-amp circuitry)

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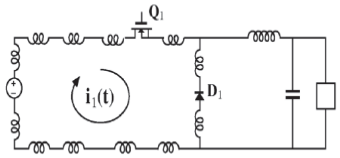
Ground Plane Example

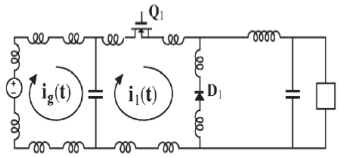
https://www.analog.com/en/analog-dialogue/articles/reducing-ground-bounce-in-dc-to-dc-converters.html

Half Bridge Loop Inductance

Parasitic inductances of input loop explicitly shown:

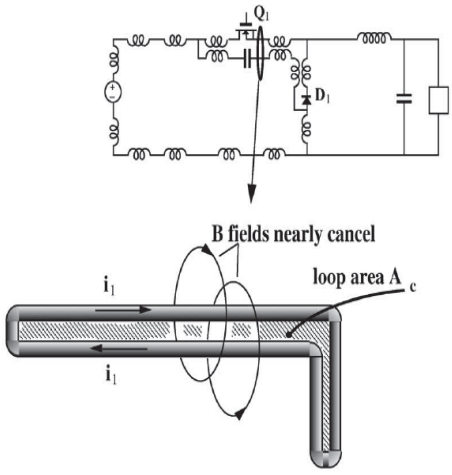


Addition of bypass capacitor confines the pulsating current to a smaller loop:

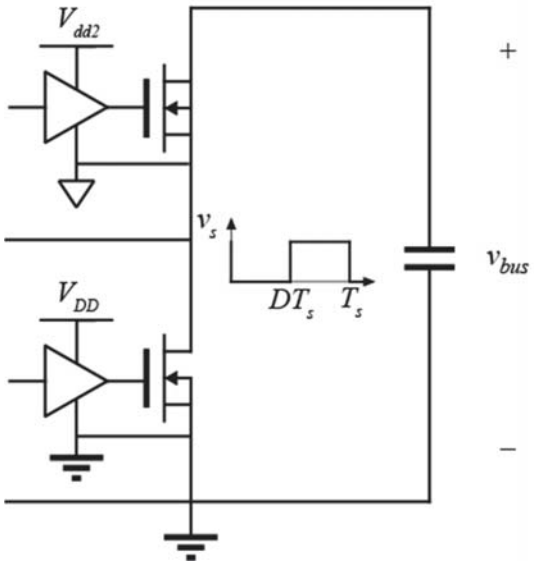


high frequency currents are shunted through capacitor instead of input source

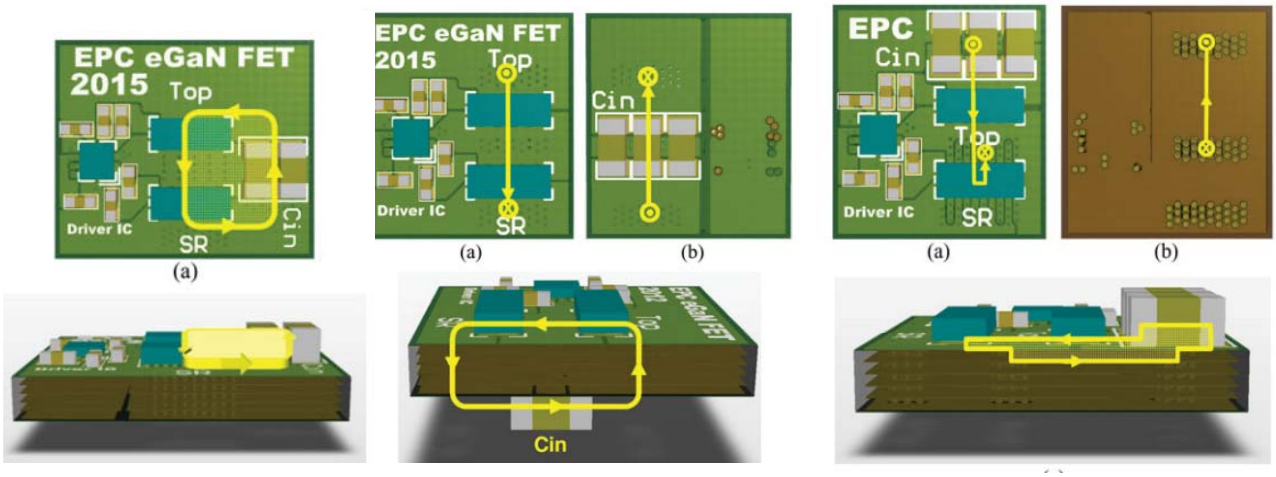
Even better: minimize area of the high frequency loop, thereby minimizing its inductance



Bridge Layout

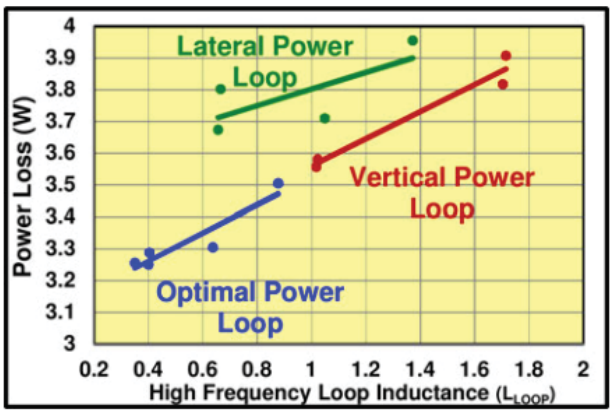


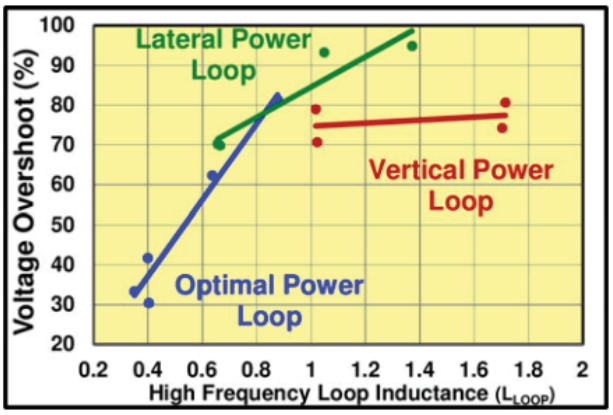
Half Bridge Layout: Another Example



Lateral Vertical "Optimal"

Layout Impact Measurements





- Smallest Loop Area results in
  - Smaller overvoltage
  - Lower switching loss

D. Reusch & J Strydom, "Understanding the Effect of PCB Layout on Circuit Performance in a High-Frequency Gallium-Nitride-Based Point of Load Converter"

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Experiment 5: Starting Files